Multipath-switching device utilizing a GaAs-based multiterminal nanowire junction with size-controlled dual Schottky wrap gates

Seiya Kasai,[a] Tatsuya Nakamura, and Yuta Shiratori
Graduate School of Information Science and Technology, Hokkaido University, North 14, West 9, Sapporo 060-0814, Japan and Research Center for Integrated Quantum Electronics, Hokkaido University, North 13, West 8, Sapporo 060-8628, Japan

(Received 20 March 2007; accepted 21 April 2007; published online 16 May 2007)

A multipath-switching device using a multiterminal nanowire junction with size-controlled dual gates is proposed and demonstrated experimentally. The device switches a number of output terminals according to multiple-valued input voltages for electrons entering from a root terminal. The switching function is implemented by dual gating on multiple nanowires with different threshold voltages V_{th}. Systematic V_{th} shift is made by changing gate lengths in nanometer scale. A triple-path-switching device is fabricated using AlGaAs/GaAs etched nanowires and nanometer-scale Schottky wrap gates. Its correct operation is confirmed at room temperature. Obtained results are explained by a simple analytical model. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2739085]

Multipath switching according to multiple-valued input is one of the key functions to implement multiple-valued logic (MVL) architecture. For example, logic circuits based on a multiple-valued decision diagram can be designed by integrating only multipath-switching devices.[1,2] Such logic architecture has a possibility to provide advanced performance to graph-based logic circuits.[3,4] The multipath switching is also important for conventional digital and memory large-scale integrated circuits (LSIs). Previously, a number of transistors are required to realize the function and they occupy a large area. Then, demand on simple and compact implementation of the multipath-switching function has increased as the increase of bit size and memory capacity in the digital systems. In this letter, a simple and compact multipath-switching device utilizing a multiterminal nanowire junction with dual size-controlled nanometer-scale gates is proposed, and it is demonstrated by fabrication and characterization of the device using a GaAs-based nanowire junction with nanometer-scale Schottky wrap gates.

Figure 1(a) shows a basic structure of the proposed device. This device has a root branch and n number of output branches $(n>2)$ with size-controlled dual gates labeled A and B. Each branch is formed by a conductive nanowire channel whose conductance can be controlled by the gate utilizing the field effect. The function of the device is schematically shown in Fig. 1(b). When two gate voltages, V_{GA} and V_{GB} for gates A and B, respectively, are swept at the same time in complementary way, output terminals are switched one by one as shown in Fig. 1(b). Then, electrons entering from the root go out from the selected output terminal according to multiple-valued gate voltage as input signal.

To implement the multipath-switching function, threshold voltages V_{th} for gates are assigned in multiple ways as shown in Figs. 1(c) and 1(d). Assuming n-type depletion-mode channels, threshold voltages in output j $(j=0, 1, \ldots, n-1)$, V_{thAj} and V_{thBj} for gates A and B, respectively, should be assigned so that $V_{thA0}>V_{thA1}>\cdots>V_{thAj}>\cdots>V_{thA(n-1)}$ and $V_{thB0}<V_{thB1}<\cdots<V_{thBj}<\cdots<V_{thB(n-1)}$. In this study, V_{th} is controlled by changing the gate length in nanometer scale using the short channel effect.[5] To satisfy the above conditions, gate lengths are designed as shown in Fig. 1(a), that is, $L_{GA0}>L_{GA1}>\cdots>L_{GAj}>\cdots>L_{GA(n-1)}$ and $L_{GB0}<L_{LB1}<\cdots<L_{GBj}<\cdots L_{GB(n-1)}$, where L_{GAj} and L_{GBj} denote gate lengths of gates A and B on the output branch j, respectively. These should be short enough so that the short channel effect takes place.

For the device operation, we set $V_{GB}=-V_{GA}+\alpha$, where α is constant. V_{th} and α need to satisfy $\alpha-V_{thBj}=V'_{thBj}>V_{thAj}$ in order to form a conductance peak. Then conductances under gates A and B in the output j, $G_{Aj}(V_{GA})$ and $G_{Bj}(V_{GB})$, exhibit curves as shown in Figs. 1(c) and 1(d), respectively. When V_{GA} increases, G_{Aj} increases, whereas G_{Bj} decreases. The total conductance in the output j is given by a harmonic average of G_{Aj} and G_{Bj}. Using a first order approximation for the transfer characteristics and assuming an equal transconductance value of g_m for all gates, $G_{Aj}=g_m(V_{GA}$

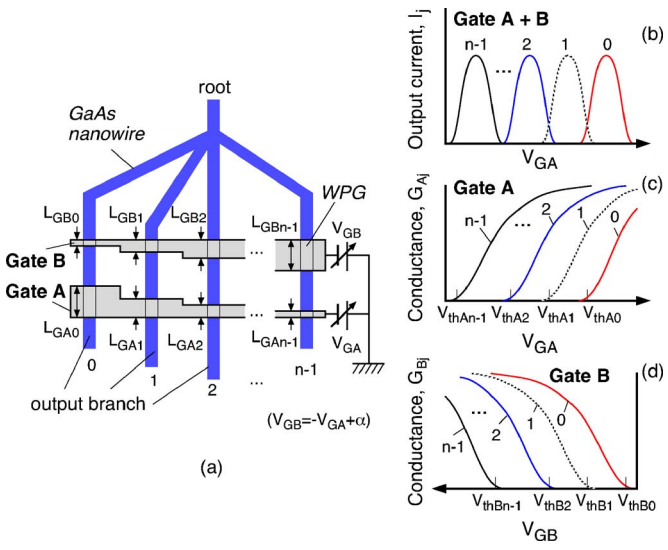

FIG. 1. (Color online) (a) Basic structure of the multiple-path-switching device, (b) fundamental operation of the device, and [(c) and (d)] transfer characteristics in each output branch for gates A and B, respectively.

[a]Electronic mail: kasai@rciqe.hokudai.ac.jp

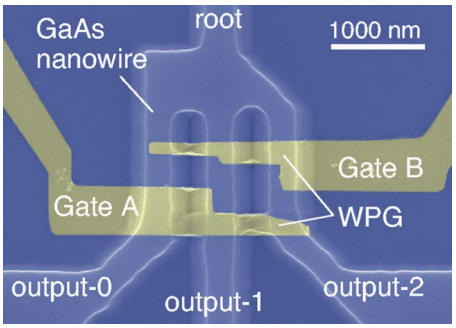

FIG. 2. (Color online) SEM image of a fabricated device.

$-V_{\mathrm{thA}j})/V_{\mathrm{DD}}$ and $G_{\mathrm{B}j}=-g_m(V_{\mathrm{GA}}-V'_{\mathrm{thB}j})/V_{\mathrm{DD}}$ are obtained, where V_{DD} is the supply voltage to the root terminal. Then the current from the output j, $I_j(V_{\mathrm{GA}})$, is given by

$$I_j(V_{\mathrm{GA}}) = \frac{g_m}{V'_{\mathrm{thB}j} - V_{\mathrm{thA}j}} \left\{ \left(\frac{V'_{\mathrm{thB}j} - V_{\mathrm{thA}j}}{2} \right)^2 - \left(V_{\mathrm{GA}} - \frac{V'_{\mathrm{thB}j} + V_{\mathrm{thA}j}}{2} \right)^2 \right\}. \quad (1)$$

This formula indicates that the output current in a branch has a single peak in $V_{\mathrm{thA}j} < V_{\mathrm{GA}} < V'_{\mathrm{thB}j}$. Current peak position $V_{\mathrm{p}j}$ and height $I_{\max j}$ are given by $V_{\mathrm{p}j}=(V_{\mathrm{thA}j}+V'_{\mathrm{thB}j})/2$ and $I_{\max j}=g_m(V_{\mathrm{thA}j}-V'_{\mathrm{thB}j})/4$, respectively. The full width at half maximum (FWHM) of the peak is $(V_{\mathrm{thA}j}-V'_{\mathrm{thB}j})/\sqrt{2}$, which depends on α but not on g_m. Therefore, path-switching characteristics are mostly determined by the assignment of threshold voltages. Uniform V_{th} shift and g_m values are desirable for uniform peak heights, widths, and peak separations. This multipath-switching mechanism is very simple and easy to implement. The use of metal-insulator-semiconductor gates and V_{th} shift by changing gate insulator thickness is obviously applicable to this device.

To demonstrate the operation experimentally, we fabricated a device that had three output branches ($n=3$) and root branches utilizing a GaAs-based etched nanowire junction and nanometer-scale Schottky wrap gates (WPGs). The WPG is a fine Schottky gate wrapped around a nanowire and realizes tight potential control due to three-dimensional (3D) gate configuration.[6] We confirmed that systematic V_{th} shift took place by suitable gate length design when $L_{\mathrm{G}} < 400$ nm in the WPG structure.[7] Figure 2 shows a scanning electron microscope (SEM) image of a fabricated device. Nanowire branches were formed by electron beam lithography and wet etching on a conventional AlGaAs/GaAs modulation-doped heterostructure. Typical nanowire width was 300 nm. A couple of size-controlled WPGs were formed on each output branch. Fabricated WPG gate lengths on output branches 0, 1, and 2 were 570, 260, and 160 nm for gate A and 130, 260, and 570 nm for gate B, respectively. dc I-V measurements were carried out at room temperature for characterization.

Figures 3(a) and 3(b) show measured transfer characteristics in each output branch for gates A and B, respectively. dc voltage was applied to the root terminal, and currents in all output terminals were measured at the same time. In this figure, only gate A or B was swept while keeping another gate open. All WPGs operated as standard field-effect transistors and showed normal transfer characteristics. Evaluated transconductances from linear slope regions were 6 μS at

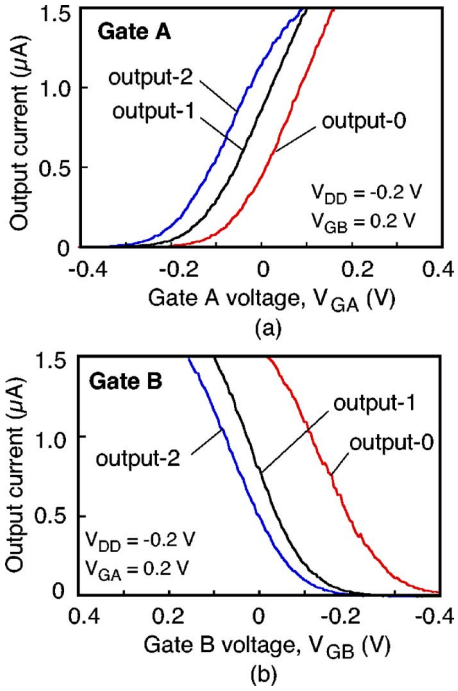

FIG. 3. (Color online) Transfer characteristics in the three output branches for (a) gate A and (b) gate B.

$V_{\mathrm{DD}}=0.2$ V for all output branches. Threshold voltages in output branches 0, 1, and 2 were −20, −100, and −152 mV for gate A and −254, −78, and −40 mV for gate B, respectively. Shorter gate length resulted in decreased V_{th}, and situations in Figs. 1(c) and 1(d) were successfully realized in the fabricated device. Threshold voltage shift ΔV_{th} was lager than 38 mV. Relatively large V_{th} shift for gate B in output 0 came from unintentionally lateral shift of the WPG position.

Figure 4 shows a measured multipath-switching characteristic. In this operation, we set $V_{\mathrm{GB}}=-V_{\mathrm{GA}}$ and $\alpha=0$. Clear three current peaks from each output terminal appeared, and the multipath switching was successfully obtained. The peak positions were 100, 0, and −36 mV for outputs 0, 1, and 2, respectively. They were reasonably consistent with the theoretical values of 120, –11, and −56 mV estimated by Eq. (1) with parameters extracted from the data in Fig. 3. The peak position in each output also corresponded to V_{GA} position at which two conductance curves for the two gates in Figs. 3(a) and 3(b) cross. From the model and data, uniform peak separation would be obtained when regular intervals of V_{th} were realized by precise alignment of WPGs on nanowires. Wider peak separation would be obtained by larger V_{th} shift. For

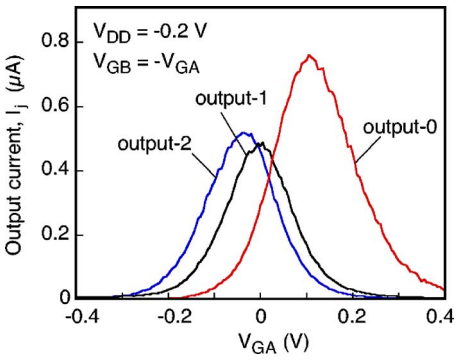

FIG. 4. (Color online) Measured multipath-switching characteristics.

device design, we deduced the gate length dependence of threshold voltage shift from the analytical model,[8] $\Delta V_{\mathrm{th}} = \alpha e V_{\mathrm{bi}} \exp\{-\pi(L_{\mathrm{G}}+\Delta L)/2d\}$, where V_{bi} is built-in potential, d is the top AlGaAs layer thickness, α is constant, and ΔL is gate length offset coming from the suppression of the short channel effect in 3D-gate structures.[9] From the 3D potential simulation, $\alpha=8$ and $\Delta L=40$ nm were estimated at $d=70$ nm. Then, large ΔV_{th} of 200 mV was found possible in the present nanowire when $L_{\mathrm{G}}=50$ and 70 nm. Such gate lengths can be easily fabricated using a modern semiconductor fabrication technology. Current peak heights for outputs 1 and 2 were similar to each other, although that for the output 0 was higher than the others. The analytical model indicated that it was caused by the relatively large shift of V_{thB0}. On the other hand, absolute peak heights could not be reproduced by the simple model. This is because g_m values included the effect of series resistance in the nanowire. Correction of the model taking account of the series resistance is necessary for exact evaluation of peak heights. Measured FWHM values of 195, 164, and 171 meV for outputs 0, 1, and 2, respectively, were in reasonable agreement with the estimated values of 194, 126, and 136 meV. Peak tails came from subthreshold characteristics, which were not included in Eq. (1). Elimination of tails is also necessary for clear peak separation. It is important for suppressing cross-talk of signals between the outputs and increasing the number of output branches as well as the number of multiple levels for the MVL.

In conclusion, a simple and compact multipath-switching device was proposed. The device was demonstrated using the GaAs-based multiterminal nanowire junction with size-controlled nanometer-scale dual WPGs. Clear multipath-switching operation was confirmed experimentally. Obtained results were explained by a simple analytical model.

The authors thank T. Fukui and T. Hashizume for their continuous supports. This work is supported in part by the 21st Century COE program in Hokkaido University, "Mememedia Technology Approach to the R&D of Next-generation ITs," Grant-in-Aid for Young Scientists (A), and Exploratory Research from MEXT, Japan.

[1] S. N. Yanushkevich, D. M. Miller, V. P. Shmerko, and R. S. Stankovic, *Decision Diagram Techniques for Micro- and Nanoelectronic Design Handbook* (CRC, Boca Raton, FL, 2006), pp. 545–565.
[2] T. Sasao and J. T. Butler, Proceedings of 26th International Symposium on Multiple-Valued Logic, 1996 (unpublished), p. 248.
[3] S. Kasai and H. Hasegawa, IEEE Electron Device Lett. **23**, 446 (2002).
[4] S. Kasai, T. Nakamura, Y. Shiratori, and T. Tamura, J. Comput. Theor. Nanosci. (to be published).
[5] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, Hoboken, NJ, 2007), pp. 328–338.
[6] S. Kasai, K. Jinushi, H. Tomozawa, and H. Haseegawa, Jpn. J. Appl. Phys., Part 1 **36**, 1678 (1997).
[7] M. Yumoto, S. Kasai, and H. Hasegawa, Appl. Surf. Sci. **190**, 242 (2002).
[8] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, New York, 1998), pp. 427–433.
[9] T. Hiramoto, T. Saito, and T. Nagumo, Jpn. J. Appl. Phys., Part 1 **42**, 1975 (2003).