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Author(s)	Ikeda, Susumu; Shimada, Toshihiro; Kiguchi, Manabu et al.
Citation	Journal of Applied Physics, 101(9), 094509 https://doi.org/10.1063/1.2734077
Issue Date	2007-05-01
Doc URL	https://hdl.handle.net/2115/29731
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Type	journal article
File Information	JAP101-09.pdf

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Visualization of induced charge in an organic thin-film transistor by cross-sectional potential mapping

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(Received 26 February 2007; accepted 15 March 2007; published online 15 May 2007)

Kelvin probe force microscopy was applied to the cross-sectional potential imaging of a working organic thin-film transistor (OTFT). The bottom-contact-type OTFT with an active layer of copper-phthalocyanine (CuPc) was cleaved and internal potential distribution of its channel region was visualized. The potential distribution on the cross section changed depending on the applied drain and gate voltage. Horizontal potential distribution in the semiconductor film from source to drain direction was roughly consistent with the results of surface potential imaging previously reported. Vertical potential distribution from bottom (gate) to top (CuPc film) showed that a potential peak appeared along the semiconductor/insulator interface when a negative voltage was applied to the gate. The charge injection process is discussed based on the visualized potential peak at the interface. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2734077]

I. INTRODUCTION

Organic thin-film transistors (OTFTs) are now attracting much attention as next-generation electronic devices due to their cost reduction, flexibility, large-area electronic applications, and reduced environmental effect.[1,2] However, the low carrier mobility of organic semiconductors compared to silicon is a significant problem for their practical use. In order to improve their performance, it is important to clarify the various working mechanisms of OTFTs, for example, carrier injection by electric fields and the transport process. One of the most important and progressive approaches is to measure the potential distribution in working OTFT devices. This has a direct relationship with the spatial distribution of the carriers. There have been a number of approaches to measurement: for example, potentiometry[3] and potential imaging (mapping)[4] by contact mode atomic force microscopy (AFM) and potential imaging by Kelvin probe force microscopy (KFM, also known as scanning Kelvin probe microscopy or SKPM).[5–9] KFM is a powerful tool to investigate the spatial potential distribution in working electronic devices. So far, surface potential imaging has been performed using KFM with respect to the working OTFTs of P3HT,[5] M5T,[6,7] and pentacene.[8,9]

Although *surface* potential imaging has provided useful information, it is evident that the direct imaging of the *internal* potential distribution of the devices would, if possible, prove more significant. The most important processes of device performance probably occur just at the interface between the semiconductor and gate insulator.[10] Experimental data of internal potential distribution are required to understand the field-effect transistor (FET) performance and to verify theoretical works.[11–13] In the present study, we tried to measure the internal potential distribution of the working OTFT devices by cross-sectional potential imaging using KFM. To the best of our knowledge, the cross-sectional potential imaging of OTFTs has not yet been achieved, though there are several reports in the research field of inorganic devices.[14–21] The difficulty lies, however, in cleaving organic devices, because the fragility of organic materials makes this more difficult than with inorganic materials. There is a very low probability of successfully cleaving the channel region without electrical shorting between the organic film and the gate electrode. This notwithstanding, after many trials we succeeded in cleaving a sample and achieving cross-sectional potential imaging of a working OTFT.

Since measurable potential was limited (±5 V) in our KFM experiment (as described later), the TFT sample was required to work at a low gate voltage in the present experiment. A material which could work in air was also needed because of our KFM conditions (in air). For these reasons, we used copper-phthalocyanine (CuPc) as the active layer because CuPc TFTs have a relatively low threshold gate

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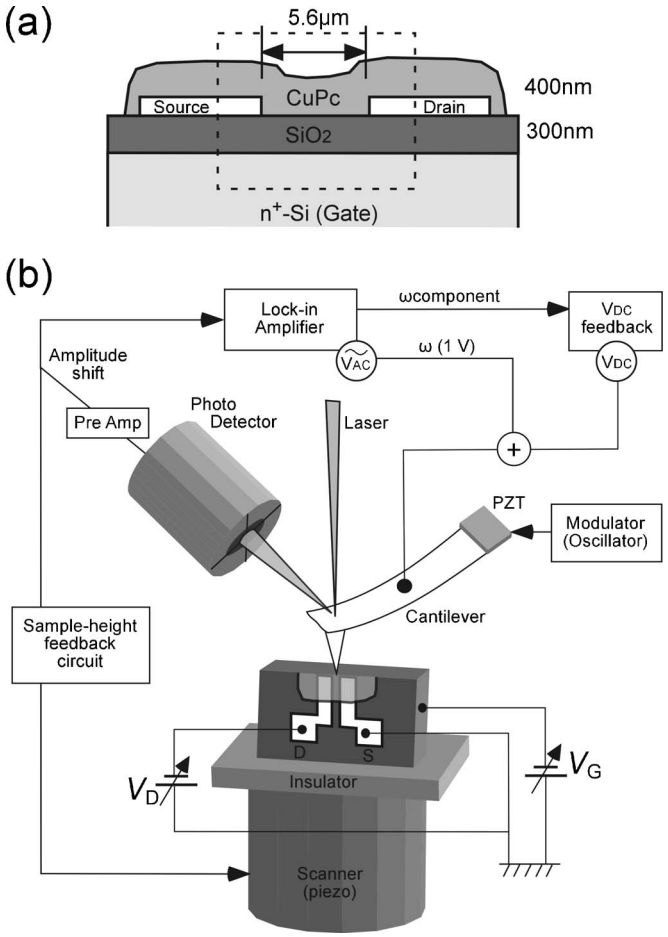


FIG. 1. Experimental setting of the cross-sectional potential imaging. (a) Schematic illustration of structure of bottom-contact CuPc-TFT device in present study (the rough area for potential imaging is also indicated). (b) Schematic illustration of KFM measurement of working TFT.

voltage[22] and also work in air. Under such experimental restrictions, we managed to obtain vivid potential images and useful results.

II. EXPERIMENT

A. Sample preparation

We prepared a CuPc-TFT with a bottom-contact configuration as shown in Fig. 1(a). Source and drain electrodes of Au (25 nm)/Cr (10 nm) were first prepared by photolithography on a highly doped *n*-type Si(100) substrate with a thermally oxidized surface (300 nm in thickness). The channel length (5.6 ± 0.1 μm) was confirmed by AFM prior to film deposition. A CuPc film (400 nm) was formed by molecular beam deposition (MBD) at a base pressure of 8×10^{-7} Pa. The film thickness was monitored using a quartz crystal microbalance (QCM). The growth rate of the film was 0.1 nm/s and the substrate was kept at room temperature. The CuPc-TFT device showed *p*-type, normally on characteristics, probably due to impurities and oxygen in the air (mobility $\sim10^{-6}$ cm^2/Vs). The drain current increased at a negative gate voltage and decreased at a positive one. This specimen was cleaved into halves for cross-sectional observation. After cleaving, there was little leakage through the SiO_2 dielectric layer and *p*-type operation still remained. Part

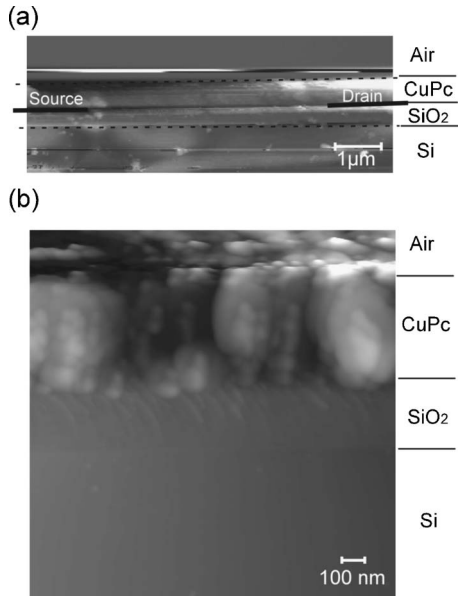


FIG. 2. AFM topographies of cross-section. (a) Exact area of cross-sectional potential imaging. (d) Higher magnification image of channel region.

of the cleaved device was put on an insulating sample holder as shown in Fig. 1(b), and morphological and KFM observations were carried out.

B. Cross-sectional measurement of topography and KFM

Because of the thinness of the source and drain electrodes, the positions of the electrodes were difficult to completely identify only by the topography. Accordingly, we sought the area comprising the electrodes according to the following procedure. By applying a voltage to the source and drain electrodes, a change of the potential distribution in the CuPc film was observed near the electrodes. Areas were selected at which the potential change was symmetrically observed on the left and right sides. The distance between the responding areas was almost the same as the channel length (5.6 ± 0.1 μm) measured by AFM. Thus, the source-channel-drain region could be clearly identified.

KFM is a tool to measure the surface potential distribution based on ac-mode AFM detecting the electrostatic force between the sample surface and a metal-coated cantilever. In our KFM measurement, a mixed potential $V_{ac}(\omega)+V_{dc}$ was applied to the cantilever, which oscillated at the resonance frequency of $\sim$150 kHz. Here, $V_{ac}(\omega)$ was 1.0 V and ω was chosen taking account of the imaging condition (ω must be less than half of the oscillation frequency of the cantilever). During a scan, the electrostatic force between the sample surface and the tip is expressed as

$$F=\frac{1}{2}\left(\left(V_{dc}-\frac{\Delta\Phi}{q}\right)^2+\frac{1}{2}V_{ac}^2\right)\frac{\partial C}{\partial z}+\frac{\partial C}{\partial z}\times\left(V_{dc}-\frac{\Delta\Phi}{q}\right)V_{ac}\sin(\omega t)+\frac{1}{4}\frac{\partial C}{\partial z}V_{ac}^2\cos(2\omega t), \quad (1)$$

where $\Delta\Phi/q$ is the contact potential difference and C is the capacitance between the top of the tip and the sample

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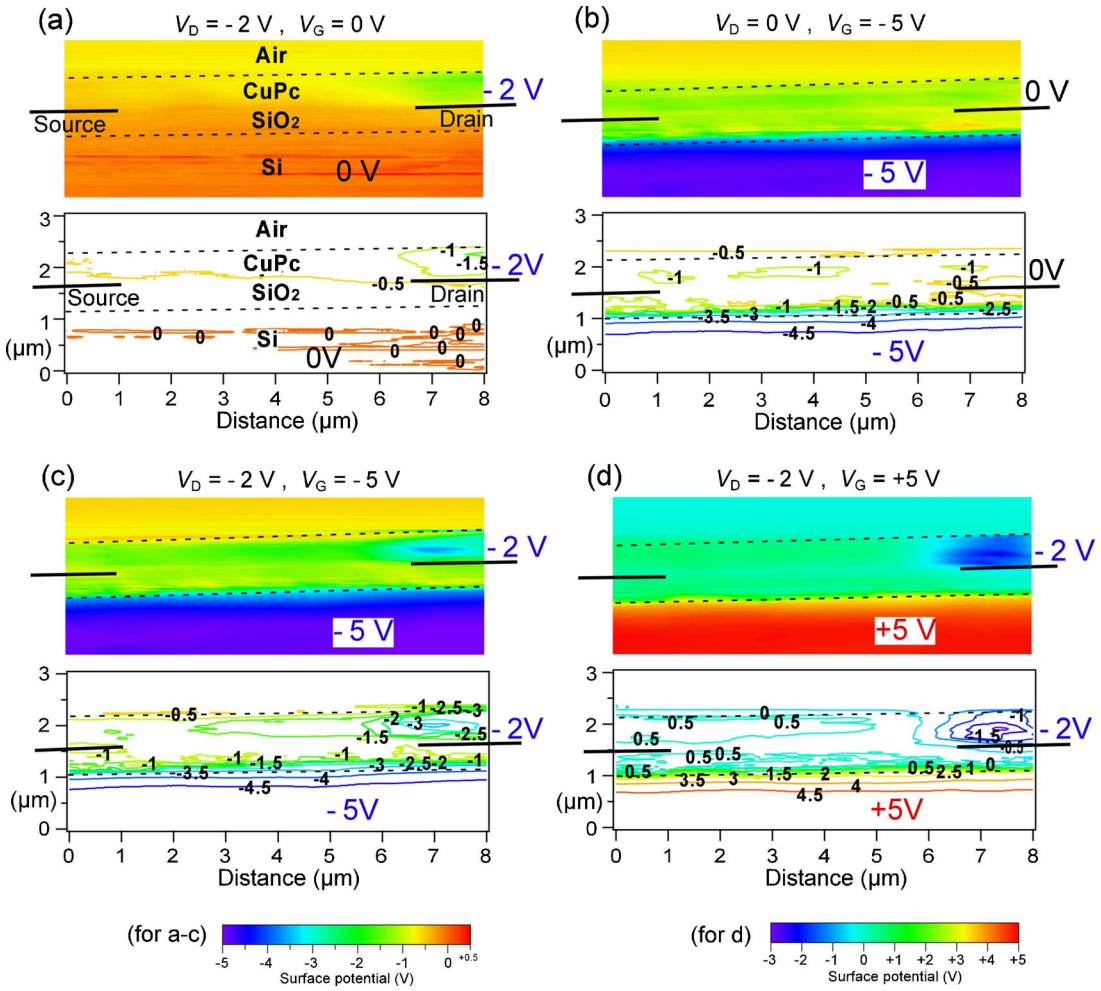


FIG. 3. (Color online) Cross-sectional potential maps observed by KFM. Color maps and contour maps are also shown. Contour lines are drawn every 0.5 V. Conditions of applied voltage to the electrodes were (a) V_D=−2 V and V_G=0 V; (b) V_D=0 V and V_G=−5 V; (c) V_D=−2 V and V_G=−5 V; and (d) V_D=−2 V and V_G=+5 V. Left color bar is common for (a), (b), and (c), while right color bar is only for (d).

surface.[23] The lock-in amplifier extracted the ω component of the amplitude shift of the cantilever oscillation (second term of the equation), and the feedback loop was operated so as to maintain the second term as zero. Under this condition, the V_{dc} applied to the cantilever corresponds to the local potential of the sample surface. In this study, a platinum (Pt)-coated cantilever was used and the work function of Pt was the standard level of potential.

We used JEOL JSPM-5200 for the KFM measurement. Although the dynamic range of the KFM was 10 V, we could not obtain clear data when the applied voltages to the TFT sample exceeded ±5 V. Based on this restriction, the voltage applied to the electrodes (gate and drain) of the TFT device was limited to within ±5 V in this study. The spatial resolution of the KFM study depends on the size of the measurement area and the number of pixels in the images. In the present study, the width of the measured area was 8 μm and the number of horizontal pixels was 256, so that the spatial resolution (the size of 1 pixel) was ~30 nm. Scanning of the tip started from the n^+-Si region, then entered the SiO_2 and CuPc regions, and finally terminated in the air region. Each scanning line was almost parallel to the layered structure of the device.

III. RESULTS

Figures 2(a) and 2(b) show the cross-sectional topographies after cleaving. Figure 2(a) corresponds to the area observed by KFM in which the source and drain electrodes are included, while Fig. 2(b) is a larger magnification image of the channel region. The Si region was well cleaved, showing a flat surface, and the root-mean-square (rms) surface roughness of this region was less than 2 nm. Part of the oxidized layer (amorphous) was also well cut, although it showed a texture somewhat like broken glass (rms ~ 3 nm). The cross-sectional surface of the CuPc was rougher than those of the Si and SiO_2 layers (rms ~ 15 nm). The CuPc layer consisted of small grains 80−100 nm in diameter. Judging from the results of the potential imaging, however, this roughness did not seriously influence the present KFM work. KFM detects the average electronic properties of the depth direction, and the images are not easily influenced by any surface roughness such as molecular defects.[24]

Figure 3 shows color maps and contour maps of the potential distribution of the working CuPc-TFT. This is the first observation of the cross-sectional potential imaging of a working OTFT. The imaged area is shown in Fig. 1(a) by the box (broken line). The area includes Si, SiO_2, CuPc, air, and

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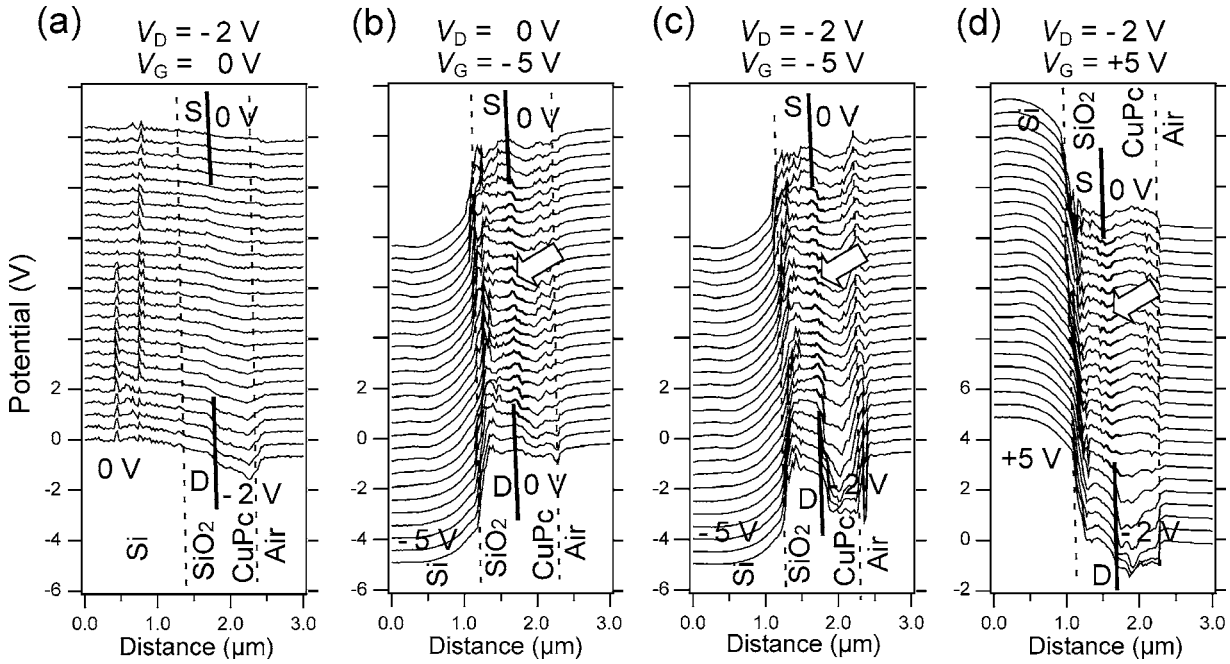


FIG. 4. Line profiles of potential from bottom (n^+-Si side) to top (air side) of potential maps. Conditions of applied voltage to the electrodes were (a) V_D =−2 V and V_G=0 V; (b) V_D=0 V and V_G=−5 V; (c) V_D=−2 V and V_G=−5 V; and (d) V_D=−2 V and V_G=+5 V. The peaks and valleys observed at the CuPc/SiO_2 interface are signified by arrows. The potential values indicated on the vertical axis correspond to the values for the lowest (drain side) profiles. The other profiles are moved with the increment of 0.5 V for convenience.

also a part of the source and drain electrodes. In the potential images, various changes appear depending on the gate voltage (V_G) and drain voltage (V_D). In particular, the interesting potential change in the CuPc film is easily recognized by the contour maps shown in Fig. 3. In the contour map of V_D= −2 V and V_G=0 V [Fig. 3(a)], the negative potential region is seen only near the drain electrode in the CuPc film. In the images of V_D=−2 V and V_G=−5 V [Fig. 3(c)], the negative potential region around the drain electrode extends to the source electrode. On the other hand, when a positive voltage (+5 V) was applied to the gate [Fig. 3(d)], the negative potential region is localized near the drain electrode and does not extend toward the source electrode.

In the potential maps, we can find another interesting feature. In Figs. 3(b) and 3(c), there is a line showing a higher potential along the CuPc/SiO_2 interface. Since this signal is weak and not easy to see, potential distribution was shown as a line profile. Figure 4 shows the potential variation from the bottom to the top of the device. In the diagram of V_G=0 V [Fig. 4(a)], no peak is recognized at the CuPc/SiO_2 interface. In the two diagrams of V_G=−5 V [Figs. 4(b) and 4(c)], there appear rows of peaks along the CuPc/SiO_2 interface (arrows). On the contrary, in the diagram of V_G=+5 V [Fig. 4(d)], there is a row of "valleys" along the CuPc/SiO_2 interface. One interesting point is the difference in the peak intensity between Figs. 4(b) and 4(c). Under the condition of V_D=0 V [Fig. 4(b)], the intensity of the peaks is almost the same in both regions near the source and drain electrodes. On the other hand, the intensity of those peaks near the drain electrode decreases by applying a negative voltage to the drain electrode [Fig. 4(c)].

IV. DISCUSSION

A. Potential mapping on gate insulator

First, we discuss the problem of potential distribution in the gate dielectric (SiO_2) region. According to electromagnetic theory, the potential should linearly change in the SiO_2 region at finite V_G just like the parallel-plate capacitors. However, the observed potential changes sharply at the SiO_2/Si interface and is almost uniform (~0 V) in the SiO_2 region. There are two possible explanations for this uniformity. One is due to the principle of the KFM measurement. Owing to a very small amount of charge on the insulator surface, the cantilever does not sense the electrostatic force on it. The cantilever senses the electrostatic force through the interaction with the charge in the gate material (n^+-Si) and/or semiconductor (CuPc) far from the tip. In this situation, however, the tip cannot detect the electrostatic force effectively because the vibration direction of the cantilever is perpendicular to the direction of the electric field.

The other explanation relates to screening by adsorbed charge. There have been a number of theoretical and experimental investigations of surface potential imaging on the dielectric and ferroelectric surfaces using scanning probe microscopy.[25,26] One of their conclusions is that surface potential on dielectric surfaces is often screened by surface adsorbates when the potential measurement is carried out in air.

It is difficult to identify the reason for the flat potential distribution on the gate insulator in a biased complex system. However, it is likely that the observed potential distribution in the SiO_2 region does not reflect the real potential for the reasons mentioned above. Thus, in the present study, we focused only on the conductive channel region in which the

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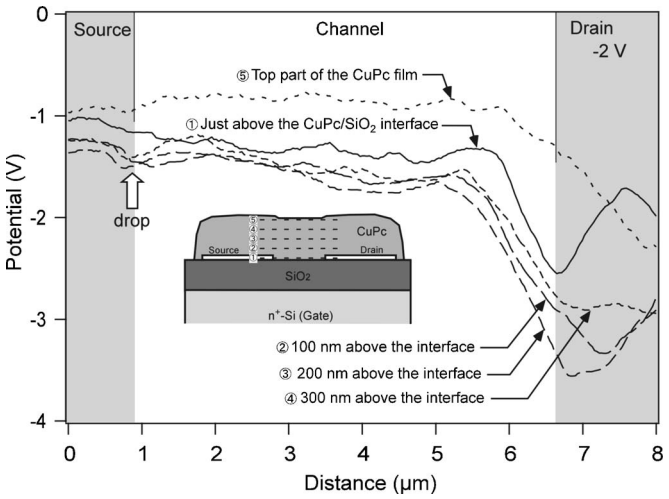


FIG. 5. Horizontal potential profiles from source to drain in CuPc film. The solid curve indicates the profiles just above (<30 nm) the CuPc/SiO_2 interface. Other curves are 100, 200, and 300 nm above the interface. The curve near the top surface of the CuPc film is also shown.

above problem did not matter at all. Of course, this problem should be further discussed in the interests of better potential mapping.

B. Horizontal potential distribution in the CuPc film

Here, we discuss the horizontal potential distribution in the CuPc film from source to drain. There are a number of reports of surface potential measurement from source to drain in OTFTs. Bürgi *et al.* first succeeded in surface potential imaging of a working OTFT and showed the horizontal distribution of the potential from source to drain.[5] One of their achievements was that they clearly showed the potential drops at electrodes-channel boundaries which Seshadri and Frisbie[3] had previously suggested using contact-mode AFM potentiometry. Bürgi *et al.* also showed that the potential distribution (slope) in the channel region changes depending upon V_G. As well as these findings, potential distribution of monolayer OTFTs, dependence of electrode metals (work function effect), and difference between top-contact and bottom-contact OTFTs were investigated using KFM by Miyazaki *et al.*,[6,7] Nichols *et al.*,[8] and Puntambekar *et al.*,[9] respectively. Nakamura *et al.*[4] describe how top-contact pentacene TFTs also show such potential drops at both source and drain regions owing to damage to the pentacene near electrodes, although Puntambekar *et al.*[9] maintain that there is little potential drop in top-contact TFTs. The consensus derived from these potential mappings is that potential does exhibit a drop at the electrode-channel boundaries in OTFTs, and that these drops can be attributed to contact resistance (Schottky barrier) or damage to organic films (in the case of top-contact TFTs).

Figure 5 shows the horizontal potential distribution from source to drain in the CuPc film using the cross-sectional mapping data of Fig. 3(c) (V_D=−2 V and V_G=−5 V). In the curves 100, 200, and 300 nm above the CuPc/SiO_2 interface, a small potential drop can be seen at the source-channel boundary. However, there is no clear potential drop in the diagram just above the interface. The reason is not clear, but

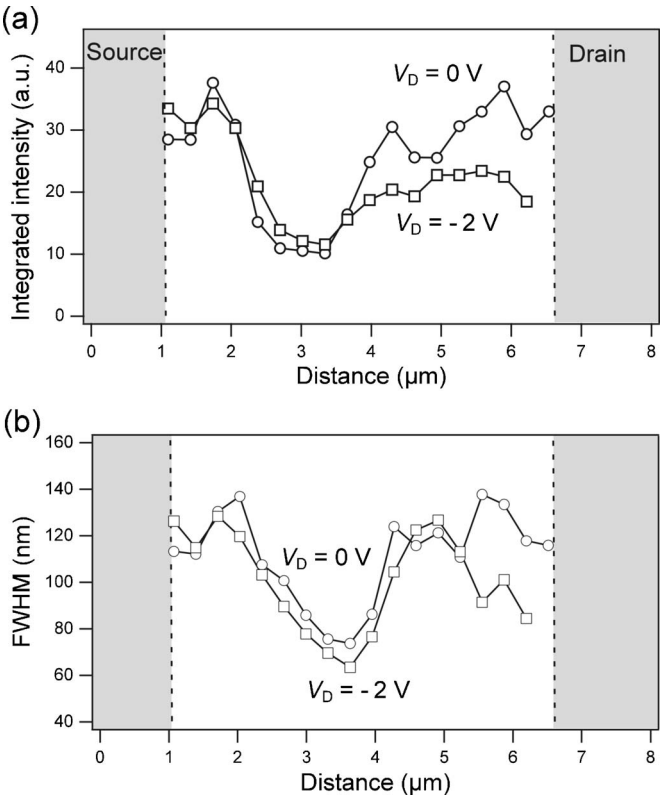


FIG. 6. Integrated intensity (a) and FWHM (b) of potential peak along interface obtained by least-squares fitting of Gaussian function. Integrated intensity indicates the area of the peak. Open circles indicate the data for V_D=0 V and open squares indicate those for V_D=−2 V. Gate voltage was −5 V for both diagrams.

it probably relates to the potential peak observed at the interface (Fig. 4). In our measurement, the potential peak along the channel (about +0.3 V) was coincidentally the same as the potential drop (about −0.3 V) at the source/channel interface, so the potential drop cannot be clearly seen just above the CuPc/SiO_2 interface. According to this result, there is a possibility that horizontal potential distribution just at the semiconductor/insulator interface is a little different from that on the film surface.

C. Potential peak at the CuPc/SiO_2 interface

As shown in Fig. 4, the potential *peak* or potential *valley* was observed at the CuPc/SiO_2 interface when *negative* or *positive* voltages were applied to the gate. Figure 6 shows the variation of integrated intensity (area) and full width at half maximum (FWHM) of the potential peak at the CuPc/SiO_2 interface under conditions of V_D=0 and −2 V (V_G=−5 V). The integrated intensity and FWHM of the peak was determined by fitting of the symmetrical Gaussian function for convenience (because this function fitted data well). Position, integrated intensity, and FWHM were used as the variable fitting parameters.

First, we focus on the peak intensity (area) near the source and drain electrodes. The peak intensity near the source electrode is almost the same at both V_D=0 and −2 V, while the intensity near the drain electrode is smaller at V_D =−2 V than at V_D=0 V. The induced charge Q at the interface is generally proportional to $C|V_G-V_L|$, where C is the

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capacitance of the gate insulator (SiO_2) and V_L is the local potential at the interface. The decrease in intensity of the potential peak near the drain at $V_D=-2$ V suggests that the peak intensity corresponds to the amount of induced charge, and thus direct visualization of the charge could be achieved.

Ishizuka *et al.* performed the cross-sectional potential imaging of a silicon on insulator (SOI) system by KFM.[21] They observed a similar positive potential peak of 189 mV at the interface between the SOI and buried-insulator (BOX), which was fabricated by implanting oxygen. They assigned the peak as the accumulation of positive charge, though they did not mention any physical interpretation. In our measurement, the height of the potential peak is around 300 mV and of the same order as their value. This similarity in different devices indicates that this kind of potential peak is a common feature for accumulation layers in electronic devices. We can conclude therefore that the induced charge or its related features were successfully visualized.

The intensity (area) and width of the peak around the center of the channel is not so simple. The intensity around the channel center is evidently smaller than that near the electrodes. If the intensity reflects the amount of induced charge, Fig. 6(a) implies a lower induced charge at the channel center than at either end. One possible explanation is that the accumulation of carriers is insufficient around the center of the channel because, for example, the absolute value of V_L in $Q=C|V_G-V_L|$ is larger than that expected (actually, the potential in CuPc showed a negative value at negative V_G). Another simple explanation is that the actual amount of induced charge is almost the same everywhere, and the origin of the lower intensity around the center is only due to a smaller peak width [Fig. 6(b)], because the area of the peak is a multiple of width and height. In this case, the issue is why the peak width is smaller around the center of the channel. If the smaller width of the peak means a thinner accumulation layer, then this different thickness of accumulation layer along the channel is certainly a new finding and important for the modeling of organic TFTs.

For the valley of the potential as shown in Fig. 4(d) (at positive V_G), one possible explanation is the injection of a negative charge at the interface. However, it is more probable that the potential valley indicates the exhaustion of the inherently existing positive charge. The native positive charge was due to doping by impurities in the CuPc reagent or oxygen adsorbed during measurement. The decrease of drain current at positive V_G supports this idea.

D. Grain boundary charge model to reproduce the experimental potential (a second hypothesis)

Here, we present another possible model to explain the origin of the potential peak at the $CuPc/SiO_2$ interface. Based on the electromagnetic theory, and assuming that OTFTs are basically capacitors consisting of two parallel electrodes, there is no potential peak at the conductor/insulator interface. In an ideal capacitor, the electric field is finite only between the parallel electrodes and zero outside of the capacitor. Here, we consider the charge distribution that reproduces the potential peak based on electromagnetic theory. For the calculation, we used ELECNET v6.10 (INFOLYTICA Corp.) software, which solves the Poisson's equation by the finite-element method. Figure 7(a) shows the geometry of the calculation, almost identical to the KFM measurement region. Dielectric constants of 3.9, 4.0, and 1.0 were assumed for the SiO_2, CuPc,[27] and air, respectively. The boundary conditions were set as follows: 0 V at the top of the air, and the derivative of the potential with respect to the horizontal direction was zero at the right and left edges of the calculated region. In the present study, we placed the positive charge as a sheet along the $CuPc/SiO_2$ interface. The amount of input charge (positive) was 3.6×10^{11} cm^{-2} to satisfy $Q=CV$, where V is the potential difference (−5 V). It is known that the charge injection satisfying $Q=CV$ can occur in OTFTs (Ref. 28) if the organic active layer is not too thin.[29] After several trials, however, we needed to inject a small amount of negative charge into the CuPc layer 80 nm above the interface. In the case of $V_D=0$ V, the negative charge (1.1×10^{11} cm^{-2}) was about 30% of the positive charge at the interface (3.6×10^{11} cm^{-2}). In the case of $V_D=-2$ V, the input positive charge was manually changed to reproduce the effective electric field ($3.6-2.2\times10^{11}$ cm^{-2} from source to drain). The amount of negative charge was also changed ($1.1-0.4\times10^{11}$ cm^{-2}) to correspond to the change in the positive charge. Using these models of charge distribution, the potential peak in Figs. 4(b) and 4(c) was well reproduced as shown in Figs. 7(b) and 7(c). Note that the potential distribution in the SiO_2 region is different between the observed and calculated data, as already explained.

A height of 80 nm above the $CuPc/SiO_2$ interface roughly equates to the position where the first horizontal grain boundaries exist in the CuPc film [Fig. 2(b)]. The good agreement between the experimental and calculated potential peak suggests that this model, in which opposite charge is induced at the grain boundaries, is probable. Based on this model, the thickness dependence of the FET characteristics of CuPc-TFT can be explained. Hoshino *et al.* first reported data on thickness dependence in which CuPc-TFTs show maximum mobility at a thickness of 80 nm.[22] We also confirmed the similar tendency by our *in situ* FET measurement during film deposition.[30] In a TFT with a thin active layer, the electric field is almost the same as that of a simple capacitor with two conductive plates [Fig. 7(e)]. However, after starting the formation of the second layer of CuPc grains, a negative charge is induced at the first horizontal grain boundaries, and this modifies the electric field in the device and decreases the apparent carrier mobility [Fig. 7(f)]. This model suggests that for making OTFTs, the thickness of the active layer should be lower than the vertical grain thickness [t_g in Fig. 7(f)].

V. CONCLUSION

A vivid potential distribution in a working OTFT was imaged by cross-sectional KFM. This cross-sectional mapping provides new information that previous surface (in-plane) potential mapping could not reveal. In particular, the potential peak observed at the $CuPc/SiO_2$ interface is the major result of this study. Since we could not determine the

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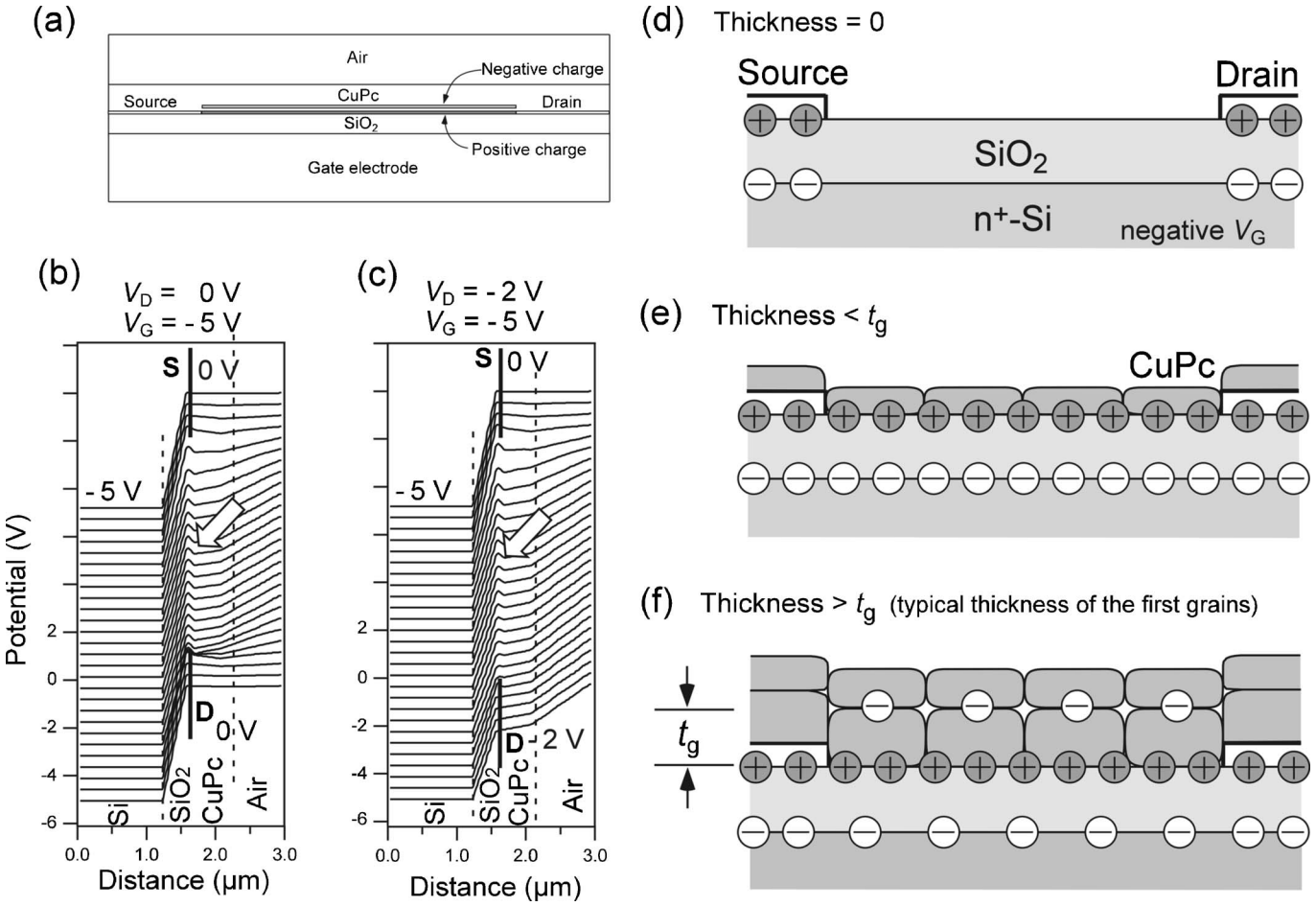


FIG. 7. Another possible explanation of the potential peak. (a) Geometric model for calculations with negative V_G (the positive charge was input at the $CuPc/SiO_2$ interface and the negative charge was input 80 nm above the interface to reproduce the observed potential distribution). (b) and (c) Calculated results corresponding to observed profiles of Figs. 4(b) and 4(c). (d), (e), and (f) Charge injection model changing during film growth [t_g is the average thickness (vertical grain size) of the first grains grown on the gate insulator, which were ~80 nm in the present case].

origin of this potential peak completely, we proposed two interpretations (Secs. IV C and IV D). One is this potential peak indicates exactly the amount of induced charge (Sec. IV C). Variation of area and width of the potential peak in the channel region is an interesting feature. The other interpretation (Sec. IV D) is that this potential peak originates from the combination of two kinds of charge, that is, the expected charge ($Q \sim CV$) induced at the $CuPc/SiO_2$ interface and a small opposite charge induced at the grain boundaries. This hypothesis can explain the strange thickness dependence of the performance of CuPc-TFTs. In either case, we can conclude that we succeeded in visualizing an induced charge or its related features. This kind of cross-sectional potential imaging will also provide the key to solving the important physical issue of "band bending," though the spatial resolution in this study was not sufficient to actually see the bending. The internal potential distribution is a fundamental factor of the device performance, and our cross-sectional mapping contributes to a better understanding and performance of OTFTs.

ACKNOWLEDGMENTS

We would like to thank Professor H. Aoki (University of Tokyo) and Dr. Y. Hong (University of Cambridge) for helpful discussions. Thanks are also due to Dr. T. Miyazaki (Kyoto University) for technical suggestions on KFM measurement. This research was supported by a Grant-in-Aid for Scientific Research from the Ministry of Education, Science, Sports, and Culture of Japan (14GS0207).

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