Control of Metal/III-V Compound Semiconductor Interfaces and Its Application to Quantum Effect Devices

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to my parents

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Contents

Chapter 1
Introduction

1.1 Historical background

1.1.1 *Importance of III-V compound semiconductor devices*

Information-dominated society in present day has been established by the semiconductor-based electronics. This is a result of the tremendous progress in the area of the digital integrated circuit technology since the invention of the transistor in 1940s. This has brought us high performance equipments dayly used in our life, such as computers, cars, audio-visual systems, washing machines and so on. The integration level of the produced digital ICs (integrated circuit) has became high year by year, going through stages of LSIs (large scale integration), VLSIs (very large scale integration) and ULSIs (ultra large scale integration). These semiconductor ICs include micro-processing units and high capacity semiconductor memories, and they contain today a few million devices in only one chip with a area of a few cm^2 and each device dimension reaches submicron-meters.

Most of present ICs have been made by silicon (Si)-based semiconductors. There are several reasons that Si is the dominant material in semiconductor devices. High-quality single crystals can be obtained economically and Si-based oxide (SiO_2) serves as an excellent passivation film. The accumulation of research has amply clarified its material properties, and the processing technologies have also been extremely well developed for many years on Si-based materials.

On the other hand, the development of the non-Si-based digital and analog devices and ICs has brought the development of communication systems in a recent years, too. High density, high speed and wide area communication systems have

become possible and they have been realized by optical fiber network, satellite communication and so on. Various infrastructures based on these communication systems are being constructed and spread rapidly in the present society. It should be that which support communication systems are the III-V compound semiconductor devices and not the Si devices, because III-V compound semiconductors have several essential advantages and attractive properties compared with Si:

(1) In spite of indirect and narrow band gap of Si, most of the III-V materials have direct band gaps and luminescence efficiency is much larger than that of Si.
(2) Most III-V compound semiconductors posses high electron mobility due to much smaller electron effective mass than Si.
(3) Typical III-V materials possess wide band gaps (GaAs:1.43eV, InP:1.35eV in room temperature), which gives semiconductor devices capability to operate in high temperature environments. Furthermore, due to wide band gaps, semi-insulating substrates with the resistivity of 10^7-10^8 Ω·cm can be realized in III-V compound semiconductors by using deep levels. This makes devices isolation easier and the parasitic capacitance between devices can be very much reduced.
(4) The availability of mixed alloy semiconductors is very attractive and useful. The material properties such as the band gap and the lattice constant can continuously be changed by changing the composition ratio of mixed alloy. Therefore, it is possible to form high quality heterojunction between different semiconductors under the lattice-matched condition or the pseudomorphic lattice matching with strain.

For the reasons described above, optoelectronic devices such as light emitting diode (LED), semiconductor laser, photo-detector for various light wave length and high-frequency (micrometer-wave, millimeter-wave, etc.) devices including high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs) are

realized by III-V compound semiconductors, where equivalent function and performance are difficult to be realized by Si. With far more development of Si-based logic ICs, the needs for high speed, high density communication systems becomes strong towards multi-media era in very near future. Therefore, the importance of III-V compound semiconductor devices is growing rapidly now.

1.1.2 *The status of metal/III-V compound semiconductor interfaces in semiconductor devices*

Previous semiconductor devices are composed by various semiconductor interfaces, which are insulator/semiconductor (I-S) interface, semiconductor/ semiconductor (S-S) interface and so on. Metal/semiconductor (M-S) interface is an basic and important element for realization of the semiconductor devices. This interface is mainly classified into two different types. The one is "Ohmic contact" that follows Ohm's low in I-V characteristics and the another is "Schottky contact" which has the rectification property in I-V characteristics. This is due to electric barrier formed at the M-S interface, which is called "Schottky barrier". This Schottky barrier plays very important roles in organization of various functions of present semiconductor devices. Most of the semiconductor devices cannot help establishing without the Schottky barriers.

Because of their importance in direct current and microwave applications and as tools in the analysis of other fundamental physical parameters, the M-S interfaces have been studied extensively. Specifically, the M-S contacts have been used as the gate electrodes of a field-effects in MESFETs and HEMTs, millimeter and submillimeter detector diodes, photodetectors, solar cells and so on. The earliest systematic investigation on M-S rectifying systems is generally attributed to Braun, who in 1874 noted the dependence of the total resistance on the polarity of the

applied voltage and on the detailed surface conditions.[1] The point-contact rectifier in various forms found practical applications[2] beginning in 1904. In 1938, Schottky suggested that the potential barrier could arise from stable space charges in the semiconductor alone without the presence of a chemical layer.[3] The model arising from this consideration is known as the Schottky barrier.

The importance of III-V semiconductor Schottky barriers is also emphasized by the difficulty of formation of well-behaved insulator/III-V semiconductor interface such as SiO_2-Si interface. This is due to a large amount of interface state existing at insulator/III-V compound semiconductor interfaces, whose density is 1 or 2 order larger than that of 10^{10}~10^{11} $cm^{-2}eV^{-1}$ in SiO_2/Si system. This problem prevents the realization of metal/insulator/semiconductor (MIS) devices which is necessary for highly integrated circuits of III-V compound semiconductor devices. On the other hand, stable and enough large Schottky barriers can be realized easily on GaAs and related materials. Therefore, they are widely used for gates of FETs and the GaAs MESFET has been practically used as ICs with low integration level or MMICs (monolithic microwave integration circuits).

Control of Schottky barrier height (SBH) is very interesting issue in a semiconductor engineering, because the threshold voltage control of rectifiers and FETs, suppressing the gate leakage current by high barrier, reducing ohmic contact resistance and so on become possible. Therefore, many attempts have been made for this purpose. On the other hand, the formation mechanism of Schottky barriers have not been clear yet, although it is necessary for the SBH control. It is known that gap states generated at M-S interfaces dominate the formation of Schottky barrier as predicted by Bardeen.[7] In III-V compound semiconductor M-S interfaces, the position of interface Fermi level is fixed within a certain narrow range of the band gap due to high density gap states located at interfaces. This phenomenon is called "Fermi

level pinning". Several models are proposed to explain the origin of the interface states.[8-10] However, at present, they do not completely succeed in explaining those pinning positions. Recently, detailed investigation of the M-S interfaces comes to be possible by the development of novel interface/surface characterization methods in atomic scale, such as scanning tunnel microscopy (STM)[4] and scanning tunnel spectroscopy (STS)[5], ballistic electron emission microscopy (BEEM)[6]. These methods gives us much more information about the formation mechanism of the M-S interface, however, far more investigation is needed for full understanding of the mechanism and the origin of the interface state. Our research group also insists on unified disorder induced gap states (DIGS) model to explain the generation mechanism of the interface states.[11,12] According to this model, the origin of the interface state is the disorder generated near the semiconductor surface at the time of interface formation, and the decrease of the disorder is considered to result in the decrease of the gap state. Therefore, to establish the method of control of the interface so as to decrease the disorder, which is called "interface control", is a shortcut to obtain a applicable metal/III-V compound semiconductor interface. Based on this idea, a special treatment of the M-S interface or inserting interface layer into the M-S interface resulting in the improvement of an interface structure are considered to be most possible ways to control of SBH.

1.1.3 *Quantum effect devices for future electronics*

Great efforts to scale down of semiconductor devices have been made for realizing high performance, high speed, high integration, and low power consumption of the devices, which follows well-known "scaling principle".[13] However, this principle is broken when the device dimension reach nanometer order, because the "wave-particle" feature of electron that is "quantum effects" appear. Moreover, to

realize high density and high speed signal processing capability as high level as human brain by the semiconductor ICs, newly functional devices and new architecture need to replace Neimann's architecture organized by the combination of switching and memory devices of which dominant physics has been used since Shockley, Bardeen and Brattain's transistor. The limitation of the previous approach is predicted formerly, and "quantum effect devices" have been studied both for fundamental researches and device applications actively, as next generation devices. The quantum phenomena interest us from the view point of not only its physics but also device applications, for example, single mode transport of electron waves, control of wavelength and phase of the electron waves, interference of the waves, tunneling, and Coulomb blockade due to single electron charging. For the study of quantum effects, III-V compound semiconductors have been widely used because of following reasons.

(1) Mean free path is as long as submicron-meter or micrometer order and this enable quantum wave to coherent transport in the structure without phase breaking.
(2) The size that the "wave" feature of electron appears is larger than those of metals or Si.
(3) Ideal potential can be formed by using heterointerfaces.
(4) Precise control of electron density and wave length of electron wave are possible by utilizing heterostructures.
(5) It is possible to control thickness of epitaxial layers in atomic order.

Most of these advantages are supported by the development of epitaxial growth techniques such as molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE) techniques of III-V compound semiconductors. These sophisticate growth techniques have made us to fabricate various layer structures in atomic order and to study various quantum mechanical phenomena experimentally.

The one of the famous examples of the study in this area is a semiconductor superlattice by Esaki and Tsu in 1969-1970,[14] which is a one-dimensional periodic structure having artificial alternating layers with its period less than the electron mean free path. In 1978, Dingle et al. confirmed the formation of two-dimensional electron gas (2DEG) with extremely high mobility in the modulation-doped GaAs/AlGaAs superlattice.[15] Single and multiple quantum well structures have been also studied extensively.

The quantum wires and dots with low dimensions are attractive and important quantum structures. Lasers applying quantum wires or quantum dots are expected to show excellent performance that is very narrow emission linewidths, lowered threshold current and reduced temperature dependence of threshold current due to the additional sharpening. The quantum wire and dot also give interesting and useful properties to electron-transport devices. For example, H. Sakaki theoretically predicted extremely high electron mobility in the quantum wire due to suppression of the elastic scattering.[16] Transport through single- or multiple-quantum dots have attract us very much in a resent few years because of new phenomenon due to single electron charging and single electron tunneling effects, so-called Coulomb blockade phenomena,[17] which are caused by "particle" feature of electron having discrete unit charge e=1.6x10^{19} C. These phenomena strongly connect to the ultimate electron device which operate only a single electron.

If these quantum devices can operate stably in near room temperatures, they may lead to a revolution of the fundamental architecture of LSIs from the physical device level up to the system level.

1.2 The purpose of this work

The function of a semiconductor device is realized by design and control of electrical potential to control the behavior of electrons. Interfaces obtained by the combination of semiconductor and various materials give such a potential. Especially, the M-S interface is one of the most important element for construction of semiconductor devices since it forms large potential barrier at the interface. However, in order to realize quantum effect devices which are promised as next-generation semiconductor device, more precise potential control in nano-scale is needed so as to control smaller number of electron that behaves as quantum-wave or quantum-particle.

Establishment of systematic control of III-V semiconductor Schottky barriers and realization of quantum effect devices are very important issues, respectively. Moreover, if Schottky barrier can be well controlled, it becomes very attractive tools for realization of quantum effect devices since it gives well-controlled electrical potential.

The purpose of this work is to find and establish a systematic method of control of III-V compound semiconductor Schottky barrier and to apply these Schottky barriers to realization of more practical quantum effect devices. The following specific points are focused in this work.

(1) Basic study and investigation of control method of metal/III-V compound semiconductor interfaces in view points of chemical states of interfaces, Schottky barrier height and carrier transport through the interfaces.

(2) Proposition, fabrication and characterization of novel quantum effect device structures including lateral surface superlattice, quantum wire and single electron devices which are realized by SBH-controlled Schottky interfaces and Schottky in-plane-gates and wrap-gate structures.

1.3 Synopsis of each chapter

In **chapter 2**, the basic physics of M-S interfaces including several models for formation mechanism of Schottky barrier and characterization methods of M-S interface, x-ray photoelectron spectroscopy and several electrical characterizations are described. The ultrahigh vacuum-based fabrication/characterization system used in this work consisting molecular beam epitaxy (MBE) chamber, x-ray photoelectron spectroscopy (XPS) chamber, metal deposition chamber, focused ion beam (FIB), electron beam (EB) lithography chamber is also introduced.

In **chapter 3**, theoretical study of Schottky barrier height (SBH) control by two methods is made, which are improvement of interface property and inserting interface control layer at M-S interfaces. The basic concept of the control methods based on the unified DIGS model are explained, first. Theoretical calculation of SBH controlled by ICL is performed for ideal case and realistic case considering band gap narrowing effect of the ICL due to strain and heavy doping and interface states at IC L/semiconductor interface. From the calculation, a few requirements are derived theoretically for ICL materials to sufficient control of Schottky barrier height with retaining ideal current transport.

In **chapter 4**, the results of experimental study of various metal/III-V compound semiconductor interfaces and the result of optimization of ICL for SBH control are described. Chemical and electrical characterization were performed on these interfaces in view of not only chemical status and Schottky barrier height but also carrier transport through the interface. It is indicated that the most of the M-S system has an interface layer and it plays important role in Schottky barrier height and current transport properties.

In **chapter 5**, control method of GaAs and InP Schottky barrier heights by Si ICL technique are investigated experimentally. This consists inserting MBE grown ultrathin Si layer into the M-S interface. Doping and Si ICL thickness dependence of

Schottky barrier heights are discussed. It is pointed out that Si ICL must be pseudomorphic to the compound semiconductor and GaAs and InP SBH can control over the range of 300meV, when the pseudomorphic condition is satisfied.

In **chapter 6**, an unique approach to formation Schottky interfaces by in-situ electrochemical process and experimental results of Schottky barrier formation by this method are described. It is found that the metal-workfunction dependence of SBH is improved by this method because of low energy and damage free process. The result of application of this method to Pt gate MESFETs is also described.

In **chapter 7**, the result of application of present SBH control technique by doped Si ICLs to a novel lateral surface superlattice (LSSL) structure is described. A LSSL device is the one of attractive quantum effect devices, which causes electron-wave interference by introducing periodic potential into compound semiconductor heterointerface form its surface. In this study, this potential modulation is achieved by alternation of 200nm-pitch Schottky gates with different SBH controlled by Si ICLs. By the I-V and EBIC characterization, it is found that the effective potential modulation is introduced in the structure and this method is useful for realization of quantum effect devices.

In **chapter 8**, novel quantum nanostructures utilizing potential control of 2DEG by Schottky in-plane gate (IPG) and warp gate (WPG) are introduced and discussed based on the result of potential characterization by electron beam induced current (EBIC) method. First, the EBIC method is explained, which can directly characterize electric field and potential in the III-V compound semiconductor devices. Then, Schottky IPG and WPG structures is found to be effective and useful for realization of quantum effect devices through the application of the EBIC method to the various quantum nanostructures utilizing Schottky IPGs and WPGs.

In **chapter 9**, novel single-electron transistors (SETs) utilizing potential control of 2DEG by Schottky IPG and WPG are described. Single and multiple-dot devices are fabricated and characterized. All the fabricated SET shows clear conductance

oscillation and its maximum operation temperature is found to be much larger than that of SETs realized by the split-gate structure. These results shows the present Schottky IPG and WPG structures are effective and useful.

Chapter 10 summarizes the present work and gives the conclusions.

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Chapter 2
Physics and Characterization Methods of Metal/Semiconductor Interfaces

2.1 Introduction

Metal/semiconductor (M-S) contacts are mainly classified into two different contacts. The one is ohmic contact that follows Ohm's low in its I-V characteristic and the another is Schottky contact which shows the rectification property in its I-V characteristic. This is due to electric barrier formed at M-S interfaces, which is called Schottky barrier. The Schottky barriers show several interesting properties including the rectification, variable capacitance and etc. They play very important roles on present semiconductor devices.

An artificial control of the Schottky barrier height (SBH) will evidently be extremely useful for device applications. Unfortunately, however, the SBH values of III-V compound semiconductors are known to depend on the semiconductor material, but hardly on the work function of the metal as is expected from the Schottky's ideal model.[1] This phenomenon is called "Fermi-level pinning" whose mechanism has been a long standing issue of dispute among various models. In order to control the SBH, it is important to understand the basic idea of formation mechanism of Schottky barrier.

In this chapter, in first, the basic model of formation of M-S interfaces including Schottky contact and ohmic contact, and two limits of Schottky barrier formation mechanism called Schottky limit[1] and Bardeen limit[2] are described. Then, the proposed models for Schottky barrier formation mainly concerned with the origin of interface state are introduced. Next, the basic physics and properties of Schottky interfaces are shown briefly. Finally, the various characterization methods of M-S

interfaces and instrument used for formation and characterization of M-S interfaces in this work are described.

2.2 Model for formation mechanism of Schottky barrier

2.2.1 *Ideal condition and surface states*

When a metal is making intimate contact with a semiconductor, electrical potential is formed at the interface which is well known Schottky barrier. Basic two limiting cases are considered for this barrier formation.

The one is Schottky limit.[1)] In this limit, surface states are assumed to be absent in the semiconductor surface. The surface state is electron state that discharges by capturing or emitting electron exists in forbidden band of the semiconductor surface. **Figure 2-1** shows the electronic energy relations at an ideal contact between a metal and an n-type semiconductor based on Schottky's model. If thermal equilibrium is established, the Fermi levels on both sides line up. Relative to Fermi level (E_F) in the metal, the Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work functions, denoted by $q\phi_m$ for the metal and $q(\chi - V_n)$ for the semiconductor, where $q\chi$ is the electron affinity measured from the bottom of the conduction band E_C to the vacuum level, and qV_n equals to E_C-E_F. The potential difference $q\phi_m$-$q(\chi+V_n)$ is called the contact potential. As the distance δ decreases, increasing negative charge is built up at the metal surface. An equal and opposite charge must exist in the semiconductor. Then, the value of the Schottky barrier height (SBH) $q\phi_{Bn}$ is given by

$$q\phi_{Bn}=q(\phi_m-\chi). \qquad (2.1)$$

The barrier height is the difference between the metal work function and the electron affinity of the semiconductor. For a p-type semiconductor, the barrier height $q\phi_{Bp}$ is given by

$$q\phi_{Bp}=E_g-q(\phi_m-\chi) \qquad (2.2)$$

For a given semiconductor and for any metals, the sum of the barrier heights on n-type and p-type semiconductor is expected to be equal to the bandgap. On the other hand , the contact potential is negative, electrical potential is no formed as shown in **Fig.2-1(g)**. This situation does not give rectifying property, thus this is called Ohmic contact.

The second limiting case is shown in **Fig.2-2**, where a large density of surface states is assumed to be present on the semiconductor surface. This case corresponds to Bardeen limit.[2] When the distance between the metal and the semiconductor is long enough, equilibrium is not established between them, however, it is established between the surface states and the bulk of the semiconductor. In this case, the surface states are occupied to a level E_0 which is charge neutrality point. When the M-S system is in equilibrium, the Fermi level of the semiconductor relative to that of the metal must fall an amount equal to the contact potential $q\phi_m-q(\chi+V_n)$ and electric field is produced between the metal and the semiconductor. If the density of the surface states is sufficiently large to accommodate any additional surface charges resulting from diminishing δ without appreciably altering the occupation level E_0, the space charge in the semiconductor will remain unaffected. As a result, the barrier height is determined by the property of the semiconductor surface and is independent of the metal work function at all. In Bardeen limit, SBH for n-type and p-type semiconductor is given by,

$$q\phi_{Bn}=E_g - E_0$$

$$q\phi_{Bn}=E_0. \qquad (2.3)$$

Figure 2-3 shows the experimentally obtained metal-workfunction dependence of SBH for some semiconductors.[3] The metal-work function dependence of SBH is generally characterized by interface index,

$$S=d\phi_B/d\phi_m. \qquad (2.4)$$

Interface index of each semiconductor material in **Fig.2-3** is smaller than unity and is different from each other. Especially, SBHs of Si and GaAs which are widely used for semiconductor devices hardly depends on the metal workfunctions. One can find it difficult to change SBH by selection of metal material. The interface index of various material as a function of electron affinity is shown in **Fig.2-4**. The tendency that wide band gap materials have near unity of interface index can be seen. On the other hand, the interface index of most of useful semiconductors whose band gap are about 1~2eV are much smaller than unity. However, it is reported that S can be change by special interface treatment.

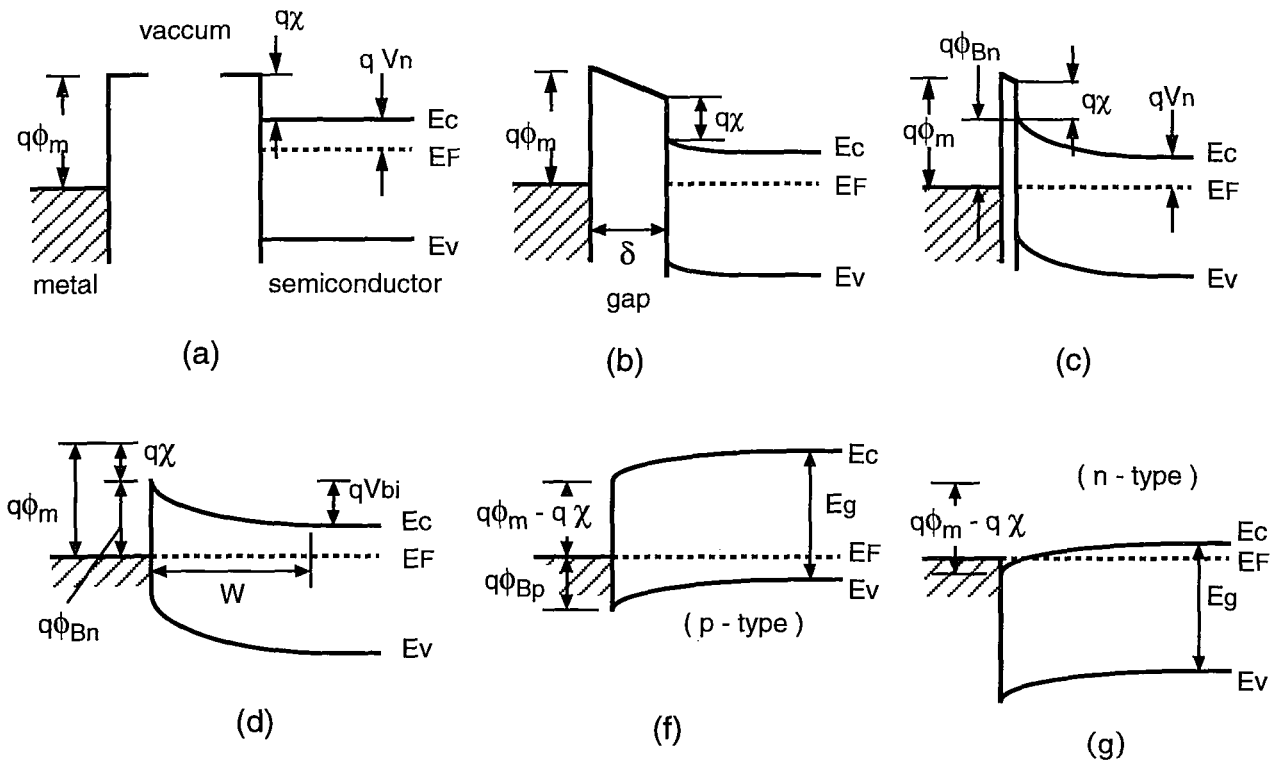


Fig.2-1. Electric energy relations at an ideal contact between a metal and a n-type semiconductor based on Schottky's model (Schottky limit).

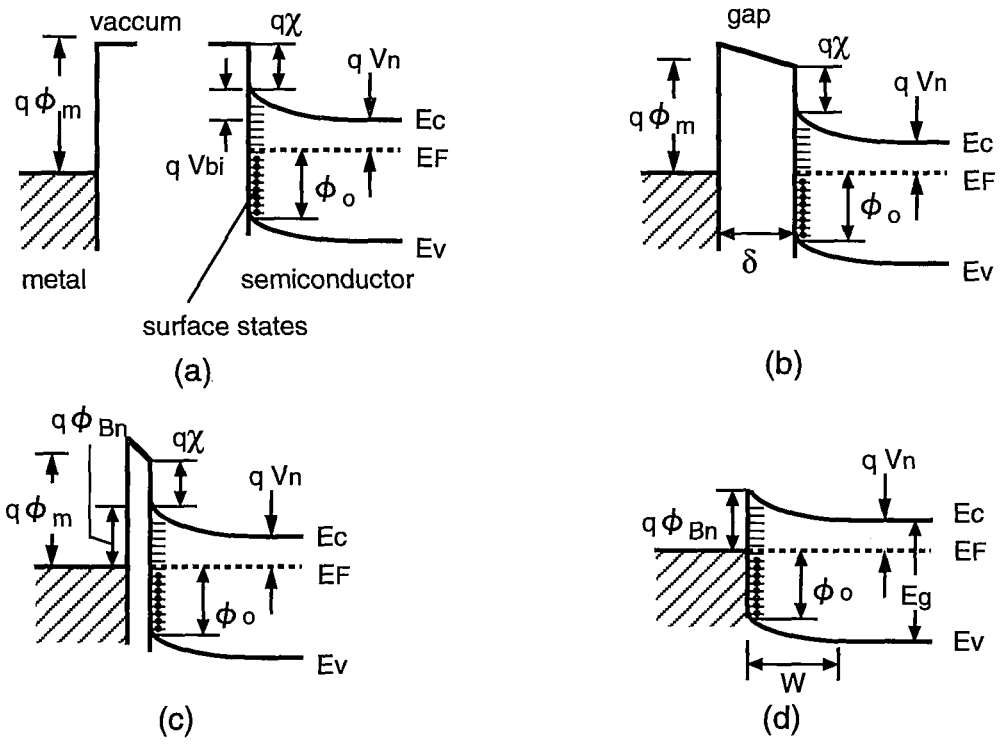


Fig.2-2. Electronic energy relations at a M-S contace with interface states based in Bardeen's model (Bardeen limit).

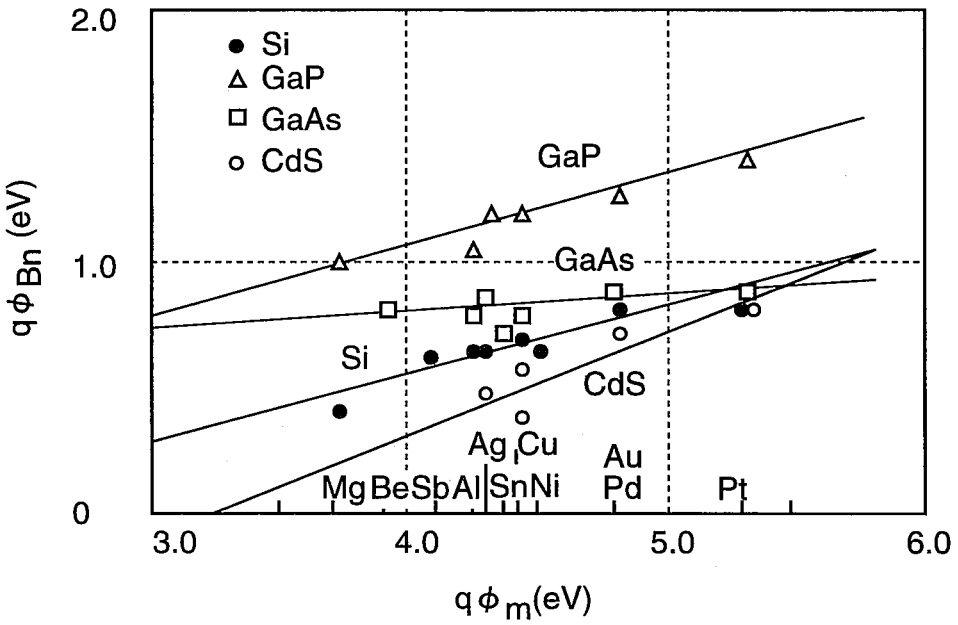


Fig.2-3. Experimentally obtained metal-workfunction dependence of SBH (ref. 3).

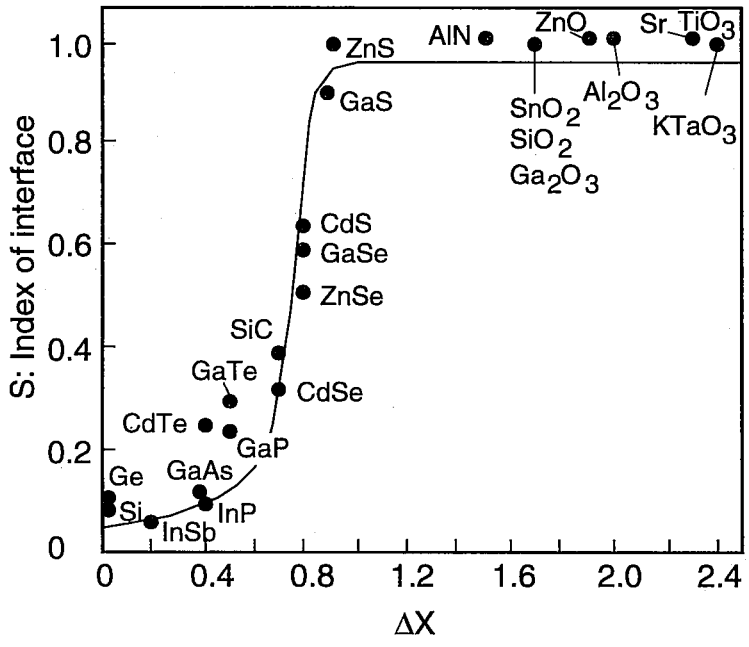


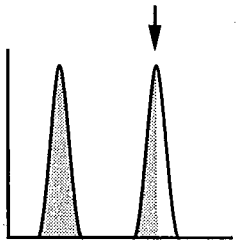
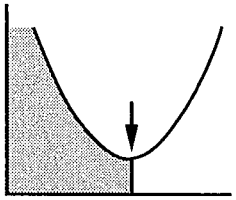
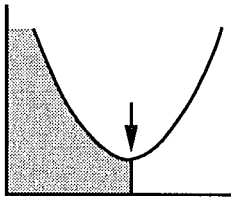
Fig.2-4. Interface index of various materials as a function of electron affinity (ref. 3).

2.2.2 *Previous models for Schottky barrier formation*

(1) Models for Fermi level pinning

Since the days of Schottky and Bardeen, the mechanism which is responsible for Fermi level pinning at the M-S interface has been a long standing issue, and numerous models have been proposed and discussed. Particularly, recent extensive studies on semiconductor surfaces have revealed existence of hitherto unnoticed strong correlations among semiconductor/semiconductor (S-S), insulator/ semiconductor (I-S), M-S interfaces. Thus, the recent models attempt to account for these correlations in explaining the origin of Fermi level pinning. **Table 2-1** summarizes the major models of such nature. It includes the unified defect model by Spicer et al.[4,5], MIGS (metal-induced gap state) model by Heine[6] and Tersoff[7], DIGS (disorder-induced gap state) model by Hasegawa and Ohno[8,9] and the effective workfunction (EWF) model by Woodall and Freeouf[10].

Table 2-1. Various models for Fermi level pinning.

model	origin of pinning	N_{SS} distribution and pinning position	applicable interfaces	nature of pinning
Unified Defect Model	deep level related to stroichiometry (intersticial, vecancy)		S-S, I-S, M-S	extrinsic
MIGS Model	penetration of metal wave function		M-S	intrinsic
DIGS Model	disorder of bonds at surface		S-S, I-S, M-S	extrinsic
Effective Work Function Model	preciptation of As and P cluster at interface	pinned at E_F of metaric cluster	S-S, I-S, M-S	extrinsic

(2) Unified defect model[4,5]

The unified defect model was proposed by W.E.Spicer and co-workers in 1979. They found out by photoemission spectroscopy using synchrotron orbital radiation (SOR) that the Fermi level on cleaved surfaces of III-V semiconductors is pinned at the same position when they were absorbed to some metals or oxygen. Then, they thought the origin of these pinning phenomenon is the point defect generated on the surface by some material adsorption.

Figure 2-5(a) shows the generating process of defects. The defect is formed with the cohesion heat (or the reacting heat) of the surface, which is far large compared with the movement energy of atoms. It is one of evidence for the defect formation that the atoms which consist the semiconductor are detected on the metal surface after deposition. And it is expected that two kind of state in band gap are made because two kind of vacancy are possible on compound semiconductor surfaces.

Figure 2-5(b) shows the surface Fermi level position as a function of oxygen coverage on cleaved GaAs (110) and InP (110) surfaces. The Fermi level settles on two different energy positions with the case of n-type and p-type. These energy positions were thought to correspond to above two kind of defects shown as **Fig.2-5(c)**.

The Schottky barrier height of M-S interface due to the Fermi level pinning are thought to be decided corresponding to the energy levels of high-density defect state, which distribute energy incontinuously. And, as shown in **Fig.2-5(c)**, the distribution of gap state at interface possesses discrete defect states peals which are overlapped on the U-shaped distribution like as Si-MOS interface. This model can explain well that the Schottky barrier height is mainly decided by only semiconductors and the Fermi level pinning position of I-S interface is mainly same as that of M-S interface. But this model can not explain that the peak of defect state density is not detected for actual MIS structures.

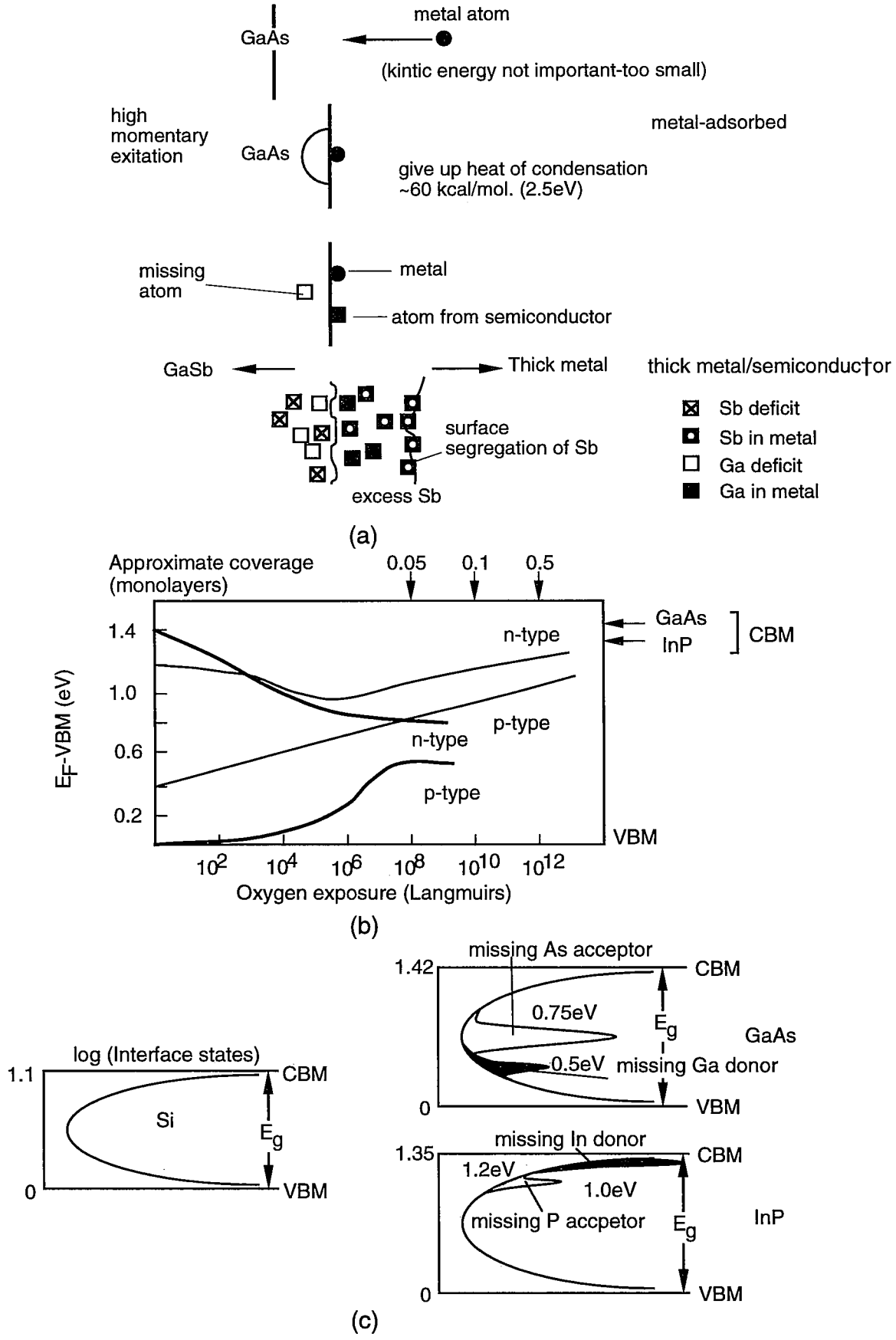


Fig.2-5. The concept of unified defect model (ref.4,5). (a) Generation process of defects, (b) the surface Fermi level positions as a function of oxygen coverage on cleaved GaAs (110) and InP (110) suefaces and (c) surface state distributions of Si, GaAs and InP.

(3) Metal induced gap state (MIGS) model[6,7]

In 1965, V.Heine insisted that the energy-continuous state, which can pin the Fermi level, is generated in the band gap near the interface owing to penetration of wave function of metal.[6] This wave function causes the mis-isolation of conduction and valence band and creates gap states in forbidden band. The state generated by metal wave function is called metal induced gap state (MIGS). Thus, the origin of MIGS is intrinsic. As shown in **Fig.2-6**, Cohen and co-workers calculated the wave function penetration on M-S interface.[11] And they presented that the Schottky barrier heights, which is calculated quantitatively according MIGS model agree well to the experimental results. But they used some of assumptions which are not essential.

This model can not explain that the Fermi level pinning position of I-S interface is mainly same as that of M-S interface and Schottky barrier height of M-S interface without oxide layer. But, recently, it was insisted by Tersoff[7] and is paid attention that MIGS possesses energy level of charge neutrality which is hybrid orbital energy like as that of DIGS model.

(4) Effective work function model[10]

The model proposed by J.M.Woodall and J.L.Freeouf is called the effective work function (EWF) model, in which the Fermi energy position at the surface (or interface) is not due to or fixed by surface states but rather is related to the work functions of microclusters of the one or more interface phases resulting from either oxygen contamination or metal-semiconductor reactions. They proposed this model from experimental study of metal/low temperature grown MBE GaAs or As deposited GaAs and related materials. The expected behavior is shown in **Figs.2-7(a)~(c)**. The UHV cleaved (110) surface is free of intrinsic surface states and hence E_F is uniform as seen in left of **Fig.2-7(a)**. All other surfaces exhibit band bending prior to any

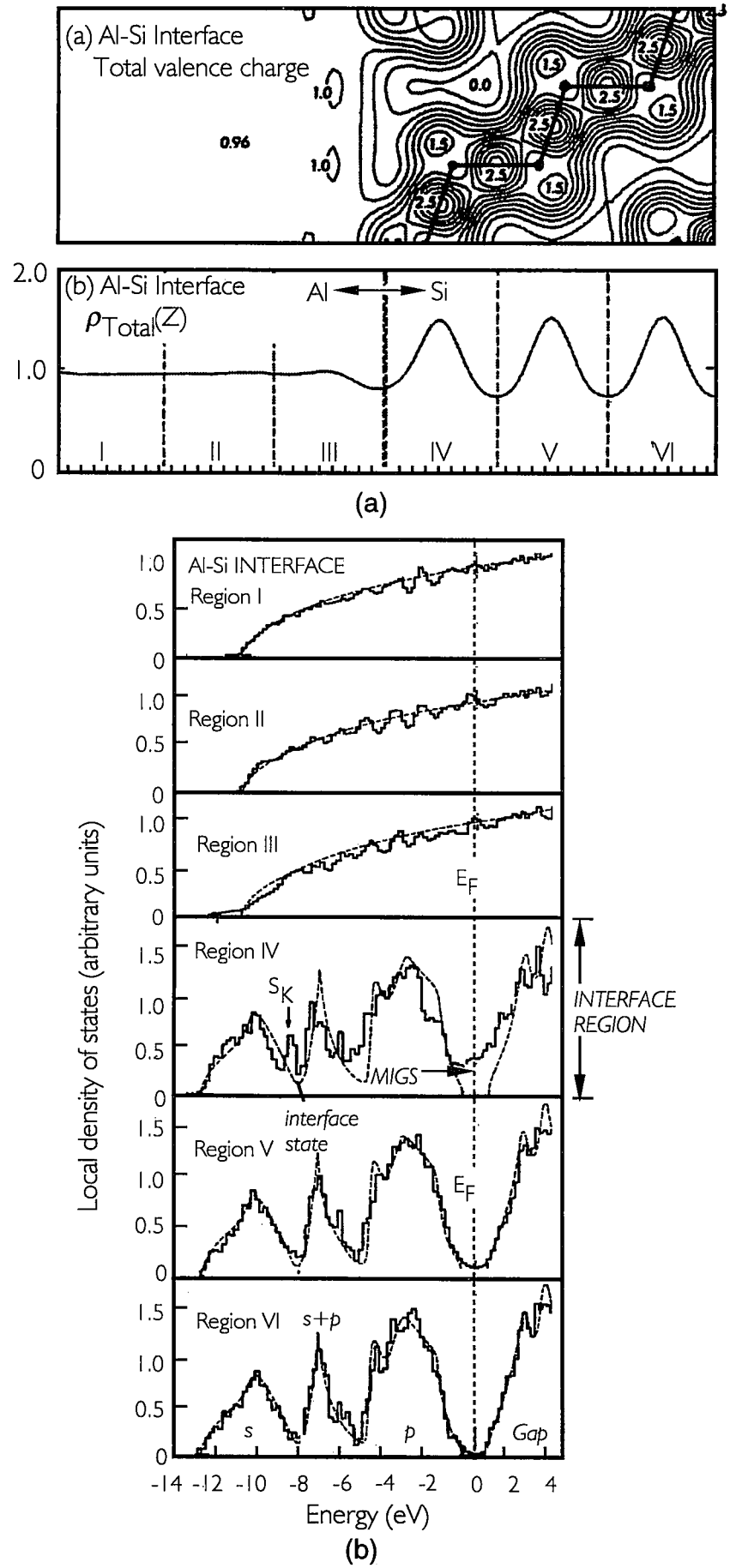


Fig.2-6. (a) Calculated wavefunction penetration of M-S interface based on MIGS model and (b) calculated density of states in each region shown in (a). (ref. 8).

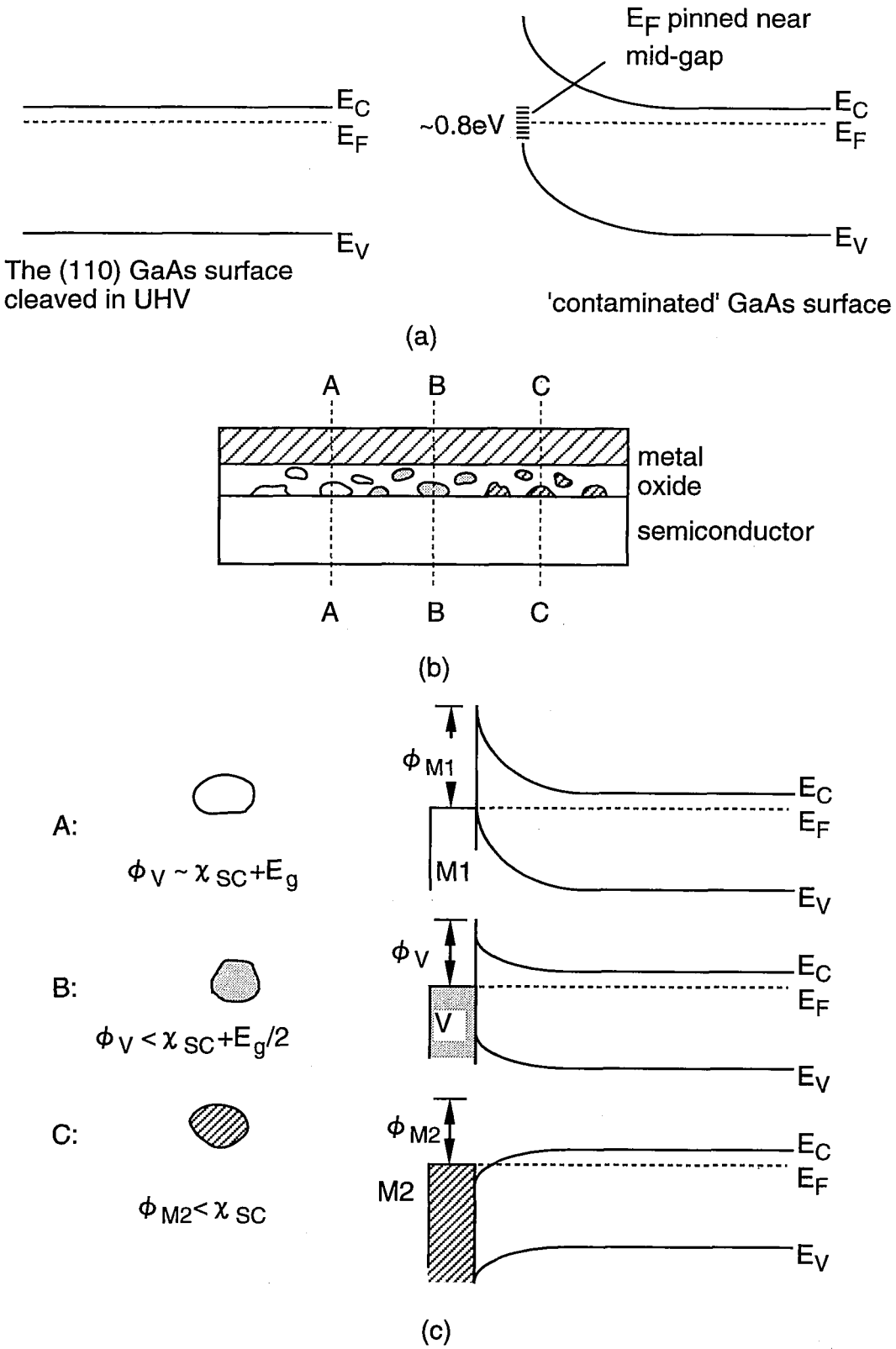


Fig.2-7. The concept of EWF model. (a) Band diagrams of cleaved (110) GaAs surface and contaminated surface, (b) metal/compound semiconductor contace with micuroclusters of different phases and (c) band diagrams of interfaces with the different micuroclusters.

intentional surface treatment or metal deposition. The theory requires that these pinned surfaces already contain microclusters of interface phases due to their exposure to air or any other surface contaminating environment as shown in right hand side of **Fig.2-7(a)**. When a metal is deposited, there is a region at the interface which contains a matrix of native oxide embedded with microclusters of different phases, which having its own work function as shown in **Fig.2-7(c)**. Since the model does not require surface state.

(5) Unified disorder induced gap state (DIGS) model[8,9]

The unified disorder induced gap state (DIGS) model is a advanced model of the surface disorder model. In the unified DIGS model, it is insisted that the interface state continuum should be generated on not only I-S interface but also M-S interface and S-S interface.

The property of DIGS continuum is explained as follows. Deposition of metal or insulator disturbs the crystalline perfection of semiconductor, which causes the disorder of bond length and bond angle in the interface region because of the stress occurred by lattice mismatch, the composition shift from stoichiometry due to chemical reaction, point defect and so on. These give the incomplete separation of bonding state and antibonding state of the bond disordered, shown as **Fig.2-8** and then the DIGS continuum that has continuous energy and spatial distribution of gap states is generated. The distribution of interface state due to the DIGS is U-shaped. The DIGS is separated into acceptor-like state related to antibonding and donor-like state reflected to bonding. The boundary of these states is characterized by sp^3 hybrid orbital energy E_{HO} which is electrical charge neutrality level and is the point of minimum density of DIGS.

The DIGS is also spatially distributed in the vertical direction on the interface which is characterized by transmission electron microscope (TEM) and RBS

(Rasaford back scattering) and the thickness of disordered layer is thought to be 1-10 Å for semiconductor. Such spatial distribution of interface state causes the hysterisis of C-V characteristic for metal/insulator/semiconductor (MIS) structures.

The Schottky barrier is formed on M-S interface because the surface Fermi level is pinned at E_{HO} of DIGS whose density is much higher than that of I-S interface. The DIGS model explains that the Schottky barrier height is determined by the balance between metal work function and interface state charge which is generated owing to slight shift of Fermi level from E_{HO}.

From a simple tight-binding picture, the charge neutrality energy level of the DIGS density spectrum is given by E_{HO}.

$$E_{HO} = -[(\varepsilon_s+3\varepsilon_p)]_{av.} / 4 \qquad (2.5)$$

where ε_s and ε_p are atomic term energies and av. denotes average over anions and cations. This energy level is equivalent to the Tersoff's midgap energy.7) The position of E_{HO} is independent of details of disorder, and lies approximately at 5.0eV from vacuum for major semiconductors. For GaAs, E_{HO} lies at 0.47eV above the valence band maximum E_V and for InP, it lies at 0.36eV below the conduction band minimum, E_C. It has been found out that the E_{HO} is related to the band line-up of heterojunctions and the energy level of transition metal impurities, ELs and DX center. **Figure 2-9** shows the relation concerning III-V compound semiconductors and their alloys. Detail discussion of Schottky barrier formation based on the DIGS model will be shown in **chapter 3**.

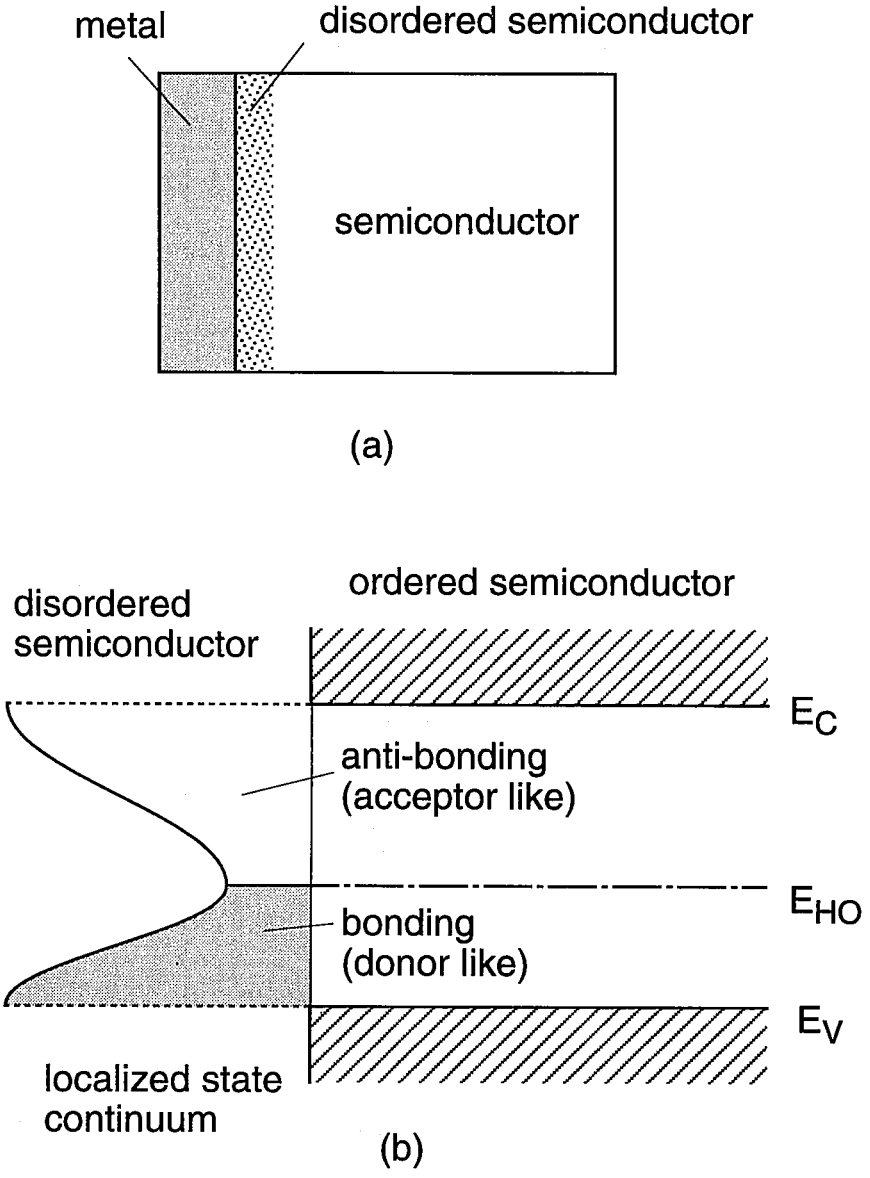


Fig.2-8. (a) Disordered layer formed at semiconductor interface and (b) U-shaped DIGS continuum due to incompleteness of energy-band separation by disorder.

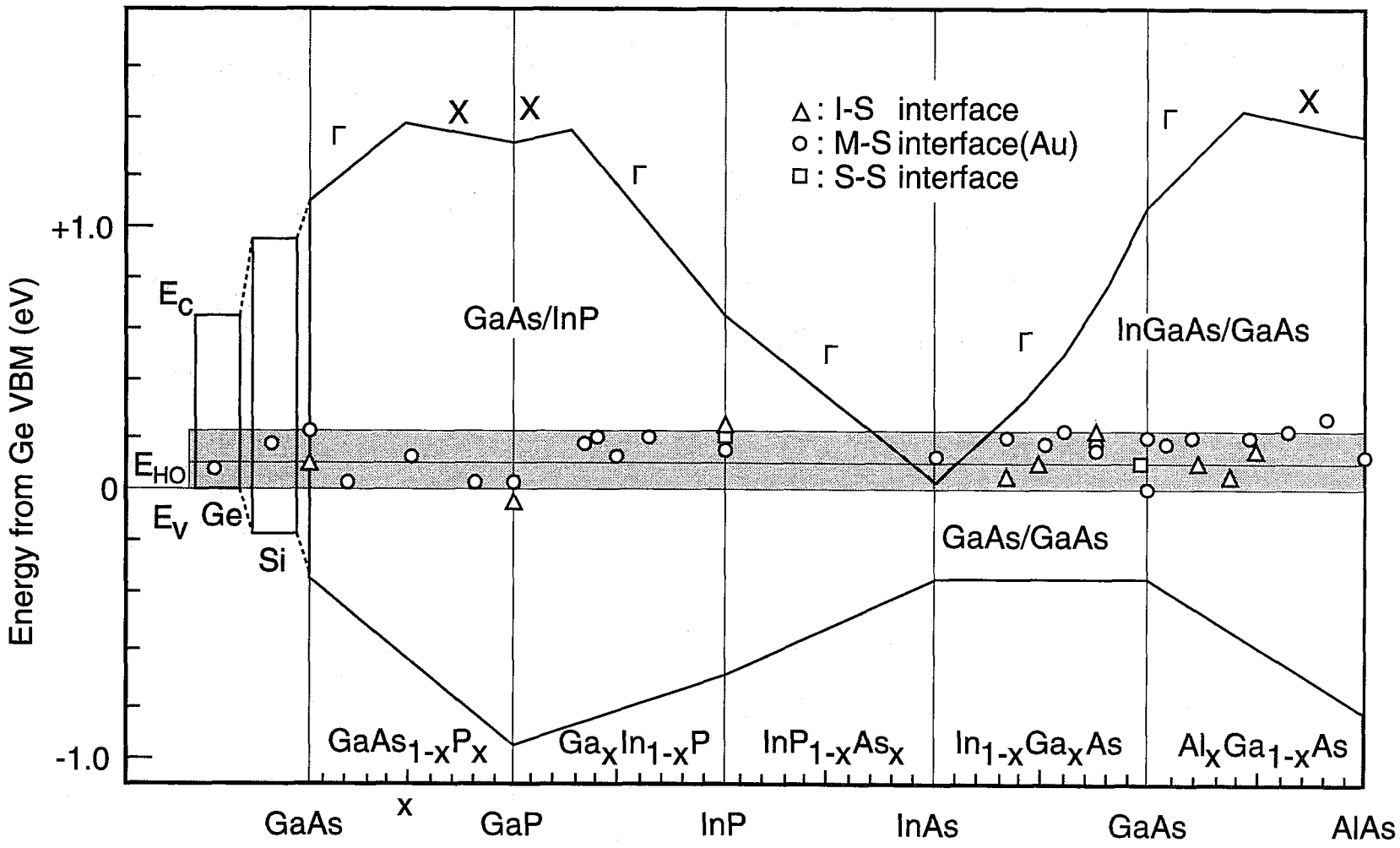


Fig.2-9. Relative energy position of conducntion and valence band edges of III-V compound semiconductors and their alloys.

2.3 Basic properties of M-S interface

2.3.1 *Electric potential and depletion layer*

When a metal contacts intimately with a semiconductor, the conduction and valence bands of the semiconductor are brought into a definite energy relationship with the Fermi level in the metal as described previous section. Once this relationship is known, it serves as a boundary condition on the solution of the Poisson's equation in the semiconductor. Electric force line form metal surface is terminated with the space charge in the semiconductor and this forms depletion layer of which width is W.

Under the abrupt approximation (so-called depletion approximation) that $\rho \sim qN_D$ for $x<W$ and $\rho \sim 0$, and $dV/dx \sim 0$ for $x>W$, where W is the depletion width. The electric potential at $x=0$ and $x=W$ are ϕ_B and E_C-E_F, respectively. Solving the Poisson's equation under the boundary conditions given above, potential $V(x)$, electric field $E(x)$ and W expressed by next equations are obtained.

$$W=[2\varepsilon_s/qN_D\ (V_{bi})]^{1/2} \tag{2.6}$$

$$|\boldsymbol{E}(x)|= qN_D/\varepsilon_s\ (W-x) = \boldsymbol{E}_m-(qN_D/\varepsilon_s)x \tag{2.7}$$

$$V(x) = qN_D/\varepsilon_s(W\cdot x - x^2/2) - \phi_{Bn} \tag{2.8}$$

where V_{bi} is built-in potential equals to ϕ_B-(E_C-E_F) and $\boldsymbol{E}_m$ is the maximum field strength which occurs at $x=0$, that is $\boldsymbol{E}_m=\boldsymbol{E}(x=0)=[2qN_D\ V_{bi}\ /\varepsilon_s\ ]^{1/2} = 2(V_{bi})/W$. The space charge Q_{sc} per unit area of the semiconductor is given by $Q_{sc}=qN_DW$ $=[2q\varepsilon_sN_D(V_{bi})]^{1/2}$ and then the depletion layer capacitance C per unit area are given by

$$C = |dQ_{sc}|/dV = [q\varepsilon_s N_D/2(V_{bi})]^{1/2} = \varepsilon_s/W \quad (2.9)$$

The barrier shape is slightly modified by image force near the contact, which is called Schottky effect. This effect causes the reduction of Schottky barrier height by $\Delta\phi_B$ and this value depends on the field, therefore effective Schottky barrier height shows the applied voltage dependence. $\Delta\phi_B$ is expressed by,

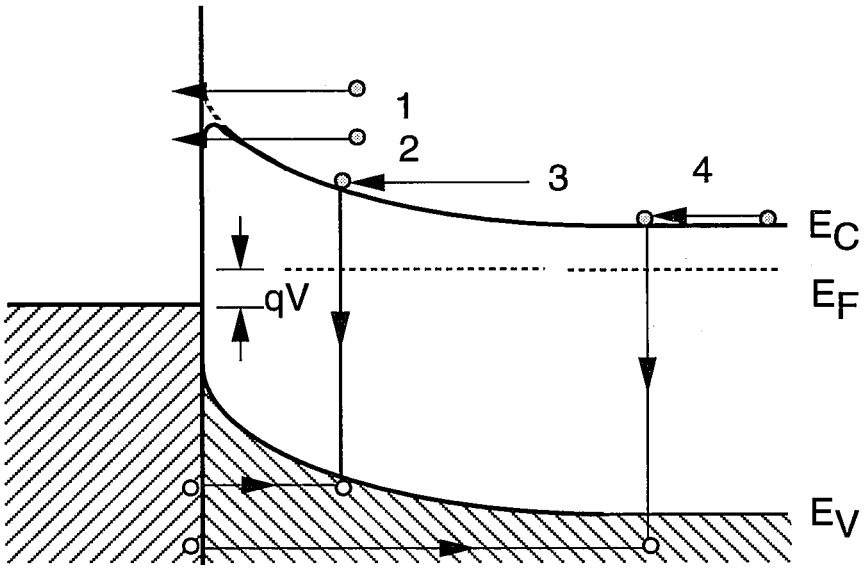
$$\Delta\phi_B = [\, qE_m/4\pi\varepsilon_0 \,]^{1/2}. \quad (2.10)$$

2.3.2 *Current transport processes*

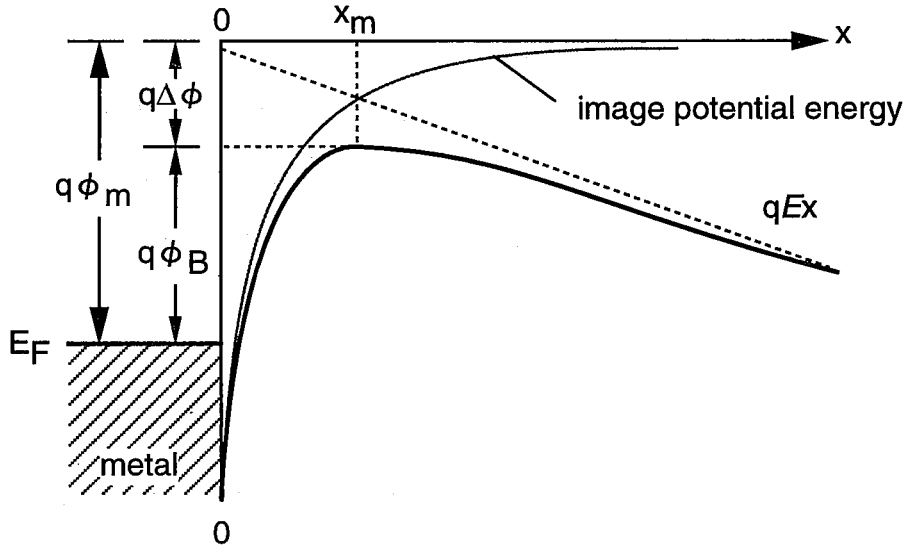
The current transport through a M-S interfaces is mainly due to majority carriers, in contrast to p-n junctions where the minority carriers are responsible. **Figure 2-10** shows four basic transport processes. These are (1) transport over the potential barrier which is assisted by thermionic emission or diffusion process, (2) quantum mechanical tunneling, (3) recombination in the space-charge region and (4) minority carrier injection. Various methods have been used to improve the interface quality and ideal current transport can be observed in recent Schottky diodes.

(1) Thermionic emission theory

The thermionic emission theory is applicable for most of semiconductors used in the present semiconductor devices, such as Si, GaAs, and InP. This theory by Bethe[12] is derived from the assumptions that the barrier height $q\phi_{Bn}$ is much larger than kT, thermal equilibrium is established at the interface that determines emission, and the existence of a net current flow does not affect this equilibrium. Then one can superimpose two current fluxes, that is one from metal to semiconductor, the other from semiconductor to metal, each with a different quasi-Fermi level, imref. Because of



(a)



(b)

Fig.2-10. (a) Basic electron transport processes through M-S interface. (b) Schottky effect.

assumptions above, the shape of the barrier profile is not important and the current flow depends on the barrier height only. The current density $J_{s\to m}$ from the semiconductor to the metal and $J_{m\to s}$ from the metal to semiconductor are then given by the concentration of electrons with energies sufficient to overcome the potential barrier and traversing in the x direction and considering the electron density of state, distribution function and the velocity required in the x direction to surmount the barrier. It is noted that the barrier height for electrons moving from the semiconductor into the metal is changed by the applied voltage, however, the barrier height for electrons moving from the metal into the semiconductor remains the same, the current flowing into the semiconductor is thus unaffected by the applied voltage. The total current density $J_{s\to m} + J_{m\to s}$ is given by

$$J_n = \frac{4\pi q m^* k^2}{h^2} T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$= A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$= J_{ST}\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$\simeq J_{ST}\exp\left(\frac{qV}{kT}\right) \qquad (qV > 3kT) \tag{2.11}$$

where

$$J_{ST} = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \tag{2.12}$$

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.13}$$

is the effective Richardson constant for thermionic emission, neglecting the effects of

optical phonon scattering and quantum mechanical reflection. For free electrons the Richardson constant A^* is 120A/cm^{2}K^2. When the image force lowering is considered, the barrier height ϕ_B in **eq.(2.12)** is reduced by $\Delta\phi$. The same expression as **eq.(2.11)** is obtained by diffusion theory [3], however, the expressions for the saturation current densities are quite different.

For semiconductors with isotropic effective mass in the lowest minimum of the conductio band such as n-type GaAs, $A^*/A=m^*/m_0$ where m^* and m_0 are the effective mass and the free-electron mass, respectively. For multiple-valley semiconductors the appropriate Richardson constant A^* associated with a single energy minimum is given by

$$\frac{A_l^*}{A}=\frac{\left(l_1^2 m_y^* m_z^* + l_2^2 m_z^* m_x^* + l_3^2 m_x^* m_y^*\right)^{\frac{1}{2}}}{m_0} \qquad (2.14)$$

where l_1, l_2 and l_3 are the direction cosines of the normal to the emitting plane relative to the principal axes of the ellipsoid, and m_x^*, m_y^* and m_z^* are the components of the effective mass tensor. For holes the two energy maxima at k=0 give rise to approximately isotropic current flow from both the light and heavy holes. Adding the currents due to these carriers, one can obtain by

$$\left(\frac{A^*}{A}\right)_{p-type}=\frac{m_{lh}^*+m_{hh}^*}{m_0}, \qquad (2.15)$$

where m_{lh}^* and m_{hh}^* are effective masses of light hole and heavy hole, respectively.

(2) Tunneling current

For a heavily doped semiconductor or for operation at low temperatures, the tunneling current may become the dominant transport process since the barrier width

becomes thin or the number of carrier which transports over the barrier assisted by thermionic emission decreases. This process is responsible for most ohmic contact. The expression for thermal emission will be modified to include both the thermionic emission and tunneling components. The current is proportional to the quantum transmission coefficient multiplied by the occupation probability in the one material and the unoccupied probability in the other material.

If the tunneling component dominates the current flow, the transmission coefficient has the form,

$$T(z) \sim \exp(-q\phi_{Bn}/E_{00}) \qquad (2.16)$$

with

$$E_{00} = qh_b/2\ (N_D/\varepsilon_s\ m^*)^{1/2}$$

and the tunneling current has a similar expression,

$$J_t \sim \exp(-q\phi_{Bn}/E_{00}). \qquad (2.17)$$

This equation indicates that the tunneling current will increase exponentially with $N_D{}^{1/2}$.It is interesting to note that tunneling current is essentially a constant for low doping but begins to increase rapidly when $N_D > 10^{17}cm^{-3}$.[3] The ideality factor, $n=q/kT\ dV/d(\ln J)$, is very close to unity at low doping and high temperatures. However, it can depart substantially from unity when the doping is increased or the temperature is lowered.

(3) Recombination in the depletion region

The recombination normally takes place through localized states, and according to the theory[13], the most effective centers are those with energies lying near the

center of the band gap. The theory of the current due to such recombination centers in Schottky diodes is similar to that for p-n junctions, and the current density for low forward bias is given approximately by

$$J_r = J_{r0}\exp\left(\frac{qV}{2kT}\right)\left\{1-\exp\left(-\frac{qV}{kT}\right)\right\} \qquad (2.18)$$

where $J_{r0}=q\cdot n_i\cdot W/2\tau_r$, n_i is the intrinsic electron concentration, proportional to exp(-$qE_g/2kT$), W is the thickness of the depletion region, and τ_r is the lifetime within the depletion region. This simple result embodies several rather drastic assumptions, namely that the energy levels of the centers coincide with the intrinsic level, that the capture cross-sections, which may differ by as much as three orders of magnitude. Depending on the ration of the capture cross-sections, the n value for recombination current may be between 1 and 2.[13] If one accepts **eq.(2-20)**, the total current density is given by the sum of thermionic emission current and recombination current.

2.4 Characterization method of M-S interfaces

2.4.1 *Current-Voltage measurement*

(1) Standard procedure

When the current assisted by thermionic emission is dominant, *I-V* characteristics of a Schottky contact in the forward direction in the case of $V>3kT/q$ is given by,

$$J=A^{**}T^{2}\exp\left(-\frac{q\phi_{B0}}{kT}\right)\exp\left(\frac{q(\Delta\phi+V)}{kT}\right) \qquad (2.19)$$

where ϕ_{B0} is the zero-field asymptotic barrier height, A^{**} is the effective Richardson constant, and $\Delta\phi$ is the Schottky barrier lowering due to Schottky effect. Since both A^{**} and $\Delta\phi$ are functions of the applied voltage, the forward *I-V* characteristics for $V>3kT/q$ is represented by $J\sim\exp(qV/nkT)$, as given previously in **eq.(2.11)**, where n is the ideality factor:

$$n=\frac{q}{kT}\frac{dV}{d(\ln J)}$$

$$=\frac{1}{1+\frac{d(\Delta\phi)}{dV}+\frac{kT}{q}\frac{d(\ln A^{**})}{dV}} \qquad (2.20)$$

The extrapolated value of current density at zero voltage is the saturation current J_s, and the barrier height can be obtained from the equation

$$\phi_{Bn}=kT/q\cdot\ln(A^{**}T^{2}/J_s). \qquad (2.21)$$

(2) Rhoderick plot [13)]

Recombination current is a common cause of departure from ideal behavior in Schottky diodes. Recombination current may therefore cause apparent deviations of ideality factor n from unity and of the pre-exponential term from the ideal value $A^{**}T^2 \exp(-q\phi_B/kT)$. Such departures become more pronounced at low temperatures. However, a logarithmic plot of $I/\{1-\exp(-qV/kT)\}$ against V shows the two components quite clearly, and illustrates very vividly the advantage of this method of plotting the I-V characteristics as shown in **Fig.2-11**.

(3) Norde plot[14)]

In the case that high series resistance exists, SBH is misevaluated from the I-V curve. Norde proposed the method to calculate SBH and series resistance in such a case by modified I-V plot called Norde plot. For the evaluation of SBH, one plots the curve given by the next function in first.

$$F(V)=V/2- kT/q \ln(I/SA^{**}T^2). \qquad (2.22)$$

When the series resistance exists, this plot shows minimum point in its curve. Obtaining the value of V_0 which gives minimum value of $F(V)$, the SBH is evaluated by using next equation.

$$\phi_B = F(V_0) + V_0/2 - kT/q \qquad (2.23)$$

The series resistance R is obtained by,

$$R = kT/q \cdot I_0 \qquad (2.24)$$

where

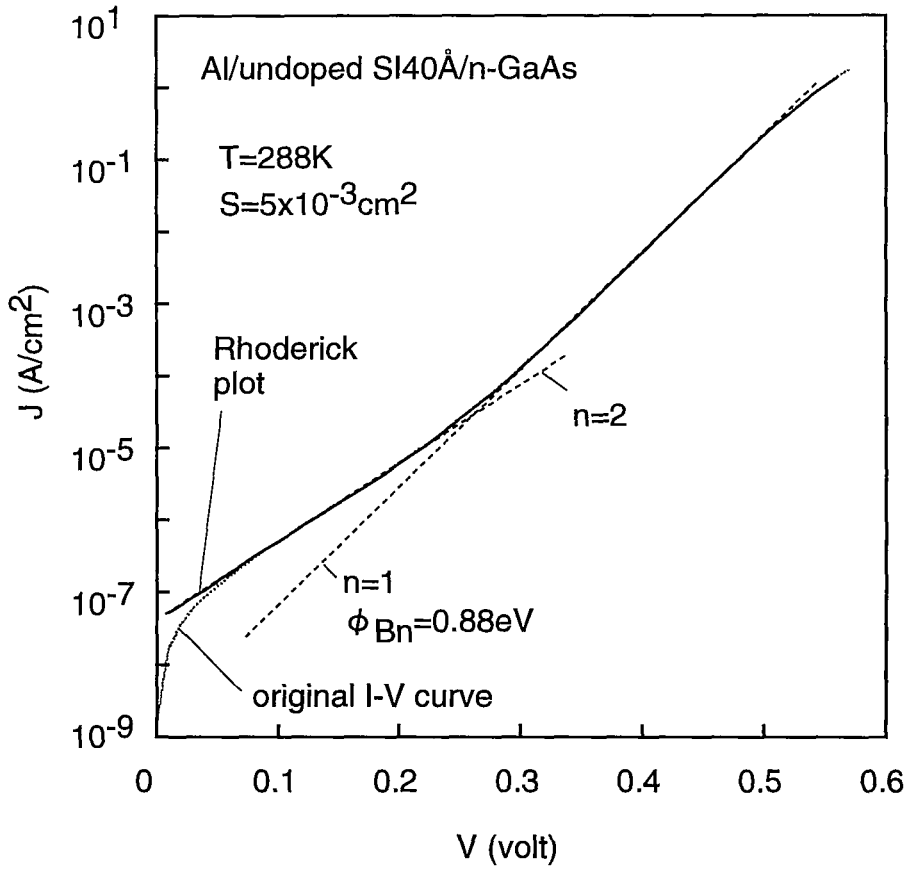


Fig.2-11. The example of Rhoderick plot

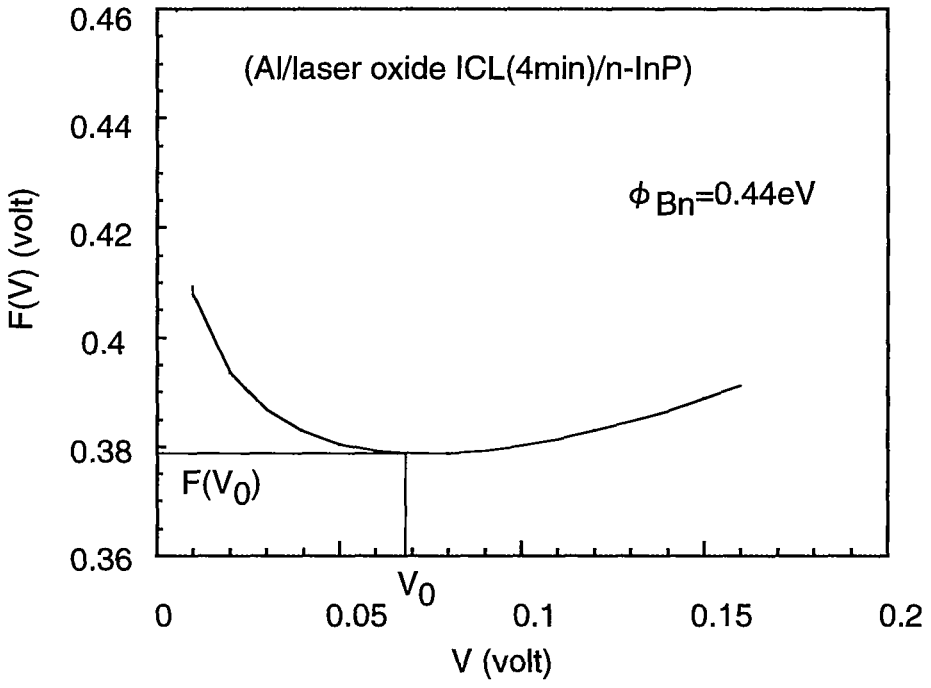


Fig.2-12. The example of Noede plot.

$$I_0 = S A^{**} T^2 \exp(qV_0/kT\text{-}1). \qquad (2.25)$$

The example of Norde plot is shown in **Fig.2-12**.

2.4.2 *Activation Energy Measurement (Richardson plot)*

This measurement consists the Arrhenius plot of saturation current. The principal advantage of SBH determination by means of an activation energy measurement is that no assumption of electrically active area is required. This feature is particularly important in the investigation of novel or unusual M-S interfaces, because often the true value of the contacting area is not known. In the case of poorly cleaned ore incompletely reacted surfaces, the electrically active area may be only a small fraction of the geometric area. On the other hand, a strong metallurgical reaction could result in rough nonplanar M-S interface with an electrically active area that is larger than the apparent geometric area. The other advantage for this measurement is that Richardson constant can be evaluate at the same time by this method. The Richardson constant becomes important parameter for considering the current transport through the M-S interface formed by various techniques.

If **eq.(2-11)** is multiplied by S_e, the electrically active area, next equation is obtained

$$\ln(I_F/T^2) = \ln(S_e A^{**}) - q(\phi_{Bn}\text{-}V_F)/kT \qquad (2.26)$$

where $q(\phi_{Bn}\text{-}V_F)$ is the activation energy. Over a limited range of temperature, the value of A^{**} and ϕ_{Bn} are essentially temperature-independent. Thus for a given forward bias V_F, the slope of a plot of $\ln(I_F/T^2)$ versus $1/T$ yields the barrier height ϕ_{Bn}, and the ordinate intercept at $1/T=0$ yields the product of the electrically active area S_e

and the effective Richardson constant A^{**}.

2.4.3 *Capacitance-Voltage measurement*

The barrier height can also be determined by the capacitance measurement. When a small ac voltage is superimposed upon a DC bias, charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. **Equation (2-9)** can be written in the form

$$1/C^2 = 2V_{bi}/q\varepsilon_s N_D \qquad (2.27a)$$

or

$$-\frac{d(1/C^2)}{dV} = \frac{2}{q\varepsilon_S N_D} \qquad (2.27b)$$

$$N_D = -\frac{2}{q\varepsilon_S \frac{d(1/C^2)}{dV}}. \qquad (2.27c)$$

When bias V is applied, V_{bi} should be replaced by V_{bi}-V in the equations given above. If N_D is constant throughout the depletion region, one should obtain a straight line by plotting $1/C^2$ versus V. If N_D is not a constant, the differential capacitance method can be used to determine the doping profile from **eq.(2.27c).**

$1/C^2$ plot against the applied voltage shows the liner curve. From the intercept on the voltage axis, the barrier height can be determined.

$$\phi_{Bn} = V_{bi} + V_n \qquad (2.28)$$

where V_{bi} is the voltage intercept, and V_n the depth of the Fermi level below the

conduction band, E_C-E_F, which can be computed if the doping concentration is known.

2.4.4 *X-ray photoelectron spectroscopy*

The photoelectron spectroscopy, which is the one of powerful and important surface analysis techniques, detects and analyzes energy of photoelectron emitted from atom ionized by x-ray or ultraviolet (UV) ray. Very various samples can be measured by this method, which includes solid surfaces, gases and liquids. The photoelectron spectroscopy using x-ray for excitation source is often called x-ray photoelectron spectroscopy (XPS) and that using UV source is often called ultraviolet-ray photoelectron spectroscopy (UPS). Since excitation source energy is different, the obtained spectra using x-ray mainly reflects electron energy from corelevels and spectra using UV source reflects molecular orbit of outer shell and valence band structure. In addition to these, these measurement are also named as ESCA (electron spectroscopy for chemical analysis) and this calling is used widely too.

The photoelectron spectroscopy was highly developed in chemical analysis and study of electron state in the solid state surface. Therefore, this technique is very powerful tool for characterization of semiconductor surface and interfaces in not only chemical status but also valence band structure and determining surface Fermi level position.

(1) Principles of this technique

Surface analysis XPS is accomplished by irradiating a sample with monoenergetic soft x-rays and energy analyzing the electrons emitted. Mg $K\alpha$ x-rays (1253.6eV) or Al $K\alpha$ x-rays (1486.6eV) are ordinarily used. These photons have

limited penetrating power in a solid, of the order of 1-10μm. They interact with atoms in this surface region by the photoelectric effect, causing electrons to be emitted. The emitted electrons have kinetic energies given by

$$E_K = h\upsilon - E_B - \phi_S \qquad (2.29)$$

where $h\upsilon$ is the energy of the photon, E_B is the electron binding energy of the atomic orbital from which the electron originates, and ϕ_S is the spectrometer work function. The energy relationship is illustrated in **Fig.2-13.**

The binding energy may be regarded as an ionization energy of the atom for the particular shell involved. Since there is a variety of possible ions from each type of atom, there is a corresponding variety of kinetic energies of the emitted electrons. There are a different probability, or cross section, for each process and these determine the each peak intensity of spectra. The Fermi level corresponds to zero binding energy (by definition), and the depth beneath the Fermi level indicates the relative energy of the ion remaining after electron emission, or the binding energy of the electron. The spin-degenerated *p*, *d*, and *f* levels become split upon ionization by spin-orbital interaction. In addition to the photoelectrons emitted in the photoelectric process, Auger electrons are emitted due to relaxation of the energetic ions left after photoemission. The Auger process is shown in **Fig.2-14(b)**. The Auger electron possesses kinetic energy equal to the difference between the energy of the initial ion and the doubly-charged final ion, and is independent of the mode of the initial ionization.

Probabilities of interaction of the electrons with matter far exceed those of the photons is of the order of micrometers, that of the electrons is of the order of tens of Angstroms. Thus, only those electrons that originate within tens Angstroms below the solid surface can leave the surface without energy loss. It is these electrons which

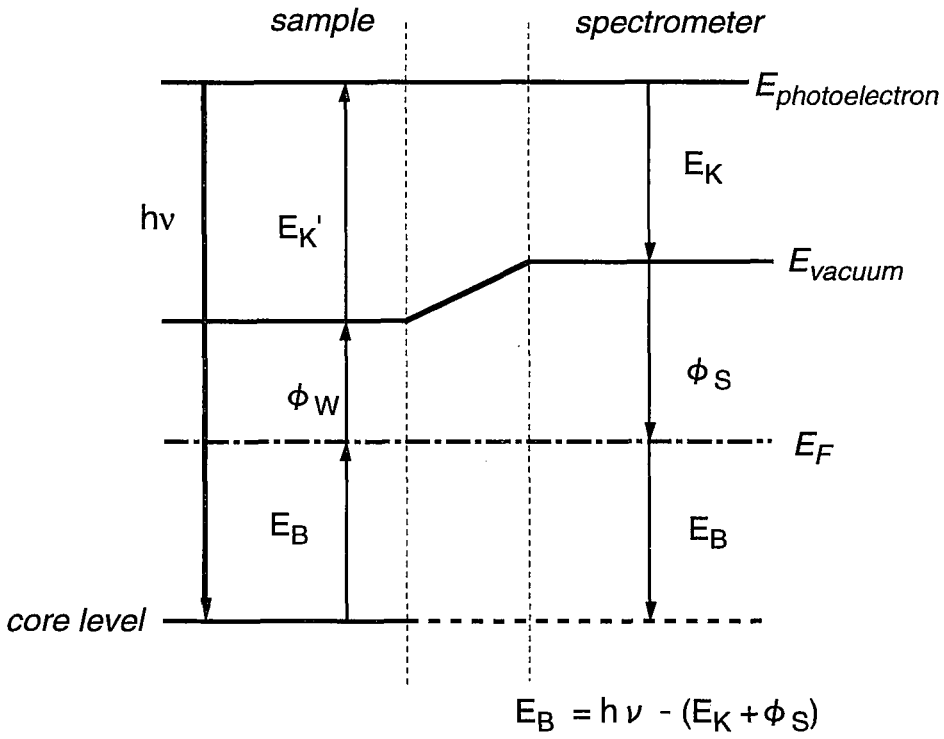


Fig.2-13. Energy relationship of the sample and spectrometer on x-ray photoelectron spectroscopy.

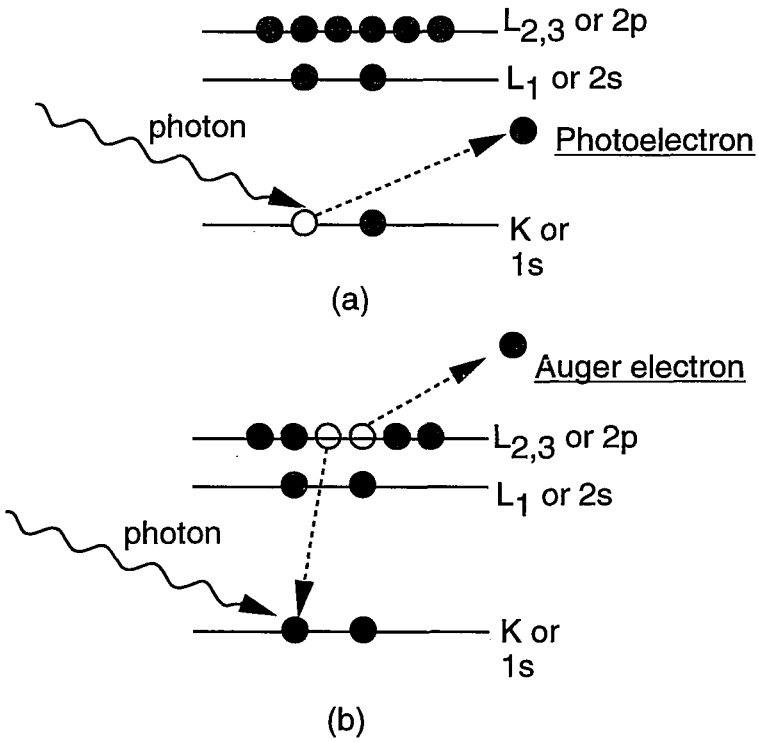


Fig.2-14. (a) Photoelectron and (b) Auger electron emission processes.

produce the peaks in the spectra and are most useful. Those that undergo loss processes before emerging form the background. Experimental data on mean free paths of electrons in various materials are shown in **Fig.2-15**.

The electrons leaving the sample are detected by an electron spectrometer according to their kinetic energy. The analyzer normally is operated as an energy window, accepting only those electrons having and energy within the range of this fixed window, referred to as the pass energy. Scanning for different energies is accomplished by applying a variable electrostatic field, before the electron reaches the analyzer. Electrons are detected as discrete events, and the number of electrons for a given detection time and energy is stored as data.

(2) Analysis of photoelectron spectra

XPS spectra from a solid is formed by two kind of electrons. The one is electron from corelevel which is bound into each atoms in solid, and the another is electron from valence band which makes bonding orbit in the solid. The valence band state density of a solid reflects on the spectrum in photoelectron spectroscopy. But, it is difficult to observe details of valence band structure, because obtained valence band spectrum is obscure in energy due to very short relaxation time of photoemission final state in valence band. The corelevel electron is affected sensitively by the potential changing due to the partial charge around the atom, which is generated by the electronegatively difference from the neighbor atom. On the other hand, both of the corelevel electron and the valence band electron is affected by the potential changing due to the space charge layer.

For the detail analysis of the spectrum, experimentally obtained peak is decomposed to some single peaks by curve fitting procedure supposing Gaussian-Lorentzian function. One analyzes the decomposed peak position and intensity obtained by the curve fitting.

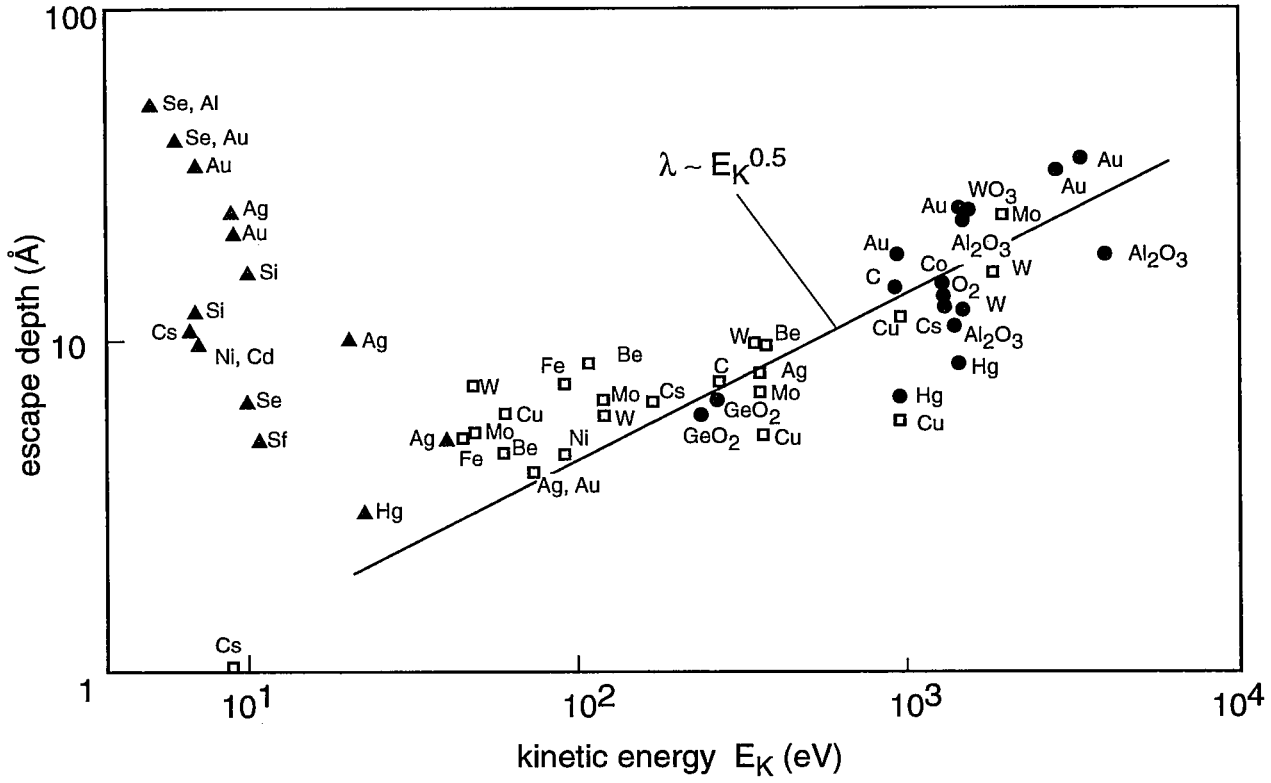


Fig.2-15. Experimental data on mean free paths of electrons in various materials.

Chemical shift

Electron confined in each corelevel does not affect on the bond between atoms. On the other hand, electrons in bonding orbital moves toward atoms having large electronegativity and this causes the change of static potential in the system. This change shifts corelevel energy also. Such reformation of electrons in bonding orbital corresponds to the change of chemical bonding. Therefore the energy shift of corelevels reflects the chemical bonding. The chemical shift is not observed when physical adsorption, but chemical adsorption happens. The chemical shift is unique and useful phenomenon in XPS measurement and this is the reason that the XPS is suitable for chemical analysis. Concretely, the chemical shift is clarifies what a atom is bonded to the atom from which detected photoelectron is emitted, referring the results measured in advance or the various compounds.

Band bending measurement [15]

Both of the corelevel electron and the valence band electron is affected by the change of macroscopic potential due to space-charge layer. The surface band bending of semiconductor is characterized with the abstract value of the corelevel binding energy.

$$E_B = E_{B0} + V \tag{2.30}$$

where E_B, E_{B0} is the corelevel energy measured from Fermi level with and without effect of space charge and V is the change of macroscopic potential. But, E_B is sensitive to excluding effects that are the charge-up of a sample and photovoltaic effect.[16] The charge-up phenomenon are happened if the sample is hard conductive as an insulator. This is the phenomenon that the sample surface is charged positively due to little supply of electron from the sample bulk which compensates electron emitted from surface. When the potential change due to the charge-up and the

photovoltaic effect are negligible, the shift of corelevels reflects the surface potential directly since the depth that photoelectron come from is only a few ten Å is much smaller than that band bending occurs, 100Å-1000Å. Surface Fermi level position E_{FS} is characterized by the next equation.

$$E_{FS} = E_B(x=0) - (E_V - E_B) \qquad (2.31)$$

where E_V and E_B are valence band edge and binding energy of corelevel in bulk, respectively. When E_V-E_B is known, E_{FS} can be estimated. The values of E_V-E_B is obtained by measurement of valence band spectra and corelevel spectra at the same time. In this characterization, spectra from corelevels with small binding energy should be used in order to minimize the relative error of energy level measurement. This method is also applicable to determination of SBH as shown in **Fig.2-16**, when metal thickness is less than the mean free path of photoelectron and the depletion layer is much thicker than the mean free path. The SBHs of p-type and n-type semiconductor are given by

$$q\phi_{Bn} = E_g - \{E_B(0) - (E_V - E_B)\}: \quad \text{n-type} \qquad (2.32)$$

$$q\phi_{Bp} = E_B(0) - (E_V - E_B)\}: \quad \text{p-type} \qquad (2.33)$$

where, E_g is the band gap of the semiconductor, $E_B(0)$ is measured corelevel energy emitted from the surface compared with Fermi level. To obtaining the value of E_V-E_B, one needs to take valence band spectra and determine E_{FS} directly, however, in this work, reported values E_V-E_B of Ga3d(GaAs)=18.75eV, As3d(GaAs)=40.74eV[17], $In3d_{5/2}$(InP)=443.5eV and P2p(InP)=128.2eV[18,19] are used in this study.

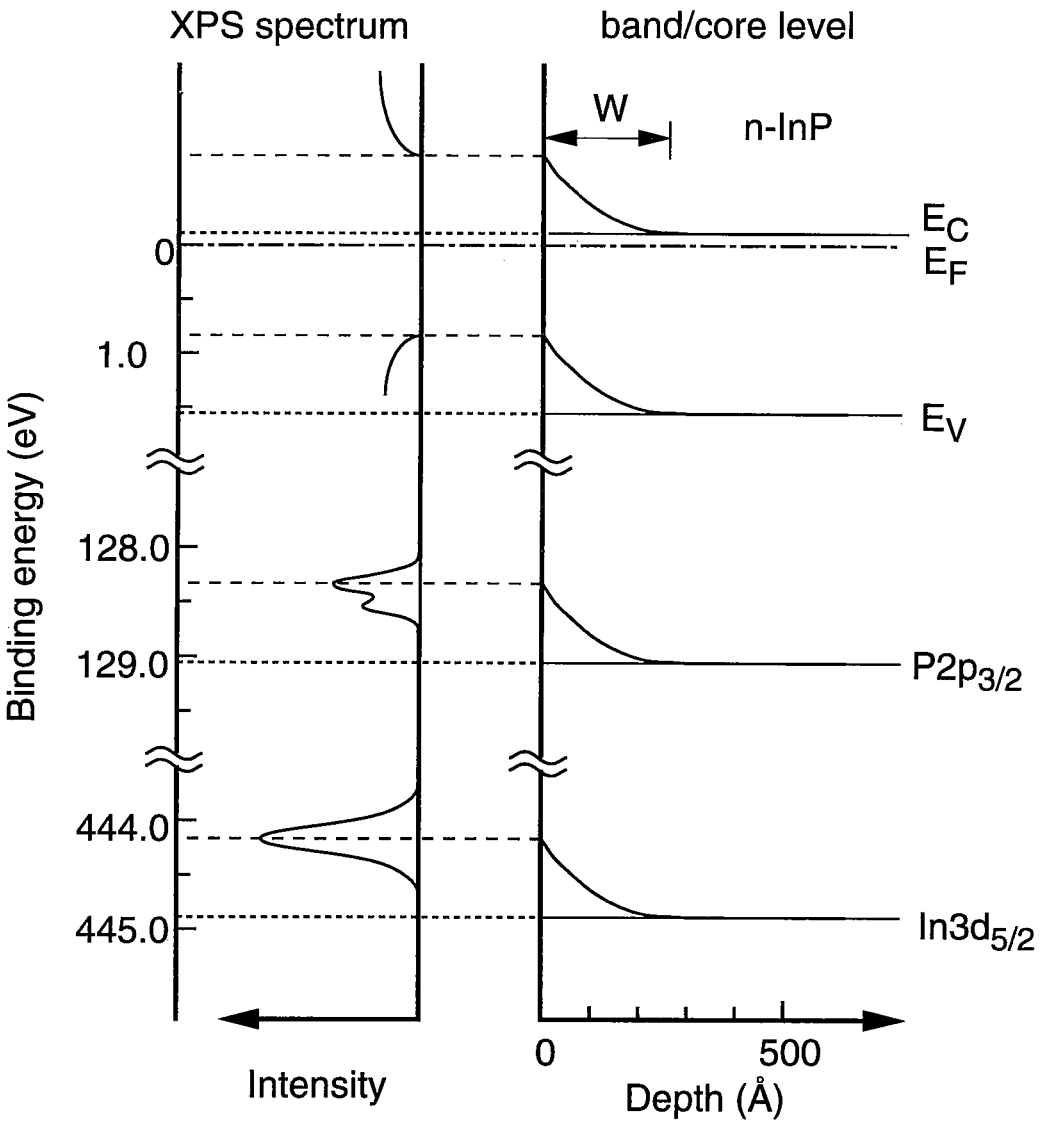


Fig.2-16. Relationship between band bending, corelevels of the sample (n-InP) and XPS spectrum.

Depth profile

A part of electron excited near the surface forms the corelevel peak and the valence band peak, which escapes from surface without suffering such energy loss and losing the energy information of the electron binding in solid. The dominant energy-loss process in a solid is the inelastic scattering, and the probability of offering this scattering increases by a distance advanced in the solid. The photoelectron escape depth is defined as the depth at which number of electron without offering energy loss decreases to $1/e$ of the number of all excited electron. The intensity of the generated photoelectron from the depth x,

$$I(x) = I(0) \exp(-x/\lambda) \qquad (2.34)$$

The escape depth λ is slightly different from the electron mean free path in the material because of the surface roughness and the non-uniformity of composition near the surface. The escape depth is experimentally obtained for various materials by XPS and AES (Auger-electron spectroscopy). As shown in **Fig. 2-15**, the reported measurement results of the escape depth relates to the photoelectron kinetic energy E_K. This relationship is possible to approximate as follows in the range of E_K>100eV,

$$\lambda = \alpha \cdot E_K^m, \text{ (m=0.54 - 0.88)} \qquad (2.35)$$

λ increases in proportion to the decrease of E_K in the range of E_K<100eV, because E_K comes near the band gap so that the non-elastic scattering does not frequently happen. When **eq.(2-34)** is given, the intensity of spectra S from the material on the surface of the sample is expressed by the next equation.

$$S = \int_0^d \{I(0)\exp(-x/\lambda)\}\,dx \qquad (2.36)$$

where d is the thickness of outer layer, $I(0)$ is the number of photoelectron from x=0. Comparing S from the inner and outer layers, one can obtain quantitative value of the thickness d by next equation.

$$\frac{S_B}{S_A} = \frac{I_B(0)\lambda_B\{1-\exp(-d/\lambda_B)\}}{I_A(0)\,\lambda_A exp(-d/\lambda_A)} \qquad (2.37)$$

where S_B, S_A, $I_B(0)$ and $I_A(0)$ are obtained peak intensity and numbers of photoelectron from x=0 for inner (A) and outer (b) layers, respectively, as shown in **Fig.2-17(b)**. In the case that same element composes both of inner and outer layer, i.e.$I_A(0)$=$I_B(0)$ and λ_A=λ_B and then d is given by

$$d = \lambda \ln(1+S_B/S_A) \qquad (2.38)$$

The angle between the surface of the sample and the axis of the spectrometers called the photoelectron exit angle, which decides the effective escape depth $\lambda^*(=\lambda\sin(\theta))$. In this work, almost measurement was done with this angle 45° as shown in **Fig.2-17**. Since less exit angle gives more surface-sensitive signal as indicated by **eq.(2.38)**, therefore the exit angle is also set 15° when more detailed-surface analysis must be done.

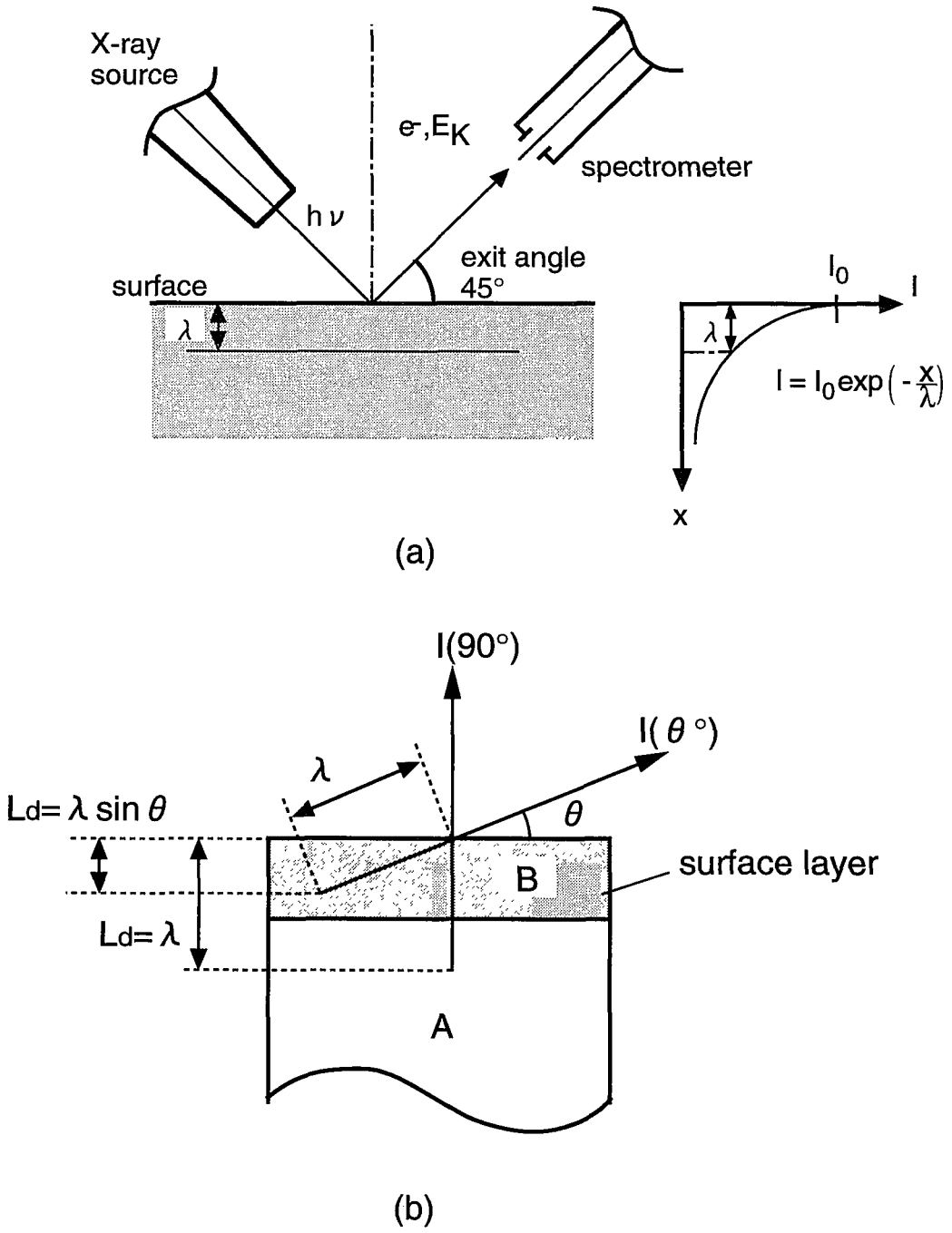


Fig.2-17. Angle-resolved XPS meausurement.

2.5 Instruments used in this work

2.5.1 *UHV-based multi chamber system*

An UHV-based multichamber system is used for fabrication and characterization of the samples in this work. This system consists MBE (molecular beam epitaxy), XPS, photo-CVD (chemical vapor deposition), EB (electron beam), FIB (focused ion beam), STM (scanning tunneling microscopy), ECR (enhancement cyclotron resonance), MOMBE (metalorganic molecular beam epitaxy), PL (photoluminescence), RIBE (reactive ion beam etching), contactless C-V, metal deposition and sample loading chambers which are connected with UHV transfer chambers as shown in **Fig 2-18**. A sample is mounted on a sample holder and loaded into the UHV system through the sample loading chamber. Then the sample holder with the sample is mounted on the truck and is transferred to each UHV chamber. The UHV based characterization and fabrication chambers mainly used in this work are MBE, XPS and metal deposition chambers.

2.5.2 *Molecular Beam Epitaxy (MBE)*

Molecular beam epitaxy (MBE) is one sophisticated growth technology compared with liquid phase epitaxy (LPE) and vapor phase epitaxy (VPE) which are generally used as crystal growth method. MBE growth method was found in the study of phenomena of absorption, deposition and chemical reaction of metal molecular beam with solid surface, and is a kind of vacuum evaporation method. MBE growth under the ultra-high vacuum lower than 10^{-10} Torr by the development of vacuum technology can prevent the mixing of the remaining impurity gas and contamination of surface.

The characteristics of MBE compared with other growth method are,

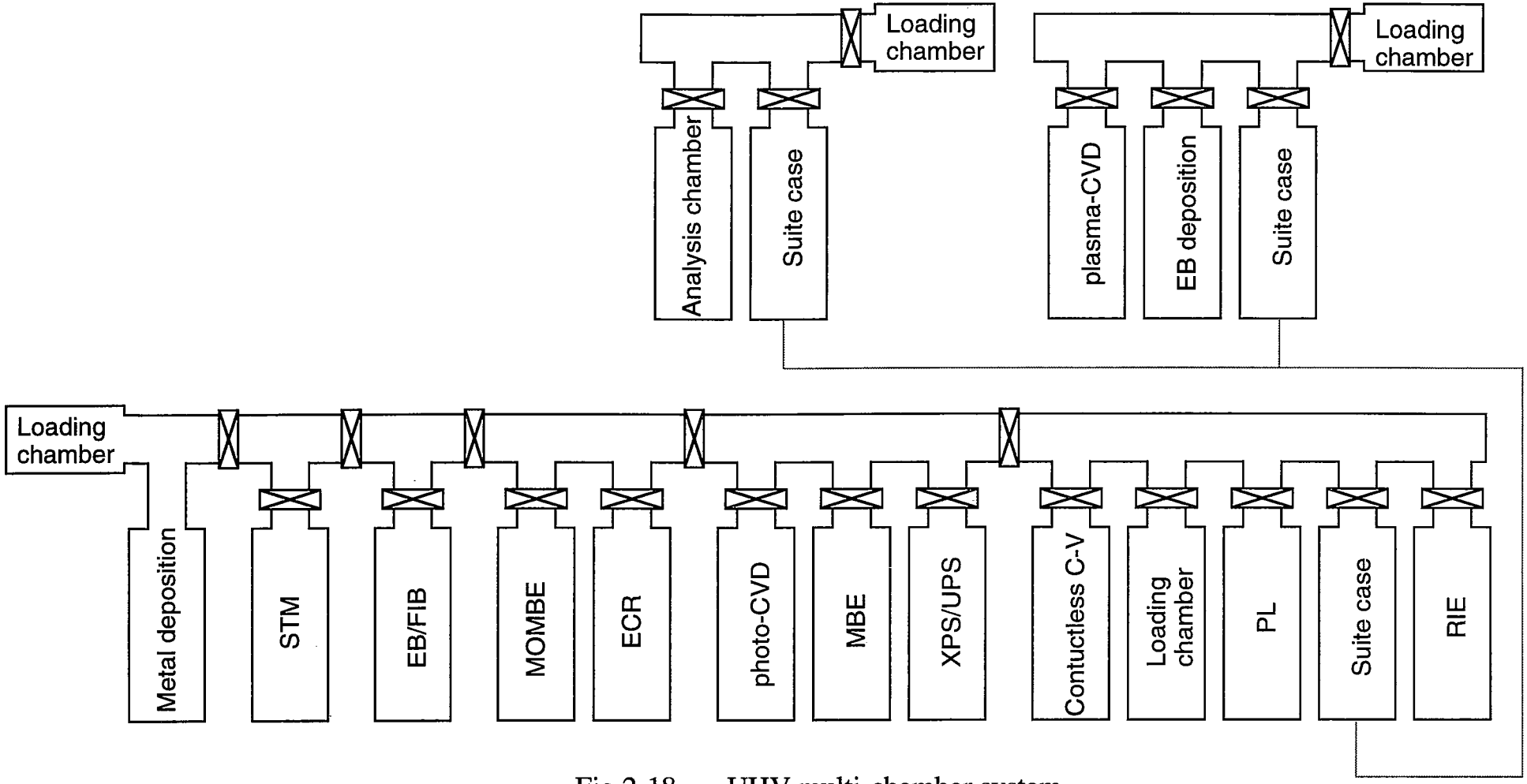


Fig.2-18. UHV multi-chamber system.

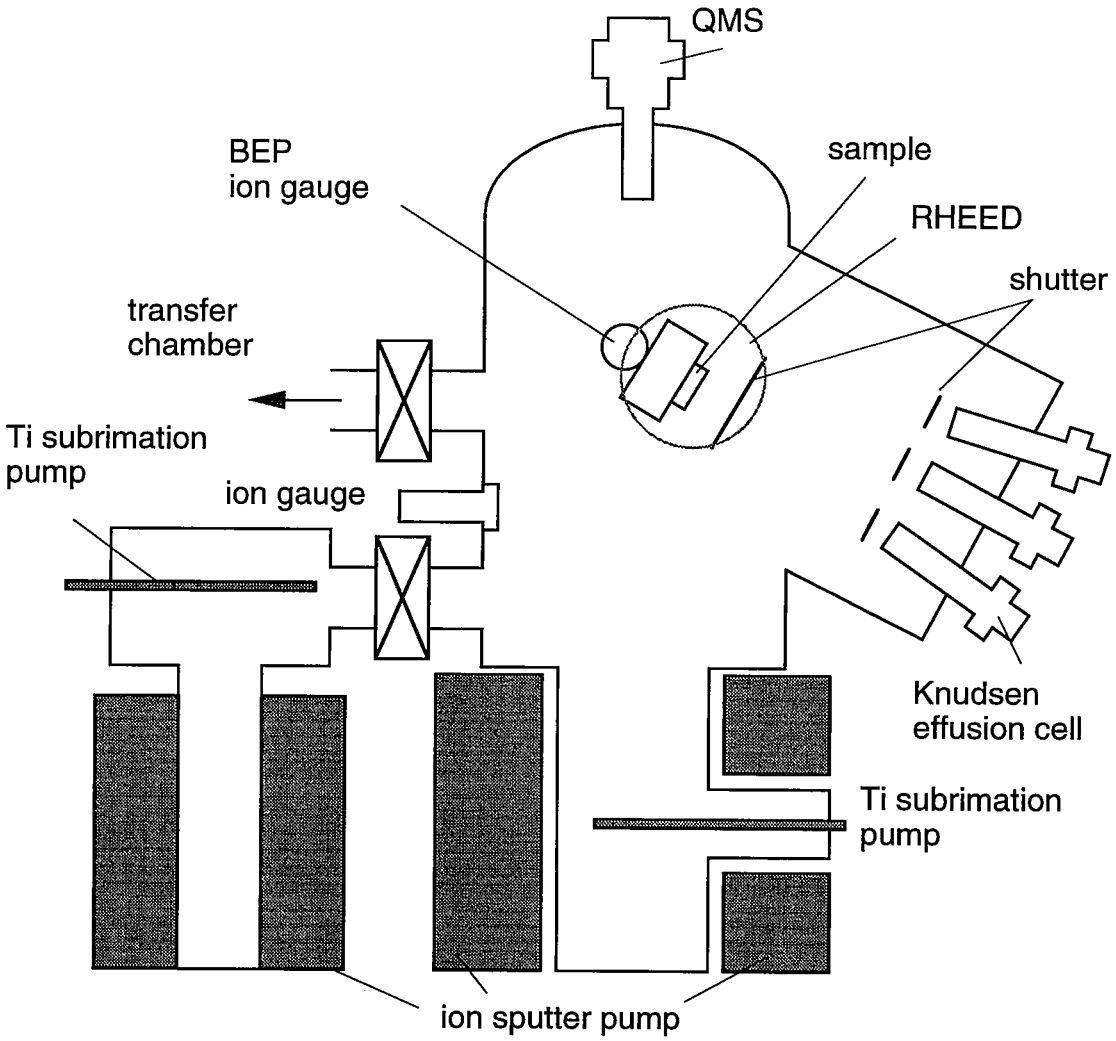


Fig.2-19. MBE chamber used in this work.

(1) precise control of growth thickness, layer-by-layer growth, composition and doping density can be realized since the source supply is started and cur off immediately by opening and closing the shutter and the growth rate is very low.
(2) Growth is performed at lower substrate temperatures. There is little thermal diffusion of atoms during growth.
(3) In-situ monitoring of the crystal quality and composition of the growth layer can be performed before and during growth due to vacuum process.

A schematic view of MBE chamber is shown in **Fig.2-19**. Liquid nitrogen (LN_2) cooled shrouds installed around the sample holder, the evaporators and the ion pump of this MBE machine prevented the residual gases from mixing with epitaxial layer that are brought out mainly by heating the evaporators. This MBE chamber is equipped with an ionization vacuum gauge for monitoring the pressure during MBE growth and with a quadrupole mass spectrometer (QMS) for monitoring the residual gases. The background pressure of this machine has been usually kept in the range of 10^{-10} Torr and the arsenic pressure during GaAs and InGaAs lattice matching with InP growth was $4\sim6\times10^{-7}$Torr and $1.0\sim1.2\times10^{-6}$Torr, respectively. The surface condition of the sample grown by this method was in-situ characterized by reflection high energy electron diffraction (RHEED).

Source of molecular beams in this work were gallium, aluminum and indium metal as column-III, arsenic metal as column-V, and silicon crystals as n-type dopant, respectively. The crucibles, in which these sources were placed, were in Knudsen effusion cells (K-cells). Evaporation of the source was performed by heating the resistance curled around the cell and the temperature of the k-cell was controlled by a PID system.

2.5.3 *XPS system*

Figure 2-20 shows the schematic diagram of the entire system which includes the photoelectron spectrometer used for this work. The sample is carried from atmosphere into the analysis chamber where the XPS measurement is performed through the sample-loading chamber. The attainment pressure of the analysis chamber is about $5x10^{-10}$ Torr.

It is preferable to use monochrome radiation which is arranged as possible as same energy for radiation source of which an excite the valence band or corelevel electron of sample is used. However, in this work, the soft x-ray source whose anodes are Mg and Al was mainly used. The characteristic x-ray is generated by making the thermoelectron from the filament accelerate into 15 kV field and collide against anode. The characteristic x-ray spectra of Mg (C1s peak and related satellite peaks) is shown in **Fig.2-21**. The continuous radiation of the background is cut off by a thin film filter of Al. Among various transition line, the $K\alpha_{1,2}$ line of most strong is used, whose energy is 1253.6eV for Mg anode and 1486.6eV for Al anode, Besides $K\alpha_{1,2}$ line, small line such as $K\alpha_{3,4}$ and $K\beta$ etc. in the spectra affect the measurement, but their effect can be easily removed by the calculation because relative strength and the energy difference of those related to $K\alpha_{1,2}$ are identified. Recently, the x-ray of which monochromatic is improved with the monochrometer and synchrotron orbit radiation are used.

The electron energy analyzer, which measures the kinetic energy of photoelectron, is the most important part for XPS system. The electron of a certain energy is selected and passes over the analyzer, and reach to the electron detector where the number of passing electron is counted. The spectrometer is roughly divided into the obstruction electric field method and the inclination decentralization method by the magnetic field or the electric field. The main current in a photoelectron

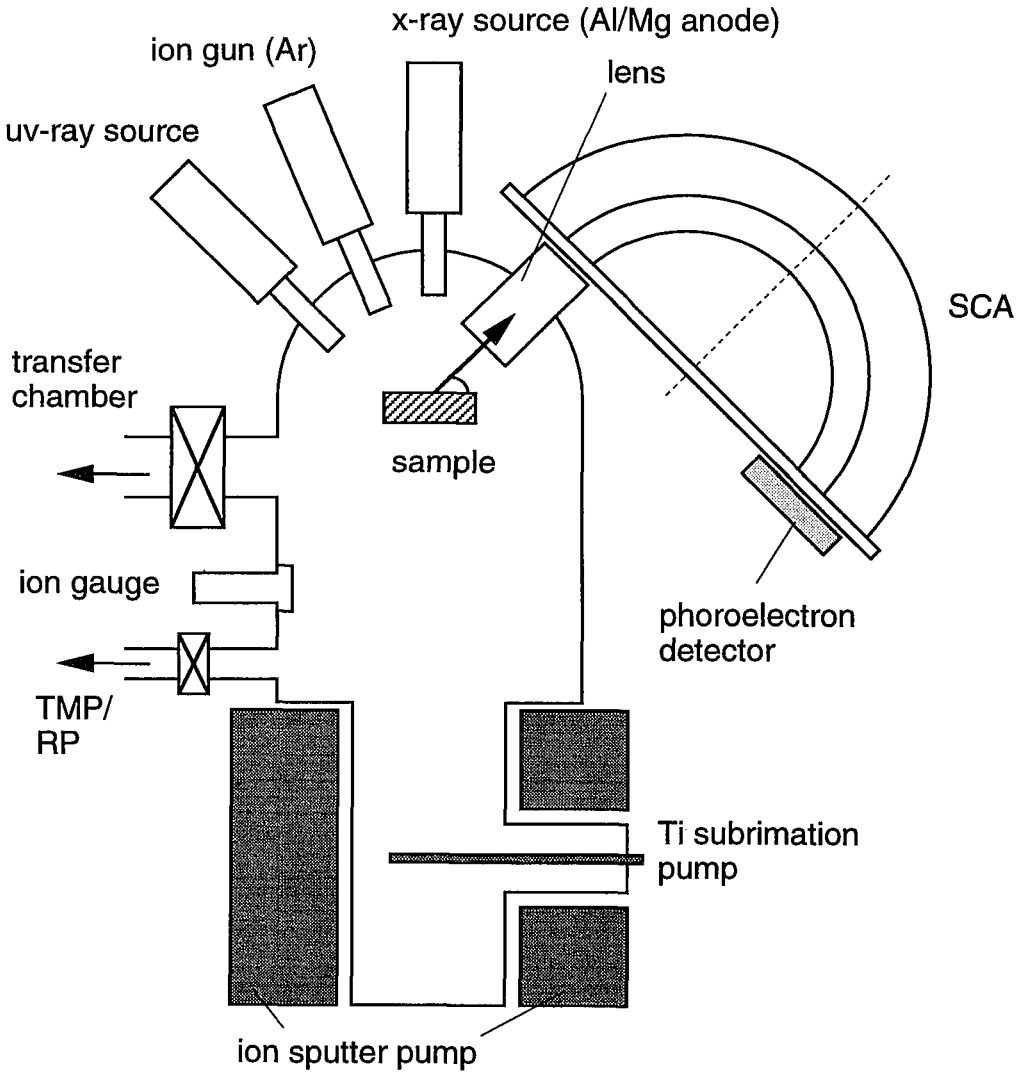


Fig.2-20. Analysis chamber used in this work.

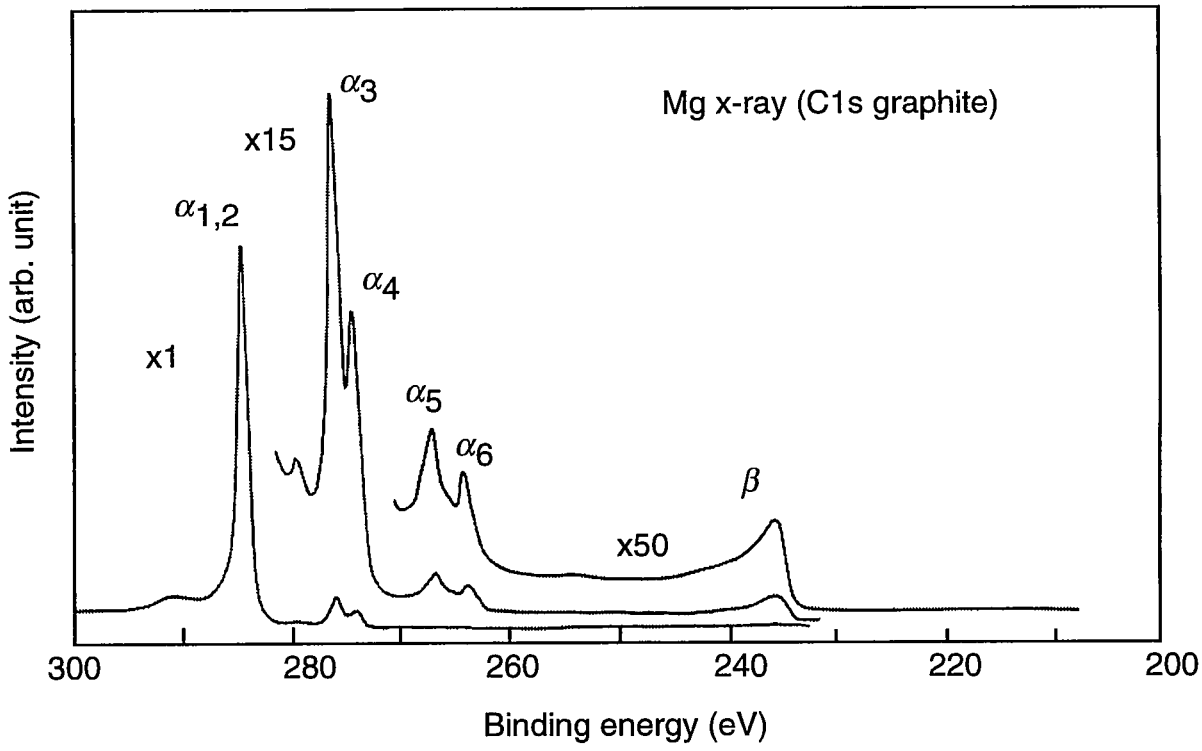


Fig.2-21. Characteristic Mg x-ray satellites (C1s graphite spectrum).

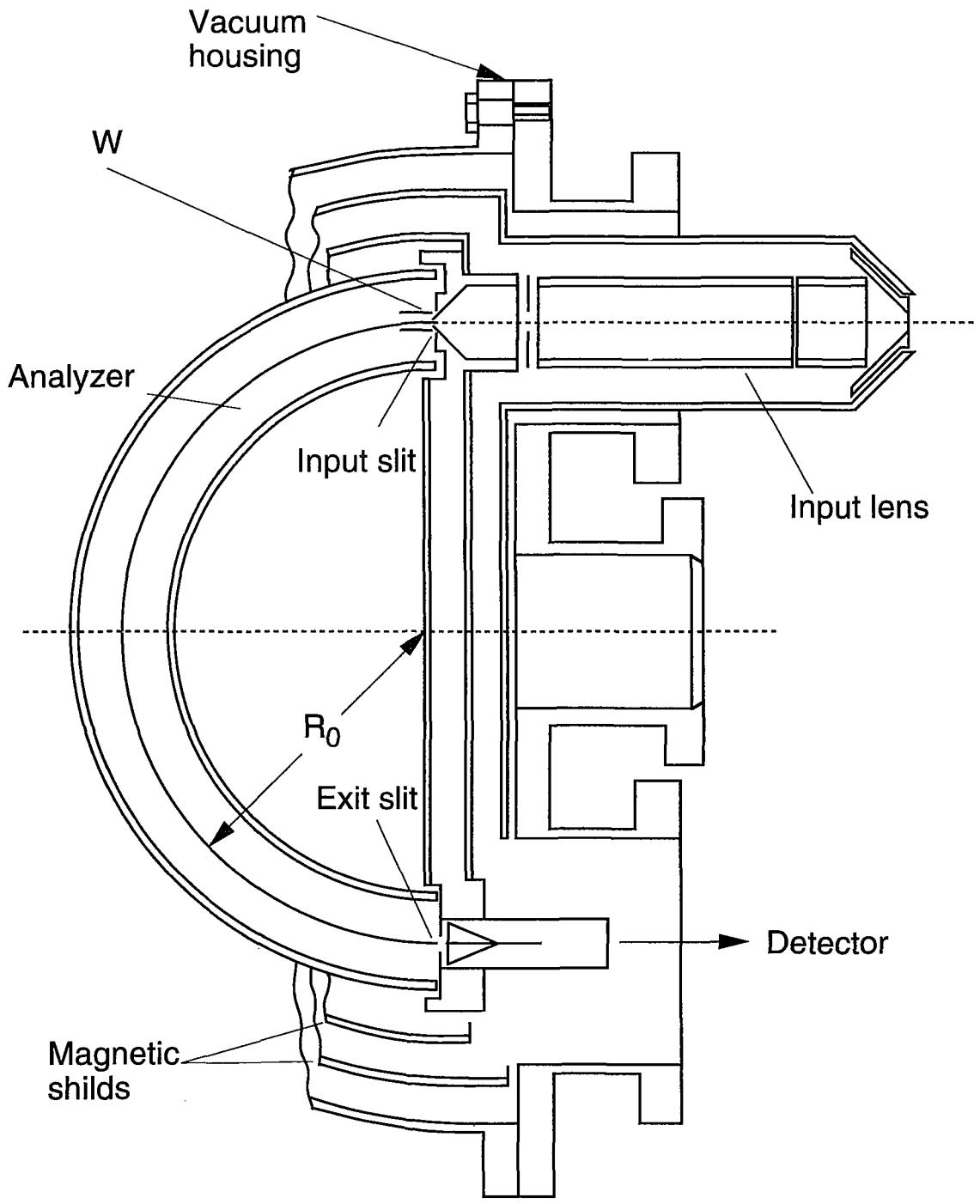


Fig.2-22. Concentric hemispherical analyzer of XPS/UPS system.

spectroscopy system now is the electrostatic inclination method because of its high decomposition ability. The concentric hemispherical analyzer (CHA) which uses above method was use in this work. As shown in **Fig.2-22**, this analyzer has the two concentric hemispherical electrodes which face each other with a constant gap. When a constant electric field is formed between the electrodes by applying a certain voltage, the electron of only a corresponding energy to the field can pass through the gap. The relationship between the applied voltage to the electrodes V_d and the energy of passing electron E_p (so-called pass energy) are written as follows,

$$E_p = q\, V_d /(R_2/R_1 - R_1/R_2) \qquad (2.39)$$

And the resolving power is written as follows,

$$(\mathrm{FWHM}) = w\, E_p/R_0 \qquad (2.40)$$

where R_1, R_2 and $R_0=(R_1+R_2)/2$ are the radius of the electrodes, shown in **Fig.2-22**, and w is the slit distance. In this work, E_p is mainly 17.9eV, where resolving power is 0.05eV as FWHM (Full Width of Half Maximum). The spectrum is able to be obtain by changing deceleration voltage which is applied to electron lens where electrons are introduced into the spectrometer.

The spectrometer calibrated using Au $4f_{7/2}$ corelevel peak (E_B=84.0eV) from a Au foil which is very stable.

2.5.4 *Electron Beam and Focused Ion Beam technique and system*

Electron beam (EB) lithography is one of the most promising patterning technologies for nanometer-scale fabrication because of its high resolution due to

highly focused beam energy and because its spot size is smaller than few 10nm. Development of high resolution resists for EB lithography based on PMMA (polymethylemetacrylate) also has assisted the development of EB lithography technology. EB lithography technique is widely used for fabrication of various quantum nanostructures.

The technology of high-resolution focused ion beams (FIB) has also advanced dramatically in the past 15 years as focusing systems have evolved from laboratory instruments producing minuscule current densities to high current density tool which have sparked and important new process. FIB incident on a solid surface produce a number of effects: several atoms are sputtered off, several electrons are emitted, chemical reactions may be induced, atoms are displaced from their equilibrium positions, and ions implant themselves in the solid, altering its properties. Some of these effects, such as sputtering and implantation are widely used in semiconductor device fabrication and in other fields. Thus the capability to FIB to submicronmeter dimensions is an important development.

Figure 2-23 shows the EB lithography and FIB systems used in this work produced by EIKO engineering CO. LTD., which consists of sample loading, transfer, main chambers, a vacuum-pumping system, electron gun and FIB gun chambers. The sample holder which is used in the previous UHV system in common is fixed on a sample stage. As seen in **Fig.2-23**, the EB system is connected directly with the neighboring focused ion beam (FIB) chamber. The EB lithography and FIB systems consist of two kinds of the pumping-out system for the main chamber, a sputter ion pump (SIP) as a main pump and titanium sublimation pump (TSP) as a sub pump, and for the gun chamber, SIP. The back ground pressure of the chamber is $1x10^{-9}$ Torr. As an electron source, the ZrO/W thermal field emission (TFE) electron gun is used in this system. The TFE gun has a small virtual source size and a high current density. Maximum acceleration voltage is 20kV. Minimum spot size of EB is about 20nm. In the case of EB lithography in this work, the spot size was about 20nm and scan

speed was 0.5μs per dot (where 1dot=100μm/65500). As EB resist, OEBR1000 (Tokyo Ohka CO.LTD) posi-type resist was used. FIB system is mainly same as EB system. Ga is used as an ion source of FIB. Mass separator is attached to the system. Maximum acceleration voltage for FIB is 25kV and maximum current is 300μA. Minimum spot size of present FIB was about 100nm. The EB and FIB is controlled by computer-based operation system. Vector-beam scan method is applied in this system and the beam position can be controlled in nm order.

2.5.5 *Scanning electron microscope (SEM) and electron beam induced current (EBIC) measurement system*

Scanning electron microscope (SEM) technique is consisted the process of irradiation and scanning of focused electron beam with the spot size of a few ten nm on the sample, detection of emitted secondary electron from the sample and 2-dimensional imaging of the obtained signal. Due to its high spatial resolution (typically 0.1-5nm), its relatively easy operation and easy preparation of the sample compared with other methods. SEM is widely used for observation of the structures with nanometer-scale dimensions. In this work, a field emission type SEM system (FE-SEM), S-4100, HITACHI CO. LTD. as shown in **Fig.2-24**, was widely used for characterization of EB-lithography patterns and fabricated sample structures. The resolution of this SEM system is about 5nm at its maximum acceleration voltage of 30kV. However, the acceleration voltage were mainly set low about 5~15kV in this work because of preventing the samples from the damage due to electron beam irradiation.

Electron-beam induced current (EBIC) measurement can be performed using the equipment based on the present SEM system. In this technique, the charge carriers generated by the electron beam of the microscope are collected by an electric field within the material and sensed as current in an external circuit. Then, for

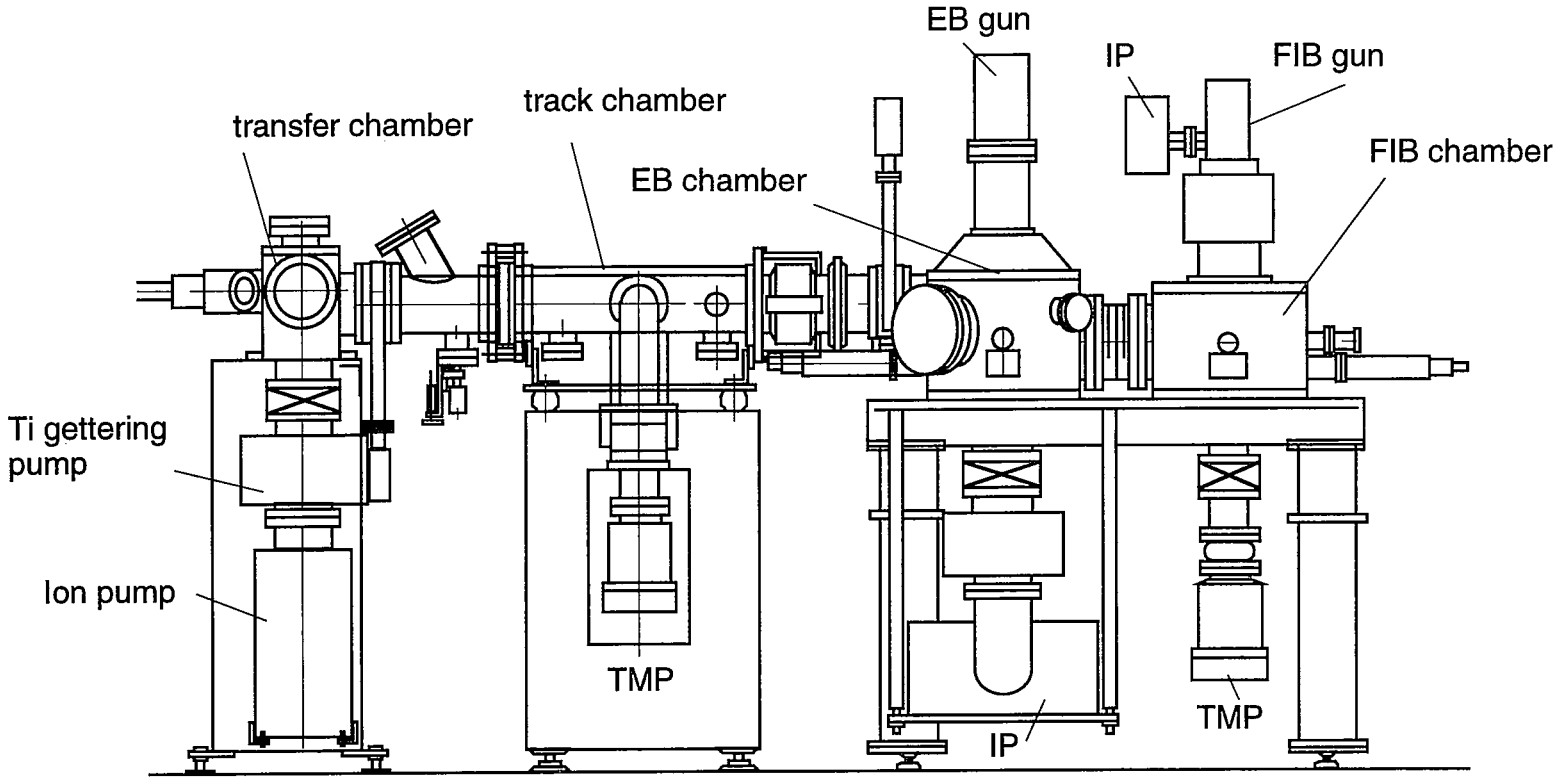


Fig.2-23. EB/FIB chambers.

characterizing a M-S structure, Schottky gate and ohmic electrode of the sample is connected to current meter and ground, respectively, and the electron beam irradiate on the surface or cross-section of the sample. The current density depends on the acceleration voltage or sample structure, and the detected current is about pA~nA by the acceleration voltage of 5~10keV. When employed as the video signal of the SEM, 2-dimensional image of collected current reveals inhomogeneities in the electrical properties of the material. The system used in this work contains a bias application circuit and bias dependence of the EBIC signal can be obtained. EBIC measurement system used in this work is schematically shown in **Fig.2-24**.

2.5.6 *Electrical measurement systems*

Electrical characterizations are most important characterization methods in this work. For characterization of Schottky diodes, *I-V* and *C-V* measurements were performed by using computer-controlled measurement systems shown in **Fig.2-25(a)** and (**b**), respectively. *I-V* measurement system containing Takeda Riken TR6147 programmable dc voltage generator and Keithley 617 programmable electrometer which were connected in series to a sample. The *I-V* measurement was done automatically using computer-controlled system. *C-V* measurement was done using Hewlett Packerd HP 4192A LF impedance analyzer. The diode impedance was characterized as a capacitance/resistant parallel circuit for various frequency. These electrical measurements were done using electrical measurement box providing electrically shield and dark condition.

For electrical characterization of quantum effect devices, I_{DS}-V_{DS} and I_{DS}-V_G dc measurements were done using HP 4156A precision semiconductor parameter analyzer. In order to low temperature measurement, Oxford superconducting magnet/LHe cryostat was used. The sample loaded in this system was enable to be cooled by using LHe to about 2K at a minimum temperature.

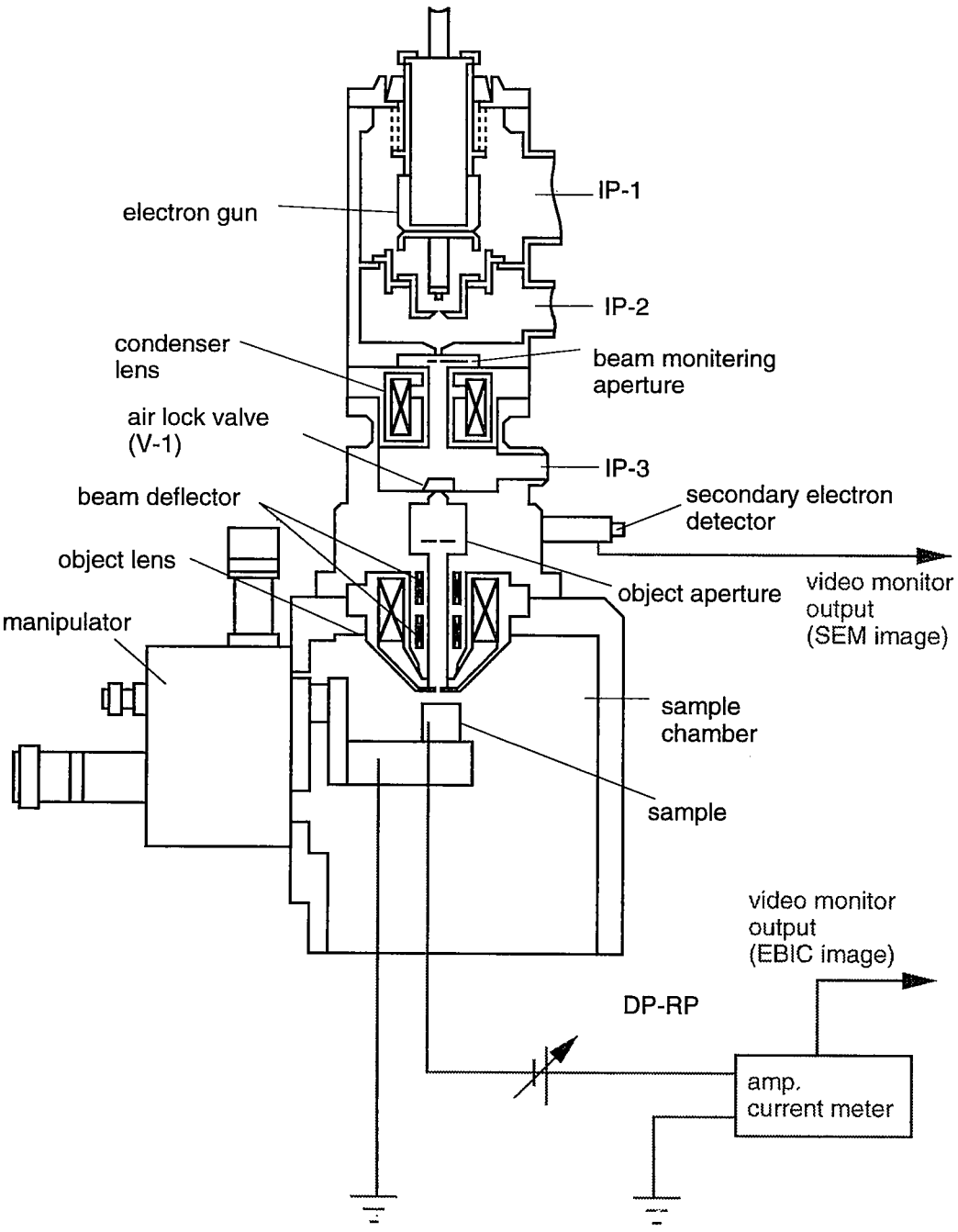
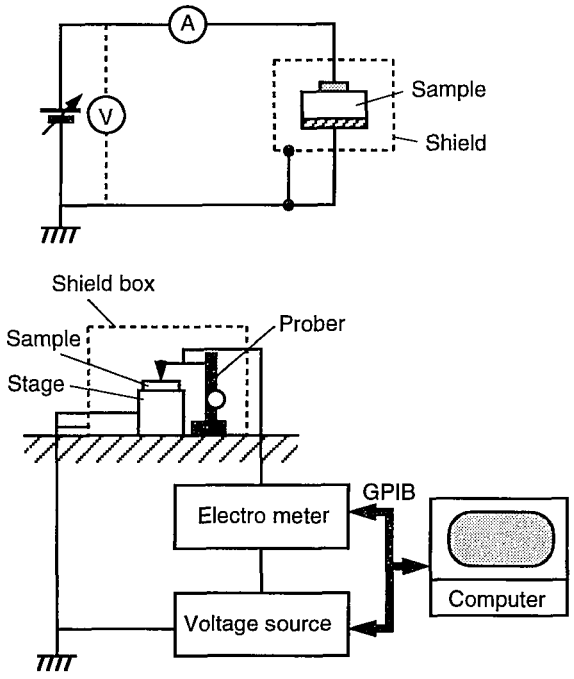
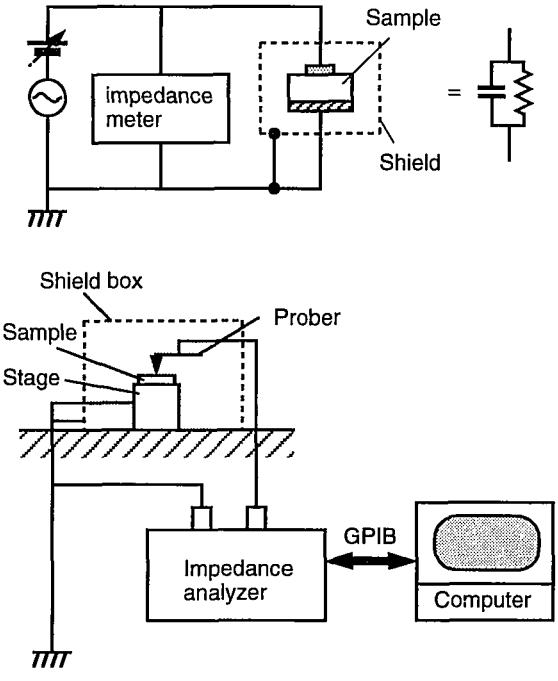


Fig.2-24. SEM/EBIC measurement system.



(a)



(b)

Fig.2-25. (a) DC I-V and (b) C-V measurement systems.

2.6 Potential simulation

Potential simulation by solving Poisson's equation is used in various situations in this work, in order to obtain basic or detailed idea of the investigated systems. Often the Poisson's equation is solved numerically using engineering work station. Mainly two methods are used for numerical solution of the Poisson's equation, the one is shooting method and the another is difference method.

The basic procedure of shooting method is as follow. First, assuming suitable boundary at one boundary point and then integration of the differential equation toward the other boundary point was done by Runge-Kutta-Guill method. Comparing given boundary condition with integrated value at the boundary in the another side, if the given and integrated values consist in sufficient small error, then the calculated value is taken as a solution. Else if the integrate value does not consist with the given boundary, then estimating next boundary value at first boundary point by Newton method or bisectional method and try integration again till the integrated value consists with the given boundary condition.

The difference method is applied to the solution of two-dimensional and three-dimensional Poisson's equation. The differential equation is solved by successive over relaxation (SOR) method. The differential equation of 2-D Poisson's equation is given by

$$\frac{\phi_{i-1,j}-2\phi_{i,j}+\phi_{i+1,j}}{\Delta x}+\frac{\phi_{i,j-1}-2\phi_{i,j}+\phi_{i,j+1}}{\Delta x}$$

$$=\frac{q}{\varepsilon(x,y)}\left(N_D^+\left(\phi_{i,j},x,y\right)-N_A^+\left(\phi_{i,j},x,y\right)-n\left(\phi_{i,j},x,y\right)+p\left(\phi_{i,j},x,y\right)\right) \tag{2.41}$$

where, N_D^+, N_A^-, n and p are ionized donor density, ionized acceptor density, electron

density and hole density, respectively. The SOR method gives quick and well convergency and the number of required matrix elements for solution by the SOR method is not so large as the one by the other methods.

For calculation of ionized donor and acceptor concentration, N_D^+ and N_A^-, strict descriptions as follows are made assuming 3-dimensional density of state.

$$N_D^+ = N_D\left[1 - \frac{1}{1+\frac{1}{g}\exp\left(\frac{E_D - E_F}{kT}\right)}\right] \tag{2.42a}$$

$$N_A^- = \frac{N_A}{1+g\exp\left(\frac{E_A - E_F}{kT}\right)} \tag{2.42b}$$

where N_D and N_A are doped donor and acceptor concentrations and E_D and E_A are activation energies for donor and acceptor ionization. g is the ground-state degeneracy factor, 2 for the donor level and 4 for acceptor level in the case of GaAs and InP. In order to calculate electron and hole concentrations, n and p, one must evaluate Fermi-Dirac integral which cannot be evaluated analytically. Usually, Boltzmann approximation is used, however, in this work, more accurate approximation is applied to the evaluation of n and p. Fermi-Dirac integral is replaced by the next equation, in the case of electron.[20]

$$n = N_C\frac{2}{\sqrt{\pi}}F_{1/2}\left(\frac{E_F - E_C}{kT}\right)$$

$$\approx N_C A\,(1+0.15A) \quad with \quad A = \ln\left(1+\exp\left(\frac{E_C - E_F}{kT}\right)\right) \tag{2.43}$$

where N_C is the effective density of state in the conduction band and $F_{1/2}$ denotes the Fermi-Dirac integral. Hole concentration is calculated by the similar equation.

Boundary conditions are given by Schottky barrier height at the metal/ semiconductor interface (0.9eV for n-GaAs, 0.36eV for n-InP and 0.67eV for n-Si) and electric field E~0 or midgap energy at the inside of the structure.

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Chapter 3

Theoretical Investigation for Control of III-V Compound Semiconductor Schottky Barrier Height

3.1 Introduction

Schottky barrier height (SBH) control is very important issue not only for the previous semiconductor device technology but also for the realization of state-of-arts quantum effect devices. Generally, the idea that SBH depends on metal work-function indicated by Schottky[1] has also been recognized experimentally and many attempts have been made to control SBH based on this idea. The examples of the attempts are sulfur treatment of semiconductor surfaces[2] and low temperature metal deposition[3].

On the other hand, another approach utilizing an interlayer has also been investigated for this purpose. Many studies found out the possibility of the SBH control by inserting a very thin interface control layer (ICL) at metal/semiconductor (M-S) interface, which improves interface properties or produces interface dipole that results in artificial strong field and band bending of the semiconductor by introducing charges into the ICL. Our group have investigated this technique[4-6] which has applied to insulator/semiconductor (I-S) and semiconductor/semiconductor (S-S) interface control for III-V compound semiconductors. [7-11] From the investigations, it was found that ultrathin Si ICL is useful for GaAs and InP SBH control [4-6] and it was also found that the possibility of fabrication of quantum effect device by using this techniques.[12] However, the precise control of SBH will be needed for realizing future semiconductor devices, since a small number of electrons must be controlled sensitively. Therefore, more detail analysis of M-S interface is needed.

In this chapter, theoretical investigation of the SBH control scheme for III-V compound semiconductor Schottky interfaces is made from a point of view not only SBH control but also the forward and reverse current transport through the interface, for more precise and systematic control of SBH. First, the basic two methods for SBH control are explained. Second, the formation mechanism of Schottky barrier is discussed based on the unified disorder-induced gapstate (DIGS) model for Fermi level pinning. [13,14] Next, the result of calculation of SBH having an ICL by potential simulation will be shown. Detailed analysis including the effects of band gap narrowing and interface state at the ICL/semiconductor interface is made. Then, the current transport properties through the M/ICL/S structure will be discussed.

3.2 Basic concepts for Schottky barrier height control

3.2.1 *SBH control based on Schottky model*

As indicated by Schottky[1], SBH seems to be changed by selecting metal having different work function,

$$\phi_{Bn} = \phi_m - \chi \qquad (3.1)$$

where ϕ_{Bn} is Schottky barrier height of n-type semiconductor, ϕ_m is a metal workfunction and χ is the electron affinity of the semiconductor. However, experimentally obtained values of SBHs of most in M-S contacts hardly depend on the metal workfunction due to a large amount of interface states exist at M-S interface[15]. Therefore, one can control SBH by changing metal-workfunction if he knows how to reduce the interface states as shown in **Fig3-1**. Based on the unified disorder induced gap state (DIGS) model[13,14], the interface states are produced by

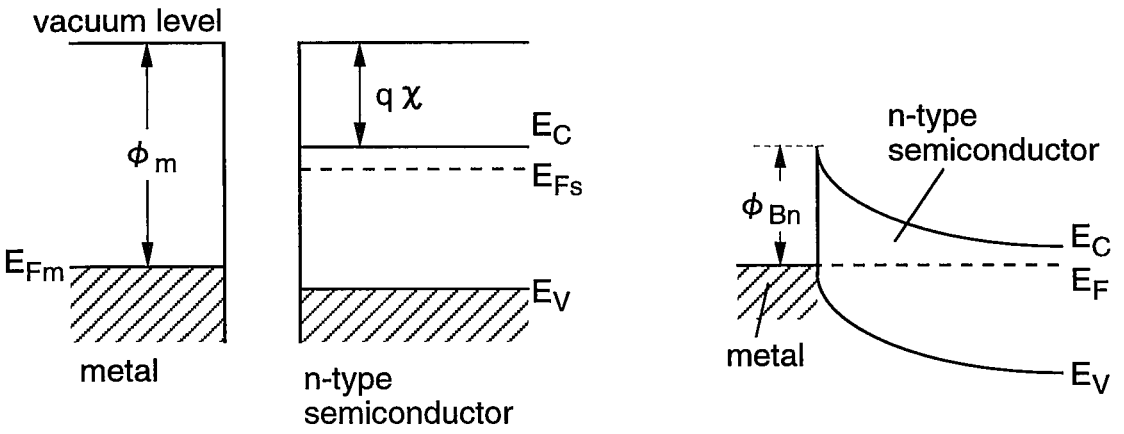
the disorder of the interface, therefore the metal workfunction dependence of SBH will be recovered by reducing the disorder. This is the one approach to reach the goal of the purpose of this work.

3.2.2*SBH control by interface control layer (ICL)*

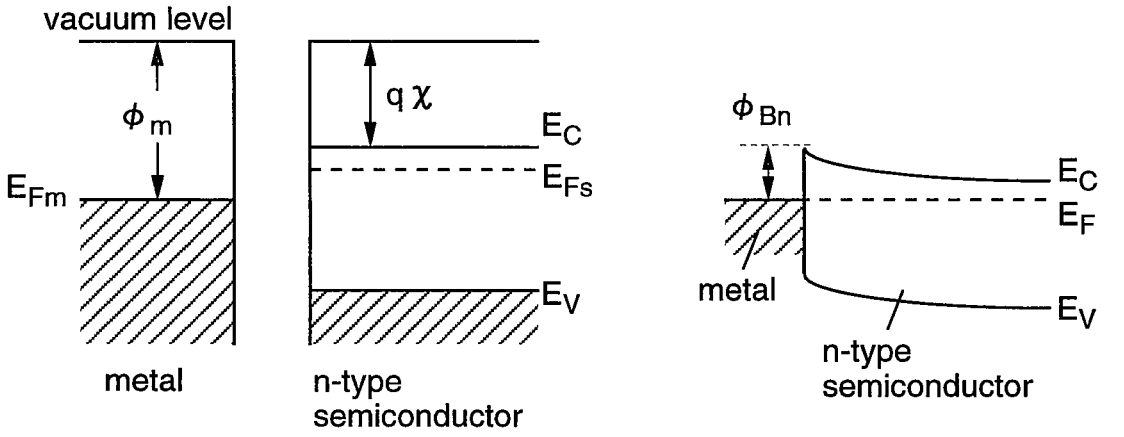
The another approach for the SBH control is using the technique by inserting "interface control layer" at M-S interface. The basic structure of an M-S system investigated in the present study is schematically shown in **Fig.3-2(a)**. Here, an ICL is inserted to control SBH as well as the current transport properties. As the ICL, an insulator ICL and a semiconductor ICL shown in **Fig.3-2(b)**, are investigated theoretically. The basic principle for control of SBH by the ICL is schematically shown in **Fig.3-2(c)**. SBHs for n-type or p-type semiconductors correspond to the energy difference between the Fermi level in the metal and the edge of the conduction band or the valence band of the semiconductor, respectively, on the assumption that the ICL is thin enough to allow tunneling of carriers through the ICL. If negative or positive charges are introduced into the ICL, band bending of the ICL is caused, and SBH of n-type semiconductor becomes high or low, respectively, provided that the firmly Fermi level pinning takes place at metal/ICL interface and that no pinning exists at ICL/semiconductor interface. Using the simple depletion approximation for carriers in the ICL, the change of SBH $\Delta\phi_B$ is given by,

$$\Delta\phi_B = \frac{q N_{ICL} t_{ICL}^2}{2 \varepsilon_{ICL}} \tag{3.2}$$

where N_{ICL} is the charge density in the ICL, ε_{ICL} and t_{ICL} are permittivity and thickness of the ICL, respectively. The ICL charge may be fixed ionic or defect space charge in the oxide ICL[16] and ionized donor/acceptor charge in the semiconductor



(a)



(b)

Fig.3-1. Band diagrams of ideal metal/semiconuctor contaocts in the case of (a) high- and (b) low-workfunction metals.

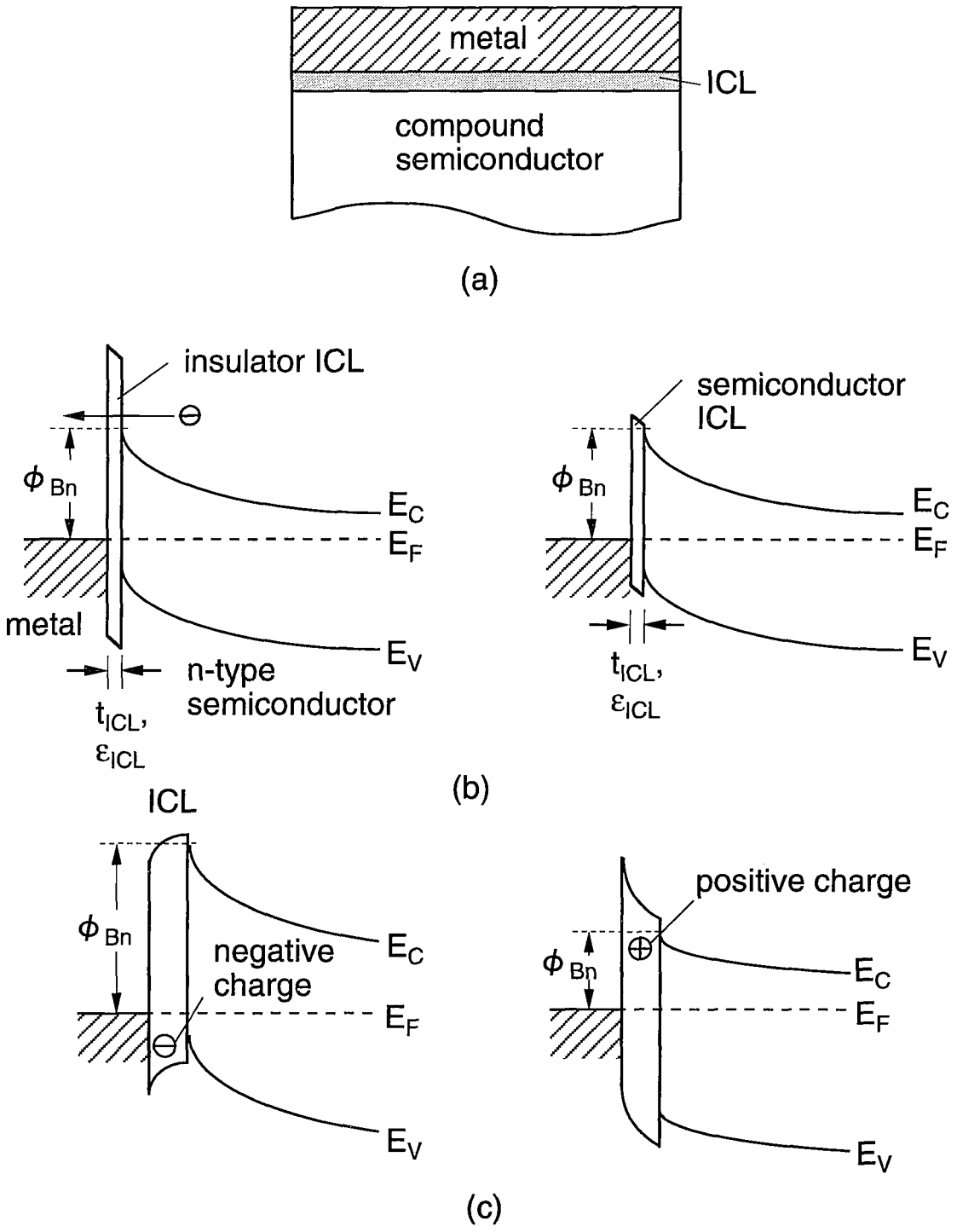


Fig.3-2. (a) The M-S structure with an ICL and (b) band diagrams of the M-S interface with an insulator ICL and with a semiconductor ICL. (c) Concept of SBH control by the ICL.

ICL. From **eq.(3.2)**, it is found that one can realize SBH value he needs by changing N_{ICL} or t_{ICL}. Large value of factor $N_{ICL}/\varepsilon_{ICL}$ gives large change of SBH, but the factor is likely to strongly depend on the material and there are several restriction on SBH control by ICL. However, the ICL thickness should be thin in order to retain the property of a direct M-S interface.

3.3 Modeling of M-S interfaces based on the unified DIGS model

Various models have been proposed and discussed about the formation mechanism of Schottky barrier.[13,14,16-21] Schottky's model indicates that SBH is determined by metal workfunction and electron affinity of the semiconductor.[1] On the other hand, if a large amount of interface states exist at M-S interface, SBH cannot be changed even if the semiconductor contacts with the metals which have different workfunction from each other according to Bardeen's model.[15] However, the results of experimental researches indicate that SBH slightly depends on metal workfunction. The metal-workfunction dependence of SBH on the metal is characterized by interface index S, which is defined by $S=d\phi_B/d\phi_m$ and S of most of III-V compound semiconductors is about 0.1 as indicated in the previous chapter.

According to the unified DIGS model, deposition of metal or insulator on a semiconductor disturbs the crystalline perfection of the semiconductor and forms a thin disordered semiconductor layer whose electronic properties are characterized by the DIGS continuum [13,14] The continuum has continuous energy and spatial distribution of gap states of acceptor type and donor type with a characteristic charge neutrality level E_{HO},[13,14] which is sp^3 hybrid orbital energy or corresponds to Tersoff's midgap energy.[20] E_{HO} lies at 0.47eV and 0.99eV from the valence band maxima E_V for GaAs and InP, respectively. Within the disordered layer, the deviation of the Fermi level from E_{HO} results in appearance of interface charge, which screens

metal workfunction as schematically shown in **Fig.3-3(a)**. Since the thickness of the disordered layer is of the order of 10Å or below, the electric field in the depletion layer of the ordered semiconductor region can be ignored. According to this model, S of a clean and intimate contact between metal and semiconductor is derived by solving Poisson's equation for the system in **Fig.3-3(a)** as [22]

$$S = sech(\delta/\lambda) \tag{3.3a}$$

$$\lambda = \sqrt{\varepsilon/q^2 N_{DG}} \quad \text{(the DIGS screening length)} \tag{3.3b}$$

where δ is the thickness of the disordered layer and N_{DG} is the DIGS density which is assumed to distribute uniformly in the band gap of the semiconductor, and interface state density N_{SS} corresponds to $N_{DG} \times \delta$.

The band diagrams of M-S interfaces with an insulator ICL and a semiconductor ICL are shown in **Fig.3-3(b)** and **(c)**, respectively. With the insulator ICL, the disorder is assumed to be caused in the semiconductor side only, since it is experimentally known that the S of the most of insulators is nearly unity.[2] Solving Poisson's equation of the system in **Fig.3-3(b)**, S is given by,

$$S = \frac{\text{sech}(\delta/\lambda)}{1 + q^2 (t_{ICL}/\varepsilon_t)\, N_{DG}\, \lambda \tanh(\delta/\lambda)} \tag{3.4}$$

where t_{ICL} and ε_{ICL} are the thickness and the permittivity of the ICL, respectively. In the case of $\delta \ll \lambda$, **eq.(3.3)** corresponds to the result of Cowley and Sze.[23] On the other hand, in the case of a semiconductor ICL, the disorder layer is assumed to be in both ICL and semiconductor sides as shown in **Fig.3-3(c)**. Assuming that whole of the ICL is disordered , S with an semiconductor ICL is given by,

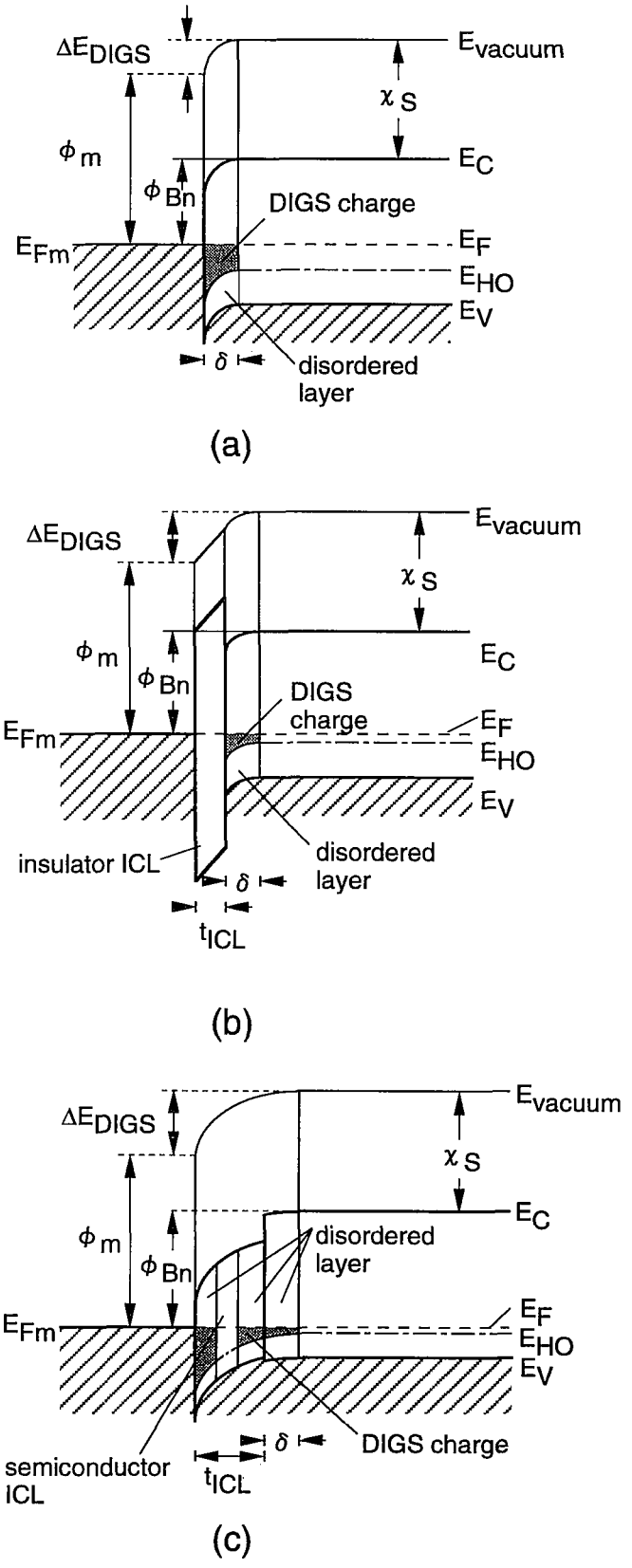


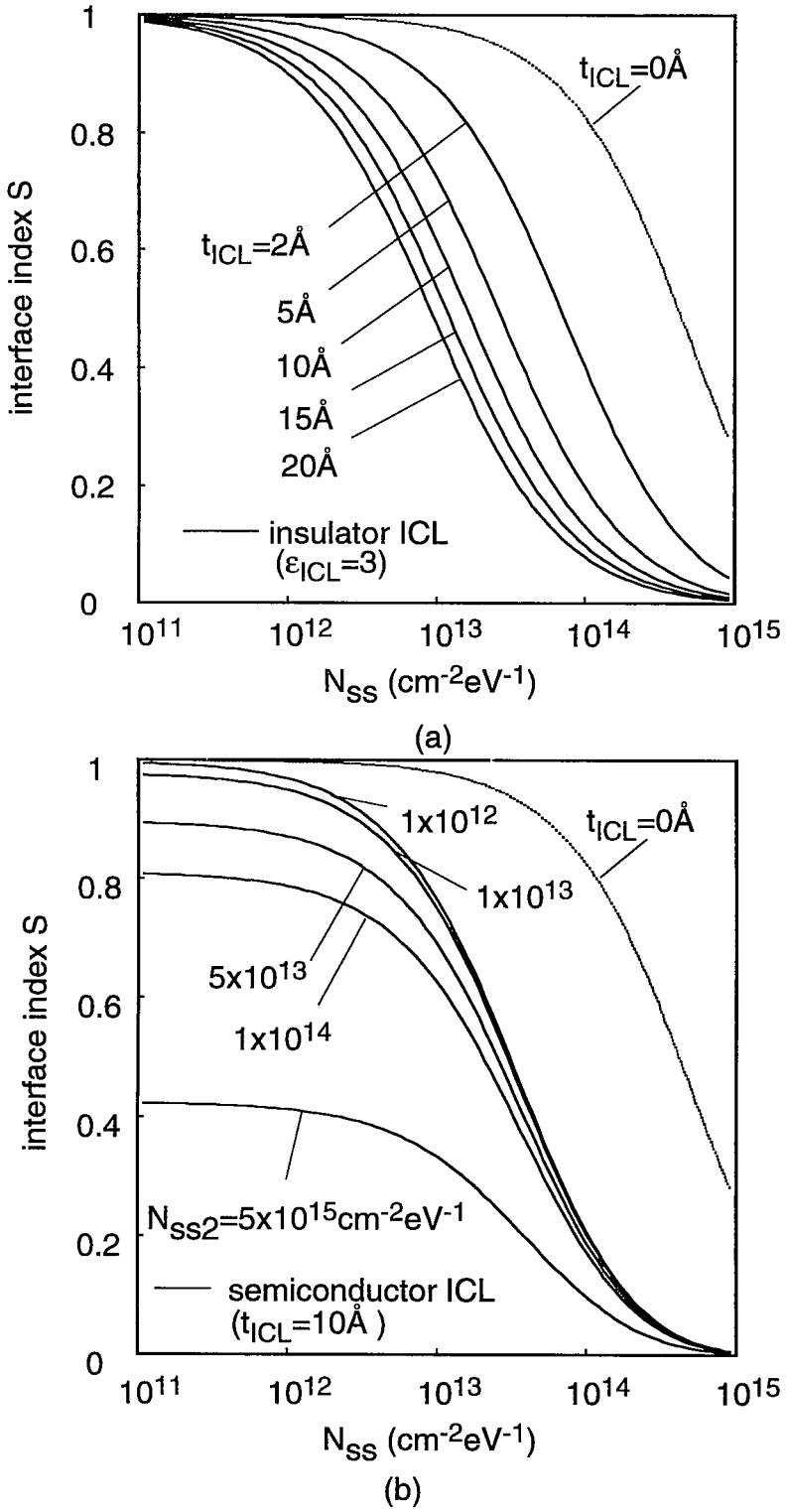
Fig.3-3. Band structures of M-S interfaces based on the DIGS model. (a) Intimate M-S contact, (b) a M-S interface with an insulator ICL and (c) a M-S interface with a semiconductor ICL, respectively.

$$S=\frac{\operatorname{sech}(\delta/\lambda)\operatorname{sech}(t_{ICL}/\lambda_t)}{1+\frac{\varepsilon_s}{\lambda}\frac{\lambda_t}{\varepsilon_t}\tanh(\delta/\lambda)\tanh(t_{ICL}/\lambda_t)} \quad (3.5a)$$

$$\lambda_t=\sqrt{\varepsilon_t/q^2 N_{DGt}} \quad (3.5b)$$

where λ_t is the DIGS screening length in the ICL side and N_{DGt} is the DIGS in the ICL.

Figures 3-4(a) and **3-4(b)** are the results of the calculation of S for three types of M-S systems shown in **Fig.3-3**. When an insulator ICL is inserted, S becomes small even if N_{DG} is the same as that of the intimate contact. The position of interface state charge is apart from the metal, then small number of charges at ICL/semiconductor interface states can screen the metal workfunction sufficiently than the intimate contact. S of a semiconductor ICL is small even if N_{DG} is zero, which is due to the metal workfunction is screened by the interface state charge at metal/ICL. The reported values of S are about 0.1~0.2 for Si and the most of III-V semicondu ctors,[24,25] this derives that S of metal/semiconductor ICL/semiconductor system is about 0.1~0.2 even if N_{DG} at ICL/semiconductor interface is small enough. In the case of SBH control using the ICL method, the appeared small S is not problem since low N_{DG} is rather important as described in next section.



N_{SS} : interface state density in metal/ICL interface
N_{SS2}: interface state density in ICL/semiconductor interface

Fig.3-4 Calculated interface index S for M-S interfaces (a) with an isulator ICL and (b) with a semiconductor ICL.

3.4 Detailed investigation of SBH control utilizing ICL

3.4.1 *Method of SBH calculation by numerical simulation*

For a quantitative analysis, a general theory on electrical properties of the Schottky barriers having insulator or semiconductor ICLs on the basis of the DIGS model has been developed using numerical potential calculation, including the effects of the band line-up, band gap narrowing, ICL thickness, fixed charge, donor/acceptor charge and interface state charge. Exact solution of Poisson's equation as follow is done for the estimation of the behavior of SBH under these effects.

$$\frac{d}{dx}\left(\varepsilon(x)\frac{d}{dx}\phi(x)\right) = -q\left(N_D^+(x,\phi)-N_A^-(x,\phi)-p(x,\phi)+n(x,\phi)+N_{add}(x,\phi)\right) \tag{3.6a}$$

$$\phi_B = \phi(t_{ICL}) \tag{3.6b}$$

where N_D^+ and N_A^- are ionized donor and acceptor concentration, and n and p are electron and hole concentration, respectively. N_{add} is the additional charge, including interface state charge. SBH is defined to be the difference of energy between the Fermi level in the metal and the band edge of the semiconductor at the IC L/semiconductor interface. Fermi integral for carrier distribution is substituted by approximated equation in **ref.26**, which gives better approximation than that of Boltzmann approximation, especially when the semiconductor is degenerated. Poisson's equation is solved numerically by using the shooting method. As boundary conditions, Fermi level is assumed to be completely fixed at metal/ICL interface. This approximation is reasonable for metal/Si ICL/semiconductor system, taking account of the experimental results that S is very close to zero.[4,27] The flat band approximation

is applied to the calculation of the semiconductor band, that is $d\phi/dx=0$ in the semiconductor, for general discussion of SBH for n- and p-type semiconductors.

3.4.2 *Band line-up, strain and heavy doping effects*

The DIGS model is applied to determination of band line-up. First, the bulk band lines up as the E_{HO} of each materials align to the same level. The band diagrams of bulk Si/GaAs and bulk Si/InP systems are shown in **Figs. 3-5(a)** and **(c)**, respectively. However, the most of ICL materials having different lattice constant from the substrate material, then the overlayer is strained and the band gap of ICL changes. In this study, not only the change of band gap but also the shift of E_C and E_V are calculated. The strain is decomposed to hydrostatic strain and share strain components. The band-edge shift due to hydrostatic strain, ΔE_C(hydrostatic) and ΔE_V(hydrostatic) are given by,

$$\Delta E_C(hydrostatic) = a_C(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \quad (3.7a)$$

$$\Delta E_V(hydrostatic) = a_V(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \quad (3.7b)$$

where a_C and a_V are the hydrostatic deformation potentials of conduction and valence band, respectively, and ε_{xx}, ε_{yy} and ε_{zz} are the elements of the strain tensor. By the share strain, the valence band edge splits by ΔE_{HH}, ΔE_{LH} and ΔE_{SO}, which are the shifts of the light hole, heavy hole and spin-orbital-splitting state, respectively. The conduction band of the indirect band gap materials also changes by the share strain. The shift of the valence band and conduction band edge, ΔE_V(share) and ΔE_C(share) respectively, are given by the highest or lowest state of split energy levels. Assuming that the semiconductor-growth direction is along [001], ΔE_C(share)

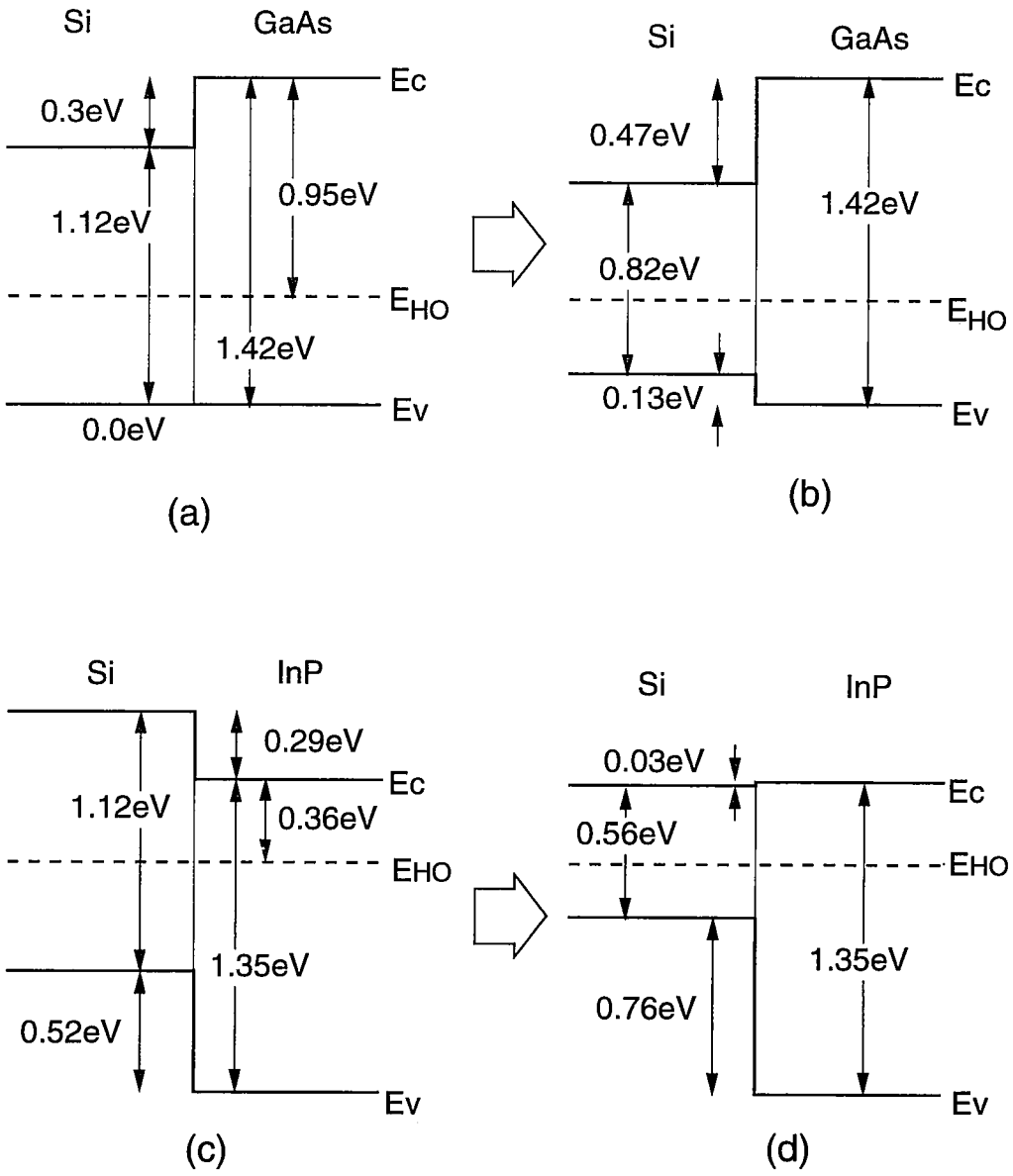


Fig.3-5. The band lineup of Si/GaAs system (a) without and (b) with strain, and that of Si/InP system (c) without and (d) with strain.

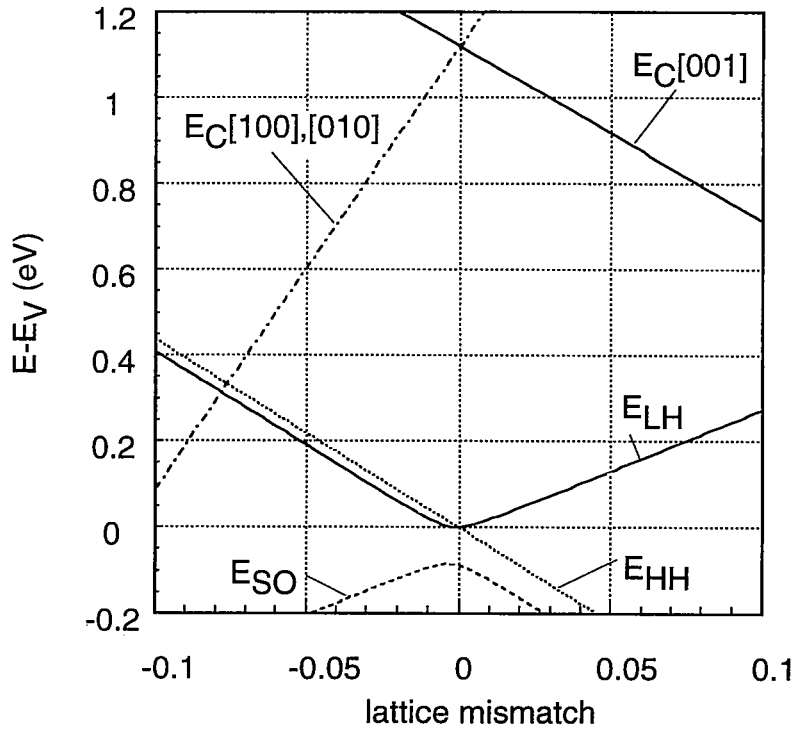
and ΔE_V(share) are given by,

$$\Delta E_V(share) = \begin{cases} \Delta E_{HH} = \varepsilon & \text{:tensile} \\ \Delta E_{LH} = \frac{1}{2}\left(\varepsilon - \Delta + \sqrt{\Delta^2 + 2\Delta\varepsilon + 9\varepsilon^2}\right) & \text{:compress} \end{cases} \tag{3.8}$$

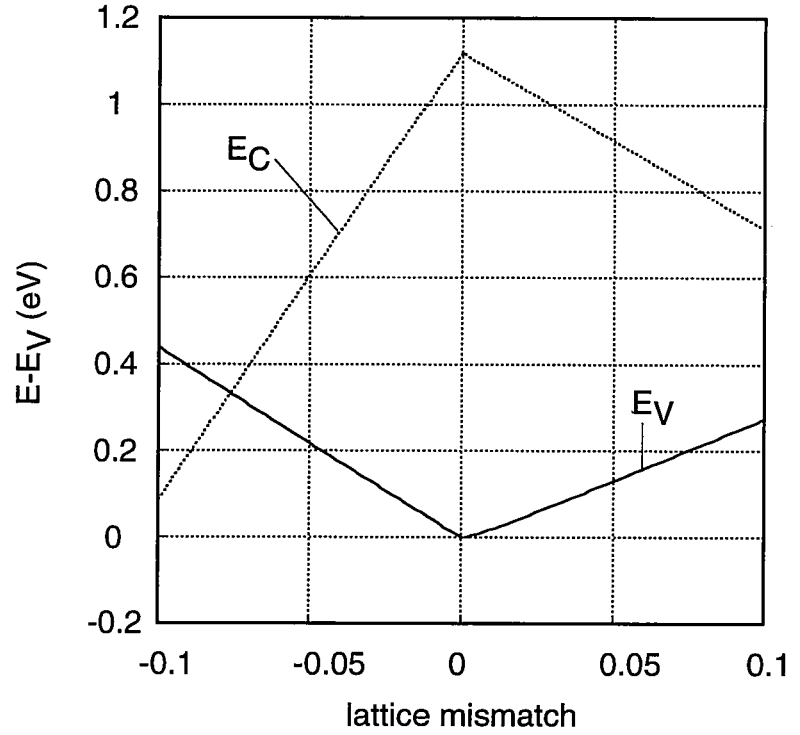
$$\Delta E_C(share) = \begin{cases} -\frac{2}{3}\Xi_u^{\Delta}(\varepsilon_{zz} - \varepsilon_{xx}) & \text{:tensile} \\ \frac{1}{2}\Xi_u^{\Delta}(\varepsilon_{zz} - \varepsilon_{xx}) & \text{:compress} \end{cases} \tag{3.9}$$

where $\varepsilon = b(\varepsilon_{zz}-\varepsilon_{xx})$, b and Ξ_u^{Δ} are the deformation potential of valence band and conduction band by share strain, respectively, Δ is the spin-orbital splitting energy. The parameters for the calculation of Si ICL are a_C=0.6eV, a_V=-1.6eV, b=-1.36eV, Δ=0.044eV and Ξ_u^{Δ}=-8.1eV.[28,29] The shift of each band edge is given by ΔE_C (hydrostatic)+ΔE_C(share) and ΔE_V(hydrostatic)+ΔE_V(share) for the conduction band and the valence band, respectively. **Figures 3-6(a)** and **(b)** shows the shift of each energy band and the Si band structure as a function of lattice mismatch, respectively. The band gap becomes narrow on both tensile and compress strain. The band line-up of Si/GaAs and Si/InP with strain effect is shown in **Fig.3-5(c)** and **3-5(d)**, where each of lattice mismatches is 4% and 8%, respectively.

Band gap narrowing is also caused by heavy doping into the ICL. This is due to broadening of the impurity band and its band tails. The band gap narrowing ΔE_g by heavy doping is given by the following formula [30]:



(a)



(b)

Fig.3-6 Calculated (a) each band and (b) entire band structure of Si as a function lattice mismatch to substrate lattice constant.

$$\Delta E_g = 0.009 \left\{ \ln\left(\frac{N_{ICL}}{10^{17}}\right) + \sqrt{\left(\ln\left(\frac{N_{ICL}}{10^{17}}\right)\right)^2 + \frac{1}{2}} \right\} \quad \text{(eV)} \qquad (3.10)$$

ΔE_g is divided to each shift of E_C and E_V. The relation between the shift of E_C and E_V by doping, ΔE_C(doping) and ΔE_C(doping), respectively, is given by,

$$\frac{\Delta E_C(doping)}{\Delta E_V(doping)} = \frac{\left(\frac{E_g}{2} - E_F\right) - T\frac{d}{dT}\left(\frac{E_g}{2} - E_F\right) + \alpha_p kT + \beta kT}{\left(\frac{E_g}{2} + E_F\right) - T\frac{d}{dT}\left(\frac{E_g}{2} + E_F\right) + \alpha_n kT + \beta kT} \qquad (3.11)$$

where $\alpha_p = \ln(p)/\ln(T)$ and $\alpha_n = 0$ for n-type ICL, and $\alpha_p = 0$ and $\alpha_n = \ln(n)/\ln(T)$ for p-type ICL and $\beta = 1.5$. The change of E_C and E_V,ΔE_C(doping) and ΔE_V(doping), can be obtained by dividing ΔE_g in proportion to ΔE_C(doping)/ΔE_V(doping). When N_{ICL} is 3×10^{19}cm^{-3}, ΔE_g is estimated about 100meV, which is not negligible for the SBH calculation.

Quantized effects seem to be important in certain case. If type-I structure that the band gap of the ICL is wider than that of the semiconductor, it is possible that the electron-state at ICL-S interface changes into two-dimensional density of state (DOS) like as a modulation-doped heterostructure. The effective band edge is substituted by the quantized-ground state at the interface, then E_F can move wider than E_g of the ICL and ϕ_B can be larger than E_g of the semiconductor. This situation can be seen in the metal/unstrained Si ICL/InP structure. However, which is suppressed by strain.

When ICL is doped heavily, the band bends paraborically and a potential well is formed. But, states in the well is not quantized since the barrier is low and very thin in the case of metal/Si ICL/GaAs or InP and wavefunction easily penetrate into the

barrier. The effect of the band gap narrowing by strain on quantized states will become important for metal-insulator-semiconductor (MIS) or S-S structures since a quantum well is formed at the interface. **Figure 3-7** shows the ground state energy E_{e0} from the conduction band of GaAs as a function of the Si ICL thickness for SiO_2/Si ICL/GaAs and GaAs/Si ICL/GaAs structures. The difference of E_{e0} with and without strain is large when the Si ICL thickness is more than 20Å for SiO_2/Si ICL/GaAs structures. However, the difference becomes small since the ground state almost aligns to the GaAs conduction-band edge both with and without strain, when the Si ICL is less than 20Å. On the other hand, the difference of E_{e0} in the S-S structure with Si ICL still remains when the Si ICL thickness is less than 10Å.

The calculated SBHs for metal/Si ICL/GaAs and metal/Si ICL/InP systems without and with bandgap narrowing effects are shown in **Figs.3-8** and **3-9**, respectively. The critical thickness of Si/GaAs and Si/InP structure are about 14Å and 7Å, respectivly.[31] However, in this calculation, Si ICL is assumed not to be relaxed even if the ICL thickness is over the critical thickness. The range of SBH control comes to narrow by strain compared with the unstrained structure, and it is found that SBH can change from 0.4eV to 1.3eV for n-GaAs and from 0 to 0.6eV for n-InP by applying Si ICL with moderate doping and thickness. The change of E_F positions is limited by mainly E_g of the ICL. Therefore, if the E_g of an ICL is larger than that of a semiconductor, it is possible that E_F moves over E_C or E_V of the semiconductor. The clear change of SBH can be seen when N_D or N_A of the ICL is over $10^{20}cm^{-3}$. From the result, in the case of the other ICL material, it needs for the material that $N_{ICL}/\varepsilon_{ICL}$ can be over $10^{19}cm^{-3}/\varepsilon_0$ in order to control SBH sufficiently.

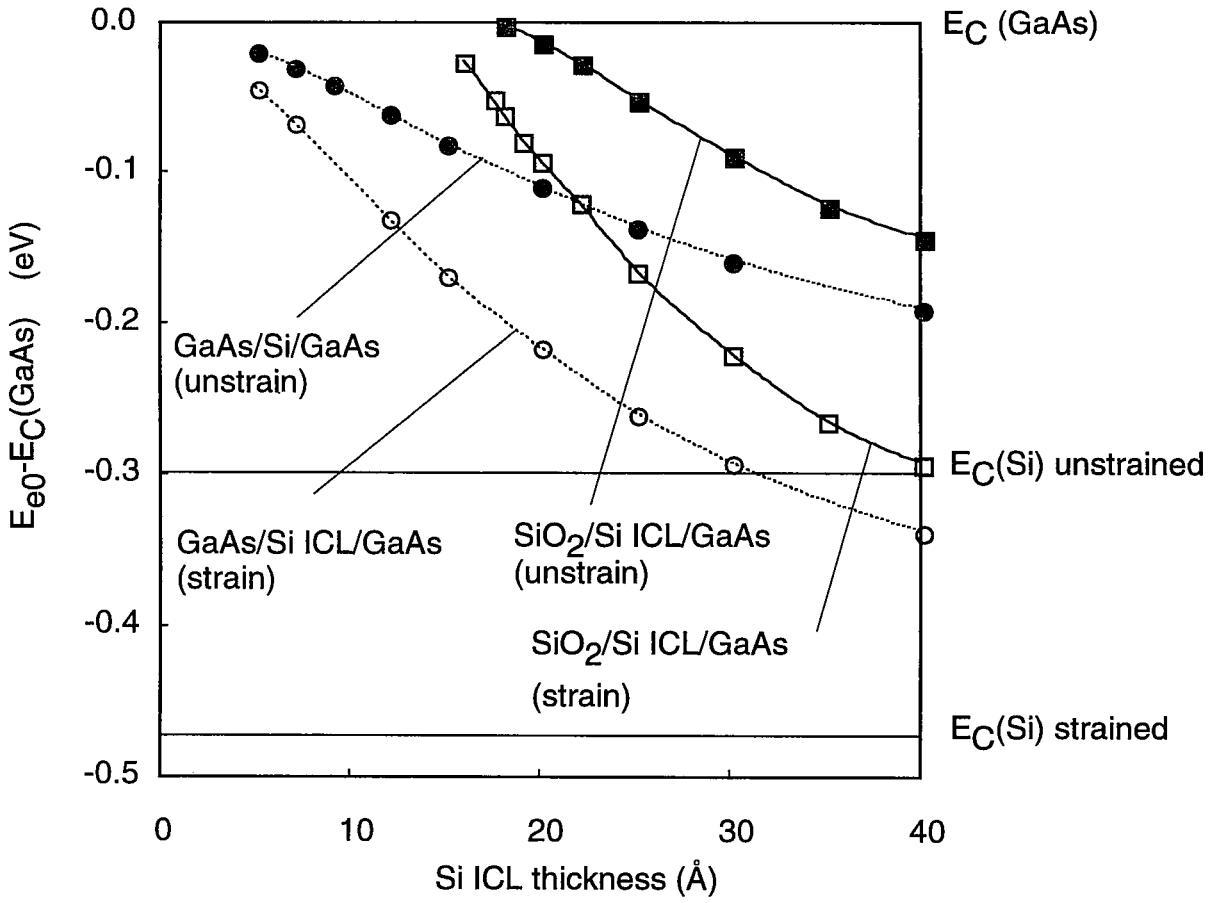


Fig.3-7 Ground state of quantized levels in SI ICL for GaAs/Si ICL/GaAs and SiO_2/Si ICL/GaAs systems with and without strain.

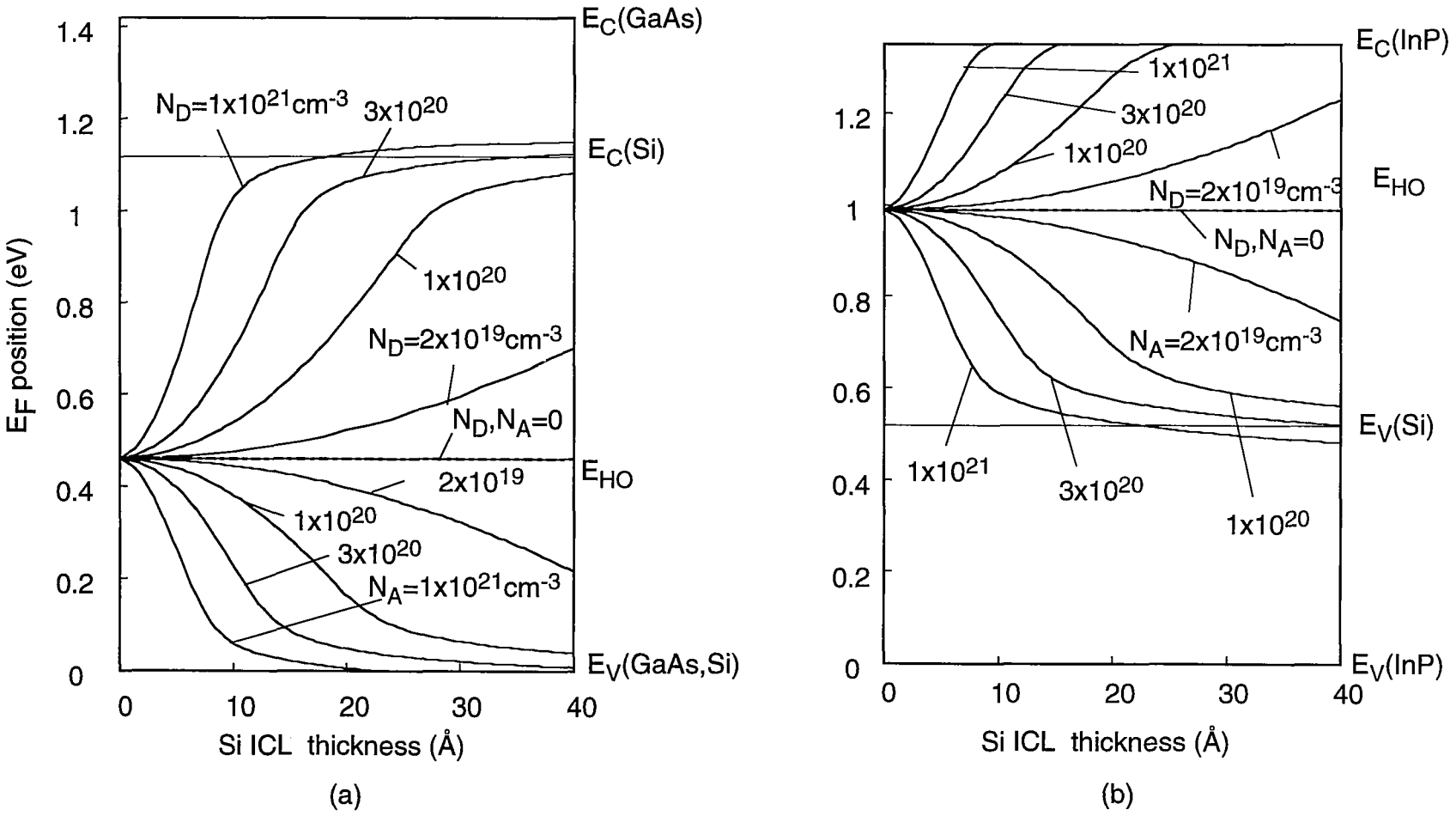


Fig.3-8. Calculated semiconductor surface Fermi level position of (a) metal/Si ICL/GaAs and (b) metal/Si ICL/InP system without strain.

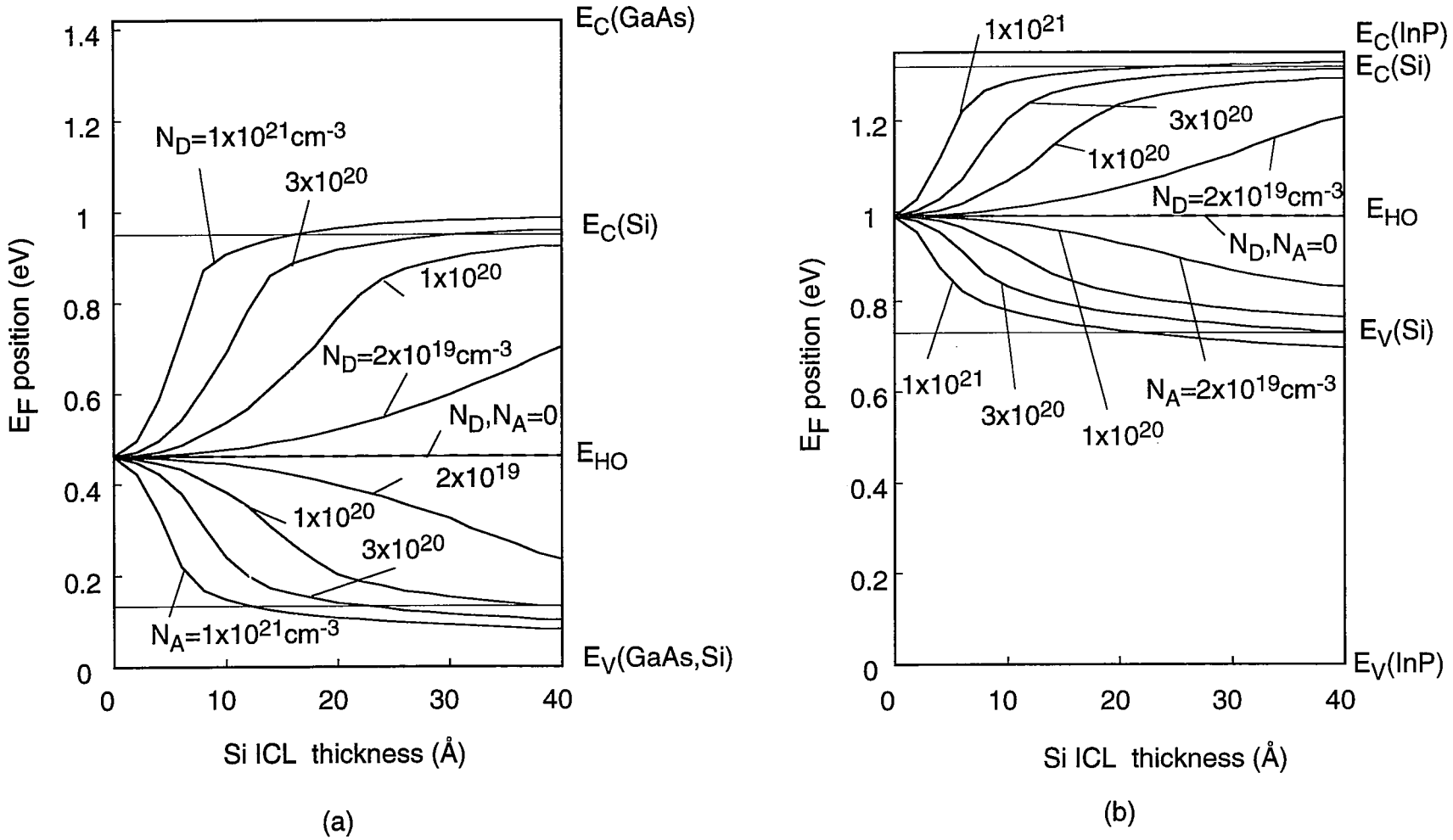


Fig.3-9. Calculated semiconductor surface Fermi level position of (a) metal/Si ICL/GaAs and (b) metal/Si ICL/InP system with strain.

3.4.3 *Effect of interface states*

The control of SBH by the ICL method is achieved by introducing charges into the ICL. On the other hand, interface states at the ICL/semiconductor interface effect on the SBH control. With the depletion approximation, the change of SBH by doping into the ICL under the effect of the interface state is given by,

$$\Delta\phi_B = \frac{q(N_D^+ - N_A^-)t_{ICL}^2}{2\varepsilon_{ICL}\left[1+\frac{q^2}{\varepsilon_{ICL}}N_{SS}t_{ICL}\right]} \tag{3.12}$$

where ε_{ICL} and t_{ICL} are the permittivity and the thickness of the ICL, N_{SS} is interface state density at the ICL/semiconductor interface, N_D^+ and N_A^- are the ionized donor and acceptor density in the ICL, respectively, and $N_{ICL}=N_D^+-N_A^-$. N_{SS} is assumed to distribute uniformly in the band gap. It is found that the interface states have a tendency to cancel the effect of doping. As the N_{SS} becomes large, the change of SBH comes to zero. The interface states distribution based on the DIGS model is approximately given by,

$$N_{SS}=\begin{cases} N_{SS0}\,exp\left(\left(|E-E_{HO}|/E_1\right)^{n_1}\right) & (E_V<E<E_{HO}) \\ -N_{SS0}\,exp\left(\left(|E-E_{HO}|/E_2\right)^{n_2}\right) & (E_V<E<E_{HO}). \end{cases} \tag{3.13}$$

where E_1, E_2, n_1 and n_2 are the parameters determining the shape of the N_{SS} distribution. **Figure 3-10** shows the calculated SBH by numerical band simulation using **eq.(3.6)**. In this calculation N_D or N_A= 3x10^{20}cm^{-3} and the uniform and U-

shaped distribution of N_{SS} are assumed. The band gap narrowing effect is also included. The SBH can be changed ideally when N_{SS} is less than $1x10^{12}cm^{-2}eV^{-1}$. The difference of the variation of E_F position between the uniform and U-shaped N_{SS} distributions is observed when N_{SS0}~$10^{13}cm^{-2}eV^{-1}$. From the curve of the uniformed N_{SS}, it is found that the control-range of E_F comes to be suppressed strongly when N_{SS0} is over $10^{13}cm^{-3}eV^{-1}$. In the case of U-shaped N_{SS}, the E_F can be changed in the band gap where N_{SS} is less than $10^{13}cm^{-2}eV^{-1}$. However, when N_{SS} is over $10^{13}cm^{-3}eV^{-1}$, the control-range of E_F is limited to the energy-range smaller than E_g of the ICL. The SBH comes not to depend on t_{ICL} and comes to be constant, when t_{ICL} is over the 20Å. From **eq.(3.12)**, in the case of $q^2N_{SS}t_{ICL}/\varepsilon_{ICL}\ll 1$, $\Delta\phi_B \sim qN_{ICL}t_{ICL}^2/2\varepsilon_{ICL}$ and the SBH changes parabolically by t_{ICL}. On the other hand, in the case of $q^2N_{SS}t_{ICL}/\varepsilon_{ICL} \gg 1$, $\Delta\phi_B \sim N_{ICL}t_{ICL}/qN_{SS}$ and the SBH changes linearly by t_{ICL}. Further t_{ICL} increases and becomes larger than the depletion width $W\sim\sqrt{2\varepsilon_{ICL}V_{bi}}/qN_{ICL}$, **eq.(3.12)** cannot be applied. The potential difference of the metal/ICL interface is completely screened by ionized impurity in the ICL and the interface state charge at the ICL/semiconductor also balances with the ionized impurity, therefore the SBH comes to independent on t_{ICL}.

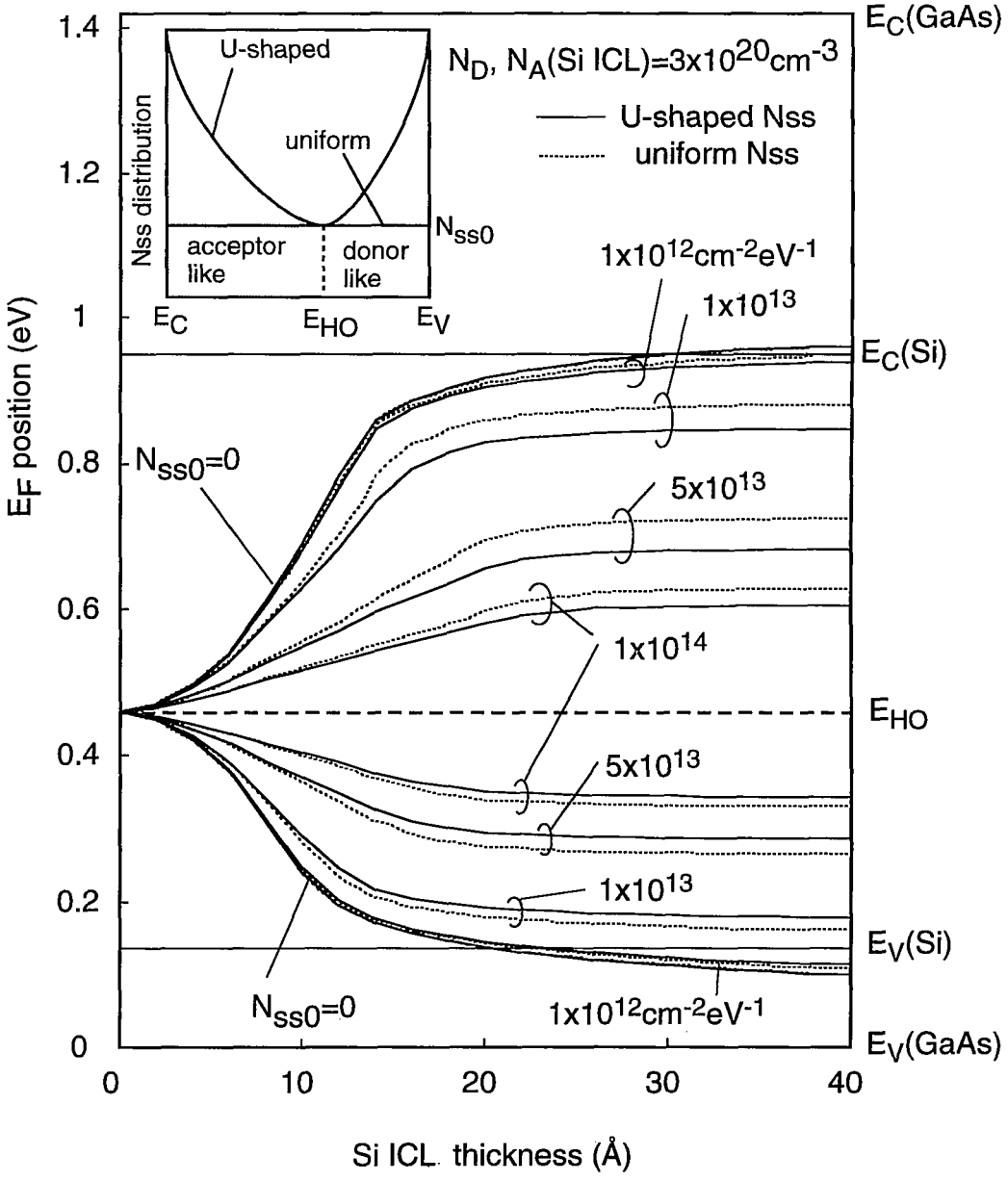


Fig.3-10 Effect of interface state at Si ICL/GaAs interface on the Fermi level position of metal/Si ICL/GaAs system. The inset shows uniform and U-shaped N_{SS} distibutions.

3.5 Current transport

3.5.1 *Forward current transport*

The current transport through the most of the III-V compound semiconductor's Schottky barriers is dominated by thermionic emission current. Richardson constant A^{**} is an important parameter for considering the current transport through the interface. Theoretically, A^{**} is given by 120 m^* A/cm^{2}T^2, where m^* is the effective mass of the majority carrier of the bulk semiconductor. A few years ago, Missous et al. pointed out that the A^{**} of Al/clean MBE GaAs Schottky barrier reduced anomalously.[32] This can not be observed for the Al/Si ICL/MBE GaAs. [6] This reduction of A^{**} seems to indicated that the current transport through the interface is disturbed by some kind of interfacial layer at the M-S interface and the property of the M-S interface with an ICL is different form that of the direct M-S interface without an ICL.

When the electrical barrier by the ICL is high, as shown in **Fig.3-2(b)**, the transition probability through the interface is possible to become small, even if the ICL is very thin. By W.K.B. approximation, the tunneling coefficient for squared potential is given by,[24]

$$T = exp\left(-a\sqrt{m^*_{ICL}\Delta E}\ t_{ICL}\right) \tag{3.14}$$

where m_{ICL}^* is the effective mass of the ICL, ΔE is the band discontinuity of the ICL/semiconductor system, t_{ICL} is the ICL thickness and a is constant. The current through the interface becomes the multiplication of T and thermionic emission current. In the case of $\Delta E>0$, T becomes smaller than unity and the thermionic emission current decreases, which is observed as if the SBH turns to be high in *I-V*

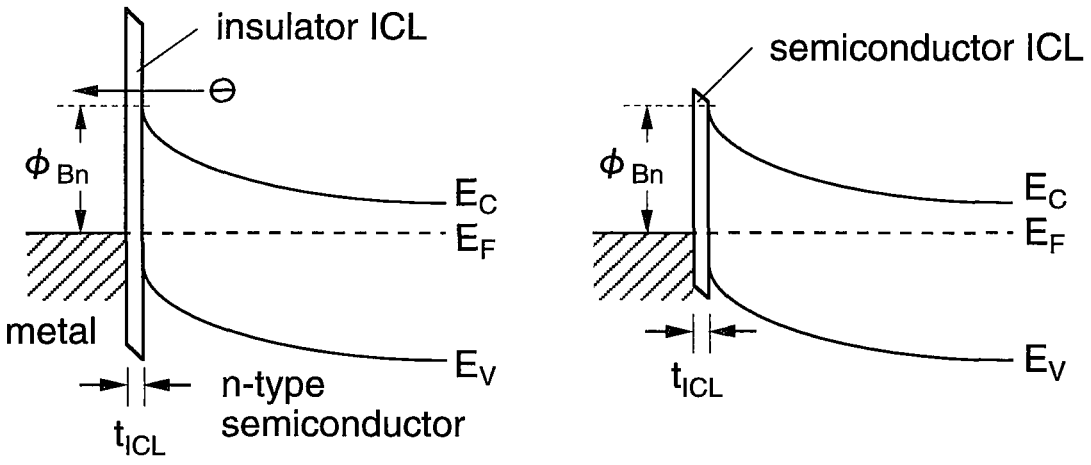
characteristics. This equation also indicates that ΔE and t_{ICL} make A^{**} from Richardson plot smaller than the theoretical one, that is,

$$A^{**}(\text{expeliment}) = A^{**}(\text{theory})\ exp\left(-a\sqrt{m^{*}\ \Delta E}\ t_{ICL}\right) \tag{3.15}$$

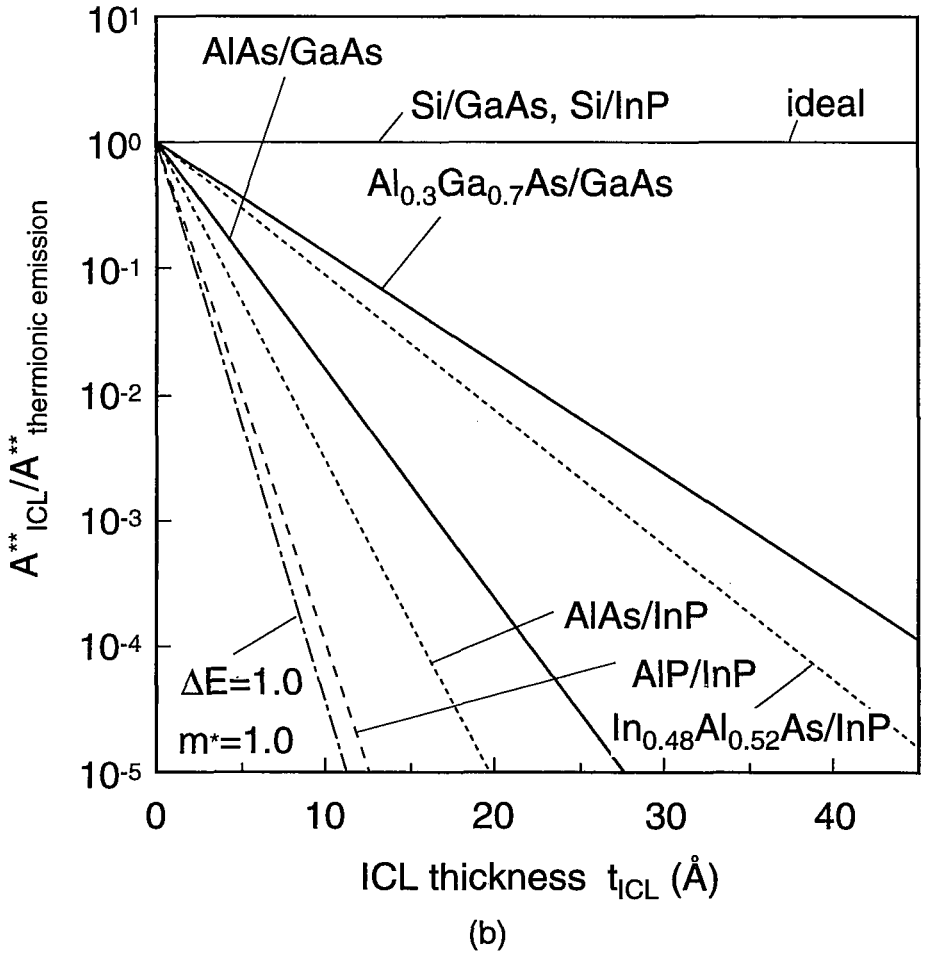
Calculated A^{**} for GaAs and InP M-S interfaces with various ICLs is shown in **Fig.3-11**. It is found that A^{**} with a certain ICL becomes anomalously small even if the ICL is a few ten angstrom. The AlAs interfacial layer with only a few monolayers causes anomalous reduction of A^{**} since the ΔE_C of AlAs/GaAs is as large as about 400meV. On the other hand, with the use of Si ICL for GaAs and InP SBH control, the reduction is not observed even if the t_{ICL} is 40Å. This seems to show that Si/GaAs and Si/InP has type-I structure that E_g of Si is smaller than that of GaAs and InP as shown in **Fig.3-5(b)** and **3-5(d)**, and the Si ICL is not barrier for carrier transport. The barrier ΔE by the ICL does not give high Schottky barrier essentially, so this interface barrier should be considered to block the thermionic emission current at the M-S interface. From this point, materials having small ΔE and being thin are required for ICLs.

3.5.2 *Reverse current transport*

Reverse leakage current of Schottky barrier is the one of the important problems for device application. Experimentally, the Schottky diodes with some kind of oxide ICLs are known to give unexpectedly large reverse leakage current that is far from the thermionic emission current. [5, 15, 33] But such a current is not observed with Si ICL.[5] This implies that the ICL affects not only the forward current transport but also the reverse current. The DIGS model including the existence of an interface layer shows the bias dependence of SBH as follow,



(a)



(b)

Fig.3-11 (a) Model for reduction of A** and (b) calculated Richardson constant A^{**} with various ICLs.

$$\phi_B(V) = \phi_B(0) + (\alpha+\beta)\, E\,(V), \tag{3.16a}$$

$$\alpha = \frac{\varepsilon_S q\, t_{ICL}}{\varepsilon_{ICL} + q^2\, t_{ICL} N_{SS}} \quad , \tag{3.16b}$$

$$\beta = \sqrt{\frac{q}{4\pi\varepsilon_S}} \tag{3.16c}$$

where $E(V)$ is the maximum field in the semiconductor. ε_S is the permittivity of the semiconductor. β is the constant due to the Schottky effect.[24] Calculated I-V curves with ICLs are shown in **Fig.3-12**. The difference of the current from the thermionic emission current is caused by the bias dependence of the effective SBH. The **eqs. (3.16)** show that the ICL permittivity and the interface state at ICL/semiconductor play important roles in the reverse I-V characteristics. The calculated current largely differs from the ideal current when ε_{ICL} and N_{SS} are low. Small permittivity of the ICL causes large voltage drop in the ICL, when N_{SS} is low. The effective SBH decreases with the reverse bias, which causes reverse leakage current. Therefore, the leakage current is suppressed when N_{SS} are large, but this is contrary to the requirement of the SBH control. From this point, the large value of ε_{ICL} is required.

Figure 3-13 shows the ratio of reverse current calculated by the DIGS model versus ideal current as a function of ε_{ICL} and N_{SS} at V=-1V. As the t_{ICL} increases, the leakage current ratio becomes large and the leakage current is remarkable when ε_{ICL} is small. When the permittivity is large as of semiconductors, most of them are about $10\varepsilon_0$, the bias dependence of SBH becomes much smaller because voltage drop in the ICL is suppressed even if the N_{SS} is small. In other words, using high permittivity of the ICL and introducing a large amount of charge into the ICL are needed for the control of SBH which is not changed by bias-application, in order to suppress the voltage drop in the ICL and to make high field for the sufficient change of SBH.

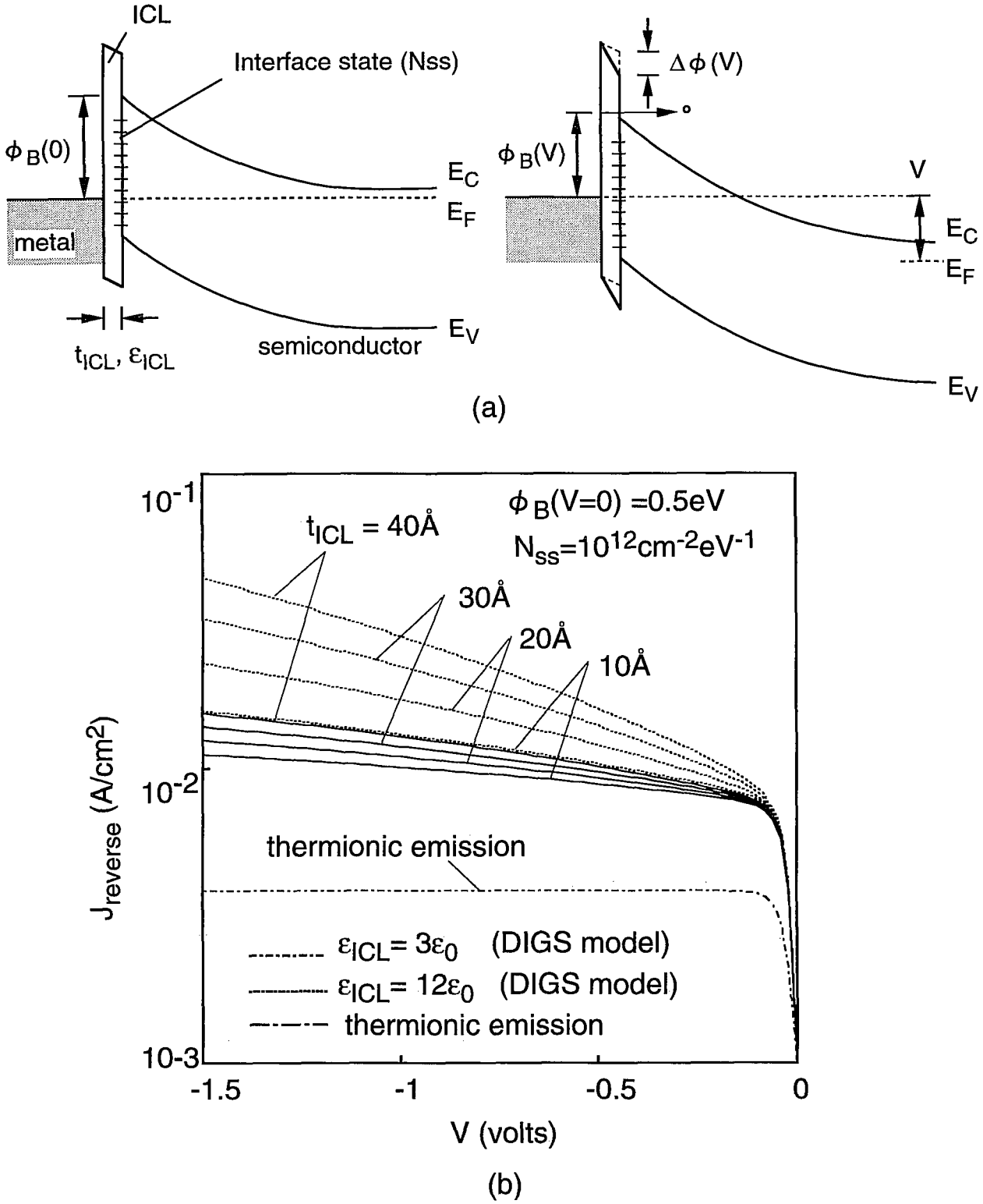


Fig.3-12. (a) Model for reverse leakage current and (b) calculated reverse I-V characteristics based on the DIGS model.

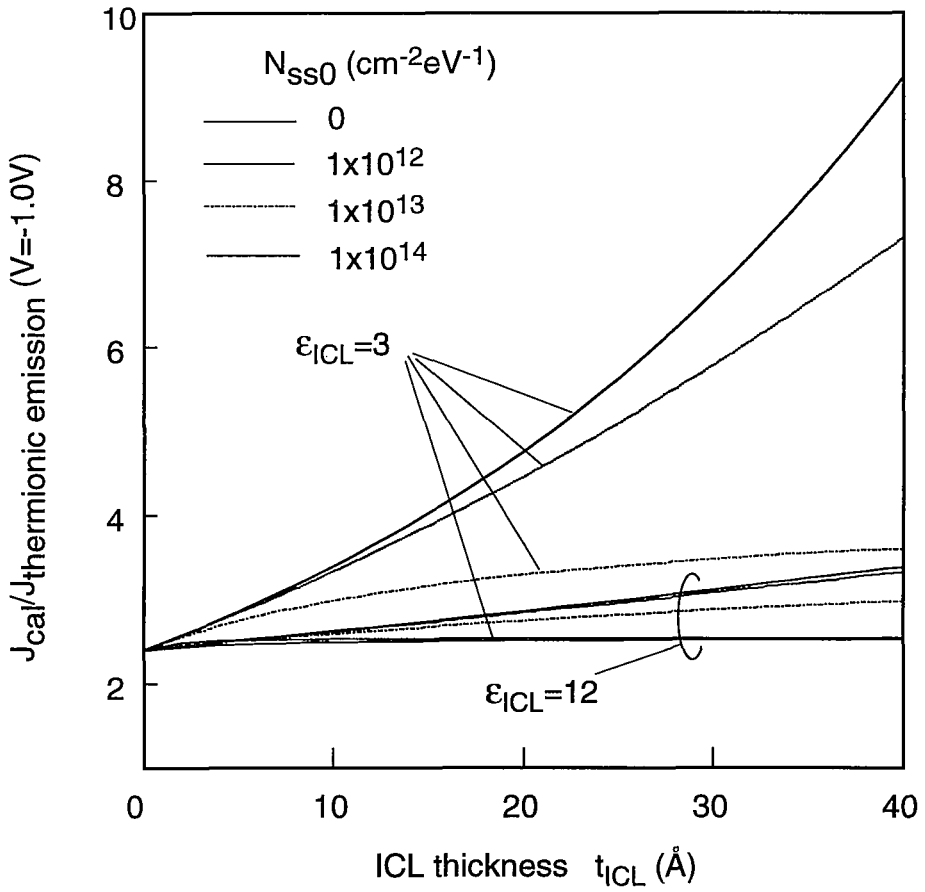


Fig.3-13. Calculated reverse current density J_{cal} of metal/ICL/ semiconductor structure versus thermionic current density as a function of ICL thickness.

3.6 Conclusions

In order to control Schottky barrier of III-V compound semiconductor precisely, the theoretical analysis of control of Schottky interface, mainly for the method using an interface control layer (ICL), was done from the point of view not only Schottky barrier height (SBH) but also forward and reverse current transport. The main conclusions are listed below:

(1) Metal/semiconductor interfaces with and without ICLs were modeled and their interface index S was calculated according to the DIGS model. The value of S was modified by inserting ICLs, which depended on the ICL material.

(2) SBH with Si ICL was calculated by the numerical potential simulation taking account of the band gap narrowing by strain and interface state effect. It was found that these effects limited the range of the SBH control. For sufficient control of SBH, it needs that the factor $N_{ICL}/\varepsilon_{ICL}$ is more than 10^{19} cm^{-3}/ε_0, and interface state density N_{SS} at ICL/semiconductor interface is less than $10^{12}cm^{-2}eV^{-1}$.

(3) Applying insulator ICLs or some kind of semiconductor ICLs with large band-discontinuities to the bulk semiconductor, the Richardson constant A^{**} reduced anomalously even if the thickness of the ICL was less than 10Å and deteriorated the forward current transport. Such a reduction could not be caused by the use of Si ICL for GaAs and InP Schottky barriers.

(4) Reverse-leakage-current property was investigated using the DIGS model. The low permittivity of ICL and low N_{SS} at ICL/semiconductor interface caused large leakage current. Such a current could be suppressed by using a material having large permittivity which is more than $10\varepsilon_0$.

(5) From these results, the requirements of ICL material are found to be moderate band gap and band line-up with the semiconductor, thin film, high doping concentration more than $10^{20}cm^{-3}$, high permittivity and low N_{SS}.

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Chapter 4
Optimization of Interface Control Layer for Control of III-V Compound Semiconductor Schottky Barrier Height

4.1 Introduction

The approach for control of Schottky barrier height (SBH) by inserting a thin interlayer at metal/semiconductor (M-S) interface has been studied experimentally using various interlayer materials. The effectiveness of this scheme is not clear although the several experimental results predict that the high Schottky barriers can be obtained for GaAs, InP and InGaAs,[1-7] since the general and unified discussion has not been made sufficiently. On the other hand, Schottky interfaces with some interlayers were discussed from view point of current transport, recently.[8] This study shows the extreme deterioration of current transport through the M-S interfaces with some kinds of interface layers, which implies that one must consider not only SBH but also the other properties, current transport, interface stability and reproducibility of Schottky interfaces when he tries to control SBH by this scheme.

In this chapter, the method of control of III-V compound semiconductor Schottky interfaces by various ICLs is discussed from experimental view point and optimization of ICL for SBH control is made in order to control SBH systematically and precisely. For this purpose, it is necessary to understand the property of M-S interfaces with ICLs in detail. Therefore, interface characterization was done on not only SBH, but also on the structures of M-S interfaces having ICLs by X-ray photoelectron spectroscopy (XPS) analysis, and on the current transport properties through the interface by current-voltage (*I-V*), capacitance-voltage (*C-V*)

measurements. For ICLs, thin and thick oxidized layers formed by various oxidation methods and ultrathin silicon interface control layer (Si ICL) are investigate. Intimate interface without intentional interlayer is also investigated.

4.2 Requirements for ICL from experimental view point

Generally, n-type GaAs SBH without ICL is as high as about 0.9eV. On the other hand, n-type InP SBH is only about 0.4eV. On the M-S system with a certain ICL, SBH of n-type semiconductor corresponds to the energy difference between the Fermi level in the metal and the conduction band minima of the semiconductor at the interface, on the assumption that the ICL is thin enough to allow tunneling of carriers. Assuming that Fermi level is firmly pinned at the metal/ICL interface but not pinned at the ICL/semiconductor interface, SBH becomes high or low by introducing negative or positive charge into the ICL, respectively, as discussed in previous chapter. Using the simple depletion approximation for carriers in the ICL, the change of SBH ($\Delta\phi_B$) is given by,

$$\Delta\phi_B = \frac{q N_{ICL} t_{ICL}^2}{2 \varepsilon_{ICL}} \qquad (4.1)$$

where N_{ICL} is the charge density in the ICL, ε_{ICL} and t_{ICL} are permittivity and thickness of the ICL, respectively. SBH can be controlled continuously and precisely by changing N_{ICL} or t_{ICL}, which is the advantage of this method. But the ICL should be thin enough not to deteriorate properties of direct Schottky contact. The ICL charge may be fixed ionic or defect space charge in oxide ICLs,[3] and ionized donor/acceptor charge in semiconductor ICLs.

Here, several materials are investigated as ICLs for GaAs- and InP-SBH control. The one is thin, about ten angstrom, oxidized layer formed on chemical etched surfaces. Intentional-oxidized layers by photochemical oxidization [3] and laser-

induced oxidization were also investigated for InP. Several authors reported that some kind of InP oxide enhances SBH of InP.[3-5] The advantage of the oxide ICL is in the simplicity of the formation process. As a semiconductor ICL, Si was chosen for both GaAs and InP M-S interfaces. Si based interface control techniques were found to be effective for control of various III-V compound semiconductor interface.[9-12]

4.3 Formation of metal/ICL/semiconductor structures

Figure 4-1 summarizes fabricated and investigated sample structures. For III-V compound semiconductors, GaAs and InP were investigated. The experimental was done in a ultra high vacuum (UHV) system having a MBE, photo-CVD, XPS, metal deposition and other chambers connected by UHV transfer chambers shown in **chapter 2**. Clean GaAs (100) surfaces were prepared by the conventional MBE technique. The carrier concentrations of the substrate were about $10^{16}cm^{-3}$. Undoped n-InP (100) substrate with the carrier concentration of about $5x10^{15}$ cm^{-3}, was used. Initial surface of InP was prepared by immersing HF solution. The oxidized layer on the surface was almost removed by this treatment. ICLs were formed on the semiconductors as follows.

(a) Thin oxide layer

Thin oxide layers of GaAs or InP were formed by chemical etching immersing the sample in conventional etchant of H_2SO_4:H_2O_2:H_2O=3:1:1, NH_4OH:H_2O_2:H_2O=8:1.4:296, or HF-based etching solution for several minutes.

(b) Laser-induced oxidized layer

The InP sample was set in the photo-CVD chamber which background pressure was about 10^{-9} Torr. Introducing O_2 gas into the chamber at the pressure of 9 Torr

and then ArF excimer laser (λ=193nm) was irradiated parallel to the sample surface at the substrate temperature of 250°C. The oxidation time was varied in order to change oxidized layer thickness.

(c) Photochemically oxidized layer [3)]

A photochemical oxide formation of InP was done by immersing the sample into HNO_3 solution (61%) kept at 50°C, under UV-lamp illumination for several seconds. The oxidation time was varied in order to change oxidized layer thickness.

(d) Si ICL

Ultrathin Si ICL was grown by MBE using Si K-cell. Substrate temperature was kept at 250°C during Si growth. Its growth rate was 20Å/hour. The Si ICL thickness was 10~40Å. The background pressure during the undoped Si ICL growth was kept in 10^{-9} Torr. The detailed procedure for doping will be described in the next chapter.

After formation of ICLs, Al (ϕ_m=4.3eV), Au (ϕ_m=5.1eV) and etc. was evaporated on the ICLs using K-cell or resistance heating method and formed metal/IC L/semiconductor structures. XPS analysis was used to characterize interface structures having ICLs and surface Fermi level position of semiconductors. Schottky diodes were fabricated by conventional photolithography and wet chemical etching. OMR-85 negative photoresist was span on the metal and circular dots were patterned. After development, the sample is immersed in the metal-etching solution, boiled H_3PO_4 for Al and cyanic solution for Au. *I-V*, *C-V* measurements and Richardson plot were used to characterize SBH and current transport properties of M-S interfaces having ICLs.

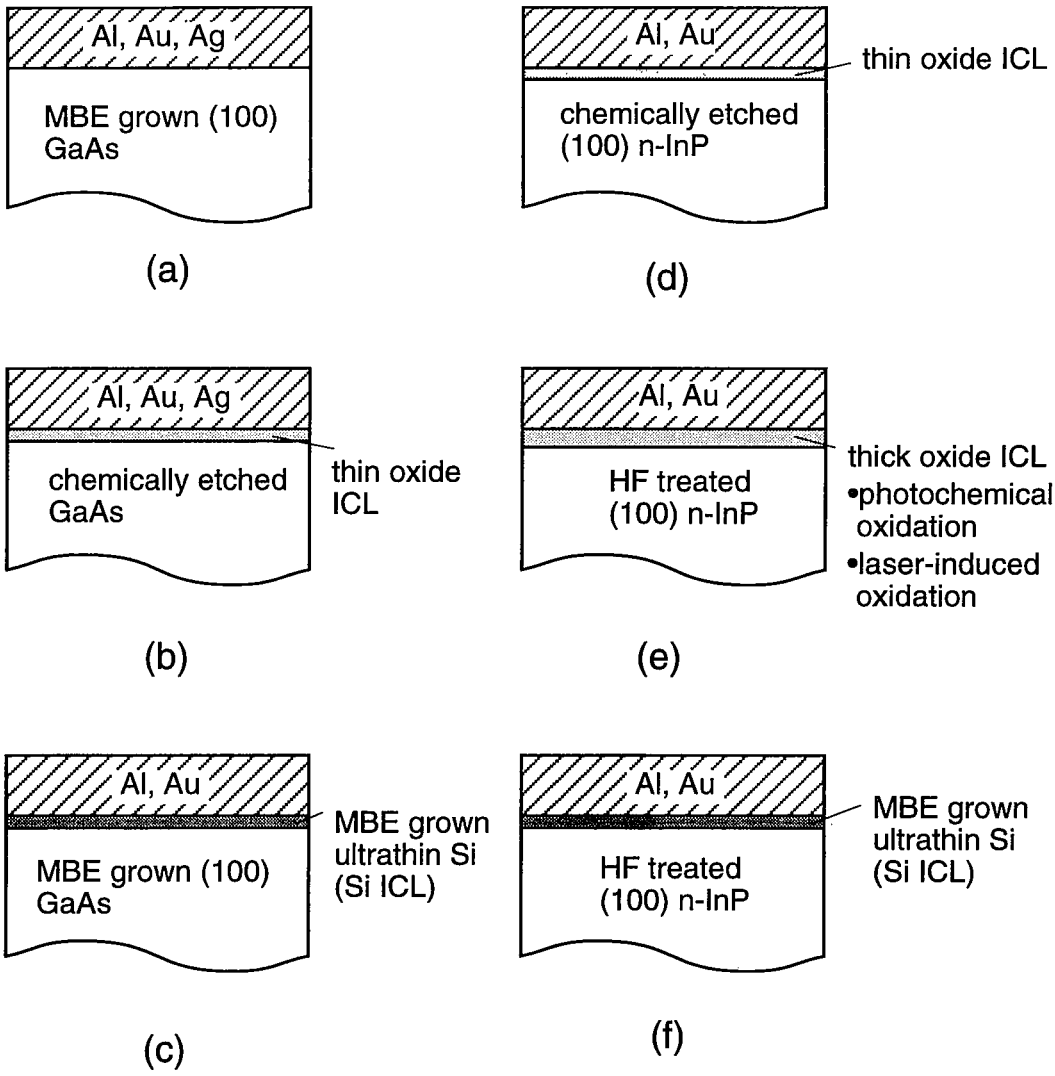


Fig.4-1. Fabricated samples. (a)~(c) GaAs M-S structrues and (e)~(f) InP M-S structrues with various ICLs.

4.4 Characterization of GaAs and InP Schottky interfaces having various ICLs

4.4.1 *Interface structures*

(1) GaAs

The XPS spectra of $Ga2p_{3/2}$ and Al2p core levels measured from Al/GaAs Schottky interfaces having various ICLs are summarized in **Fig.4-2**. In the case of Al/clean MBE GaAs interface, evidently an exchange reaction took place between Al and Ga, and unintentional AlAs interlayer was found to be formed at Al/MBE grown clean GaAs interface. It was very thin, estimated about 2 monolayers (ML) by XPS intensity ratio. With thin oxide ICL, the surface had the native oxide layer consisting of As_2O_3 and Ga_2O_3 before Al deposition, however, Ga and As oxides were deoxidized by Al and only Al_2O_3 was detected at the interface after Al deposition. The amounts of metallic Ga and As components were found to be very small. This suggested that Ga and As atoms produced by deoxidation by Al formed GaAs again. From angle-resolved XPS measurements, it was concluded that Al_2O_3 formed a continuous layer at the interface whose thickness was approximately 10Å. On the other hand, when Au was deposited, such an interface reaction was not observed. As_2O_3 and Ga_2O_3 layers were remained at the interface. With Si ICL of 10Å, a well-defined Si interfacial layer was observed together with metallic Ga and AlAs components. Most of the metallic Ga component comes from the top Al layer and not from the interface region. The intensity of AlAs in Al2p spectra was smaller than that of Al/MBE clean GaAs interface. This showed that interfacial reaction between Al and GaAs was suppressed by inserting Si ICL and well defined metal/ICL/ semiconductor structure was formed.

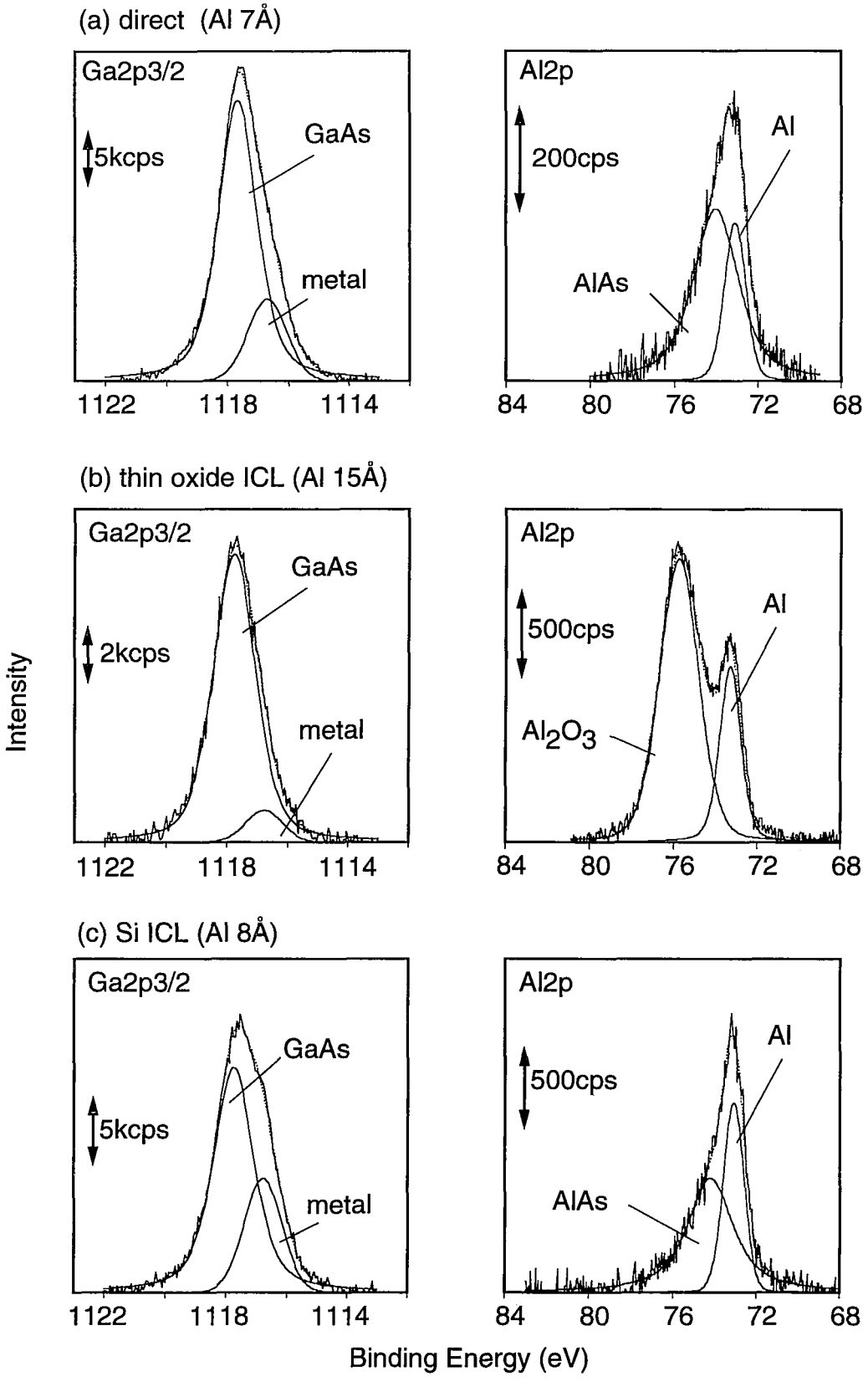


Fig.4-2. XPS spectrum of $Ga2p_{3/2}$ and Al2p from (a) Al/celan MBE GaAs, (b) Al/thin oxide ICL/GaAs and (c) Al/Si ICL10Å/GaAs structures.

(2) InP

The XPS spectra of P2p and Al2p core levels from Al/InP interfaces having thin oxide ICL by HF etching, thick oxide ICL by laser-induced oxidation, and Si ICL are summarized in **Fig.4-3**. InP oxide was almost removed and only thin oxide layer was left on the InP surface by HF treatment. However, the peak corresponded to Al_2O_3 was observed in Al2p spectra, which seemed to be caused by deoxidation of InP oxide by Al. Thick oxidized layers were formed by both laser-induced oxidation and photochemical oxidation. **Figure 4-4** shows In and P oxide layer thickness of various oxide ICL/InP structures measured by XPS. The oxidized layer thickness was about a few 10Å, depending on the oxidation time in both oxidation techniques. Analyzing chemical shifts of oxide peaks and In and P oxide layer thickness ratio, it was found that P rich and In rich oxide were presented by photochemical and laser-induced oxidation, respectively, as shown in **Fig.4-4**. The oxide layer was deoxidized by Al deposition and Al_2O_3 was formed, but InP oxide still existed at metal/InP interface and many kinds of oxide layers formed complex interfaces. On the other hand, the XPS spectrum from the interface with Si ICL was found to behave much more simply and regularly. Small amount of In and P oxides on the surface left after HF treatment was almost removed by deposition of Si ICL. The interface structure was virtually unaffected by Al deposition. Observed small peak which is seemed to be AlP,[13] however, the peak of Al_2O_3 was not observed.

Figure 4-5(a) shows XPS P2p spectrum of laser-oxide ICL before and after the formation of thin Al layer. The peak position of P oxide shifted largely, which shows the composition of the oxide was completely changed by Al deposition. At the same time, the deoxidation of In oxide was observed in the In3d spectrum. **Figure 4-5(b)** shows P2p spectrum from photochemical oxide ICL/InP interface before and after thin Au deposition. The change of interface structure was also observed by Au deposition. After Au deposition, the intensity of oxide peak decreased, on the other

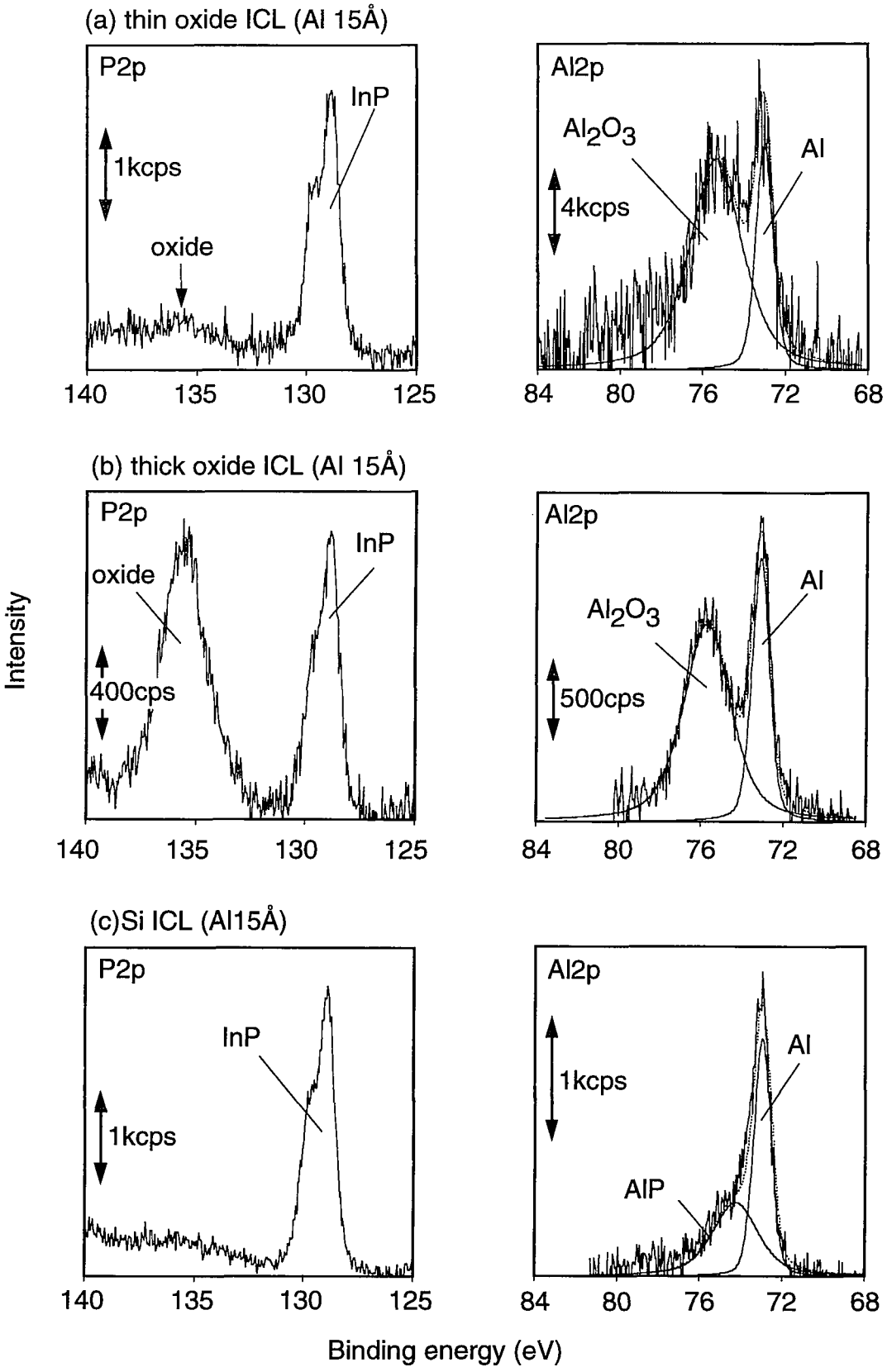


Fig.4-3. XPS spectrum of P2p and Al2p from (a) Al/InP structures with thin oxide ICL, (b) thick oxide ICL by laser-induced oxidation and (c) Si ICL 10Å.

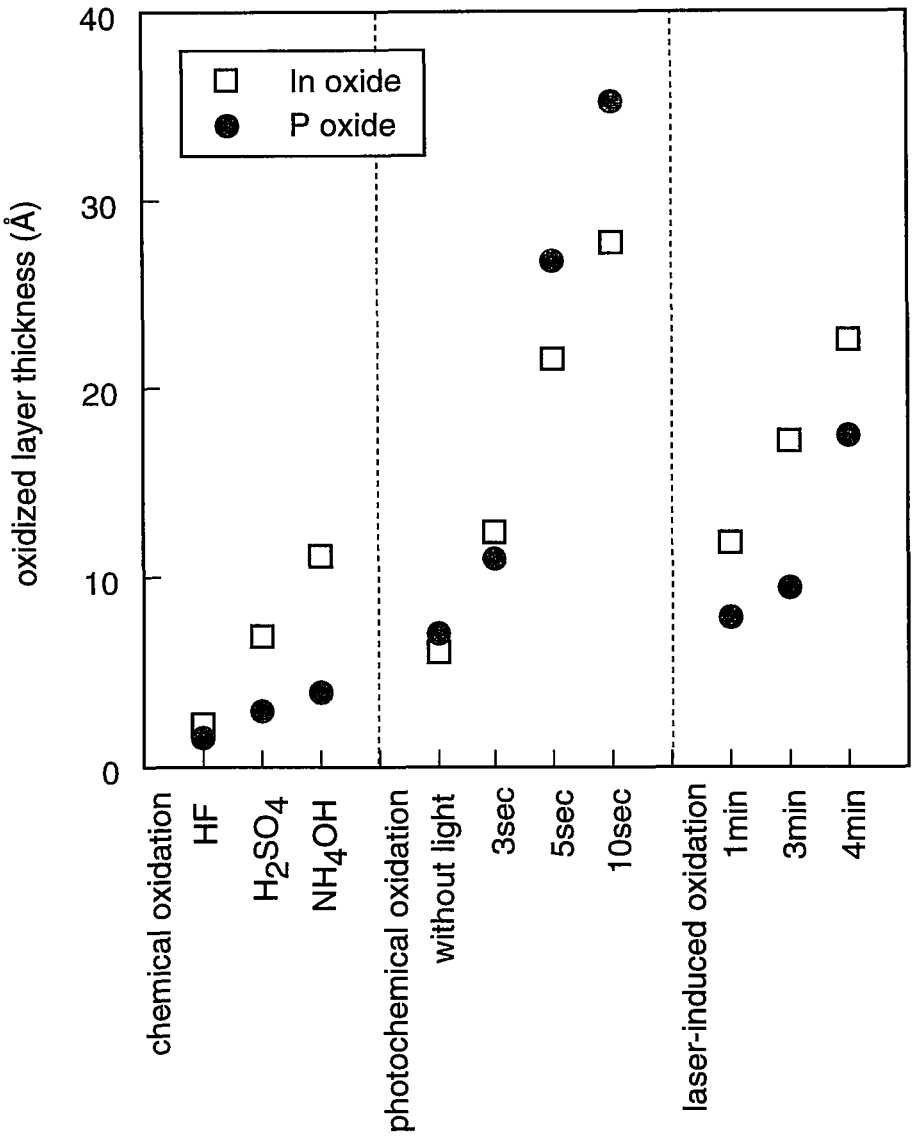
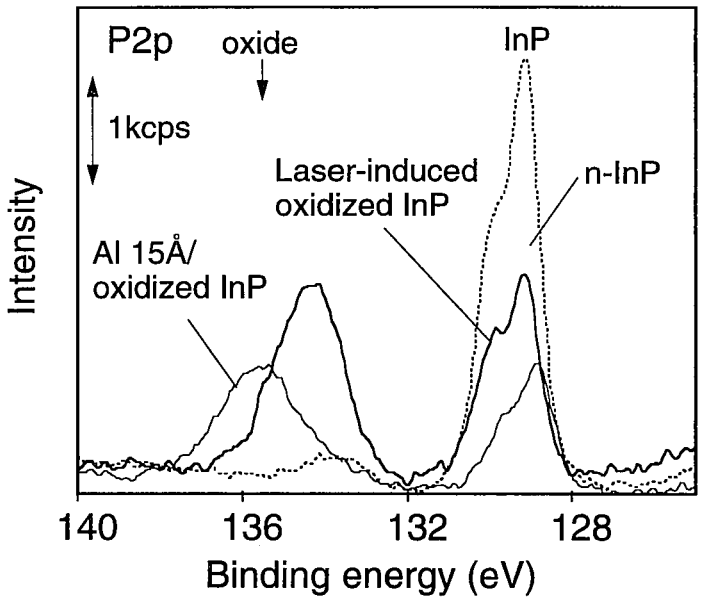
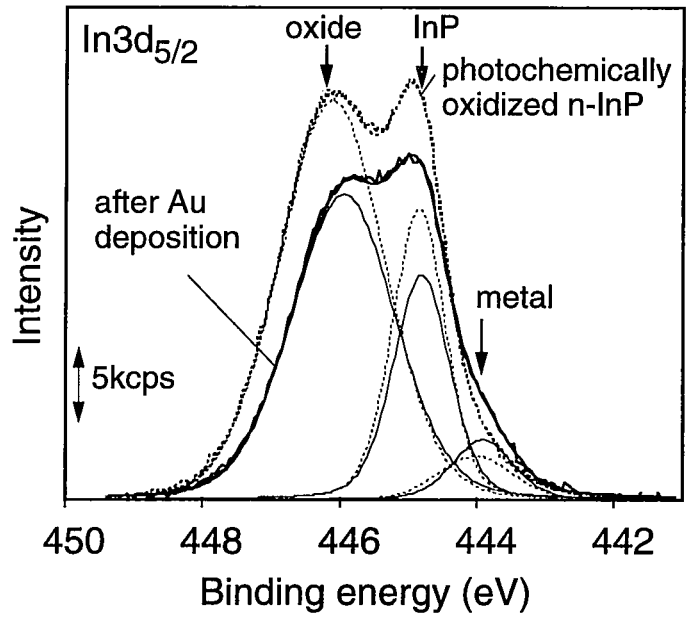


Fig.4-4. In and P oxide layer thickness of oxide ICL/InP structures formed various oxidation techniques.



(a)



(b)

Fig.4-5. (a) XPS spectrum of P2p from Al/InP interface with oxide ICL by laser-induced oxidation before and after Al deposition. (b) XPS spectrum of $In3d_{5/2}$ from Au/InP interface with oxide ICL by photochemical oxidation before and after Au deposition.

hand, the intensity of metal peak increased. The shift of the peak position of the oxide was also observed, showing the decomposition of the oxide by Au deposition. Such complex and uncontrollable interfacial chemical reactions among metal, oxide and semiconductor were always present with oxide ICLs, and this seems to be the reason for poor reproducibility of Schottky barriers with oxide ICLs. On the other hand, chemically regular interface structure can be obtain by use of Si ICL. The complex interface reaction between metal and compound semiconductors can be suppressed by replacing the semiconductor surface with Si.

4.4.2 *Comparison of SBH between M-S interfaces with various ICLs*

Figure 4-6 shows Fermi level position (E_F) of Al/GaAs and Au/GaAs interface on MBE clean surface, with thin oxide ICL by chemical etching, and with undoped 10Å Si ICL measured by *I-V* and *C-V* methods. E_{HO} corresponds to the charge neutrality level of the GaAs surface by DIGS model [14,15] which locates at 0.47eV form the valence band maxima E_V [16]. Weak metal-workfunction dependence of SBH was observed in the case of MBE clean surface and with thin oxide ICL. Metal-workfunction dependence of SBH in various metal/chemically etched GaAs structures is shown in **Fig.4-7**. From this plot, obtained interface index S was 0.2. The shift of SBH due to the fixed charge in the ICL was not also seen. E_F of Au/GaAs structures is almost fixed at E_{HO} since the Schottky limit and the Bardeen limit[17] are same. SBHs of Al/GaAs with and without thin oxide ICL were also same, even if the formed interface layers are different. On the other hand, with Si ICL, SBHs of Al/Si ICL/GaAs and Au/Si ICL/GaAs structures are nearly same and E_F positions locate near E_{HO}. Metal-workfunction dependence of SBH in various metal/Si ICL/GaAs structures including the result of Waldrop *et al.* [18] are shown in **Fig.4-8**. It is clearly found that interface E_F position hardly depends on the metal workfunction.Taking

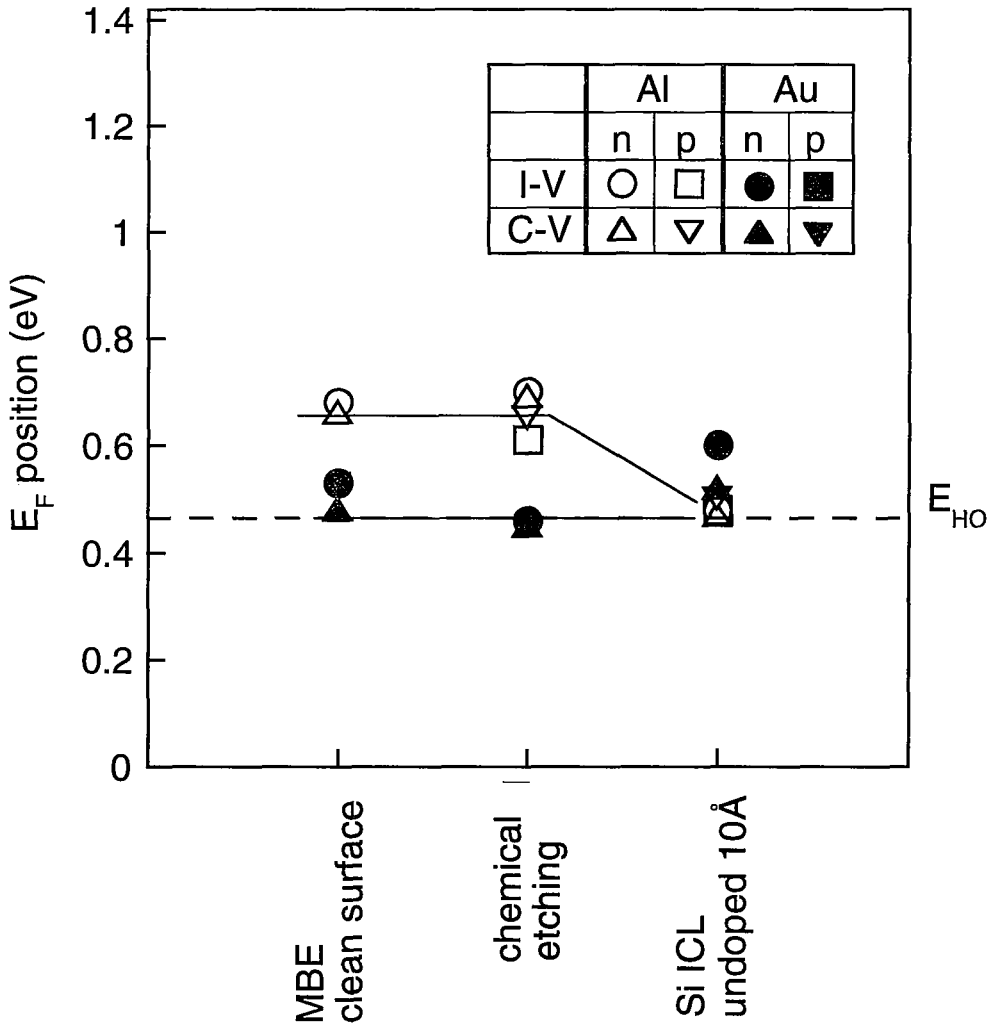


Fig.4-6. E_F positions of Al/GaAs and Au/GaAs interfaces with various ICLs.

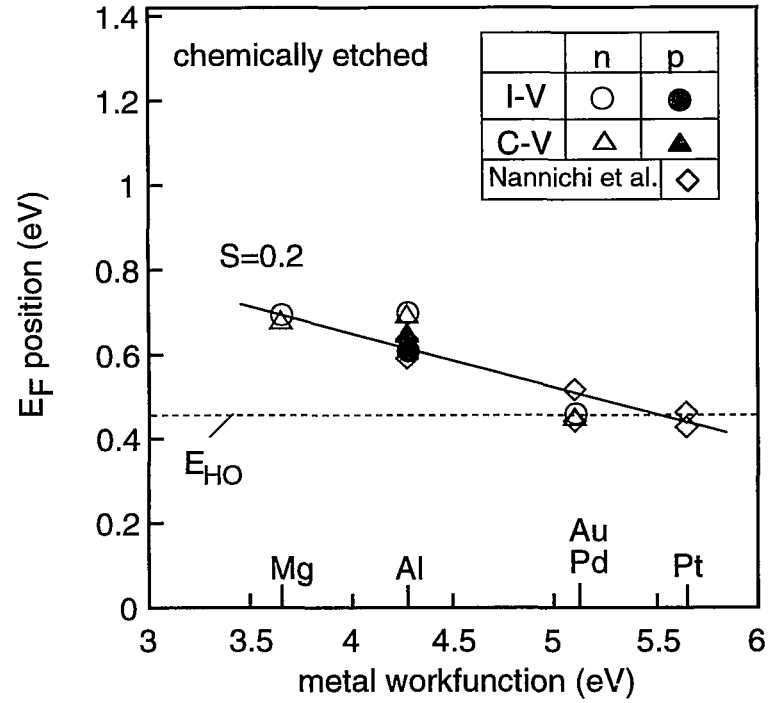


Fig.4-7. Metal-workfunction dependence of SBH on chemically etched GaAs surfaces.

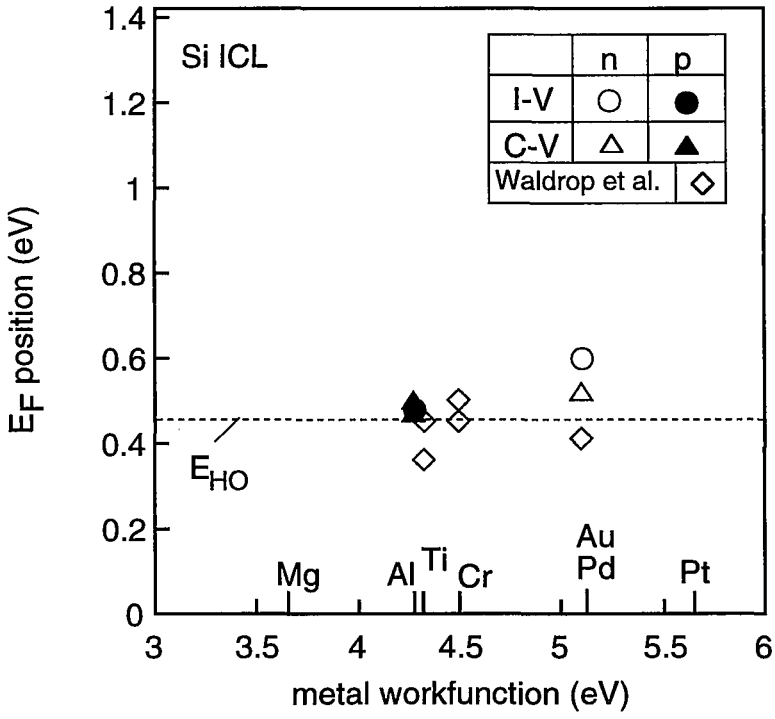


Fig.4-8. Metal-workfunction dependence of SBH on GaAs surfaces with undoped Si ICL.

account of low value of S of Si (S<0.1), [19,20] E_F is found to be fixed at metal/Si ICL interface. This suggests that SBH and band line-up of metal/Si ICL/GaAs system corresponds to that expected by the DIGS model [14].

Figure 4-9 summarizes SBHs of InP Schottky diodes with thin oxide ICL by chemical etching, thick oxide ICLs by photochemical oxidation and laser-induce oxidation, and Si ICL. The oxide ICL thicknesses were estimated from the XPS peak intensity ratio. E_{HO} of InP lies at 0.36eV from the conduction band minima E_C.[21] A maximum value of SBH of 0.7eV was obtained in Au/n-InP interface with the photochemical oxide ICL. This result corresponded to the report that P_2O_3 enhanced InP SBH[22,23], since photochemical oxidation produced P rich oxide which was found by XPS analysis as shown in **Fig.4-4**. But the value of SBH from C-V measurement was much smaller than the value from I-V measurement, and SBHs with oxide ICLs were poorly reproducible.

From view point of controllability of SBH, in the case of oxide ICLs, SBH is expected to be changed by changing the thickness or by using alternate oxide formation techniques providing different charge-density in the oxide ICL, as indicated by **eq.(4.1)**. However, experimental data showed that most of SBH values were nearly same, generally in the range of 0.4-0.5eV and the SBH hardly depends on the oxide ICL thickness or on the ICL formation techniques. The controllability of SBH by the oxide ICLs was found to be very poor. This may derive from the complex interfacial chemical reaction as seen in XPS observation.

The E_F position of the metal/InP interface with Si ICL also located near E_{HO}. This result was similar to the metal/Si/GaAs system, and indicated that SBH and band line-up of metal/Si/InP system also corresponded to the one predicted by the DIGS model. Several authors suggest that the change of SBH of Al/Si/GaAs system with respect to Al/GaAs system is due to the intrinsic dipoles created by insertion of IV-column atoms between III and V atoms, corresponding to Al and As, respectively,

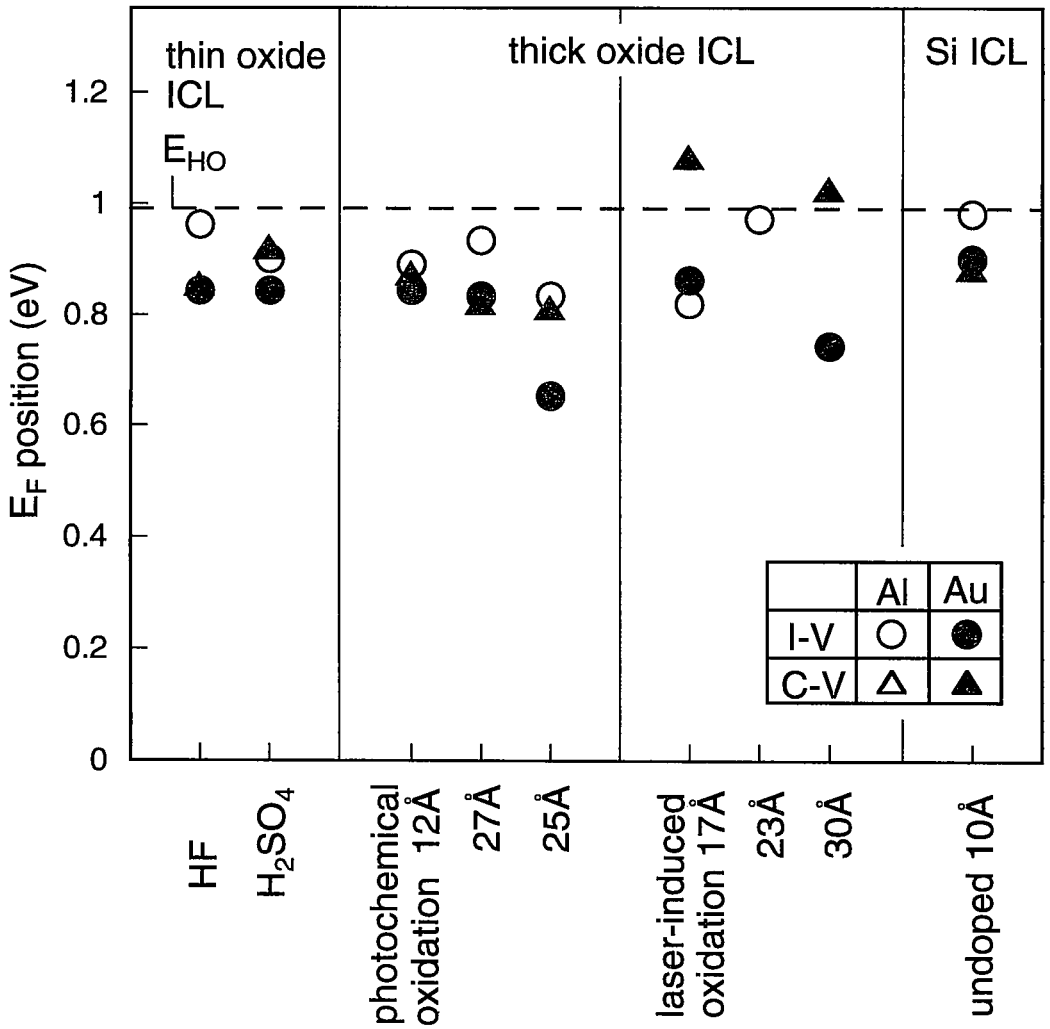


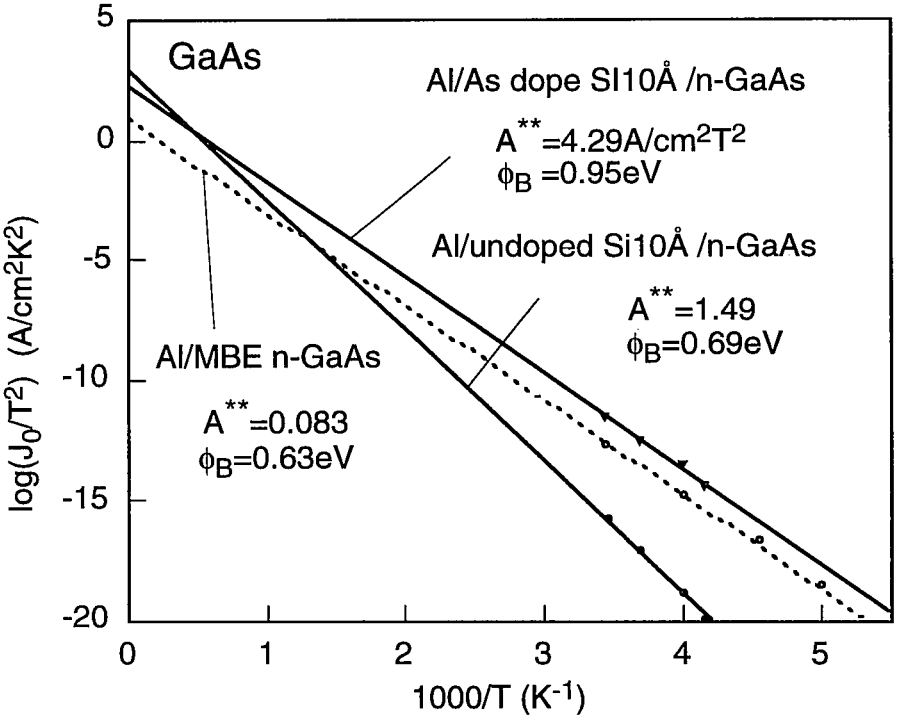
Fig.4-9. E_F positions of Al/n-InP and Au/n-InP interface with various ICLs.

which is similar to the case of III-V compound semiconductor heterointerface. [24,25] However, the change of SBH shown in Al/Si/GaAs was not be observed in Al/Si/InP system. And recent experiments by Akazawa *et al.* have indicated non-existence of such intrinsic dipole, and the experimental result has been explained in terms of delta doping and Fermi-level pinning.[12] The behavior of E_F position of metal/compound semiconductor interface with Si ICL are reasonably explained by the model of the M-S system having Si/compound semiconductor heterostructure, rather than the interface dipole model.

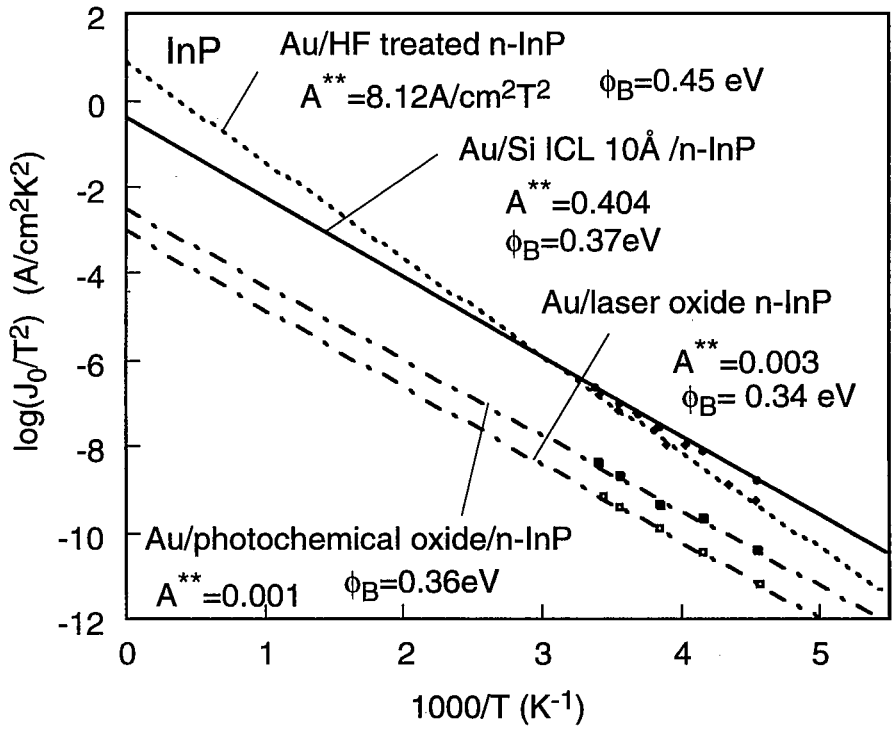
4.5 Current transport properties

4.5.1 *Forward current transport*

In order to investigate the effect of ICLs on the current transport, detailed analysis by the temperature dependence of *I-V* and *C-V* characteristics were performed, making attention to the Richardson constant A^{**}. Thermionic emission current is dominant over the current transport through the Schottky interface of III-V compound semiconductors. The effective Richardson constant A^{**} of GaAs and InP Schottky barriers with various ICLs was determined by Richardson plots. The example of the plot is shown in **Figs.4-10(a)** and **4-10(b)** for GaAs and InP Schottky diodes, respectively. The results of the measurement of A^{**} for GaAs and InP Schottky diodes with various ICLs are summarized in **Table 4-1** and **4-2**, respectively. Here, some published data are also included. [26,27] As seen in **Table 4-1**, the values of A^{**} of diodes with Si ICL was in the range 2~6A/cm^{2}K^2 being close to the theoretical value for GaAs of 8.2A/cm^{2}K^2. This clearly indicates that the Si ICL does not block the thermionic current transport. On the other hand, anomalous small values of A^{**} (~1/100 of theoretical value) for Al/GaAs diodes are consistent with the



(a)



(b)

Fig.4-10. Richardson plots of (a) GaAs and (b) InP Schottky diodes having various ICLs.

Table 4-1. Measured A** of GaAs Schottky diodes by Richardson plot.

metal	ICL	A** (A cm-2 K-2)	author
Al	MBE surface	0.088	present
Al	MBE surface	0.4	M.Missous et al (1992)
Al	thin oxide	0.2~0.9	A.K.Srivastava et al. (1981)
Al	Si ICL	1.5~6.3	present
Au	MBE surface	16	M.Missous et al (1992)
Au	thin oxide	0.8~2.8	A.K.Srivastava et al. (1981)

Table 4-2. Measured A** and SBH of InP Schottky diodes by Richardson plot, I-V and C-V methods.

metal	ICL	ϕ_{Bn} (eV)			A^{**} (A/cm^2K^2)	ϕ_{Bn} (eV)
		I-V	C-V	Richardson		I-V
Au	HF etching	0.45	0.47	0.45	8.12	0.45
Au	laser-induced oxide	0.54	0.37	0.34	0.003	0.33
Au	photochemical oxide	0.58	0.38	0.36	0.001	0.34
Au	Si ICL	0.45	0.38	0.37	0.40	0.37

literature. [22] With thin oxide ICL, the reduction of A^{**} is also observed. [23]

In the case of InP, as seen in **Table 4-2**, A^{**} with thin oxide ICL by HF etching was 8.12 A/cm^{2}K^2, which was very close to the ideal value 9.6 A/cm^{2}K^2. A^{**}s of Au/InP with thick oxide ICLs decreased anomalously, and A^{**}=0.003 A/cm^{2}K^2 and 0.001 A/cm^{2}K^2 were obtained. Such reduction of A^{**} was reported for a different oxide.[4] In addition, SBH from Richardson plot and *C-V* measurement was very lower than that from *I-V* measurement. On the other hand, A^{**} of Au/InP with Si ICL was 0.4 A/cm^{2}K^2 was somewhat smaller than the theoretical value, but anomalous decrease was not seen.

The reduction of A^{**} and current transport can be explained by the decrease of transition coefficient due to the existence of interfacial layer, since the carrier must tunnel through the interfacial layer. Using W.K.B. approximation and assuming the interfacial barrier square potential, tunnelling coefficient can be estimated as,[20]

$$T = exp(-a\sqrt{m^*_{ICL}\Delta E}\ t_{ICL}) \qquad (4.2)$$

where m^*_{ICL} is the effective mass of the majority carrier, ΔE is the band discontinuity of the ICL/semiconductor, and a is constant. It is found that tunnelling coefficient does not affect calculation of SBH from Richardson plot and *C-V* measurement. The barrier ΔE by the ICL does not give high Schottky barrier essentially, so the reduction of A^{**} indicates that the thermionic emission current is blocked at M-S interface.

Experimentally obtained A^{**} and calculated value using **eq.(4.2)** for some ICLs are compared in **Fig.4-11**. A^{**} calculated with **eq.(4-2)** for ΔE=1eV, t_{ICL}=15Å and $m^*_{ICL}=m_0$, is smaller than the ideal value in more than a few orders. Although XPS analysis shows that the oxide ICLs have thickness of a few 10Å or below, these

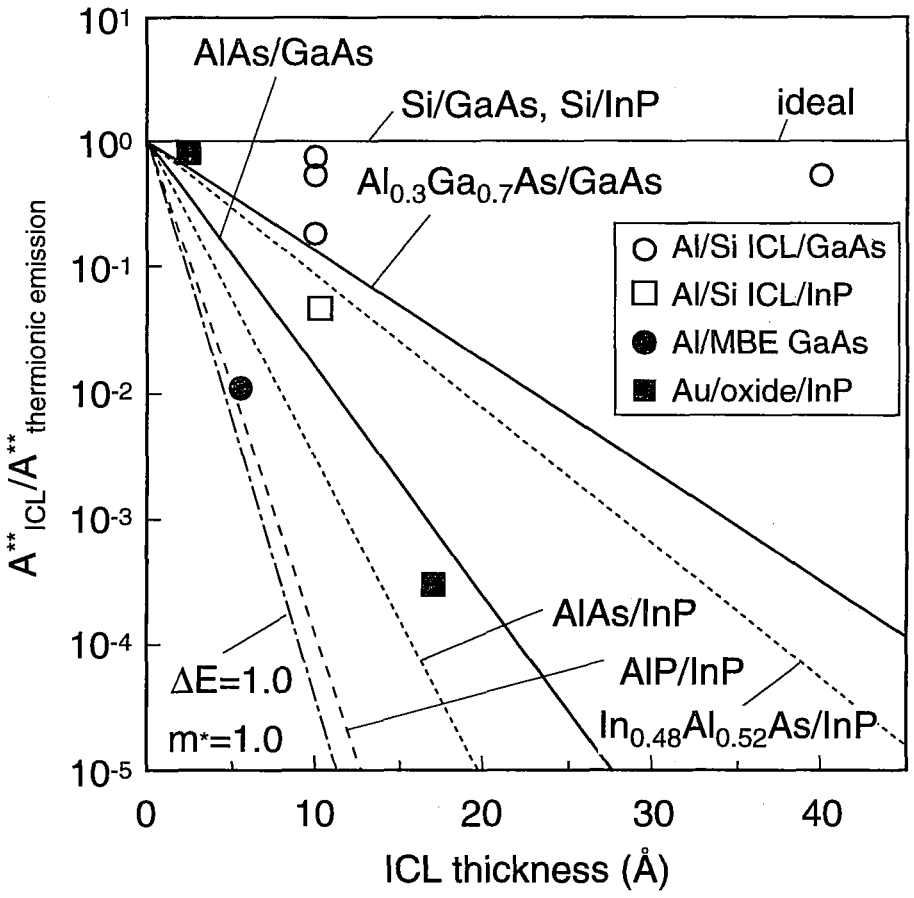


Fig.4-11. Comparison of Richardson constant A^{**} between theory and experiment.

layers come to be barrier for carrier transport, since the oxidized layers usually have large band gap.[28] As shown in **Table 4-2**, $\phi_{Bn}(I\text{-}V)$ evaluated using experimentally obtained A^{**} agrees well with ϕ_{Bn} from $C\text{-}V$ and Richardson plot. The reduction of experimental value of A^{**} and the difference of $\phi_{Bn}(I\text{-}V)$ from the other measurements can be explained qualitatively by the decrease of the tunnel coefficient due to an ICL having large potential. And this reduction indicates that oxide ICLs block the current transport through the M-S interface.

In the case of Al/clean MBE GaAs, a few monolayer AlAs interface layer was found to be formed by XPS measurement. The reduction of A^{**} of this interface may be due to AlAs layer since ΔE_C of AlAs/GaAs is 0.4~0.5eV and this is found to block the current transport sufficiently. Such a reduction of A^{**} and current transport blocking could be avoided by inserting Si ICL at Al/GaAs interface. This seems to be due to suppression of AlAs-interlayer formation by inserting Si ICL at the interface as indicated in XPS characterization and due to that Si ICL does not become electrical barrier for carrier transport as type-II band-lineup as indicated in **chapter 3**. A^{**} of Al/n-InP with Si ICL is decreased about 1/10 with respect to the theoretical value, which may be caused by thin AlP layer or thin oxide layer which could not be removed by HF treatment. But the reduction of A^{**} with Si ICL is smaller than that of oxide ICLs and the current transport of M-S interfaces with Si ICL is considered to be nearly ideal.

4.5.2 *Reverse I-V characteristics*

Figure 4-12(a) and **(b)** shows the experimental reverse I-V curves of InP Schottky diodes having oxide ICLs and the curves of GaAs and InP having Si ICL, together with the theoretical curves based on the simple thermionic emission model and combined with the DIGS model also. From the experimental data, the Schottky

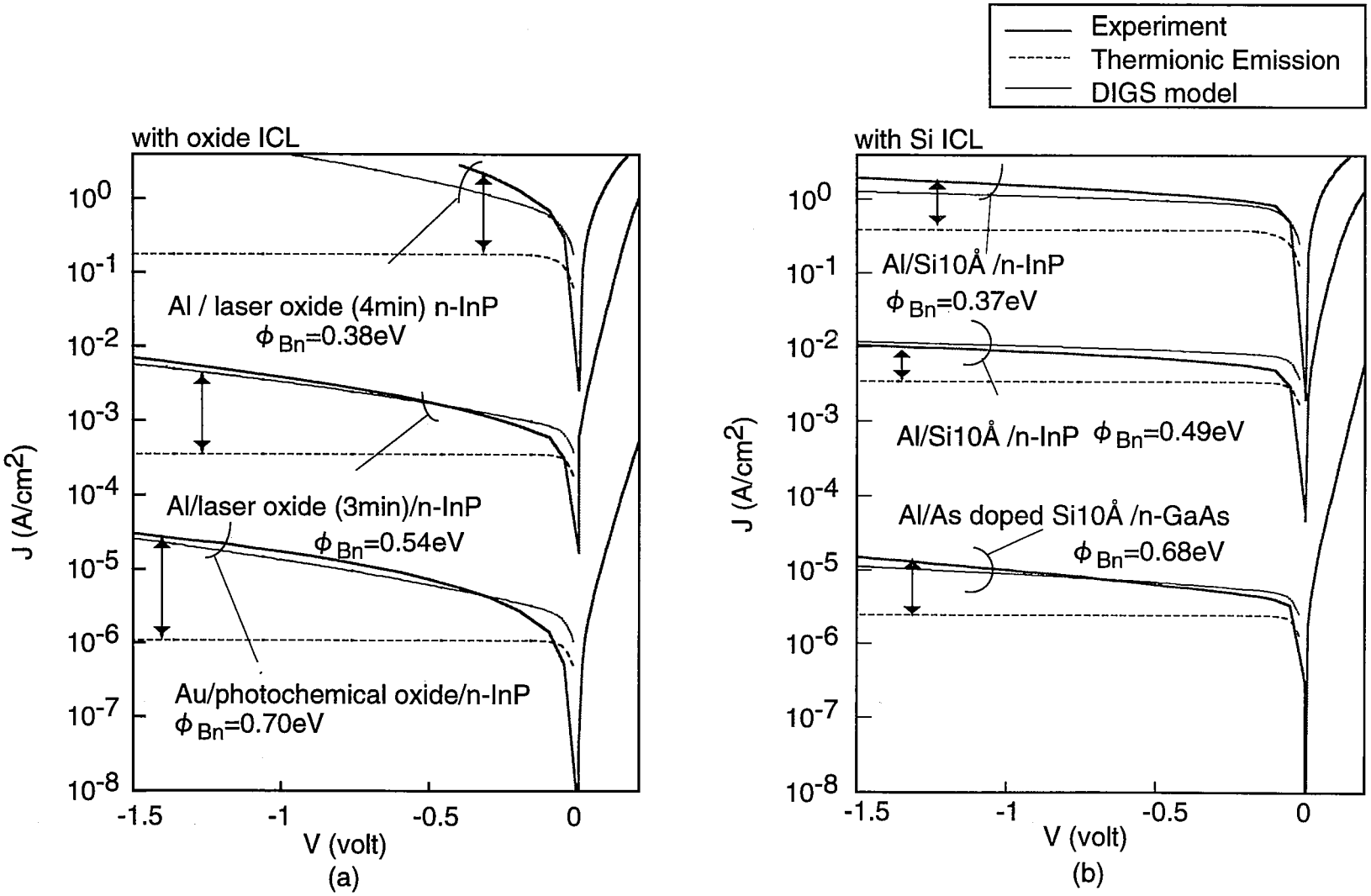


Fig.4-12. Comparison between experimental and theoretical reverse I-V curves of Schottky diodes having (a) oxide ICLs and (b) Si ICLs.

diodes with oxide ICLs give unexpectedly large reverse leakage current that is far from the thermionic emission current calculated using $\phi_B(I\text{-}V)$. On the other hand, increase of reverse leakage current is suppressed by using Si ICL for SBH control even if SBH is not so high. These experimental results implies that choice of the ICL affect not only the forward current transport but also the reverse *I-V* curves. The DIGS model including the existence of an interface layer shows the dependence of SBH under reverse bias *V* as follow,

$$\phi_B(V) = \phi_B(0) + \alpha E(V) + \text{Schottky effect},$$

$$\alpha = \beta \frac{q\, t_{ICL}}{\varepsilon_{ICL} + q^2\, t_{ICL} N_{SS}} \quad , \tag{4.3}$$

where $E(V)$ is the maximum field in the semiconductor and β is the constant depending on the permittivity and ionized impurity of the semiconductor. N_{SS} ,t_{ICL} and ε_{ICL} are the interface states density at the ICL/semiconductor interface, thickness and permittivity of the ICL, respectively. Giving suitable values to these parameters, the reverse *I-V* curve can be fitted by calculation, as shown in **Fig.4-12**. The parameters for calculation of reverse *I-V* curves are summarized in **Table 4-3**. The values of SBH from forward *I-V* characterization were used for this calculation, then the effect of reduction of A^{**} is absorbed in this parameter. The thickness of oxide ICLs are determined by XPS peak intensity ratio. The values of ε_{ICL} for oxide ICLs were determined by fitting, which are smaller than that of semiconductors. Such a small values of permittivity of InP oxides agree roughly with reported values.[29,30]

Theoretical curves by the DIGS model fit well with experimental curves. From the comparison between experimental and theoretical result, it turns out that the ICL permittivity and the interface state at ICL/semiconductor play important roles in the

reverse *I-V* characteristics. In the case of the oxide ICL, the bias dependence of SBH becomes very large because of small permittivity and low interface state density. It was reported that the InP oxide/InP MIS structure had an ideal interface and interface-state density N_{SS} at I-S interface is small (about $10^{12}cm^{-2}eV^{-1}$),[30] so the Fermi level was not pinned at the interface. And the small permittivity causes large voltage drop in the ICL. These admit the Fermi level at oxide ICL/semiconductor interface moving for applied bias. Thus the effective SBH is reduced with the reverse bias, which causes reverse leakage current. When permittivity is large ($>10\varepsilon_0$) as Si ICL, the dependence of SBH becomes much smaller because voltage drop is little even if the interface state density is low as shown in **Fig.4-12(b)**. The offset current from the thermionic emission current is mainly due to Schottky effect. The α of Si ICL is a few times smaller than that of oxide ICL. Si ICL is found to be essentially superior to the oxide ICLs in the point of view the reverse current property.

Table 4-3. Parameters for calculation of reverse I-V curves.

ICL	metal	ϕ_{Bn} (eV)	ε_{ICL}	t_{ICL}(Å)	$N_{SS}(cm^{-2}eV^{-1})$
laser oxide (3min)/InP	Al	0.54	1	15	$1x10^{12}$
laser oxide (4min)/InP	Al	0.38	1	20	$1x10^{12}$
photochemical oxide/InP	Au	0.70	1.5	30	$1x10^{12}$
Si ICL/InP	Al	0.37	12	10	$1x10^{12}$
Si ICL/InP	Al	0.49	12	10	$1x10^{12}$
As doped Si ICL/GaAs	Al	0.68	12	10	$1x10^{12}$

4.6 Conclusion

For control of metal/III-V compound semiconductor interfaces of GaAs and InP by an interface control layer (ICL), optimization of ICL including thin and thick oxide ICLs and Si ICL is studied and discussed from the points of view not only Schottky barrier height but also current transport through the interfaces. The main conclusions are listed below:

(1) With oxide ICL, unintentional interface reaction took place by formation of metal and it brought complex interface structures, which produces uncontrollablility and instability of Schottky barrier. On the other hand, M-S interface with Si ICL gives simple and coherent interface structure.

(2) Richardson plots show that the Si ICL does not block thermionic emission current transport. Richardson constants with oxide ICLs are anomalous reduced and the ICLs block the current transport even if the thickness of the ICL is about a few 10Å.

(3) Poor reverse leakage current properties are observed in Schottky diodes with thick oxide ICLs. This correlates strongly with interface states density at ICL/semiconductor interface and the permittivity of ICL. Such a current is suppressed by using Si ICL.

(4) From above reasons, Si ICL is found to be suitable for GaAs and InP SBH control by ICL method.

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Chapter 5
Control of III-V Compound Semiconductor Schottky Barriers Height by Silicon Interface Control Layers

5.1 Introduction

To control Schottky barrier height (SBH) of III-V compound semiconductors, a technique based on inserting interface control layer (ICL) is investigated basically in previous chapter, and it is found that silicon interface control layer (Si ICL) is most applicable for this purpose. The advantage of this method is in the possibility of continuous and precise control of SBH.

GaAs-SBH control technique by Si ICL layer is investigated both theoretically and experimentally by several authers.[1-5] The first indication of Fermi level shift due to formation of Si ICL on GaAs was done by Woldrop *et al.*[6] They formed thin doped and undoped Si and Ge layers, characterized the surface Fermi level position by XPS and found that large Fermi level shift happened on GaAs by formation As-doped Si layer. Then, they studied metal/GaAs Schottky diodes having Si interface layer with various doping and reported that SBH can be changed by changing Si interlayer condition.[1] Their study indicated the effectiveness of Si interlayer insertion for control of SBH of GaAs, however, more detailed research is needed for systematic control of SBH by this method.

In this chapter, III-V compound semiconductor-SBH-control technique based on Si ICL is investigated experimentally for systematic control of SBH by this technique. In first, the basic idea are shown. Secondly, experimental procedure is introduced. Next, the result of characterization Fermi level position of GaAs and InP surface with

various Si ICL, Si ICL thickness dependence, dopant-material dependence and doping-concentration dependence of SBH is shown and importance of interface between Si ICL and semiconductor for SBH control is indicated. And after spatial control method of SBH using Si ICL technique for application to quantum nanostructure is discussed briefly, a SBH control method using FIB-induced interface states is described.

5.2 Concept of SBH control by Si ICL

Fig. 5-1(a) illustrates the band diagrams of metal/Si ICL/n-GaAs based on unified DIGS model.[7,8] In this figure, the band gap narrowing effect due to strain is not considered. As described in chapter 3, SBH of metal/Si ICL/semiconductor systems correspond to charge neutrality level of surface states, hybrid orbital energy E_{HO}. Then, SBHs of n-GaAs, n-InP and n-InGaAs are expected to be 0.97eV, 0.36eV and 0.28eV, respectively. Conduction band discontinuities between these semiconductors and unstrained Si are -0.3eV, 0.31eV and 0.39eV, respectively. The more wide band gap material will give wider range of SBH control than Si ICL does. However, the value of ionized impurity concentration is also very important parameter for this method. The change of SBH is brought by the band bending of ICL due to ionized impurity in the ICL as schematically shown in **Fig.5-1(b)**. With simple consideration using depletion approximation, the change of SBH by inserting doped ICL including the effect on interface states at ICL/semiconductor interface is given by next equation assuming uniform distribution of interface state.

$$\phi_{Bn} = E_C - E_{HO} - \frac{q(N_D - N_A)t_{ICL}^2}{2\varepsilon_{ICL}\left[1 + (q^2/\varepsilon_{ICL})N_{SS0}t_{ICL}\right]} \qquad (5.1a)$$

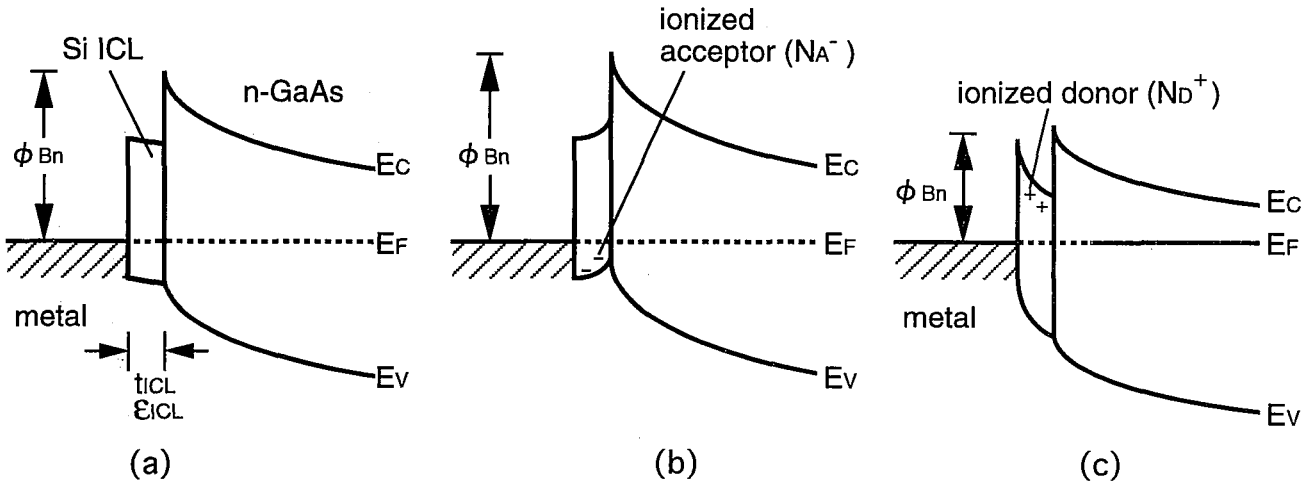

Fig.5-1. Band diagrams of M-S system (a) with undoped Si ICL, (b) with acceptor doped Si ICL and (c) with donor doped Si ICL.

$$\phi_{Bp} = E_{HO} - E_V + \frac{q(N_D - N_A)t_{ICL}^2}{2\varepsilon_{ICL}\left[1 + (q^2/\varepsilon_{ICL})N_{SS0}t_{ICL}\right]} \quad (5.1b)$$

where N_{SS0} is the interface state density, ε_{ICL} and t_{ICL} are permittivity and thickness of ICL, N_D and N_A are ionized donor and accepter density, respectively. It is found that large values of $|N_D\text{-}N_A|$ and t_{ICL} gives wide change of SBH. The possibility of high doping concentration into Si up to $10^{20}cm^{-3}$ for both acceptor and donor is very attractive for this method. **Equations (5-1)** also shows that interface states at ICL/semiconductor interface affects on the range of SBH control.

5.3 Experimental procedure

(100)-oriented clean GaAs surfaces were prepared by the conventional molecular beam epitaxy (MBE) technique. Either Si or Be was doped into GaAs for donor or acceptor, respectively, and the doping concentration was kept in the range of $10^{16}cm^{-3}$. The surface exhibited a clean As-stabilized (2x4) reconstruction pattern during growth at the substrate temperature of 580°C. (100) n-InP surfaces were prepared by HF treatment of undoped n-InP substrate with a carrier concentration of $5x10^{15}cm^{-3}$ removing surface oxide layer.

Then, MBE growth of the Si ICL was made from a Si Kundsen cell (K-cell) in the MBE chamber. The substrate temperature was kept at 250°C during the growth of the Si ICL. The growth rate of Si ICL was 20Å/h, and the thickness of the Si was varied from 10Å to 40Å. As for doping into the Si ICL, five different cases, i.e., undoped, As-doped, Ga-doped, Al-doped and B-doped cases, were investigated. For growth of undoped Si ICL, the background pressure was kept below $3x10^{-9}$ Torr. Various doping into Si ICL was done as follows.

Donor doping: As doping were done by irradiation of As flux from K-cells in the MBE chamber. It was tried to control doping concentration of As into Si ICL by changing As pressure (P_{As}) during Si growth. The As pressure was varied over the range of 0.7 to 8.5x10^{-8} Torr.

Acceptor doping: Gallium, aluminum and boron were tried for p-type doping. Ga and Al doping were done by irradiation of each molecular beam from K-cells in the MBE chamber during Si growth. For Ga doping, the sample was irradiated by Ga flux from the Ga K-cell during Si growth. The Ga flux density was maintained at 5.6x10^{10} atoms cm^{-2}s^{-1} with the corresponding cell temperature of 480°C. This flux density was chosen as doping concentration was about 1x10^{21}cm^{-3}. B doping was tried by two method, (1) undoped Si ICL formation after B_2O_3 or HBO_2 deposition on the semiconductor surface, and (2) B flux irradiation from K-cell in the MBE chamber during Si ICL formation. B_2O_3 is used for B source. In order to evaluate B concentration into Si by B_2O_3 source using K-cell in the MBE chamber, beam equivalent pressure (BEP) of B was measured. Arrhenius plot of the BEP of B and the cell temperature shows liner relationship. B doping concentration was estimated by comparing this experimentally obtained curve to the reported relationship between BEP and B doping concetraion.[9] The process described above was made by UHV chambers without exposing the samples to the air. After formation of the structures, some samples were tried to be annealed for activation and ionization of doped impurities.

After formation of metal/Si/ICL structures, Schottky diodes with circle electrodes were fabricated by conventional photolithography process and wet chemical etching.

RHEED observation was done for characterization Si ICL growth situation.

XPS analysis was used to characterize interface structures having ICLs and surface Fermi level position of semiconductors. *I-V*, *C-V* measurements and Richardson plot were used to characterize SBH.

5.4 Characterization of Si ICL before metal deposition

RHEED pattern changed when the Si ICL thickness t_{ICL} is over 10Å which is critical thickness of lattice mismatch $\Delta a/a$=4%. When t_{ICL} is over 10Å, the RHEED pattern becomes halo quickly. Starting from the As-stabilized (2x4) pattern of MBE GaAs, the RHEED pattern quickly changed and maintained either a (1x2) or (3x1) pattern during the growth of the ultrathin Si ICL up to the thickness of 10Å, depending on whether the growth was done without As-supply or under the As-stabilized condition, respectively. Above 10Å, the intensity of the Si ICL-induced RHEED pattern decreased rapidly, and the RHEED pattern became a halo. This indicates that the Si ICL maintains pseudomorphic lattice matching with an ordered surface reconstruction up to 10Å. A random three-dimensional growth mode with introduction of misfit dislocations and lattice relaxation seems to follow when Si ICL thickness is over 10Å.

The interface Fermi level position (E_F) of the Si ICL/GaAs and Si ICL/InP structures before metal deposition was determined by the XPS core level shifts. Examples of XPS spectrum from As-doped Si ICL/p-GaAs structure are shown in **Fig.5-2**. Due to the recently found surface photovoltaic effect in the XPS band bending measurement, which drastically affects the mount of core level shifts and can cause errors of several hundred meV, absolute measurements of the Fermi level position are rather difficult. Thus, the XPS measurement was undertaken in the present study only to determine the effect of doping into the Si ICL qualitatively.

Figure 5-3 shows the resultant Fermi level positions at the Si ICL-GaAs

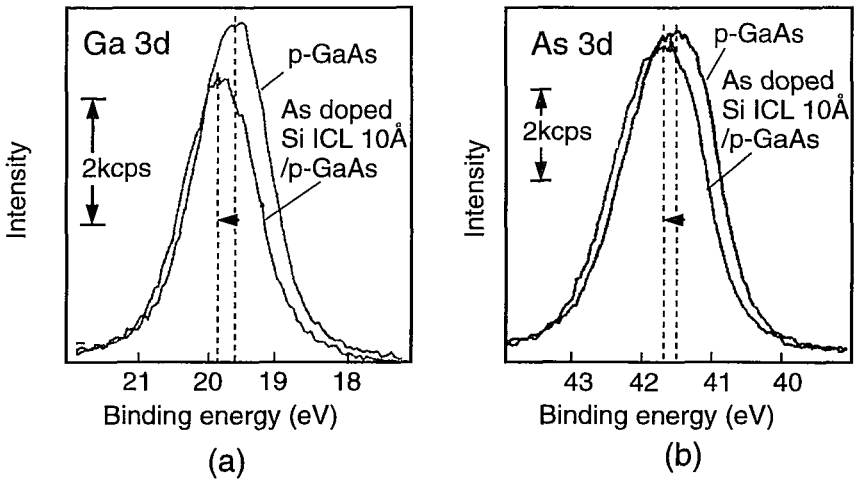

Fig.5-2. (a) As3d and (b) Ga3d XPS spectrum from p-GaAs with and without As doped 10Å Si ICL.

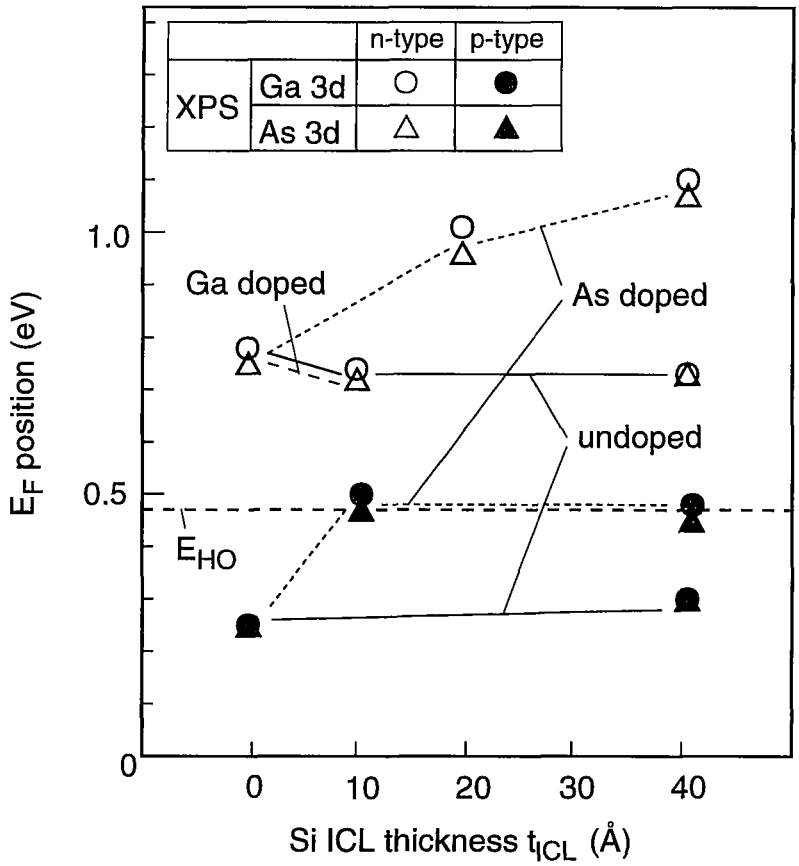

Fig.5-3. Surface Fermi level position of GaAs with Si ICLs measured by XPS (before metal deposition) .

interface as a function of the Si ICL thickness. By measurement of E_F position by XPS, a firm pinning of Fermi level exists on the top surface of the Si ICL even before metal deposition and observed shifts of core level energy by doping are due to doping-induced dipoles in the Si ICL. When the Si ICL was doped with As, the interface Fermi level position moved clearly towards the conduction band. However, when the SI ICL was doped with Ga to make it p-type, the interface Fermi level position remained the same as in the undoped case. Thus, As doping seems to be effective, but Ga doping is not.

E_F positions of InP surface with undoped or doped Si ICL are plotted in **Fig.5-4**. Systematic change of E_F by doping into the Si ICL was observed. With undoped Si ICL, the E_F position located at 0.2 higher than E_{HO}, which seemed to bedue to photovoltaic effect [10]. Thickness dependence of SBH was not seen in both undoped and As doped Si ICL. The E_F moved toward E_C or E_V of Si ICL by doping As or B into the Si ICL, respectively. The range of E_F movement was as wide as about 400meV.

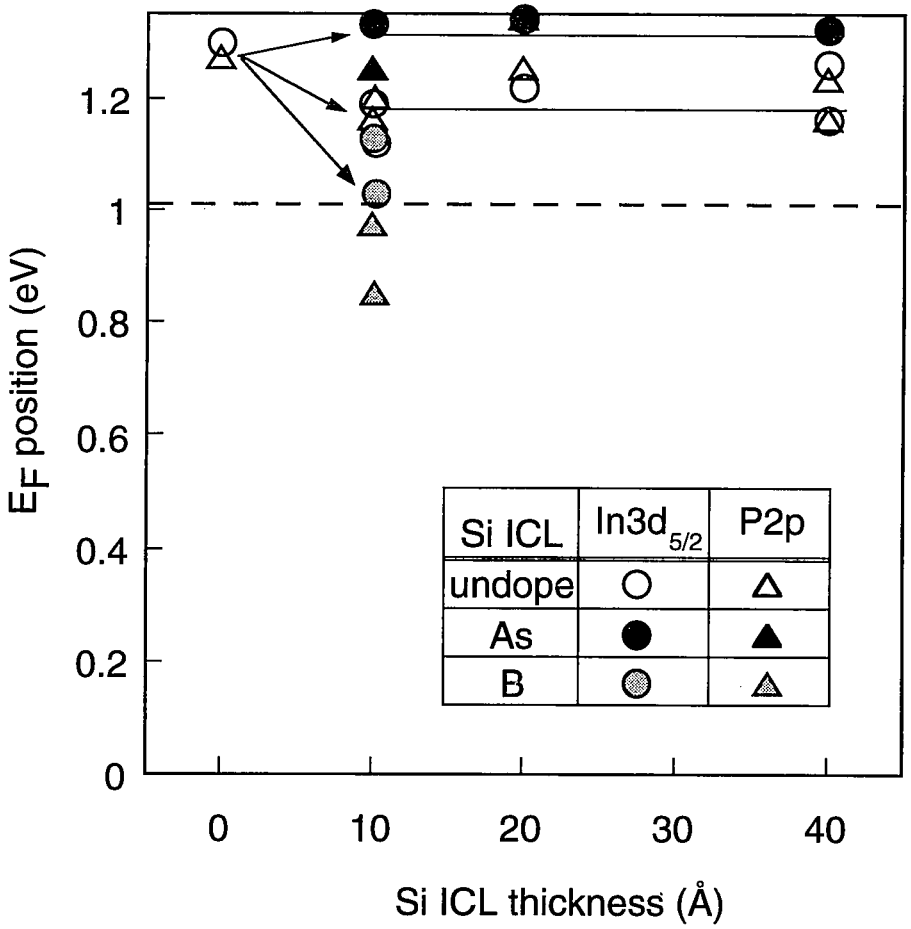

Fig.5-4. Surface Fermi level position of InP with Si ICLs measured by XPS (before metal deposition).

5.5 Si ICL thickness and doping dependence of SBH

5.5.1 *GaAs*

Figures 5-5 show the example of I-V and $1/C^2$-V characteristics of Al/Si ICL/n-GaAs Schottky diodes. The change of SBH by inserting undoped and As doped Si ICL is clearly seen. And these diodes show well behavior in electrical characteristics. **Table 5-1** summarizes measured SBH and ideal factor of fabricated samples.

Figure 5-6 shows the Si ICL thickness dependence of E_F position of Al/Si ICL/GaAs structure for various doping type in the ICL. In this figure, As doping concentration in Si ICL is fixed at $3x10^{20}cm^{-3}$. It was found that As-doping was effective but Ga or Al doping were not. Ineffectiveness of Ga or Al doping is most probably due to the fact that the maximum Ga doping into the substitutional sites of Si ICL is in the range of low $10^{19}cm^{-3}$.[11,12] SBHs value was very reproducible and the ideality factor n was close to unity, as long as the Si ICL was about or below the estimated critical thickness of about 10Å. [13]

SBH of Al/GaAs with Si ICL could be changed over 300meV by doping As into the Si ICL, however, thickness dependence of SBH could not be observed. E_F position with As doped Si ICL was limited at 0.8eV from E_V, even if the Si ICL thickness increases. Theoretical calculation shows that the range of E_F movement is limited by ΔE_C and ΔE_V of ICL/semiconductor system. On the other hand, band gap narrowing of Si layer is caused by lattice mismatching as far as the Si layer is psuedomorphic to bulk-lattice constant. This changes ΔE_C and ΔE_V. By theoreticalcalculation in **chapter 3**, ΔE_C, ΔE_V and E_g of strained Si on GaAs become 0.47eV, 0.13eV and 0.82eV, respectively, by strain with 4% lattice mismatch. However, observed E_F position was limited at 0.8eV which was 0.1eV lower than calculated E_C position of Si ICL. This is thought to be due to the limitation of ionized

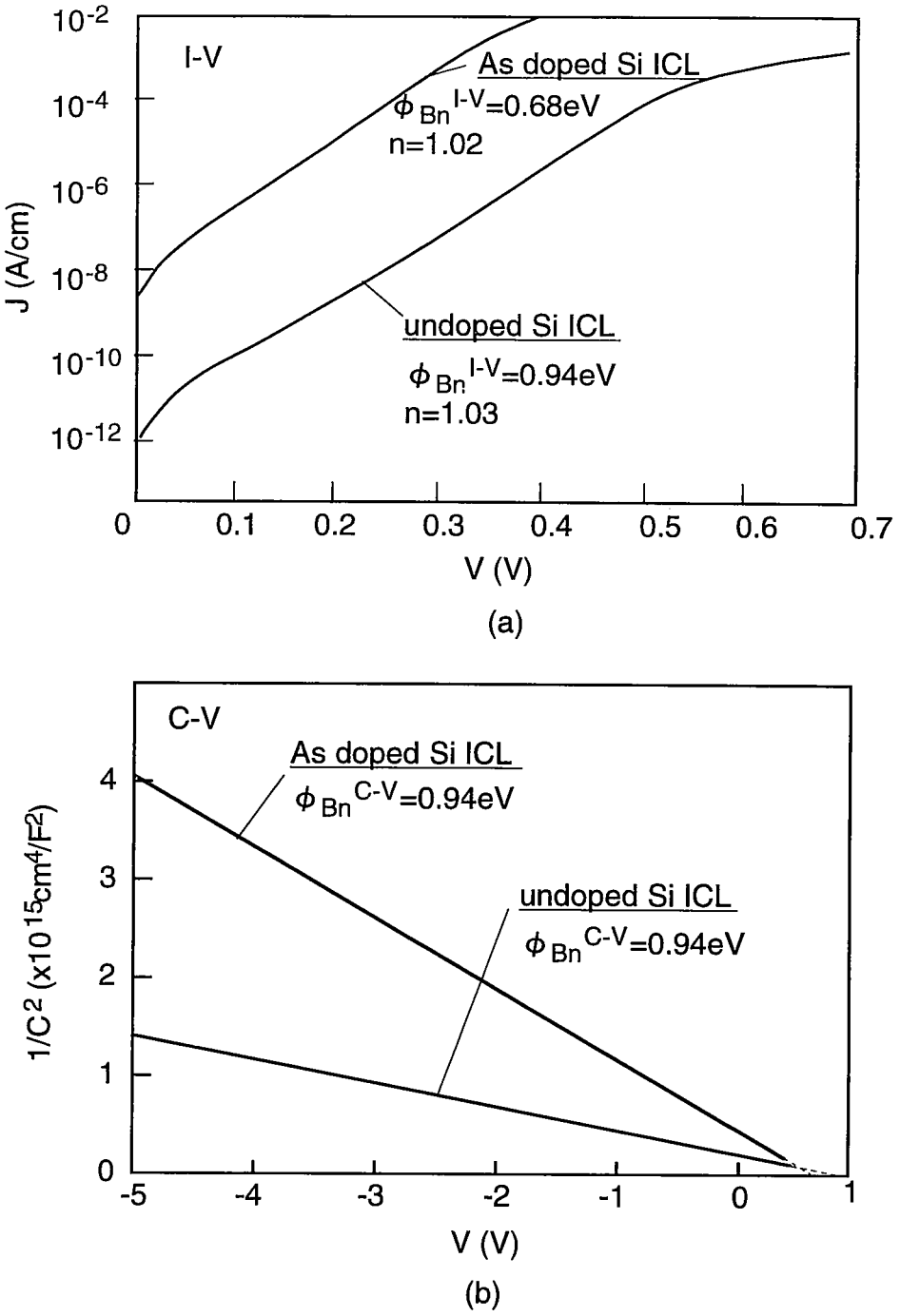

Fig.5-5. Example of (a) I-V and (b) $1/C^2$ characteristics of Al/GaAs Schottky diodes with and without Si ICL.

Table 5-1. Schottky barrier height and idality factor of Al/Si ICL/GaAs Schottky diodes.

No.	GaAs	Si ICL		ϕ_B^{C-V}	ϕ_B^{I-V}	n
		t_{ICL} (Å)	Dopant	(eV)	(eV)	
1	n	0	-	0.76	0.74	1.05
2	n	0	-	0.71	0.76	1.07
3	p	0	-	-	0.74	1.30
4	n	10	None	0.94	0.94	1.03
5	n	10	None	0.95	0.94	1.07
6	n	10	None	0.97	0.96	1.02
7	p	10	None	0.50	0.48	1.07
8	n	10	Ga [a]	0.97	0.94	1.07
9	n	10	As [b]	0.92	0.94	1.09
10	n	10	As [c]	0.85	0.84	1.07
11	n	10	As [d]	0.72	0.70	1.01
12	p	10	As [c]	0.65	0.63	1.06
13	p	10	As [c]	0.70	0.64	1.08
14	p	10	As [d]	0.79	0.73	1.15
15	p	10	As [e]	0.83	0.77	1.12
16	n	20	None	0.96	0.98	1.08
17	n	20	As [d]	0.68	0.73	1.12
18	n	40	None	0.91	0.89	1.03
19	p	40	None	-	0.54	1.27
20	n	40	As [d]	0.63	0.60	1.35
21	n	40	As [d]	0.69	0.64	1.08
22	p	40	As [d]	0.65	0.70	1.07

a) : Ga flux = 5.6×10^{-10} atoms $\cdot$ $cm^{-2} \cdot s^{-1}$

b) : $P_{As} = 7.0 \times 10^{-9}$ Torr

c) : $P_{As} = 1.5 \times 10^{-8}$ Torr

d) : $P_{As} = 3.0 \times 10^{-8}$ Torr

e) : $P_{As} = 8.5 \times 10^{-8}$ Torr

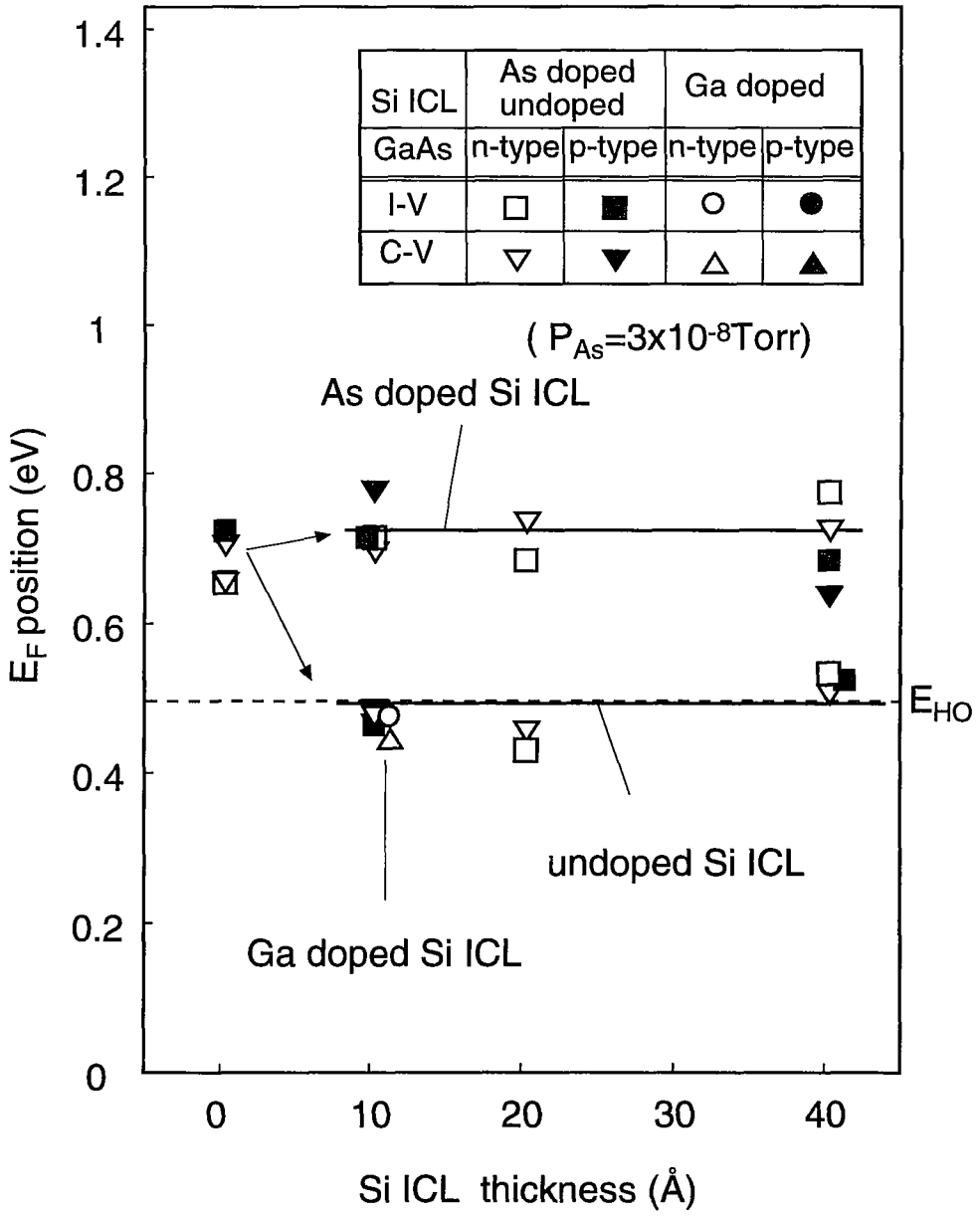

Fig.5-6. Fermi level position of Al/Si ICL/GaAs structures as a function of Si ICL thickness.

donor concentration. But when Si ICL is over 10Å, the limitation of E_F position can be explained by the interface state effect.[3)]

The calculated E_F positions of metal/n-Si ICL/GaAs by theory is compared with experimental date in **Fig.5-7**, where t_{ICL} is varied form 10Å to 40Å , Doping in Si ICL N_D(ICL) is fixed at $3x10^{20}cm^{-3}$, and N_{SS} is assumed to distribute uniformly. When t_{ICL} is 10Å, E_F position is about 0.8eV. This energy position is 0.2eV below of E_C of Si which locates 0.95eV from E_V of GaAs. This seems to be due to low concentration of ionized donor in the Si ICL, since theoretical simulation shows that ionized donor concentration of $3x10^{20}cm^{-3}$ is not enough to change the E_F position to E_C of Si. The experimental data of t_{ICL}≥20Å is very close to the result of the calculation at $N_{SS0}=5x10^{13}cm^{-2}eV^{-1}$. On the other hand, E_F positions at t_{ICL}=10Å is rather close to the calculated line at N_{SS0}=0. This difference seems to be brought by the thickness dependence of N_{SS0}.[3)] When t_{ICL} is below the critical thickness of 14Å, N_{SS0} is small and below $10^{12}cm^{-2}eV^{-1}$. As t_{ICL} increases and becomes over the critical thickness, the dislocation is critically introduced at the Si ICL/GaAs interface and N_{SS} drastically increases.[3)] When t_{ICL} is over 20Å, the change of E_F position saturates because the potential difference of metal/Si ICL interface and the interface-state charges at ICL/semiconductor interface are completely screened by ionized donor in the ICL and . From these results, it is found that N_{SS} needs to be below $10^{12}cm^{-2}eV^{-1}$ at least for the sufficient control of SBH by doping into the ICL. And the ICL thickness is required to be below the critical thickness so as to minimize the interface state at ICL/semiconductor interface for ideal control of SBH by ICL technique.

One can also find correlation between thickness of Si ICL and ideal factor in **Table 5-1**. When Si ICL thickness is under critical thickness of 10Å, the ideality factor n is close to unity and the diodes well behave, however, when the ICL thickness is over 10Å, n-value increases and fluctuates. This indicates that the

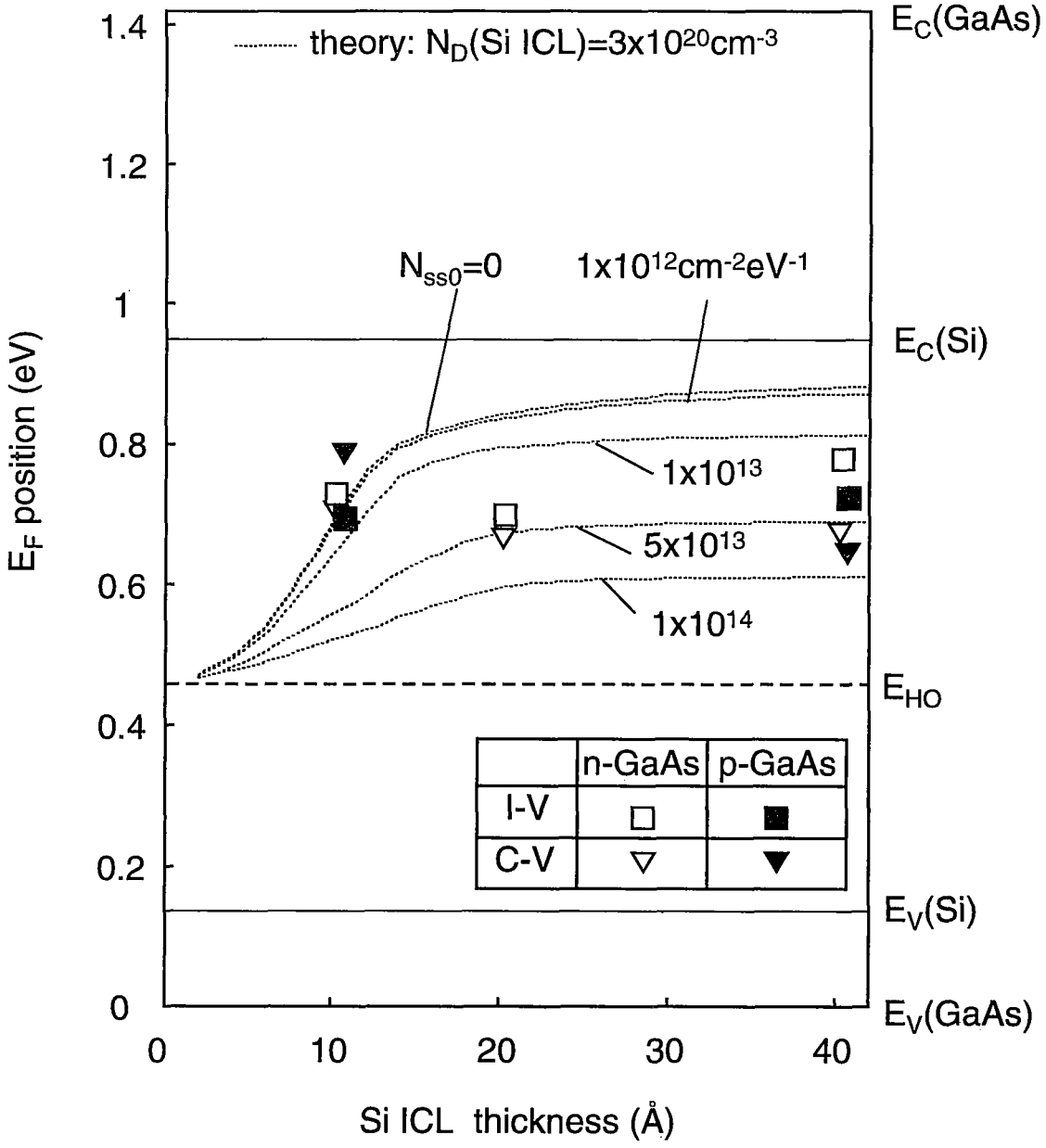

Fig.5-7. Comparison between experimental data in Fig.5-6 and calculated E_F positions for various interface state density (N_{SS}) at Si ICL GaAs interface (see chapter 3).

interface states at Si ICL/semiconductor interface affect not only on SBH control but also on electrical properties of Schottky diodes. Therefore, Si ICL must be psedomorphic to III-V compound semiconductors in order to control SBH well and to retain good electrical characteristics.

5.5.2 *InP*

Table 5-2 summarizes characterized SBHs of fabricated Al/Si ICL/n-InP Schottky diodes. SBHs of Al/n-InP with Si ICL could be reproduciblly changed over the range of 0-0.55eV by doping into the Si ICL. With As doped n-type Si ICL, ohmic like characteristics was obtained, showing that SBH became very low by doping into Si ICL. These well corresponds to the result of E_F-position evaluation by XPS in **Fig.5-4**. **Figure 5-8** shows the forward *I-V* characteristics of Al/n-InP Schottky diodes with undoped 10Å Si ICL and B doped 10Å Si ICL before and after annealing. In the case of B doping by B_2O_3, SBH came to 0.46eV. It was found that B doping was effective. From the change of SBH and the theoretical calculation of SBH in **chapter 3**, ionized acceptor concentration was estimated as high as $10^{20}cm^{-3}$. This high value consists to the reported maximum value of B doping by B_2O_3.[9] And after annealing at 300°C for 10min in H_2, SBH turned to be 0.55eV. This is the highest value for Al/n-InP studied in this work. The change of SBH by annealing seems to be due to the enhancement of the diffusion of B from B_2O_3 into Si ICL. On the other hand, Al and Ga doping was not found to be effective, which was same to the case of Al/Si ICL/GaAs. Obtained results show that SBH can be well and systematically controlled by As or B doped Si ICL for InP. Under strain by lattice mismatching, ΔE_C and ΔE_V and E_g of Si on InP are 0.03eV, 0.76eV and 0.56eV, respectively. Experimentally realized E_F position moves from E_C to E_V of Si ICL, such a behavior cannot be observed in Al/Si ICL/GaAs system. This seems to be due to the

Table 5-2. Schottky barrier height of Al/Si ICL/n-InP Schottky diodes.

before annealing

ICL thickness / doping	10Å	20Å	30Å	40Å
As	ohmic	ohmic		ohmic
undoped	0.37eV n=1.92	0.35eV n=2.00	ohmic	ohmic
Ga	ohmic			0.43eV n=2.35
Al		ohmic		
B_2O_3	0.46eV n=1.17	0.42eV n=1.29	0.41eV n=1.35	

after annealing

ICL thickness / doping	10Å	20Å	30Å	40Å
As				
undoped				
Ga	0.50eV n=1.11			
Al		ohmic		
B_2O_3	0.55eV n=1.13	0.44eV n=1.47	ohmic	

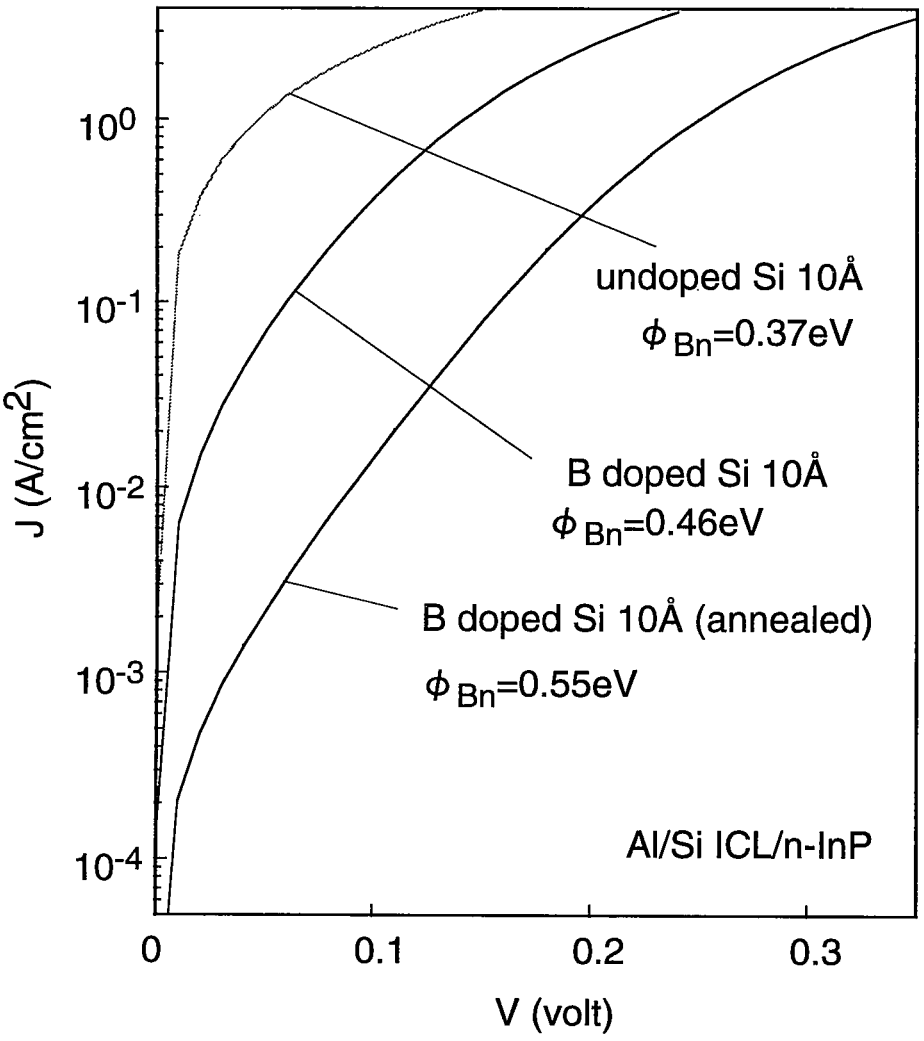

Fig.5-8. Forward I-V curves of Al/undoped Si ICL/n-InP and Al/B doped Si ICL/n-InP Schottky diodes.

low interface states density of Si ICL/InP interface.

5.6 Si ICL-doping concentration dependence of SBH

SBH control by doping into the Si ICL can be achieved when Si ICL is within critical thickness because of sufficiently low interface state density at Si ICL/ semiconductor interface. **Figure 5-9** shows the As doping concentration dependence of the SBH of Al/Si ICL/GaAs. Si ICL thickness was fixed at 10Å, which was below the critical thickness of Si on GaAs. Doping concentration was changed by controlling As pressure (P_{As}). By doping As into Si ICL to different doping levels, SBH could be precisely controlled over about 300meV for both n- and p-type samples. This behavior strongly suggests that precise and continuous control of the SBH of metal/Si ICL/semiconductor can be achieved by varying the doping type and the doping concentration into the Si ICL. The change of SBH saturated when P_{As} was over $4x10^{-8}$ Torr, which corresponded to the saturation of ionized donor density, estimated about $3x10^{20}cm^{-3}$ from the theoretical band calculation.

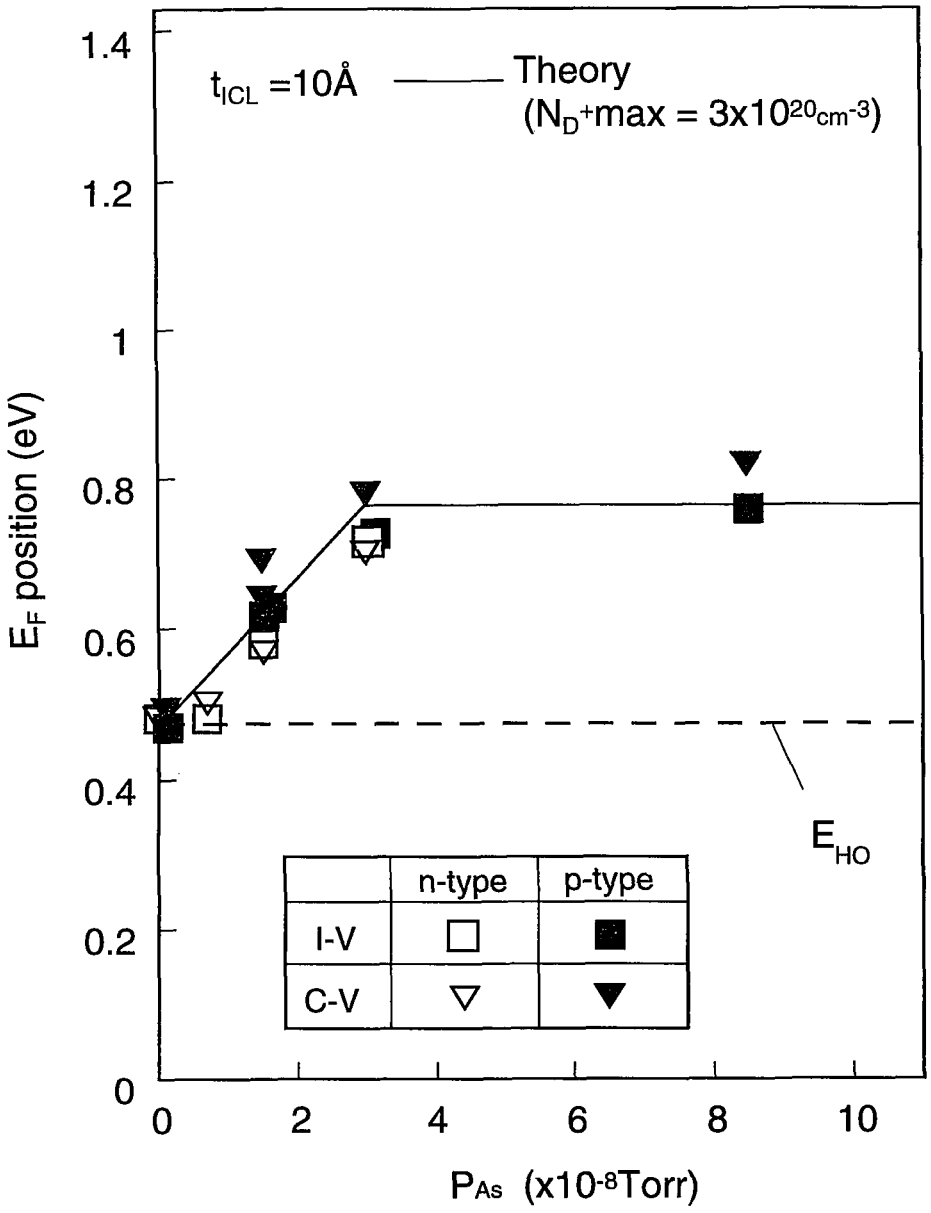

Fig.5-9. As soping conentration dependence of Fermi level position of Al/As doped Si ICL10Å/GaAs Schottky diodes.

5.7 Control by FIB-induced interface states

5.7.1 *Spatial-SBH control method in nanometer scale*

To apply controlled Schottky interfaces to quantum nanosturctures, it is necessary to control SBH in nanometer scale. For this purpose, SBH control methods assisted by electron beam (EB) or focused ion beam (FIB) seem to be effective. Possible methods to spatially control SBH utilizing EB/FIB technique are shown in **Fig.5-10**, (A) partial insertion of doped Si ICL at M-S interface or (B) inserting doped Si ICL at M/S interface and selectively inducing interface states at ICL/semiconductor interface and pinning the Fermi level locally.

Method (A) is realized as follow. After formation of metal/high doped Si ICL/ semiconductor structure, selectively remove metal and Si ICL by using EB lithography and etching and then form the second metal layer on whole structure.

Method (B) is realized by the procedure as shown in **Figs.5-11(a)~5-11(c)**, (a) formation of doped Si ICL on semiconductor, (b) introduce damage Si ICL/ semiconductor structure by partially irradiation of FIB and induce interface states the Si ICL/semiconductor interface due to disorder and pinned the Fermi level locally, (c) formation metal layer over the structure. In this section, basic investigation of method (B) is done. The study is made by using basic Schottky diode structure to obtain basic idea and to know possibility of this method.

The relationship between SBH and interface states density N_{SS} at Si ICL/GaAs interface is simply given by **eqs.(5.1)**. **Figure 5-11(d)** shows the relationship between SBH of GaAs and N_{SS} calculated for various doped Si ICLs using **eq.(5.1)**. SBH goes to E_{HO}-E_C=0.97eV with increase of N_{SS} over $1x10^{13}cm^{-2}eV^{-1}$, even if the donor concentration in Si is over $10^{20}cm^{-3}$, which seems to be sufficient quantity for control of SBH. On the other hand, it is better to use thick Si ICL for wide change of SBH

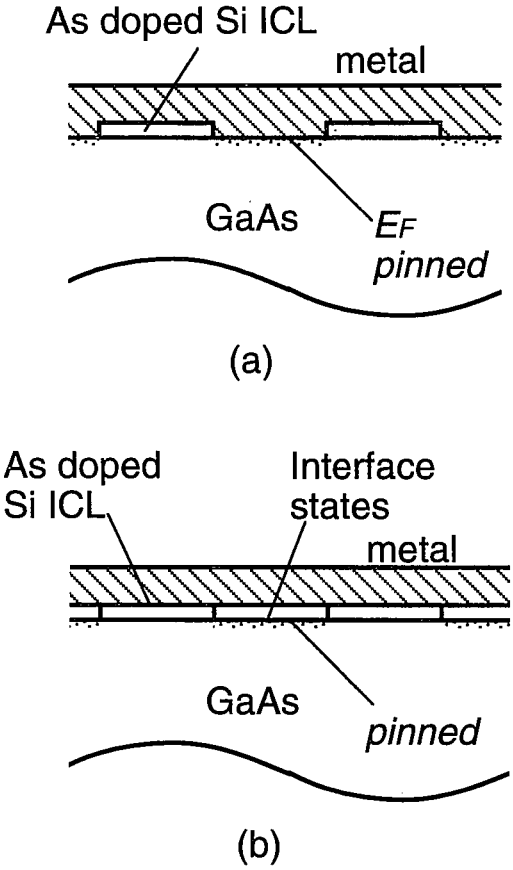

Fig.5-10. Possible methods for spatial control of Schottky barrier height utilizing Si ICL SBH control technique.

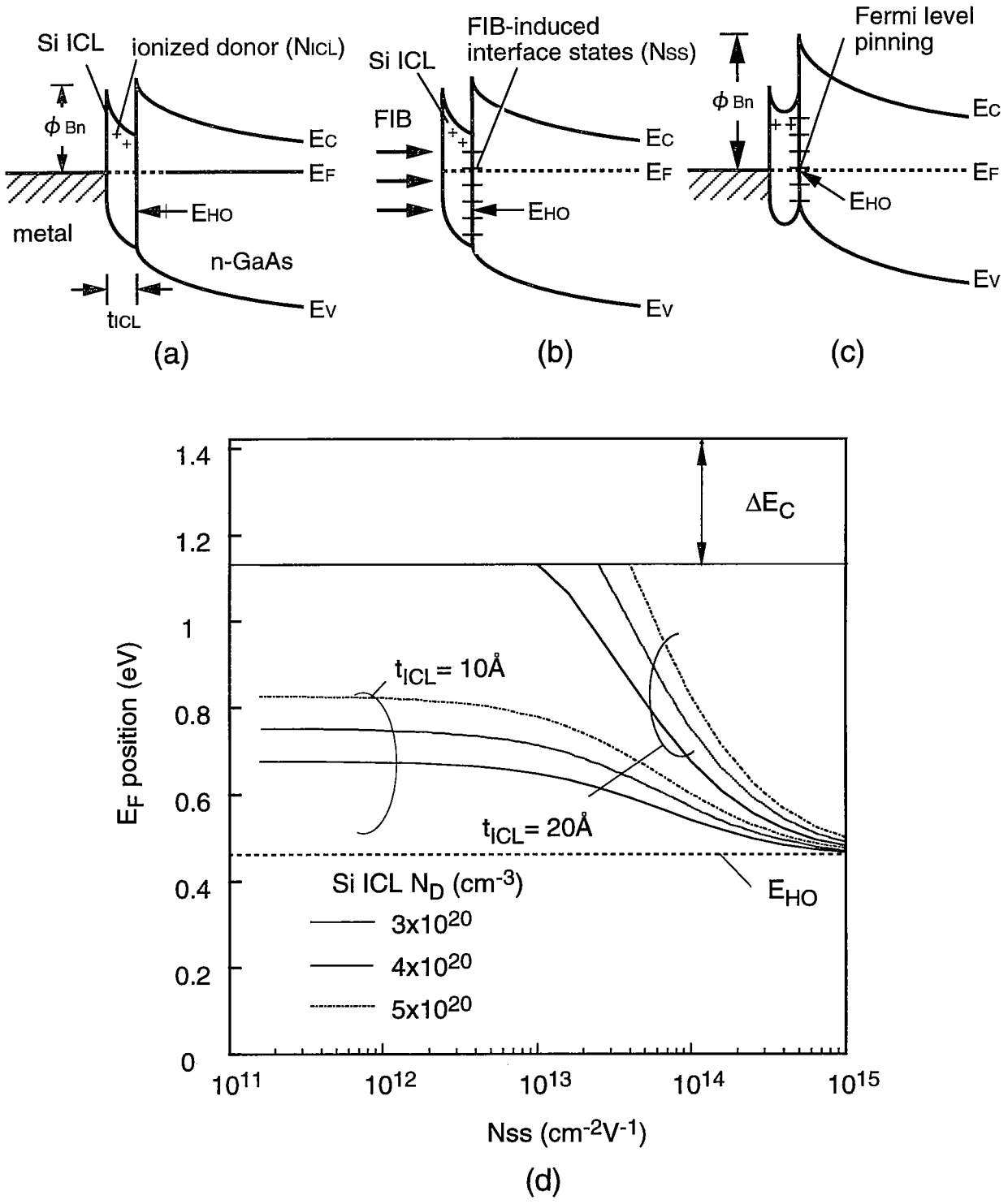

Fig.5-11. (a)~(c) Schottky barrier height control method by FIB-induced interface state and (d) calculated E_F position as a function of interface state density N_{SS}.

when the donor concentration in Si ICL is same. In order to obtain 300meV change of SBH by this method, Si ICL thickness should be over 20Å. However, over the critical thickness, unintentional interface states are already induced and this prevents the change of SBH. Therefore, suitable thickness of Si ICL and high donor concentration as possible are required for sufficient control of SBH by this method.

5.7.2 *Experimental procedure*

The sample structure and fabrication process are shown in **Fig.5-12** and **Fig.5-13**, respectively. First, n-GaAs and As doped Si ICL are grown by MBE in the same chamber. As pressure during Si ICL growth is $1x10^{-7}$ Torr and Si ICL thickness is 10 or 20Å. The sample that has 10Å crystalline Si and 10Å amorphus Si double layer was also prepared. The amorphus Si layer was inserted in order to avoid ion beam channelling into GaAs and it was grown at substrate temperature of 0°C using Si K-cell in the MBE chamber. After formation of Si ICL on GaAs, the samples were transferred from MBE chamber to FIB chamber through UHV transfer chamber without exposing the sample surface to the air. Then FIB irradiation was done on whole Si ICL surface. FIB ion source is Ga^+ and beam acceleration energy was 20kV. Does was varied $1x10^{11}$ to $1x10^{12}cm^{-2}$. The samples without FIB irradiation were also fabricated for comparison. After FIB irradiation, the samples were transferred to MBE or metal deposition chamber again without breaking UHV environment and Al evaporation was done. Then, conventional diode structure was fabricated and SBH was characterized by *I-V* and *C-V* measurement.

5.7.3 *Result and discussion*

Figure 5-14 shows the *I-V* characteristics of Al/n-GaAs Schottky diodes with

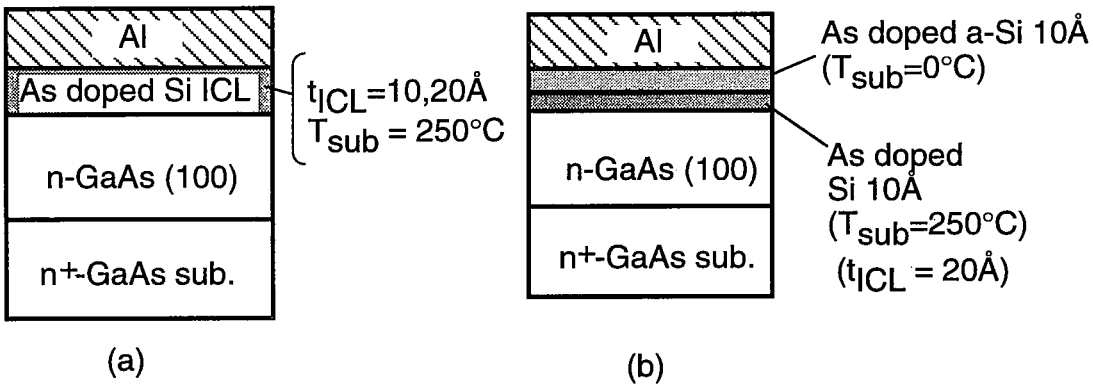

Fig.5-12. Sample structures for Schottky barrier height control utilizing FIB-induced interface states.

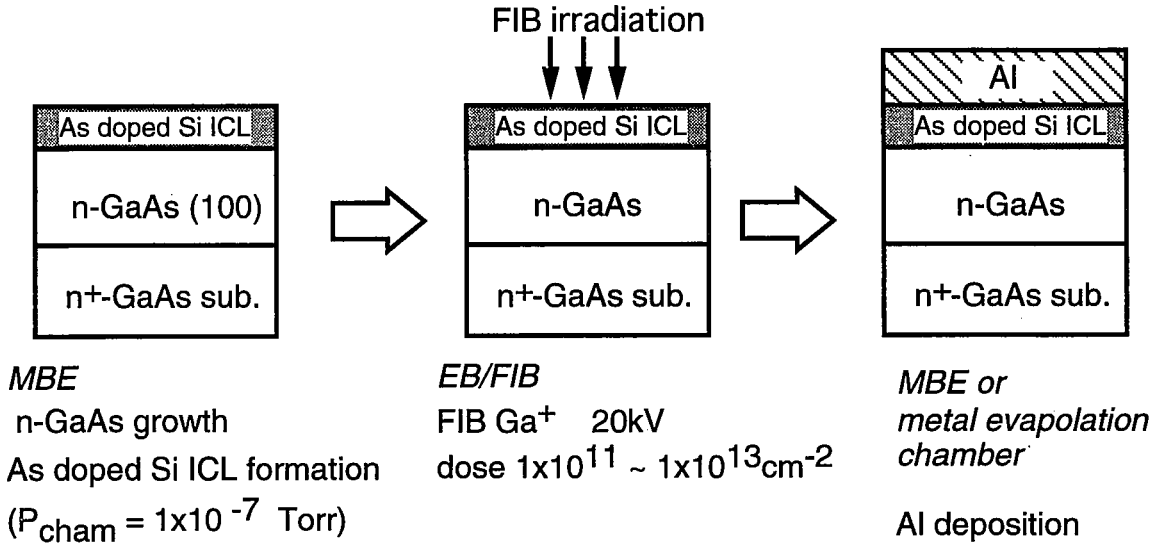

Fig.5-13. Sample fabrication process.

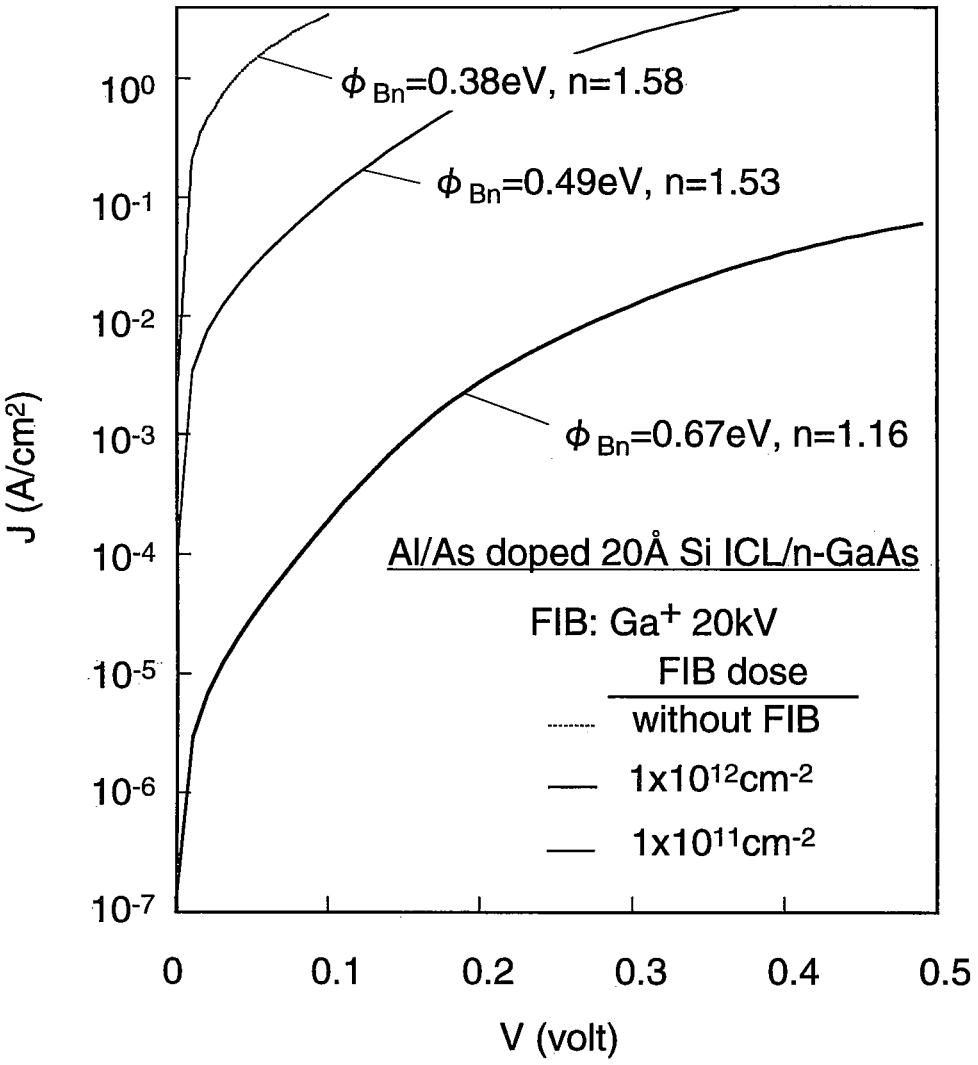

Fig.5-14. Forward I-V characteristics of Al/As doped Si ICL/n-GaAs Schottky diodes with and without FIB irradiation.

FIB irradiated As doped Si ICLs. Without FIB irradiation, ϕ_{Bn} became 0.38eV. With FIB irradiation, the effect of series resistance appeared in *I-V* characteristics, however, saturation currents went to low and this indicated that the SBH becomes high. SBH depends on dose of FIB, *N*. ϕ_{Bn} = 0.49eV and 0.67eV for N=1x10^{11} and 1x10^{12}cm^{-2}, respectively, were obtained. Ideality factor of n=1.16 was obtained, which indicated that the current transport was not strongly affected by FIB irradiation.

Figure 5-15 shows the FIB dose dependence of Schottky barrier height of fabricated 3 samples with different Si ICLs. All the samples shows the same tendency that SBH became high and approached to E_{HO} with increase of FIB dose. The maximum value of SBH was 0.71eV with 20Å Si ICL and N=1x10^{12}cm^{-2} and the range of change of SBH was 0.3eV. This result shows the possibility of spatial control of SBH by FIB with sufficient range. On the other hand, the range of SBH change seems not to depend on the condition of Si ICL formation. The ideality factors of fabricated samples are about 1.1~1.5. Any trend of the values could not be found, however, the minimum value of n=1.13 could be obtained. The scattered value of n seems to be caused by random distribution of dose of FIB irradiation. Therefore, it seems to be possible to improve the ideality value and n=1.1 may be realized if the FIB irradiation can be done uniformly.

Diodes with FIB irradiation showed the *I-V* characteristics that with series resistances R_S. The result is shown in **Fig.5-16**. R_S was evaluated by Norde plot.[14] The evaluated values were in 10^{-2}~10Ωcm^2, depending on the FIB dose. R_S increased in two order with the increase of the FIB dose in one order. On the other hand, R_S for different three ICLs scattered in the range of one order even when the dose of FIB was same. It seems to be possible to suppress R_S by optimizing the sample structure and FIB irradiation.

The relationship between FIB dose *N* and interface state density at Si ICL/ GaAs interface N_{SS} were shown in **Fig.5-17**. N_{SS} was evaluated from ϕ_{Bn} using **eq.(5.1)**.

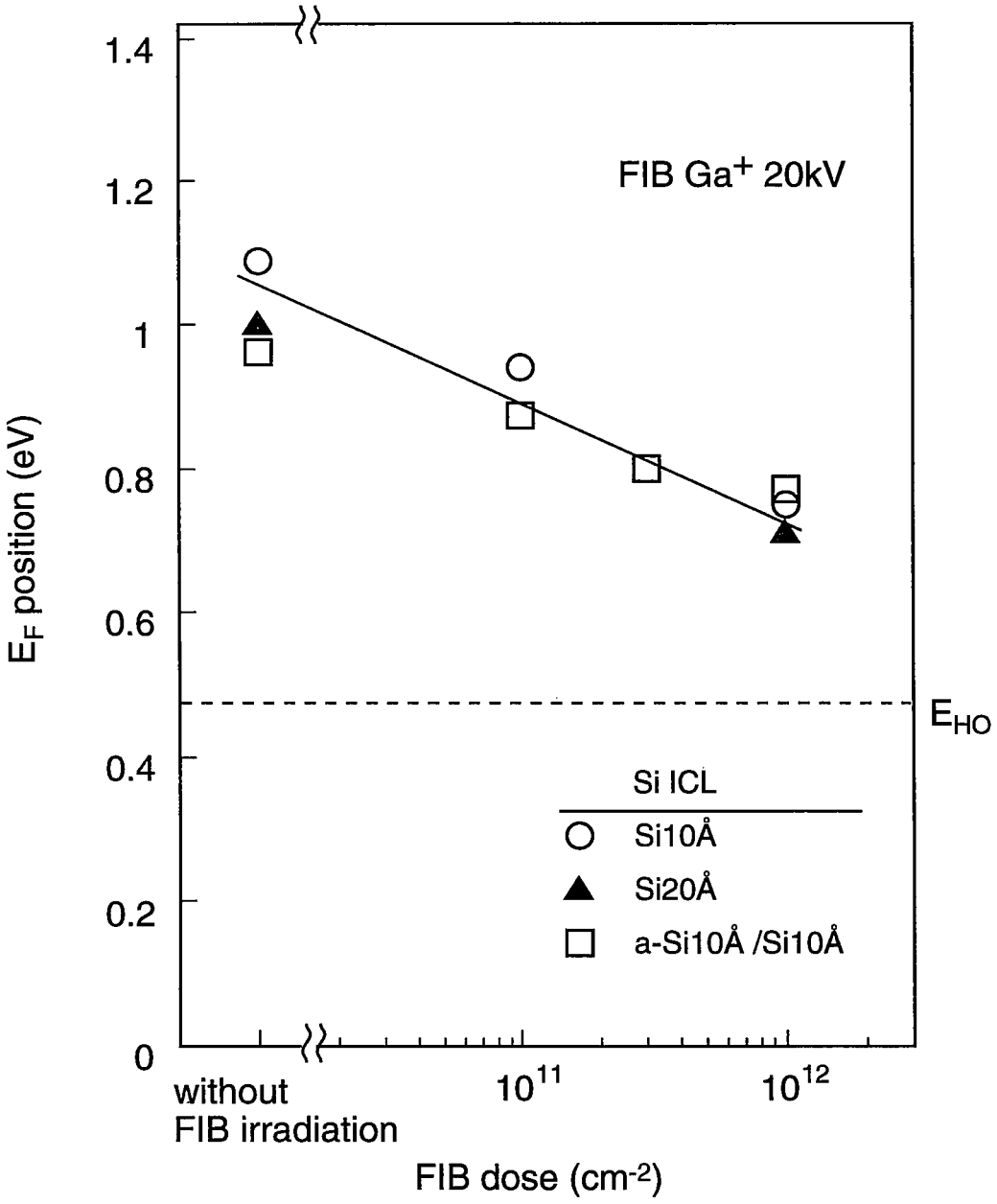

Fig.5-15. FIB-dose dependence of Schottky barrier height of Al/ As doped Si ICL/n-GaAs Schottky diodes.

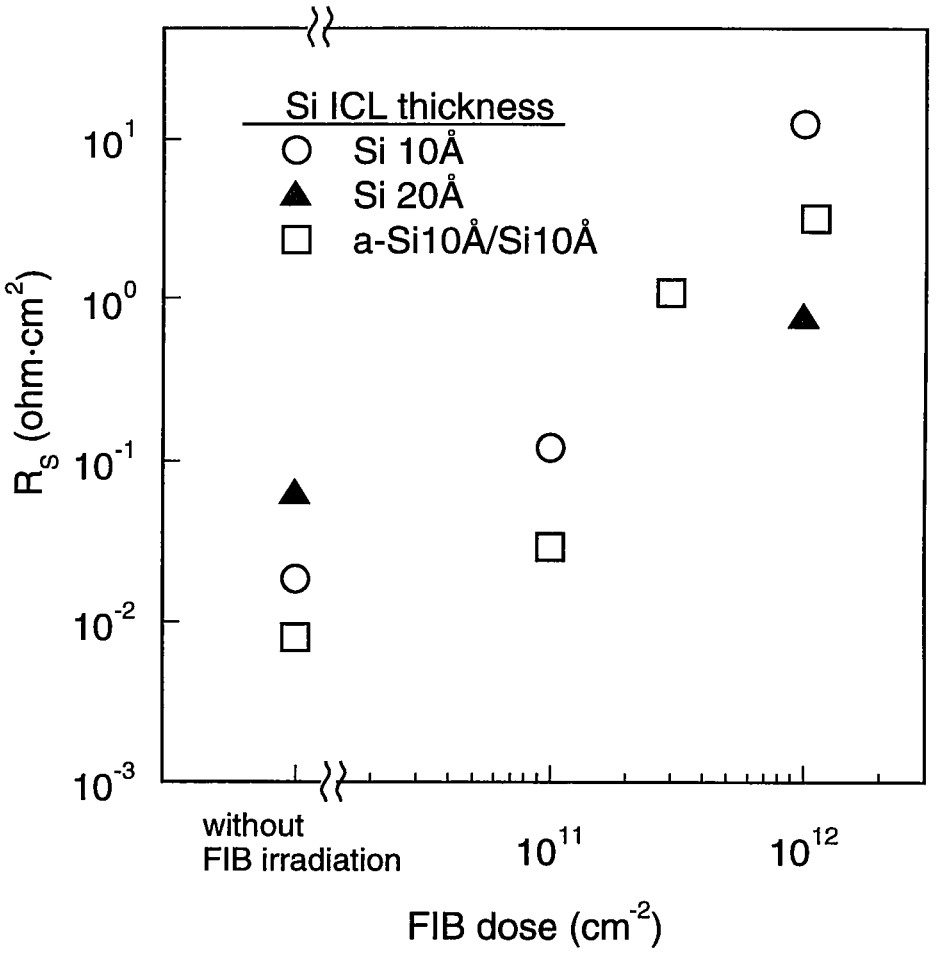

Fig.5-16. Series resistance R_S of Al/FIB irradiated Si ICL/n-GaAs Schottky diodes as a function of FIB does.

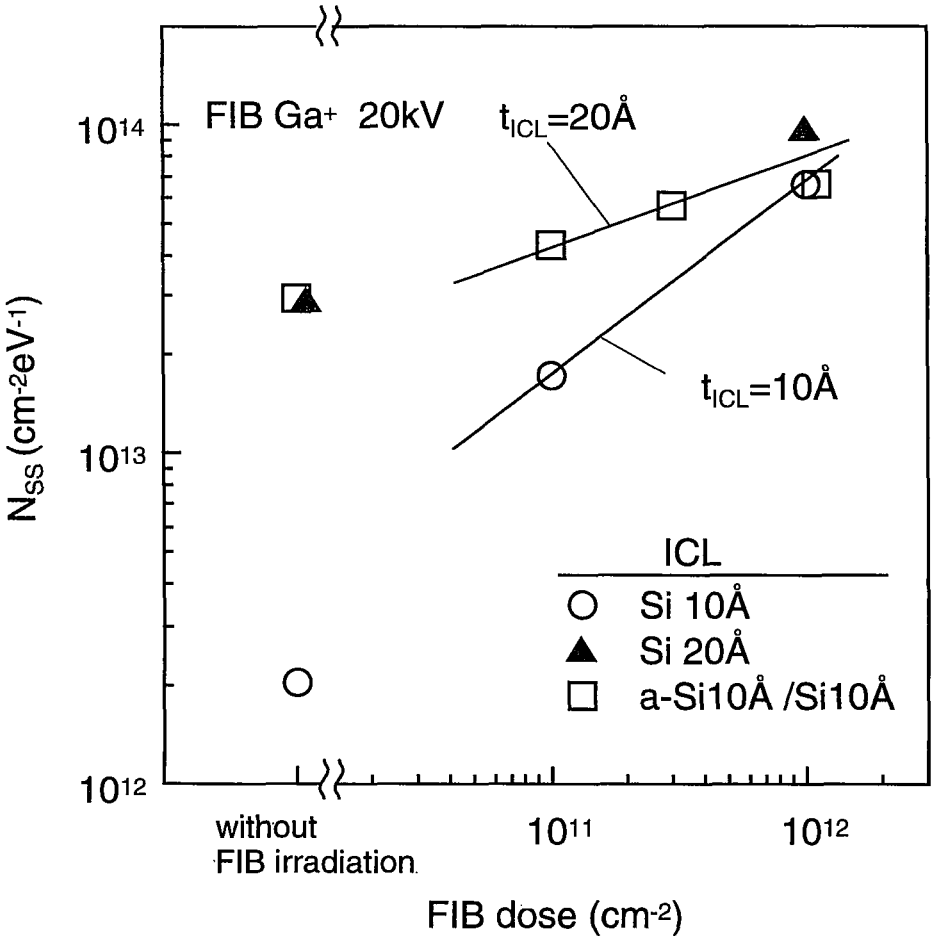

Fig.5-17. Estimated N_{SS} at Si ICL/n-GaAs interface as a function of FIB dose.

The correlation was shown between N and N_{SS}. It was found that N_{SS} increased with the increase of N. In. **Fig.5-15**, ϕ_{Bn} seemed not to depend on the condition of Si ICL, however, the N_{SS} clearly depended on Si ICL thickness when N=1x10^{11}cm^{-2}. This result indicates that the N_{SS} becomes easily high when Si ICL is thick. This is due to that the bond is easily broken in order to relax lattice mismatch when Si ICL thickness is over the critical thickness of 10Å.[13] When N=1x10^{12}cm^{-2}, induced Nss was about 10^{14}eV^{-1}cm^{-2} which did not depend on the Si ICL thickness. This value indicates that one Ga^+ ion induced of interface states of about 10~100 times higher, which corresponds to the reported value that the number of defect induced by FIB irradiation.[15] As described above, the interface states can be induced by FIB irradiation and the density of the states depend on the FIB dose, therefore it is possible to control Schottky barrier height by control of FIB dose.

5.8 Conclusions

The Schottky barrier height (SBH) control technique for metal/GaAs and InP interfaces by Si interface control layer (Si ICL) is discussed experimentally. And the method to spatially control SBH using FIB for its application to quantum nanostructures are discussed. The main conclusions are listed below:

(1) The SBH can be systematically controlled by doping into the Si ICL in the range of about 300meV for GaAs and 400meV for InP. Precise and continuous control can be achieved by changing doping concentration into the Si ICL until Si layer is pseudomorphic to the substrate semiconductor.

(2) As doping and B doping is effective, but Ga, Al doping is not.

(3) The experimentally observed behavior can be explained by theoretical models including ideal and realistic cases, with the latter taking into account the effect of the interface state at the ICL/semiconductor interfaces.

(4) To achieve high-performance diodes with controlled and reproducible barrier heights, Si ICL should be kept pseudomorphic with GaAs.

(5) By FIB irradiation on Si ICL, SBH of Al/doped Si ICL/n-GaAs changes by 300meV and this method is found to be possible for spatial control of SBH in nanometer order. SBH depends on FIB dose and this result indicates that the interface state is induced by FIB irradiation at Si ICL/GaAs interface and its density depends on the FIB dose.

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Chapter 6

Formation and Characterization of Metal/III-V Compound Semiconductor Interfaces by In-Situ Electrochemical Process

6.1 Introduction

It is known that Schottky barrier height (SBH) can be changed by improvement of M-S interface property so as to lead large metal-workfunction dependence of SBH.[1] M-S interface formation by in-situ electrochimcal process including surface etching and metal plating in the same electrolyte is found to be effective for this purpose.[2-4] This processes can be done without exposing the sample surface to the air, then the insertion of unintentional oxidized interfacial layer or contamination at M-S interface can be avoided. And this process is low energy one and damage due to metalization can be suppressed. According to the unified DIGS model, these seems to provide large metal-workfunction dependence of SBH and high Schottky barrier can be realized by using metal having large workfunction, such as Pt.

There are two unique and attractive points in Schottky barrier formation by in-situ electrochemical process. The one is that the *in-situ* electrochemical process realizes near ideal M-S interface formation. Moreover, this process can be carried out by using very simple setup. The another point is selectivity of metal plating. [5,6] Plating is carried out only where charges are supplied. This gives more flexibility to device fabrication process of not only pervious semiconductor devices[4] but also quantum nanostructures.[5-10]

In this chapter, Schottky barrier formation by in-situ electrochemical process and experimental results of characterization of fabricated planer InP Schottky diodes

are described, first. InP which is mainly studied in this chapter is the attractive material since its electron mobility is high, however, InP Schottky barrier height is very low and suffer large leakage current and insufficient gate control. Then, the result of application of Pt Schottky gate formed by in-situ electrochemical process to InP MESFETs is described.

6.2 In-situ electrochemical process

The experimental setup of the in-situ electrochemical process is illustrated in **Fig.6-1**. Three electrodes are set in the electrochemical bath which are a semiconductor sample, a Pt counterelectrode and a saturated calomel electrode (SCE) as the reference electrode. The electrolyte for Pt plating contains 1g H_2Cl_6Pt dissolved in 200ml 1M HCl with pH=1.5. The semiconductor electrode was fixed with wax to the sample holder and connected electrically to the external circuit. Metal plating by the electrochemical process is carried out selectively where the electron is supplied, so the sample is masked by photoresist or so on excepting the region which metal should be deposited. The in-situ electrochemical process was performed at room temperature. Anodic etching of the sample surface and Pt deposition onto the sample surface in the same electrolyte without exposing the sample surface into the air. The etching mode and metal-plating mode was switched by changing polarity of potential in the sample surface. The potential on the semiconductor electrode was controlled by a potentiostat with a pulse generator. The pulse generator provided voltage pulses for the avalanche pulse-assisted anodic dissolution and Pt plating as shown in **Fig. 6-2**.

When avalanche pulse is provided to the electrodes, holes are generated in the sample surface and they assist the anodic dissolution of the semiconductor surface. Pulse height is adjusted by monitoring the voltage between the semiconductor

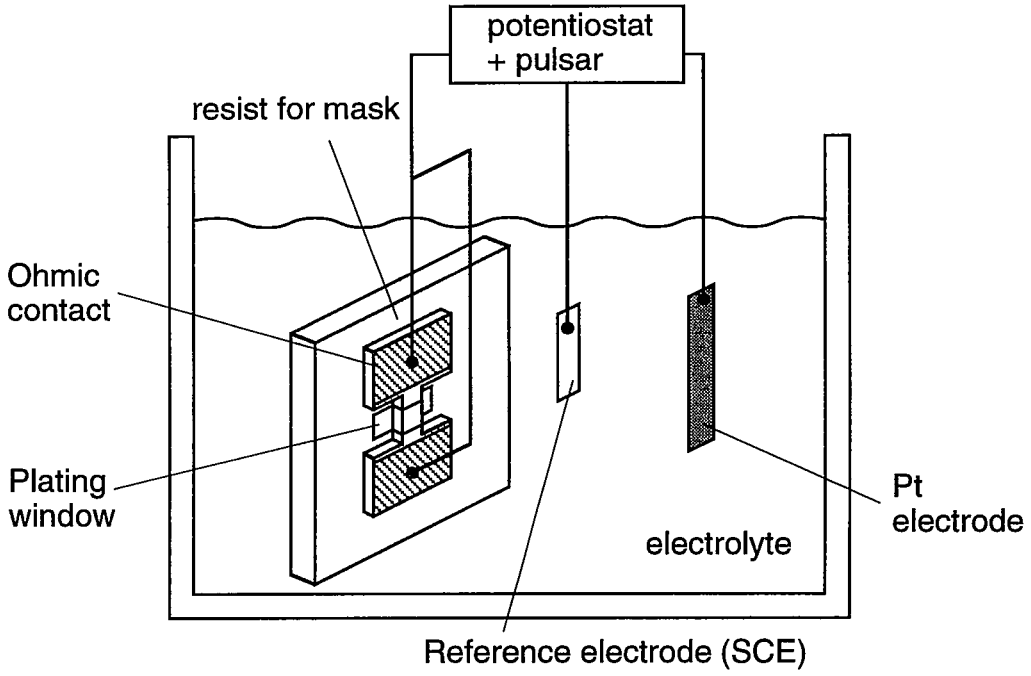


Fig.6-1. Experimental setup of in-situ electrochemical process.

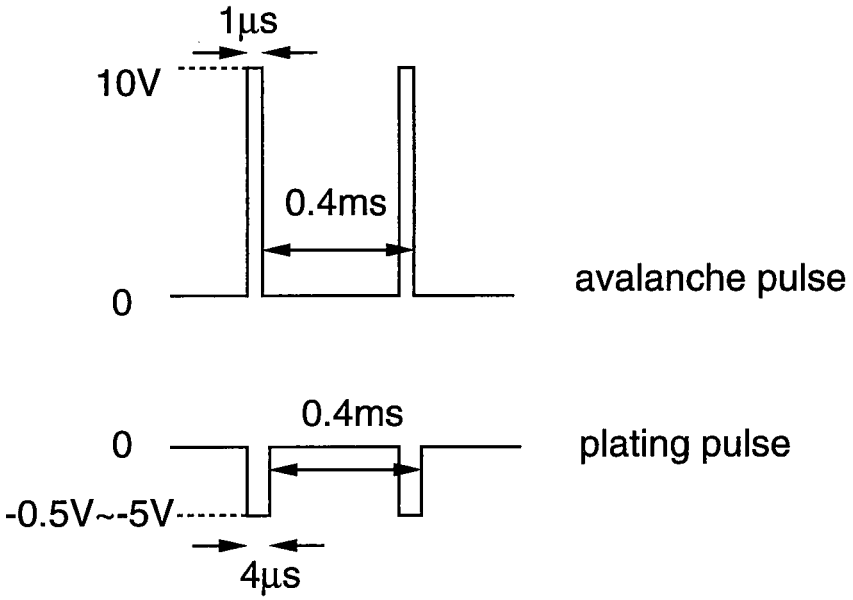


Fig.6-2.Pulse shapes for avalanche surface etching and Pt plating.

electrode and the electrolyte. Etching depth could be precisely controlled by the number of pulses. After etching of several hundred Å by the anodic pulse etching, Pt was immediately plated by pulse plating on the etched sample surfaces by changing polarity of the pulses without exposing the sample surface to the air. Use of pulses instead of direct currents (DC) was found to improve the current efficiency for Pt deposition. Since the problem of H_2 evolution at the Pt surface which takes place in DC plating could largely be avoided.

6.3 Characterization of InP Schottky interfaces formed by in-situ electrochemical process

6.3.1 *Fabrication of Schottky diodes*

An undoped n-type (100) InP wafer with a carrier concentration of n=4x10^{15}cm^{-3} was used for fabrication of InP Schottky diodes,. The wafer was cut into chips and each chip was chemically etched in a solution of H_2SO_4:H_2O_2 :H_2O=3:1:1. A Ge/Au/Ni contact layer was evaporated on the back side of the chip and alloyed in H_2 for 5min at a temperature of 350°C. Then, the sample surface was covered by photoresist (Shipley Microposit MP2400), and circular-dot windows for Schottky electrodes were defined by standard photolithography. Before the *in-situ* electrochemical process, the sample was immersed in etching solution HF:H_2O=1:1 for 60 sec in order to remove oxidized layer on the sample surface. Pt Schottky barriers were formed selectively by the in situ electrochemical process, using the photoresist as the mask, and the photoresist was removed after the process. The area of each circle was 2.3x10^{-3}cm^2.

For comparison, Pt/n-InP Schottky diodes were also fabricated by conventional electron beam (EB) evaporation process. InP surfaces were chemically etched in the

above solution for 60s followed by the treatment in HF:H_2O=1:1 solution for 60s. After blowing with the dry nitrogen gas, Pt was deposited on the InP surfaces by EB evaporation technique at a pressure of 10^{-6} Torr.

6.3.2 *Characteristics of Pt Schottky diodes*

Figure 6-3 shows the *I-V* curves of Pt/n-InP Schottky diodes formed by the electrochemical process and by conventional EB deposition. The EB process yielded a SBH value of 0.44eV with large ideality factor (n) of 1.70. This value of SBH is a typical one obtained by any conventional metal deposition process. In contrast, the novel process achieved an extremely high SBH of 0.86eV with a small n value of 1.13. And linearity of *I-V* characteristics in log plot is excellent with the linear region extending over six orders of magnitudes of current. Pt/n-GaAs Schottky diodes formed the electrochemical process are also show high and ideal Schottky barrier property, SBH of 1.02eV and n=1.06 are realized.[2] Such an increase of SBH gave rise to a corresponding reduction in the reverse leakage current. As seen in **Fig.6-3**, the difference in leakage currents reaches as large as 5 orders of magnitude at the reverse bias of -2V.

The $1/C^2$-*V* plot of the diode from **Fig.6-3** is shown in **Fig.6-4**. The plot shows excellent linearity with negligible hysteresis effects. The value of the built-in potential of 0.72eV is obtained, which corresponds to SBH of 0.84eV and is close to 0.86eV obtained from the *I-V* curve. Such consistency between *I-V* and *C-V* behavior and small values of ideality factors are difficult to obtain with Schottky barriers whose SBHs values are enhanced by insertion of thin interfacial insulation layers as shown in **chapter 4**.

XPS characterization of Pt/InP interfaces was performed in order to investigate the reason for the realization of such a high SBH by the in-situ electrochemical

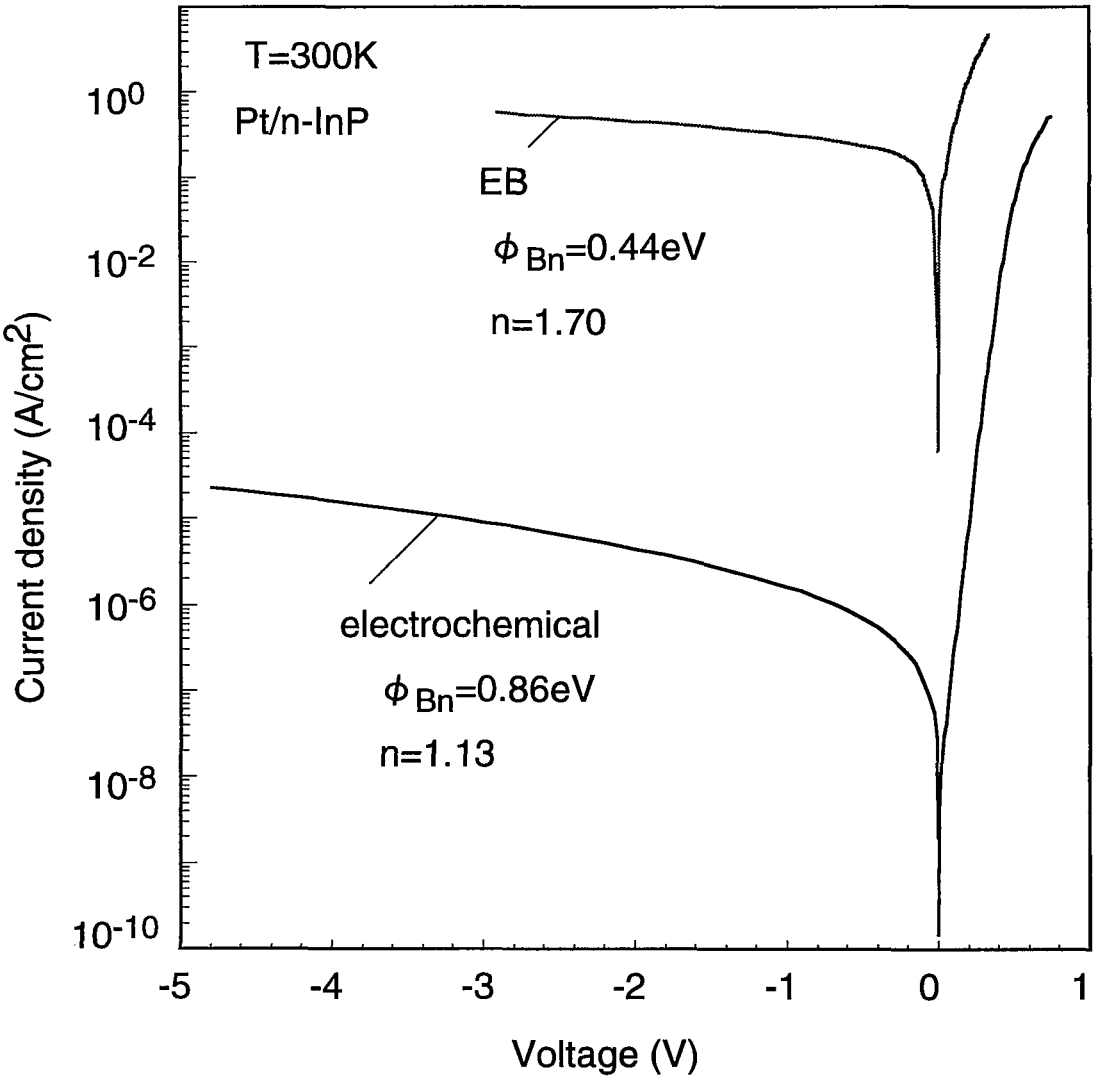


Fig.6-3. I-V characteristics of Pt/n-InP Schottky diodes formed by the electrochemical process and conventional EB evaporation.

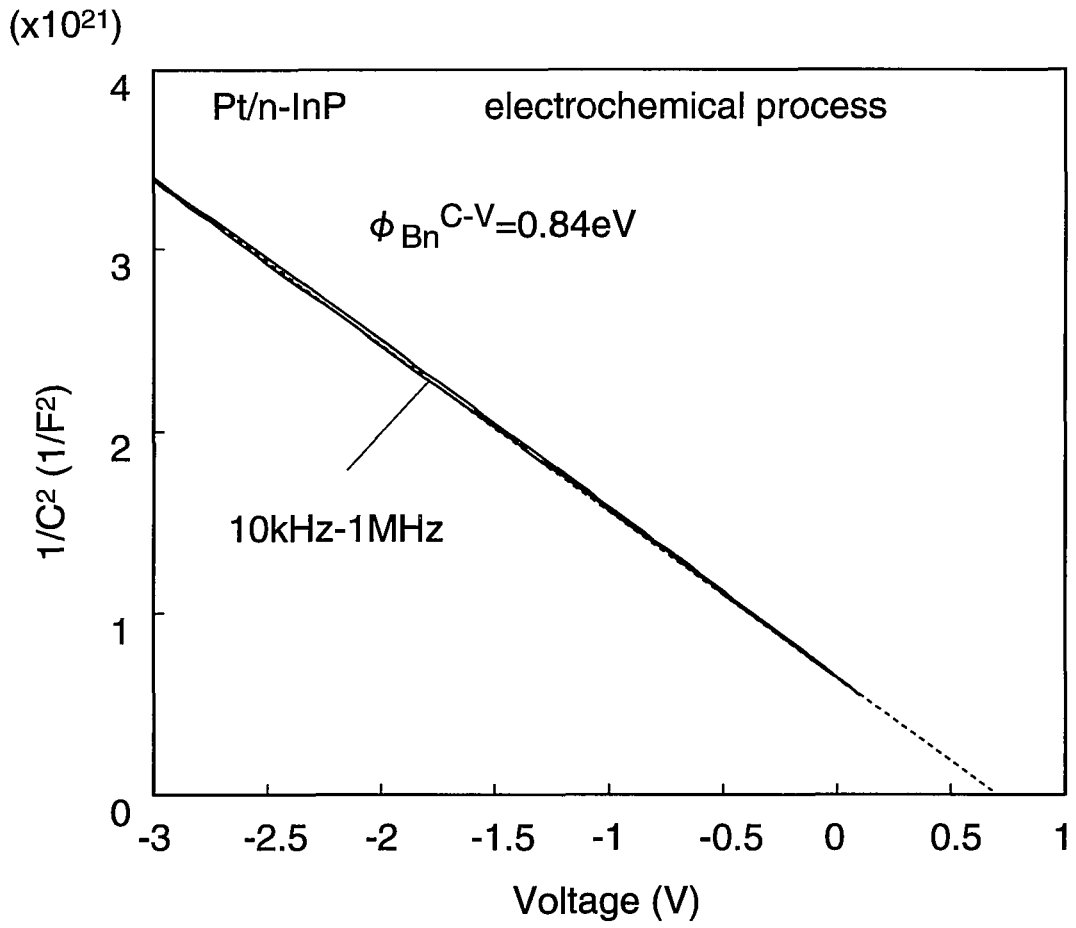


Fig.6-4. $1/C^2$-V plot of Pt/n-InP Schottky diode formed by in-situ electrochemcical process.

process. **Figures 6-5** shows the obtained $In3d_{5/2}$ and P2p X-ray photoelectron spectroscopy (XPS) spectra from Pt/n-InP interface formed by the in-situ electrochemical process and conventional EB deposition process. The spectra showing the In and P oxide layer can hardly seen for the sample by the electrochemical process and this indicates that there are no oxide phases at the interface. Deep level transient spectroscopy (DLTS) analysis of the electrochemically produced Schottky diodes have shown that no deep levels near the interface[11] although EB metalization process produces a large number of deep levels.[12] This indicates that the damage produced by metalization process isconsiderably suppressed in the electrochemical process. The electrical properties of the Pt/n-InP barriers mentioned above come from such properties of the interface.

6.3.3 *Metal workfunction dependence of SBH*

Figure 6-6 compares the metal workfunction dependence of the SBH values of the Schottky diodes fabricated by the present electrochemical process with those produced by standard vacuum deposition process. Different electrolytes were used to form Schottky diodes form each metalization.[3] The barrier heights were determined by the *I-V* methods. As seen in **Fig.6-6**, the SBH values of the electrochemical process strongly depended on the metal workfunction, although SBH of the Schottky diodes formed by EB evaporation hardly depends on the metal workfunction and the behavior agrees with Bardeen limit.[13] The broken line in **Fig.6-6** indicates the Schottky limit with interface index $S=d\phi_B/d\phi_m$ of unity based on the DIGS model, assuming that the charge neutrality level E_{HO} for InP lies at 5.2eV below the vacuum level and the 0.36eV from the conduction band edge.[14] The data point of Pt by the electrochemical process is located nearly on the line that indicates the Schottky limit. This indicates that the Pt/n-InP interface formed by the in situ process is completely

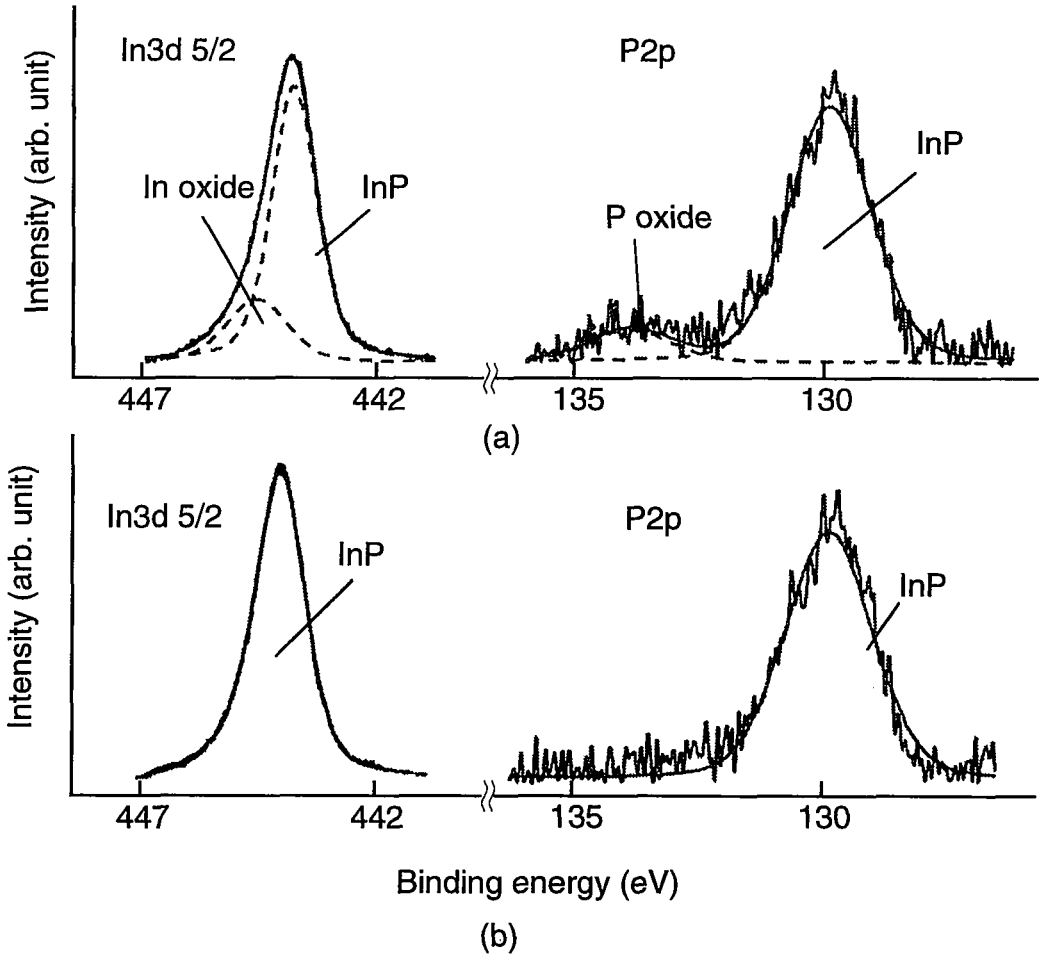


Fig.6-5 $In3d_{5/2}$ and P2p spectrum from Pt/InP interface formed by (a) conventional electron beam evaporation and (b) in-situ electrochemical process.

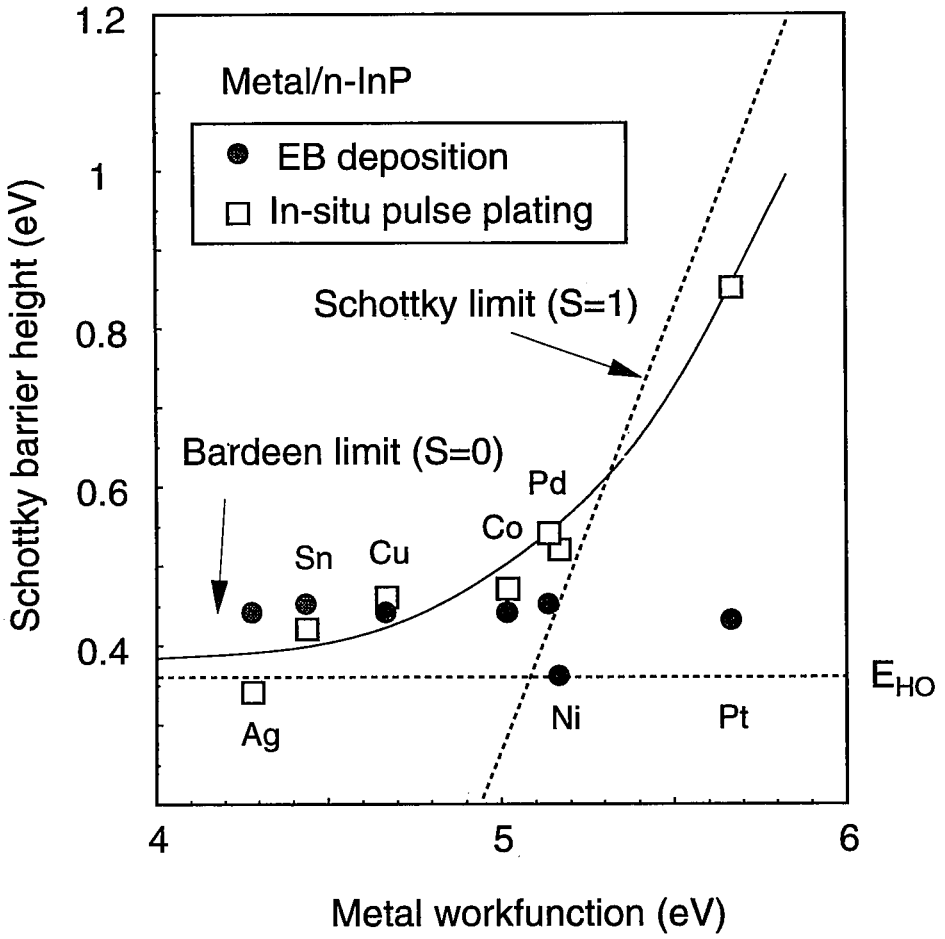


Fig.6-6. Metal-workfunction dependence of Schottky barrier height of InP Schottky interfaces formed by in-situ electrochemical process and conventional EB evaporation.

free from Fermi level pinning.

MIGS model can not explain this metal workfunction dependence of SBH since this model implies that Fermi level pinning is intrinsic and which mostly depends on semiconductor properties.[15,16] On the other hand, based on the idea of the DIGS model[14], the result that the realization of Schottky limit by in-situ electrochemical process can be explained by the realization of intimate interface without interfacial layer and extremely low processing energy. The present process does not cause crystalline disorder on the semiconductor surface since it is free from oxidization which easily incorporated into the semiconductor surface as shown in XPS result, and it is a extremely low energy process that applies only several hundred millivolts to the semiconductor at room temperature. The result that the no deep level exist atthe M-S interface by DLTS measurement also supports this point. Thus, utilizing the electrochemical process, SBH can be controlled by changing metal material as indicated by Schottky model. On the other hand, in the case of vacuum evaporation, the heated metal atoms on the semiconductor surface can produce damage and an interfacial disordered layer, resulting in the firm Fermi-level pinning.

6.4 Application of in-situ electrochemical process to fabrication of MESFETs

GaAs and InP MESFETs were fabricated utilizing Pt Schottky gates by the in-situ electrochemical process. For fabrication of GaAs and InP MESFETs, epitaxial layers were grown on semi-insulating (100) substrates by the conventional MBE an gas-source MBE equipments for GaAs and InP, respectively. For InP growth, In and tertiarybutylephosphine (TBP) as source materials were used. The carrier concentration and mobility of epitaxial layers determined by Hall measurement were $4x10^{17}$ cm^{-3} and 400 cm^2e/Vs for GaAs, and $2x10^{16}$-$1x10^{17}$ cm^{-3} and 1,100- 2,700 cm^2/Vs for InP, respectively. The fabrication process of the MESFET utilizing in-situ

electrochemical process is shown in **Fig.6-7**. First, n-GaAs or n-InP active layer was grown on semi-insulating substrate. Next, source and drain ohmic contacts were formed on mesa-etched islands on epitaxial layers. Then, the chip was covered with photoresist and the gate window pattern was defined on the photoresist layer by photolithography. Then, gate Schottky electrodes were formed by the electrochemical process supplying current from the ohmic electrodes. Gate metal can be selectively deposited using a photoresist as the mask. The plan view of the MESFET is illustrated in **Fig.6-8(a).** SEM observation showed that Pt was homogeneously plated with smooth edges following the gate pattern. Separate experiments have shown that such uniform deposition can be made on GaAs surfaces in the 0.1μm range using EB lithography as shown in **Fig.6-8(b)**. Therefore, the electroplating technology proposed here is also applicable to the fabrication of submicron-meter-gate devices.

The drain *I-V* characteristics of a InP MESFET having a gate length L_g of 3.5μm, a gate width W_g of 180 μm and a channel thickness d of 3100Å. Good current saturation behavior and a maximum transconductance (g_m) of 24mS/mm at V_G=0.6V were obtained. Drift of the drain current which is commonly seen in InP MISFETs was not observed at all. Fabricated GaAs MESFET also showed well pinch-off characteristics in I_{DS}-V_{DS} curves. Furthermore, it is also seen in **Fig.6-9** that good gate control of drain currents is achievable even under a positive gate bias up to 0.6V. This suggests that the present process is applicable to the realization of enhancement-mode MESFETs.

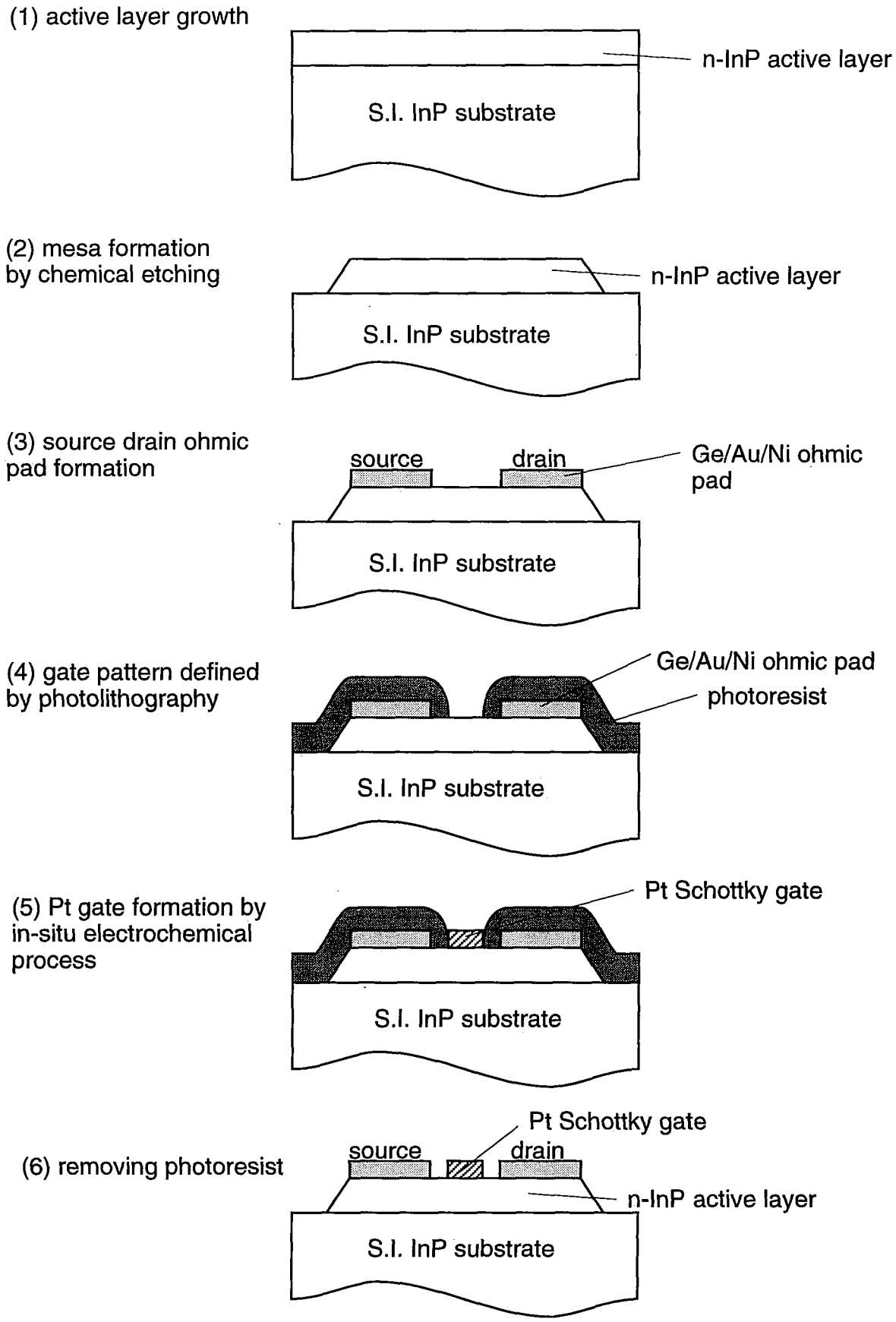
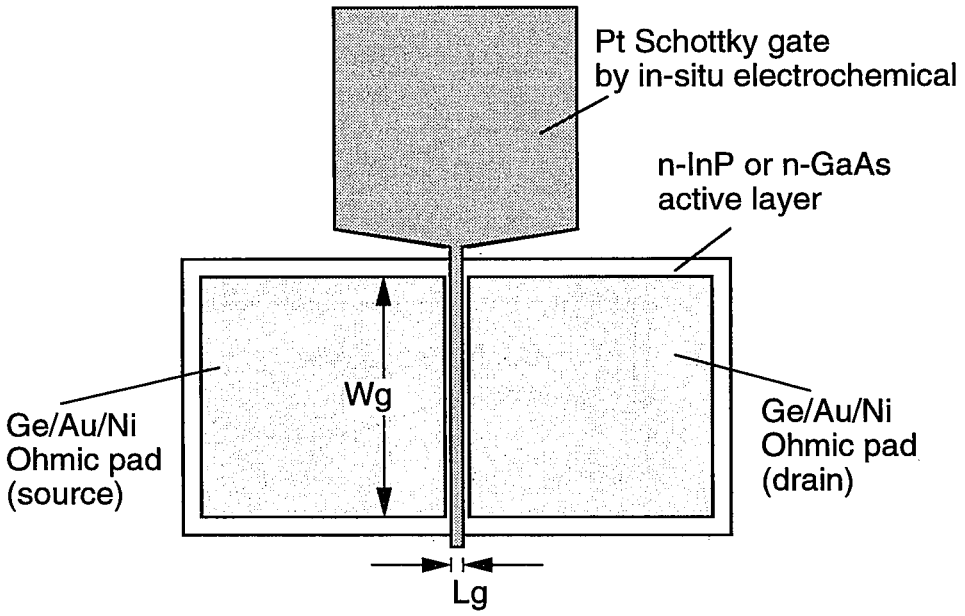
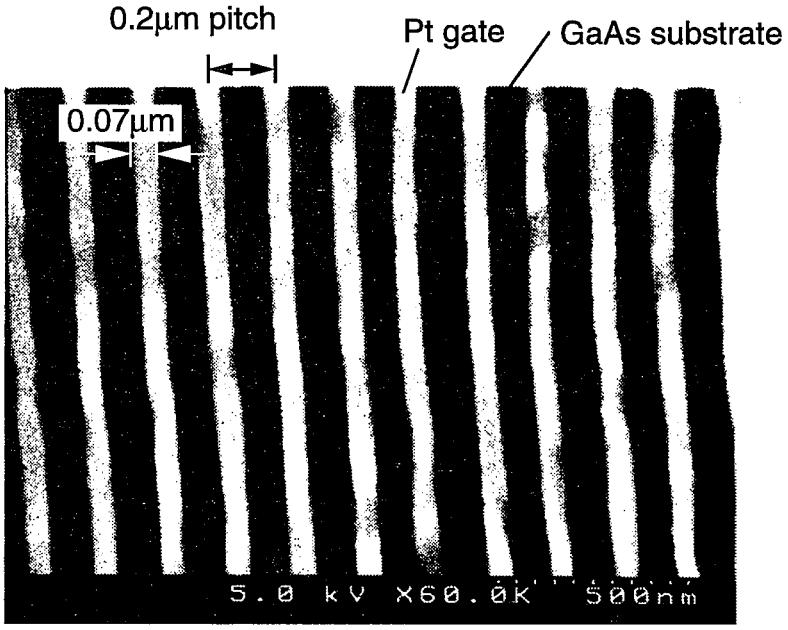


Fig.6-7. MESFET fabrication process



(a)



(b)

Fig.6-8. (a) Plan view of fabricated MESFET and (b) submicron Pt gate pattern formed by in-situ electrochemical process.

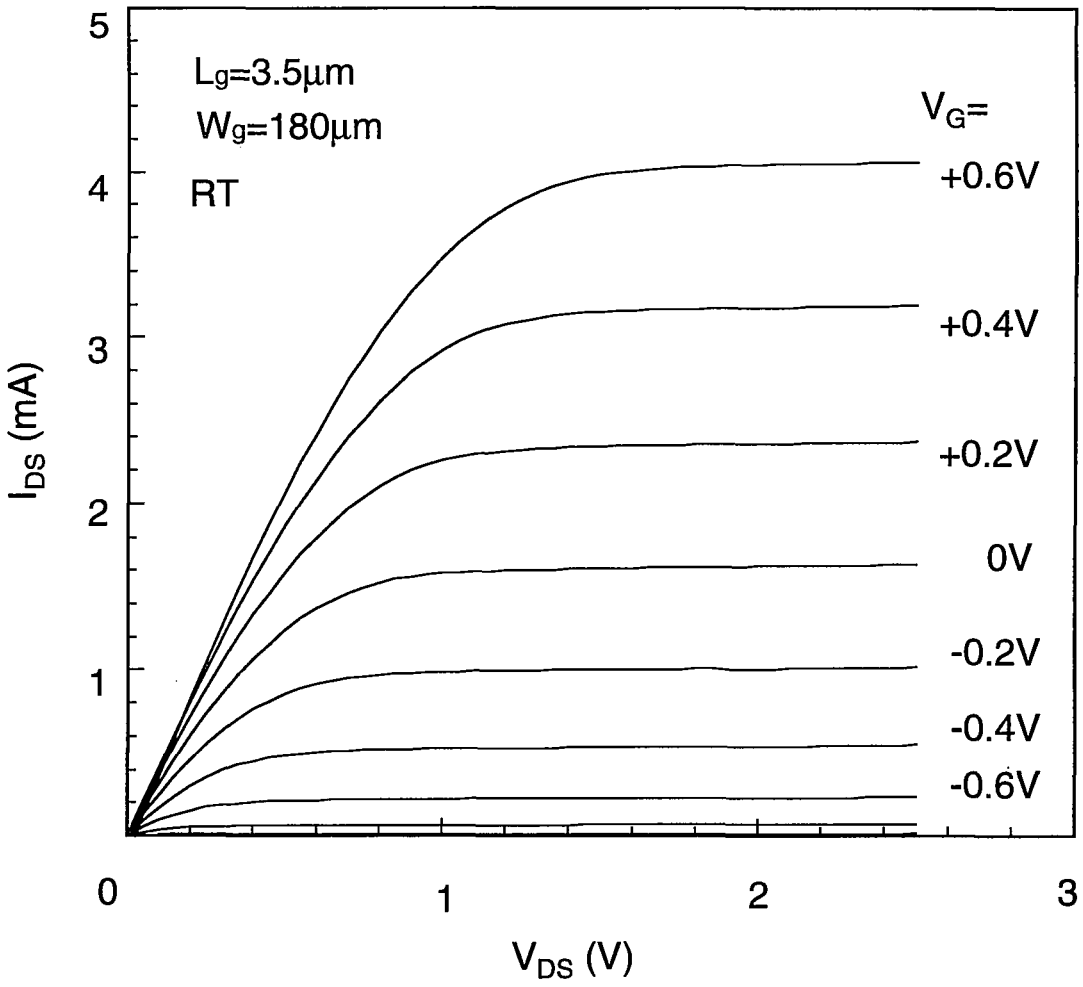


Fig.6-9. Drain I-V characteristics of fabricated Pt-gate InP MESFET.

6.5 Conclusions

InP Schottky diodes were fabricated by in-situ electrochemical process. Pt/n-InP Schottky diodes with high barrier heights (SBH=0.86eV) have been reproduciblly obtained for the first time by the novel in situ electrochemical process. This ideality factor is near unity. This novel high SBH process has led to the first realization of well-behaved InP MESFETs. Good gate control of drain current and an effective channel mobility of 1,840 cm^2/Vs have been achieved. The present InP MESFET operates even under the positive bias condition. Thus, the present in situ electrochemical process appears to be useful for realization of high-speed, low-power as well as high-power InP-based devices and integrated circuits.

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Chapter 7
Application of GaAs Schottky Barrier Height Control by Si ICL to a Lateral Surface Superlattice Structure

7.1 Introduction

Recently, a number of quantum devices have been realized on compound semiconductors by utilizing the split-gate structure which is formed by fine-pattern Schottky gates on the semiconductor surface. One of them is the lateral surface superlattice (LSSL) which is of practical interest because it has a planar geometry and is expected to produce useful negative differential resistance (NDR) characteristics at extremely high frequencies extending into the THz region.[1,2] The basic operation is based on the negative mass effect due to miniband formation in the periodical potential. A number of attempts have already been made to realize split-gate LSSLs.[3-5]

In the split-gate structure, modulation of the confinement potential for the two-dimensional electron gas (2DEG) at the heterointerface is achieved through the potential difference on its top surface. The surface potential underneath a Schottky metal is usually higher for electrons than of a free surface, and this difference is utilized. However, it is well known that a large number of surface states exists on the free surfaces of GaAs and related materials. These states not only reduce the potential difference through Fermi level pinning but also tend to make the device design and performance complex, unstable and unreproducible.

An alternative approach is either to modulate the surface-to-2DEG distance [6] or to modulate the Schottky barrier height (SBH). Unfortunately, the former requires large thickness variations to achieve significant potential modulations, and the latter

is known to be difficult due to the Fermi level pinning phenomenon. On the other hand, it is found that the SBH of compound semiconductor Schottky barriers can be changed over a wide range of about 300meV by inserting a silicon interface control layer (Si ICL) with suitable thickness and doping. [7-9]

A novel LSSL structure which utilizes SBH control technique using doped Si ICLs is proposed, fabricated and characterized. In this novel structure, periodic modulation of the potentials is achieved at the surface by lateral arrangement of Schottky barriers with different SBH values, and which gives rise to potential modulation at the heterointerface. The surface is totally covered by metal and operates as the gate. As compared with the split-gate structure, it can produce a larger variation of potential at the heterointerface. It also enables one to avoid the complexity and uncertainty of the air-exposed free surface of the semiconductor.
In this chapter, the structure and basic design of the novel LSSL are first presented and discussed. Next, the fabrication process is introduced. Then the results of the characterization of the novel structure by electron-beam-induced current (EBIC) measurements and current-voltage measurements at low temperature are presented, and finally the current transport mechanism for observed oscillations of transconductance and drain conductance is discussed.

7.2 Basic physics of lateral surface superlattice

7.2.1 *Basic property*

The idea of superlattice was came out in 1969.[10] Esaki and Tsu firstly proposed superlattice, fabricated it by III-V compound semiconductors and studied both experimentally and theoretically.[10,11] This structure is constructed by alternative epitaxial layers which are different from each other and its periodicity is mostly larger

than lattice constant of the natural crystal, and is considered to be an artificially controlled crystal. The superlattice was predicted to show various interesting characteristics based on quantum mechanical effets.[1,2,10,11] The most interesting and important property of the superlattice may be Bloch oscillation. Bloch oscillation is caused by interference between electron wave and periodic potential. Electron accelerated by applied field reached to edge of Brillouin zone and reflected to the other side of the zone, which is opposite direction of the field, and it is accelerated to the field direction again as shown in **Fig.7-1(a)**. Thus the current in the superlattice is alternatively changed by only application of dc field. Such a negative mass effect is expected to bring highest oscillation frequency in previous devices.

This effect seems to be observed in natural crystal, however, it has not been observed yet, since imperfection of the crystal easily break the acceleration of electron and electron is reflect to the other side of the zone before the electron reaches to the Brillouin zone edge as indicated in **Fig.7-1(a)**. Formation of long range periodic superlattice gives narrow Brillouin zone and this makes it easy to accelerate electron from edge to edge of the zone, therefore superlattice has been studied in order to observe Bloch oscillation. In primal experimental study of superlattice, epaxial growth technique was premature and the expected oscillation characteristics could not be observed since the mean free path through the alternative layers is not sufficiently long and phase breaking of electron wave occurs.[10]

On the other hand, electron transport parallel to the heterostructure is found to be excellent due to one dimensional quantization of electron, which is well know to be 2DEG, and its mean free path is very long and electron wave can transport in long distance in the range of micrometer without phase breaking. The superstructure utilizing 2DEG (or Si inversion layer) called lateral superlattice, which has periodic potential in heterointerface. Lateral superlattice whose periodic potential was introduced by modulating surface potential is called lateral surface superlattice (LSSL). In order to modulate surface potential, various techniques have been

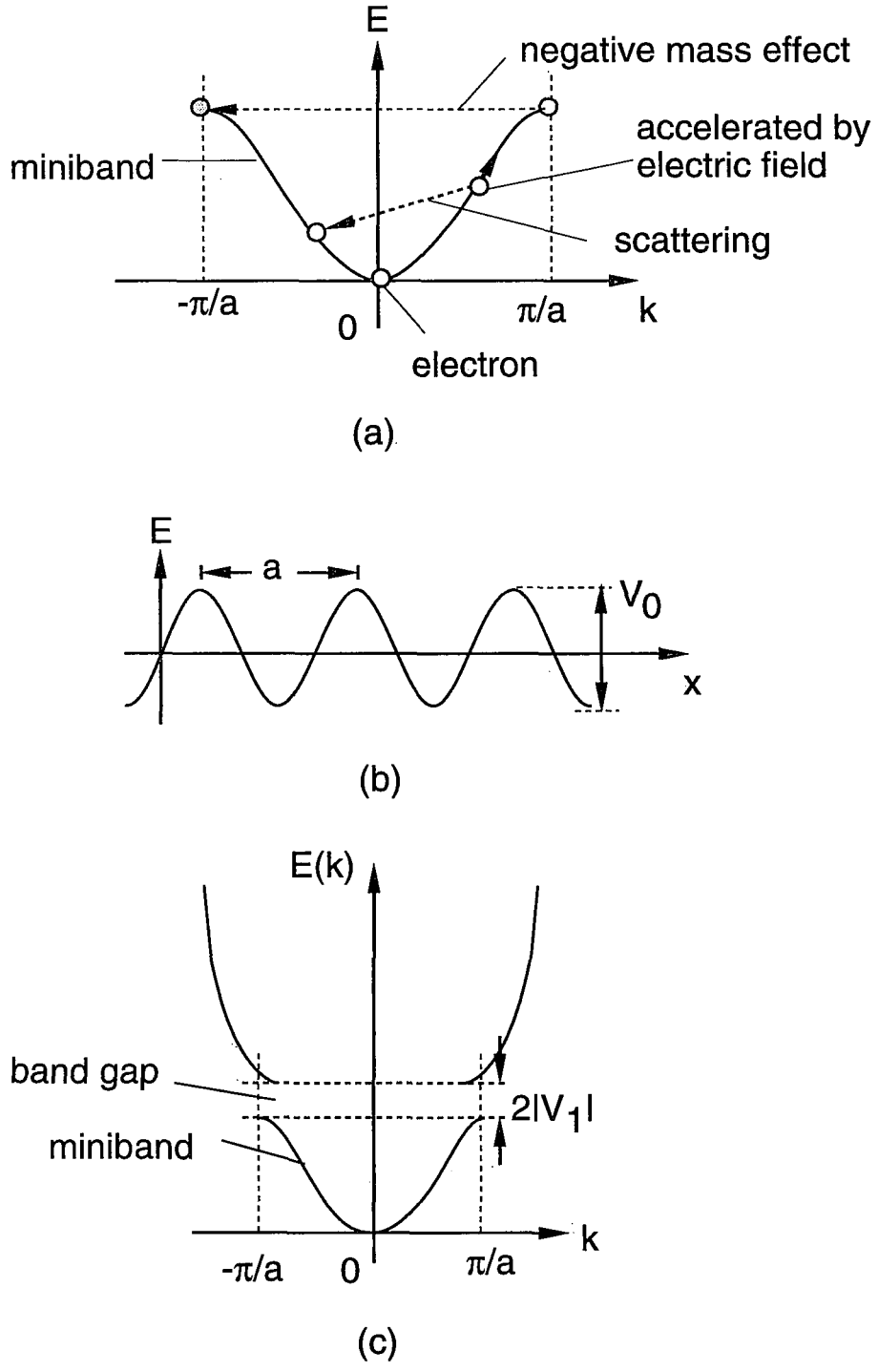


Fig.7-1. (a) Motion of electron in a miniband under electric field, (b) sinusoidal potential in heterointerface induced by surface-potential modulation of LSSL structure and (c) the miniband formation due to periodic potential.

investigated, including periodically laser irrumination[12], periodically surface etching[13], grating Schottky gate formation[3-5], periodically insertion of insulator[14] or resist[15], air gap[5] and so on. Most of investigation of LSSL was done from viewpoint Weiss oscillation[12,14-17] but Bloch oscillation. Weiss oscillation is magetoresistance oscillation due to phase matching between cyclotron radius of electron in magnetic field and periodic potential. Thus, the oscillation refracts on the periodicity of modulated potential. On the other hand, most of experimental investigation of quantum transport of LSSL was performed by Ismail *et al.*[3,4], and their LSSL has grating or grid Schottky gates on the channel of conventional high electron mobility transistor (HEMT). They observed transconductrance oscillation and negative differential resistance (NDR) in I_{DS}-V_{DS} characteristics at 4.2K. They reported that the transconductance oscillation was caused by Bloch oscillation, although the NDR characteristics was caused by sequential resonant tunneling.[4] However, the observed transconductance oscillation in dc characteristic could not be distinguished from that due to Bloch oscillation and sequential resonant tunneling effect since they show the same oscillation characteristics.[11]

7.2.2 *Bloch oscillation*

Bloch oscillation can be brought by semiclassical simple consideration as follow. The velocity v_g of electron of which wave number is k is given by

$$v_g = \frac{1}{\hbar}\frac{\partial \varepsilon(k)}{\partial k} \tag{7.1}$$

The motion equation under the condition that dc electric field $\boldsymbol{E}$ is applied is given by

$$\hbar\frac{dk}{dt}=qE \tag{7.2}$$

where, $\varepsilon(k)$ is electron energy in k-space. Electron motion is assumed to be limited in one band and the band structure is approximated to be sinusoidal.

$$\varepsilon(k)=V_0\left(1-\cos\left(\pi\frac{k}{k_m}\right)\right) \tag{7.3}$$

where V_0 and km are wave number and energy at the Brillouin zone boundary. If the electron of k=0 is accelerated by dc field $\boldsymbol{E}_0$ from t=0, the time dependence of wave number k is given by **eq (7.2)**. Electron velocity in real space v_g is

$$v_g=v_0\sin\left(\omega_0 t\right) \tag{7.4}$$

where, $v_0=\pi\varepsilon_m/2\hbar k_m$ and $\omega_0=\pi qE_0/\hbar k_m$. v_0 and ω_0 are maximum electron velocity and frequency of electron in Bloch oscillation. As seen in **eq.(7.4)**, electron velocity and its direction change alternatively under dc field and the frequency can be changed by changing the field.

7.2.3 *Miniband formation*

Artificially introduced periodic potential brings band structure in LSSL. Periodic potential in the LSSL seems to be sinusoidal as shown in **Fig.7-1(b)** and several workers calculated band structure theoretically using this assumption (this assumption is found to be almost ready by 2 dimensional potential calculation). Miniband formation can be predicted by simple theory with first order perturbation. Assuming that basis wavefunction is $\varphi_{k+Km}(r)=\exp\{(i(k+K_m)r\}$ (m=0,-1) and periodic

potential is $V(r)=V_0 \exp(ipr)$, the Hamiltonian matrix is given by,

$$\det|\mathrm{H}-\mathrm{E}|=\begin{vmatrix}(k-1)^2-\varepsilon & V_1 \\ V_1 & k^2-\varepsilon\end{vmatrix}=0 \qquad (7.5)$$

where, k is wave number, K_m is reciprocal lattice point and $V_1=\int V(r)\cos(pr)dr$. Solving this equation, E-k distribution is obtained as follows.

$$\varepsilon=\frac{1}{2}\left\{k^2+(k-1)^2\right\}\pm\frac{1}{2}\sqrt{\left\{k^2-(k-1)^2\right\}^2+4V_1^2} \qquad (7.6)$$

From **eq.(7.6)**, it is found that the miniband is formed and bandgap that equals to $2|V_1|$ exists at the boundary of Brillouin zone as shown in **Fig.7-1(c)**.

7.2.4 *Weiss oscillation*

The two-dimensional motion of electrons subjected to both a periodic potential and a perpendicular homogeneous magnetic field B leads to interesting problems, owing to the presence of two length scales, the period a of the potential and the magnetic length $\lambda=(c\hbar/eB)^{1/2}$. The magnetotransport properties of a 2DEG are expected if a and λ are roughly of the same order of magnitude. Since transport is mainly due to electrons at the Fermi energy E_F, the Fermi wavelength $2\pi/k_F$, which is related to the mean density $N_S=k_F^2/2\pi$ of the 2DEG, becomes important as a third length scale, which complicates the situation. Shubnikov-de Haas (SdH) oscillations, which are periodic in B^{-1} with period $\Delta\mathrm{SdH}(c/B)=e/\hbar k_F^2$, result from the fact that for even-integer values of the filling factor of Landau levels $\nu=\lambda^2 k_F^2$ (assuming that the

spin degeneracy is not resolved), elastic scattering leading to finite conductivity components is not possible.

In addition to the usual SdH oscillations, Weiss oscillations appear in $r_{\perp}$ at magnetic fields lower than 1T and at low temperatures. Only weak oscillations with a phase shift of 180° relative to those of $r_{\perp}$ are visible in $r_{//}$. The extreme of $r_{\perp}$ occur at B values

$$\frac{c}{B_{\lambda}}=\frac{ea}{2\hbar k_{F}}(\lambda+\phi),\ \lambda=1,2,\ldots, \qquad (7.7)$$

with ϕ=-0.25±0.06 for the minima and ϕ=+0.17±0.06 for the maxima. As the temperature is increased , the SdH oscillations are strongly damped whereas the Weiss oscillations are apparently unaffected.

7.3 Novel LSSL structure and basic design

7.3.1 *Structure of novel LSSL*

The structure of the novel LSSL devices is shown in **Figs.7-2**. The plan view in **Fig.7-2(a)** shows a standard field-effect transistor (FET) structure with gate length, L_g, and gate width, W_g, except for the grating gate region whose cross-sectional view is shown in **Fig.7-2(b)**. This is the essential part of the device, and potential modulation is achieved here by SBH control using doped Si ICL stripes which are inserted with a period of a at the top metal-semiconductor (M-S) interface of a conventional AlGaAs/GaAs modulation-doped structure with surface-to-2DEG distance, D, and dopant concentration of the carrier supply layer, N_D.

Figure 7-2(c) and **(d)** shows the basic concept of SBH control using doped Si ICL layers for a metal/n-GaAs system. It is well known that the Fermi level at the M-S interface of GaAs is firmly pinned, keeping the SBH of n-GaAs in the range of 800~900meV and independent of the metal work function, as shown in **Fig.7-2(c)**. However, by inserting a Si ICL, with thickness t_{ICL} and doped with a high concentration of donors or acceptors, at the M-S interface, strong doping dipoles are created at the interface and SBH values are modified, even though the Fermi level at the metal/Si ICL interface is firmly pinned. The band diagram for the case of SBH reduction on n-type GaAs by Si ICL doped with donors is shown in **Fig.7-2(d)**. The Si ICL must be very thin, 1~2nm, so that it retains pseudomorphic matching with GaAs and so that no Fermi level pinning takes place sat the Si ICL/GaAs interface. It should be highly doped in the range of $10^{20}cm^{-3}$ to produce strong dipoles within a small thickness. According to previous experiments, the SBH of Al/Si ICL/n-GaAs Schottky barriers can be changed systematically over the range of 200meV with As doping.[7,8] Therefore, by inserting doped Si ICL stripes with SBH=ϕ_{Bn1} periodically

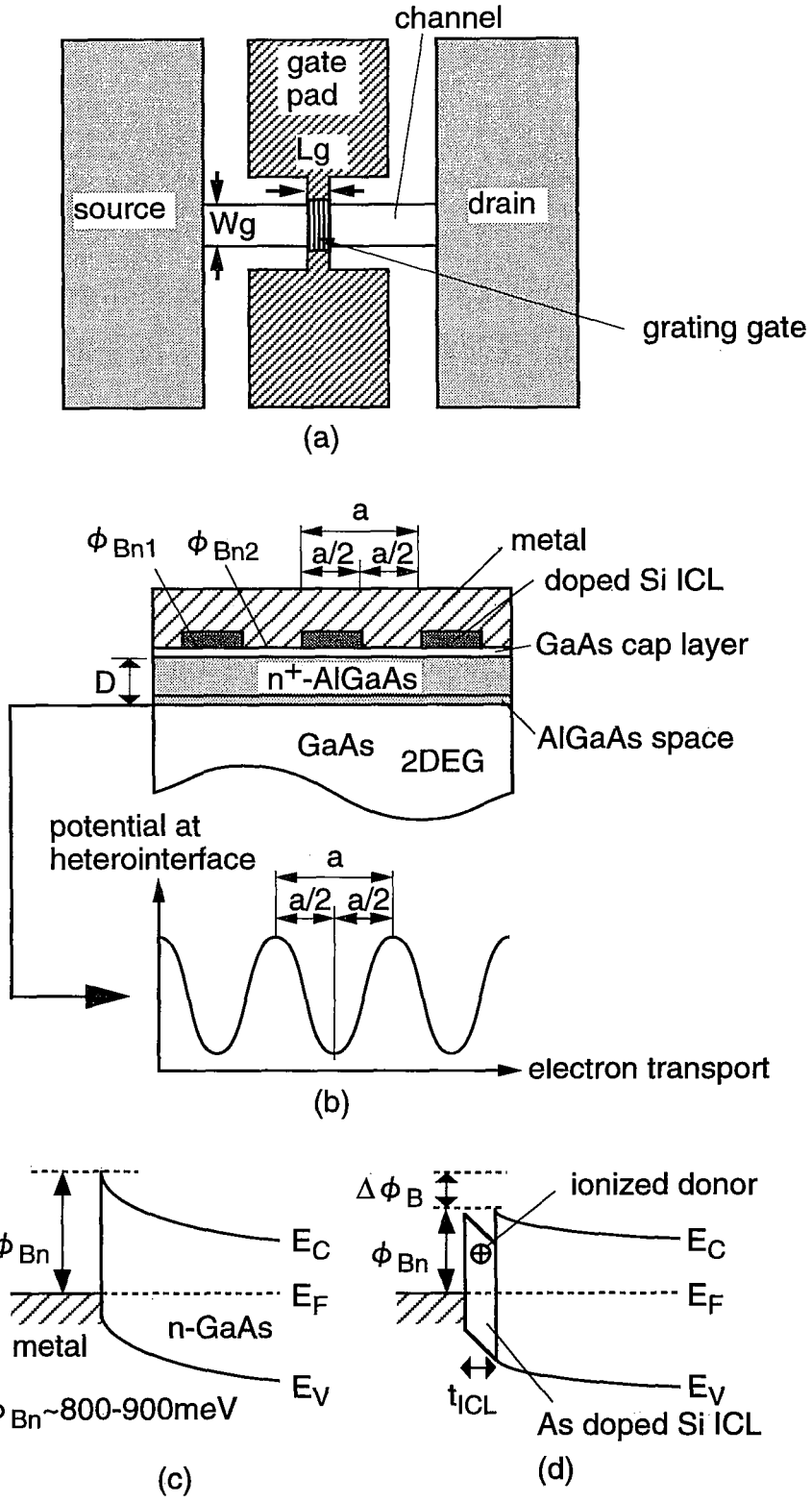


Fig.7-2. The structure of the novel LSSL. (a) Plan view of the LSSL device. (b)~(d) Principle of potential modulation by barrier-height-controlled Schottky interfaces.

at the n-GaAs Schottky interface which has SBH=ϕ_{Bn2} without Si ICL, periodic quare-wave modulation of potential between ϕ_{Bn1} and ϕ_{Bn2} should be created at the top surface of the structure, which then modulates the potential at the AlGaAs/GaAs heterointerface, as shown in **Fig.7-2(b)**.

7.3.2 *Basic design considerations*

In order to elucidate the relationships between the surface potential difference, $\Delta\phi_{Bn}$, at the top M-S interface, the modulation shape and the potentials at the heterointerface and the quantum states resulting from potential modulation, two-dimensional potential calculation was performed for the present LSSL structure. Poisson's equation was solved numerically using a finite difference method. Use of the successive over relaxation (SOR) method realized quick convergence of the solution.

Figure 7-3(a) shows an example of the calculated potential at the heterointerface for the present LSSL having two different SBH values of 800meV and 600meV with respect to the GaAs cap layer. The dimensions a=200nm and D=55nm and N_D=1x10^{18}cm^{-3} were used. Although the surface potential at the M-S interface varies in a square-wave fashion, the result of calculation plotted in **Fig.7-3(a)** shows that the shape of the potential at the heterointerface quickly becomes sinusoidal due to the long-range isotropic nature of Coulomb force. It is also seen that both the full amplitude of the sinusoidal potential modulation V_0 and the Fermi level position E_F with respect to the edge of the GaAs conduction band, E_C, vary greatly with the gate bias. This clearly showed that Fermi wavelength could be well controlled by V_G in the case of the present LSSL structure. In order to clarify possible differences in potential distribution in the split-gate device, a similar calculation was performed for the latter using the same values of dimensions. The result is shown in

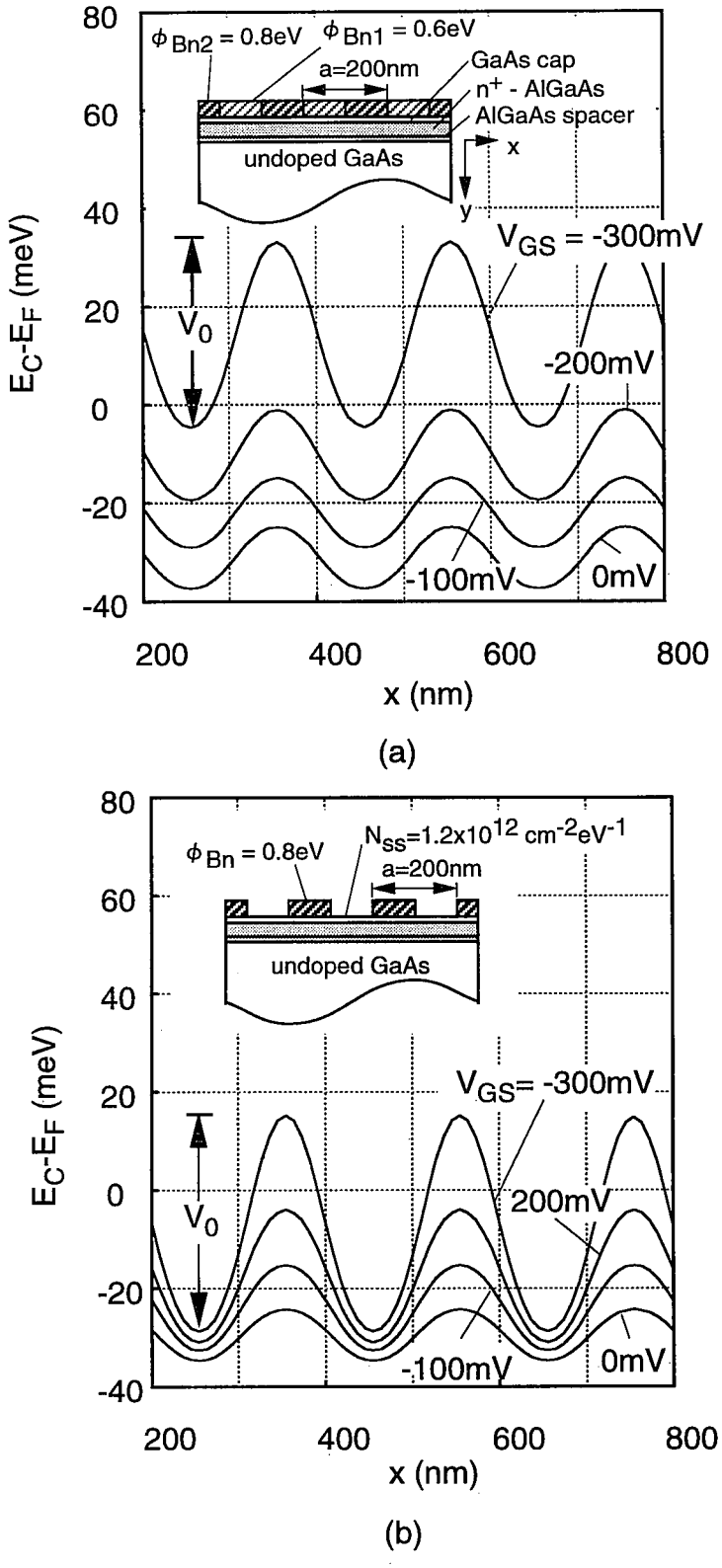


Fig.7-3. Calculated potential at heterointerface of (a) the present LSSL structure and (b) a conventional periodic split-gate LSSL structure for various gate voltages.

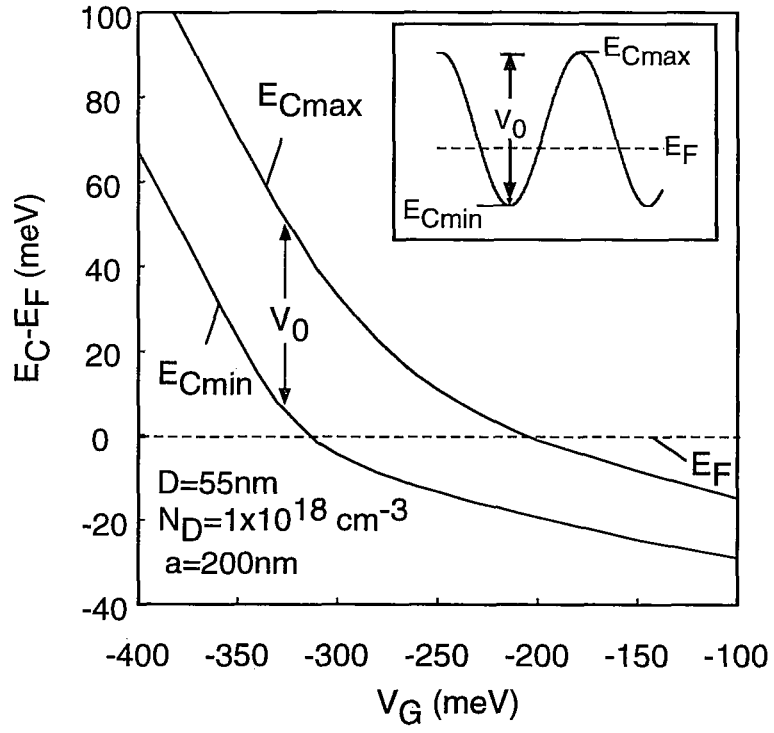
Fig.7-3(b). Here, a SBH of 800meV at the M-S interface and the presence of an uniform surface state density of $1.2x10^{12}cm^{-2}eV^{-1}$ at the free semiconductor surface were assumed, respectively. The Fermi level position at the free surface was determined self-consistently in this calculation. In **Fig.7-3(b)**, the potential shapes are sinusoidal as in **Fig.7-3(a)**. However, only the amplitude is changed greatly by gate bias, and the Fermi level position varies much less in the case of the split-gate structure.

Figure 7-4(a) shows the calculated energy positions of the potential maximum E_{Cmax} and minimum E_{Cmin} at the heterointerface as a function of gate voltage for the present LSSL device. As seen in **Fig.7-4(a)**, the Fermi level moves quickly with gate bias, and the amplitude of the potential modulation V_0 ($=E_{Cmax}-E_{Cmin}$) becomes larger with decreasing gate bias.

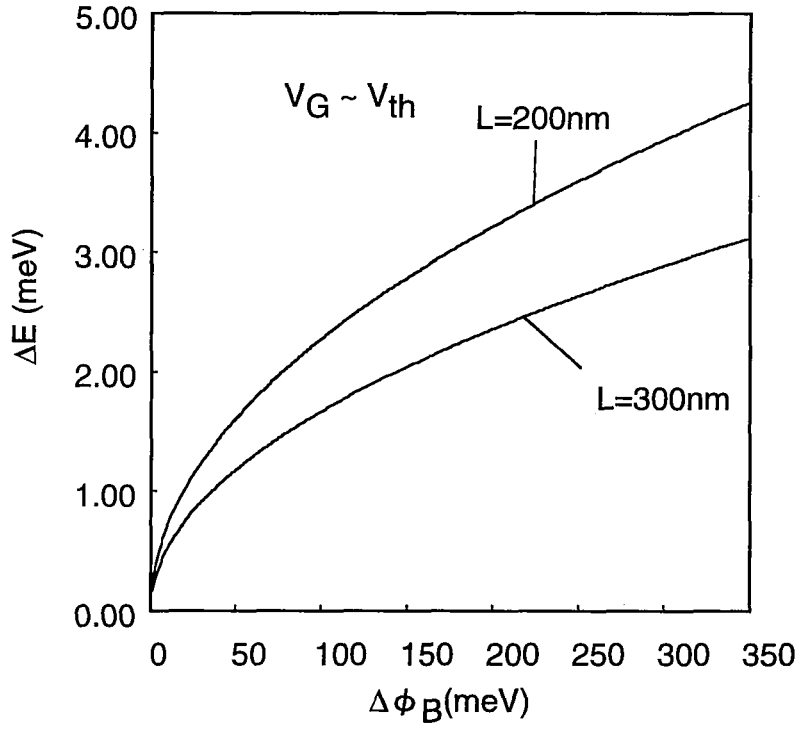
It is desirable to have a rough idea of the quantized states formed by potential modulation. Since the effect of level broadening due to miniband formation is expected to be small for the period of 200~300nm, the energy separation ΔE of subbands were estimated by applying harmonic potential approximation to the sinusoidal potential. The calculated relationship between the potential difference $\Delta\phi_{Bn}=\phi_{Bn2}-\phi_{Bn1}$ at the M-S interface and the level spacing ΔE is shown in **Fig.7-4(b)** for the device in **Fig.7-3(a)**, except that ϕ_{Bn1} changes while ϕ_{Bn2} is constant. The effect of changing a from 200nm to 300nm is also shown. It is seen that using quantized levels with spacings of 2~3meV should be realized with $\Delta\phi_B$ of 20 0~300meV. Rigorously speaking, the spacing of the levels decreases as the energy increases because of the sinusoidal shape, but this effect was found to be very small by a numerical analysis.

For the further optimization of the structure, modulated potential amplitude is calculated as a function of the carrier-supply-layer thickness for the both of the split-gate and present LSSL structures. The result is shown in **Fig.7-5**. The amplitude is

taken as the Fermi level just locates at $V_0/2$ from the bottom of the modulated potential. In order to make the modulated surface potential reflect on the 2DEG, the heterointerface should be close to the surface and the N_D should be high as possible. These may become more important when the period of the potential modulation is short. As shown in the figure, large N_D gives large potential modulation amplitude. However, the N_D is limited about $1\sim3\text{x}10^{18}\text{cm}^{-3}$ in the case of $Al_{0.3}Ga_{0.7}As$. In the case of the split-gate structure, the amplitude decreases by the decrease of the carrier supply layer thickness. Since the Fermi level position cannot be controlled by the gate voltage, the Fermi energy decreases when the heterointerface closes to the surface. On the other hand, in the case of the present structure, the potential amplitude increases by the decrease of the carrier-supply-layer thickness because the Fermi energy can be controlled by the gate bias. And, when the carrier supply layer becomes 300nm, the amplitude of the present structure becomes larger than that of split-gate structure.



(a)



(b)

Fig.7-4. (a) Calculated potential at heterointerface of the present LSSL structure as a function of V_G. (b) Calculated quantized energy ΔE as a function of SBH difference $\Delta\phi_B$ for different periodicity of the grating gate.

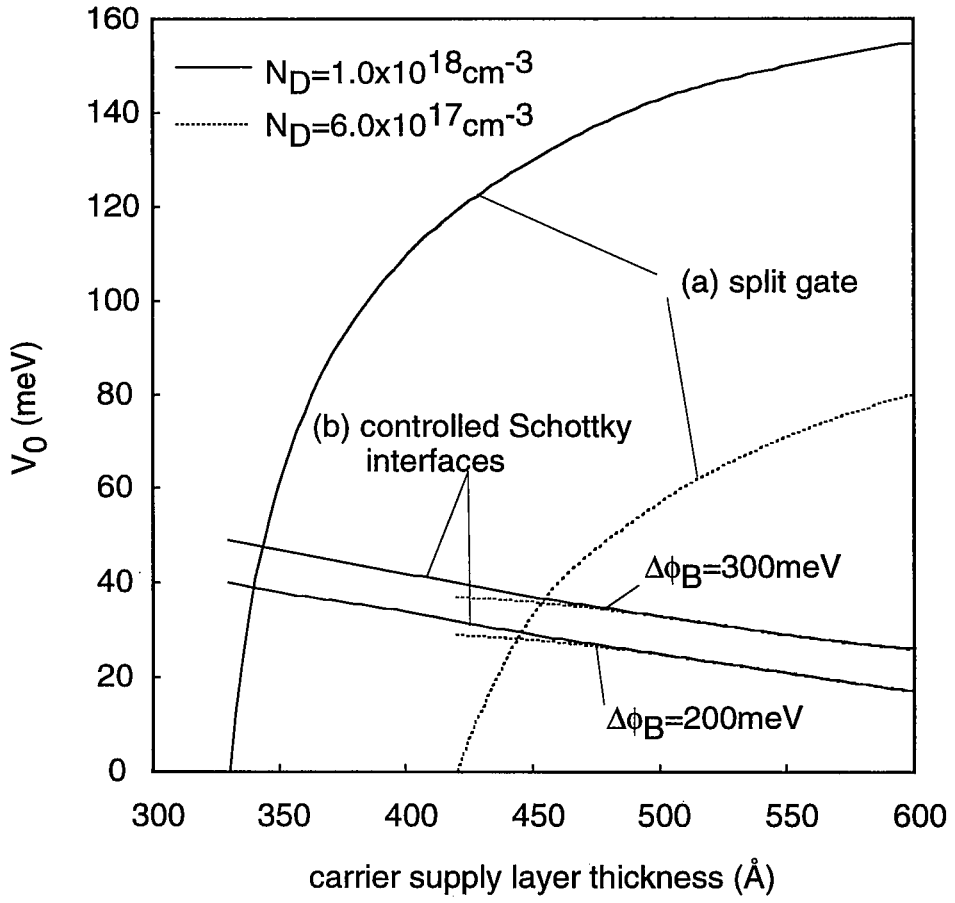


Fig.7-5. Modulated potential amplitude as a function of the carrier-supply-layer thickness of LSSL devices realized by Schottky-split gates and controlled Schottky interfaces.

7.4. Fabrication of present LSSL

The fabrication process of the LSSL device consisted of five major steps.

(1) Molecular beam epitaxy (MBE) growth of $Al_{0.3}Ga_{0.7}As$/GaAs heterostructure wafer

(2) MBE growth of Si ICL and formation of Al Schottky barrier

(3) Formation of an H-shaped mesa island by chemical etching

(4) Formation of source and drain ohmic contacts

(5) Formation of the grating gate

Figures 7-6 show the sequence of the formation of the grating gate. First, the initial structure for fabrication of the LSSL shown in **Fig.7-6(a)** was grown by steps (1) and (2), using an ultrahigh-vacuum (UHV)-based system including an MBE chamber and a metal deposition chamber connected to an UHV transfer chamber. The Si-doped ($1x10^{18}cm^{-3}$) n^+-AlGaAs layer had a thickness of 50nm. The As-doped Si ICL grown by MBE at the substrate temperature of 250°C. The Si ICL had a thickness of t_{ICL}=2nm and with estimated donor-dopant concentration of $3x10^{20}cm^{-3}$. As doping was done by irradiation of As flux during growth of the Si ICL. The film of Al metal layer was deposited to a thickness of 40nm in UHV on the Si ICL without exposing the sample to the air.

After formation of the starting structure described above, the sample was taken out from the UHV chamber and steps (3) and (4) were carried out. Ni/Ge/Au ohmic electrodes were formed as the source and drain. Then, in the final step (5) of grating gate formation, the Al film and Si ICL were periodically removed by electron beam lithography and wet chemical etching, as shown in **Fig.7-6(b)**. As the positive-type EB resist, OEBR1000 (Tokyo oka) was used. The resist was diluted by OFPR thinner, resist:thinner=3:1~2:1. For Al etching, the sample was immersed in the solution of $HCl:H_3PO_4$=1:20 or Shipley Microposit 2401 developer:H_2O=1:5 about one minute.

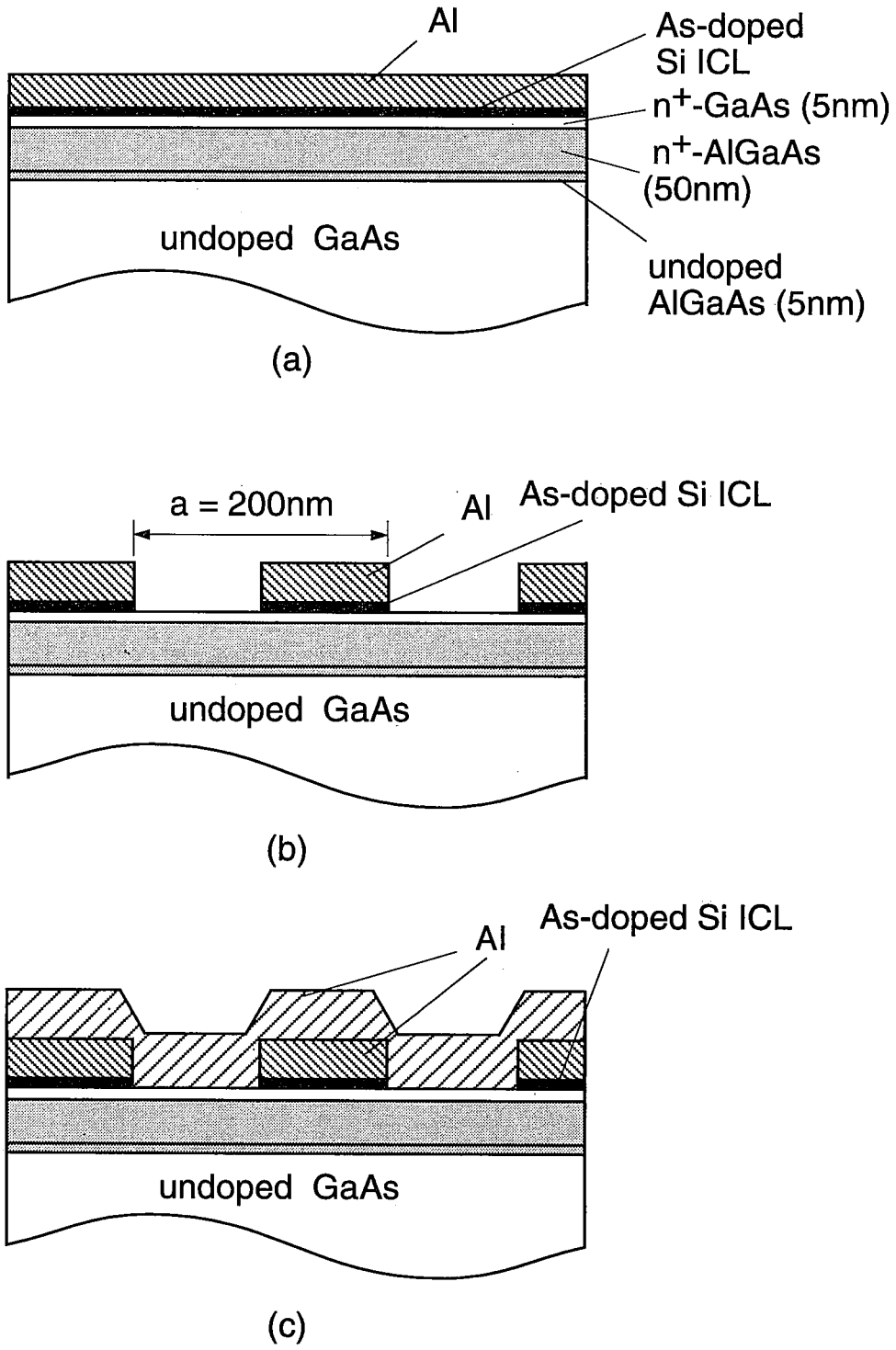


Fig.7-6. Fabrication process of the LSSL device.

Then, the second Al metal layer was deposited over the whole wafer, as shown in **Fig.7-6(c)**. Finally, the gate electrode pattern was defined by photolithography and wet etching.

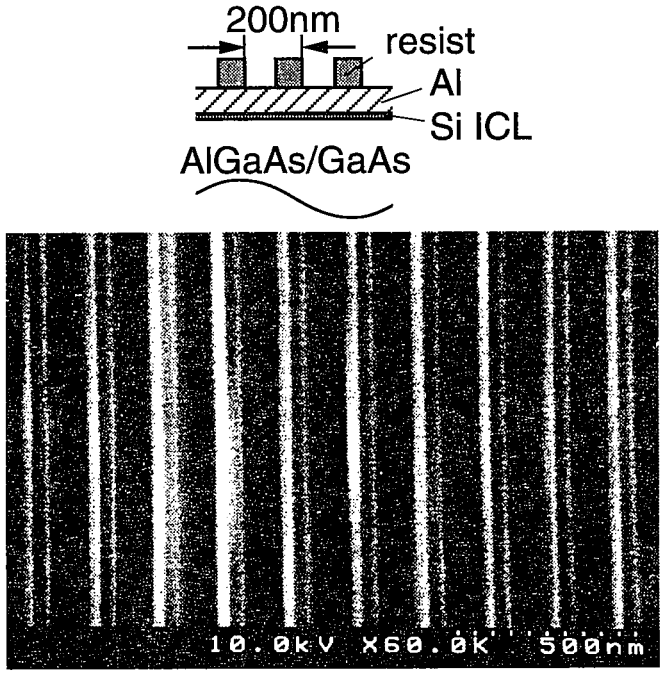
Four samples, A, B, C and D, having the same nominal structure and dimensions were fabricated and characterized. The period a of the grating gate was chosen to be 200nm. Macroscopic gate dimensions were L_g=14μm and W_g=54μm. Sample A was used for destructive SEM/EBIC study and samples B, C and D were used for electrical characterization.

7.5. Characterization of present LSSL

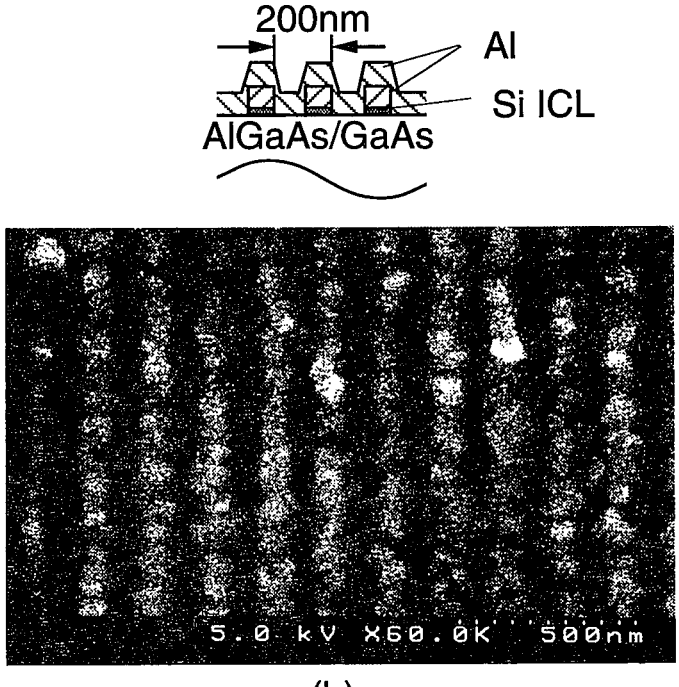
7.5.1 *SEM/EBIC study*

The plan-view SEM images of the grating gate are shown in **Fig.7-7** for the electron-beam resist pattern (a) before etching of the first Al layer, and (b) after deposition of the second Al layer. The entire surface is covered by Al in **Fig.7-7(b)**, but the periodicity of 200nm can still be recognized. Here, bright and dark regions correspond to the region of Al Schottky contact with Si ICL and the region of direct Al Schottky contact without Si ICL, respectively.

Figures 7-8(a) and **7-8(b)** show the cross-sectional SEM and EBIC images under the grating gate region of sample A. The corresponding schematic illustration of the EBIC image is also shown. In the EBIC measurement, an electron beam was irradiated on the cleaved surface of sample A, and the generated carriers were detected as a current in an external circuit.[18] This measurement was found to be extremely powerful for the investigation of the potential in nanometer-scale structures.[19,20] The detail of the EBIC measurement will be seen in **chapter 8**. In the EBIC system used in this work, the lateral resolution was estimated to be about 50nm

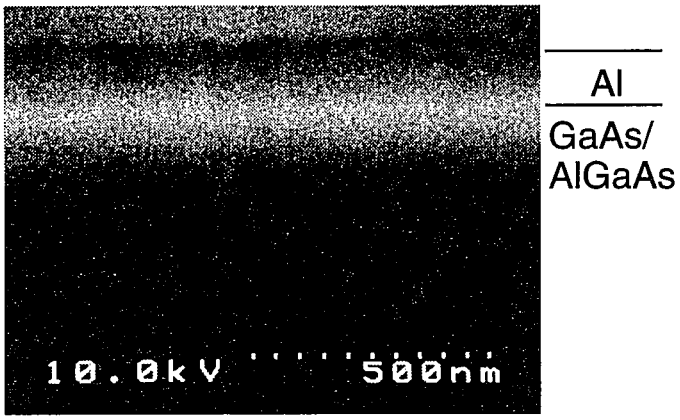


(a)

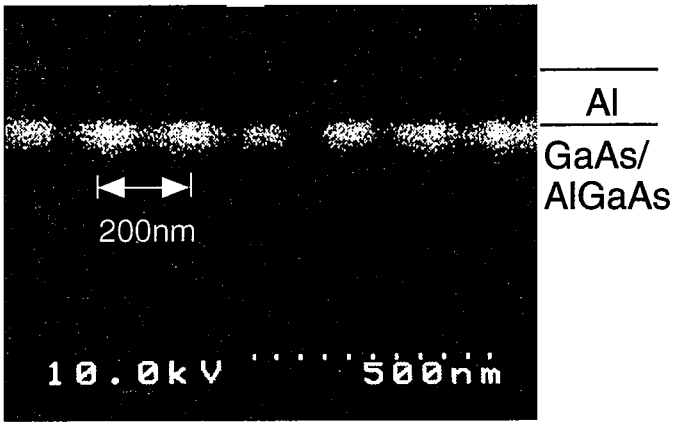


(b)

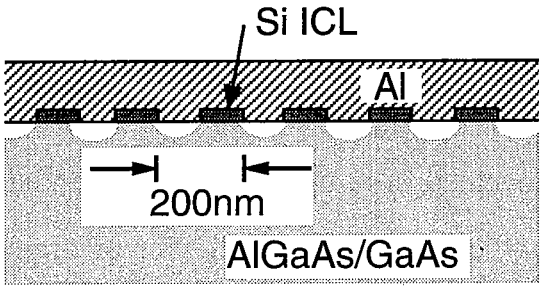
Fig.7-7. SEM images of (a) resist pattern for the grating gate and (b) grating Schottky gate after the final metallization.



(a)



(b)



(c)

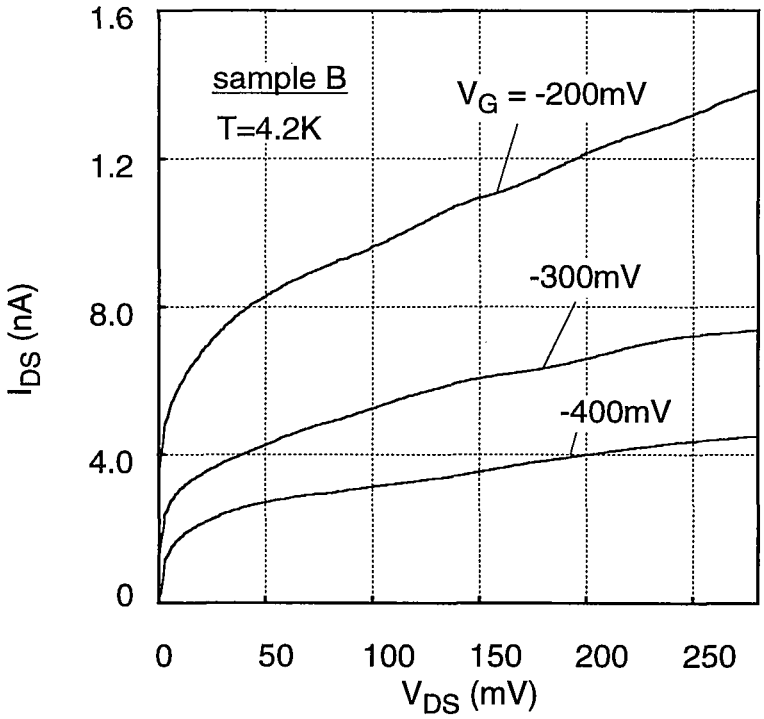
Fig.7-8. Cross-sectional (a) SEM and (b) EBIC iamges of the LSSL structure (sample A). (c) Schematical image of the EBIC image.

at the electron beam energy of 10kV. Thus, if there were any potential modulation in the present sample, it should be detectable.[18)]

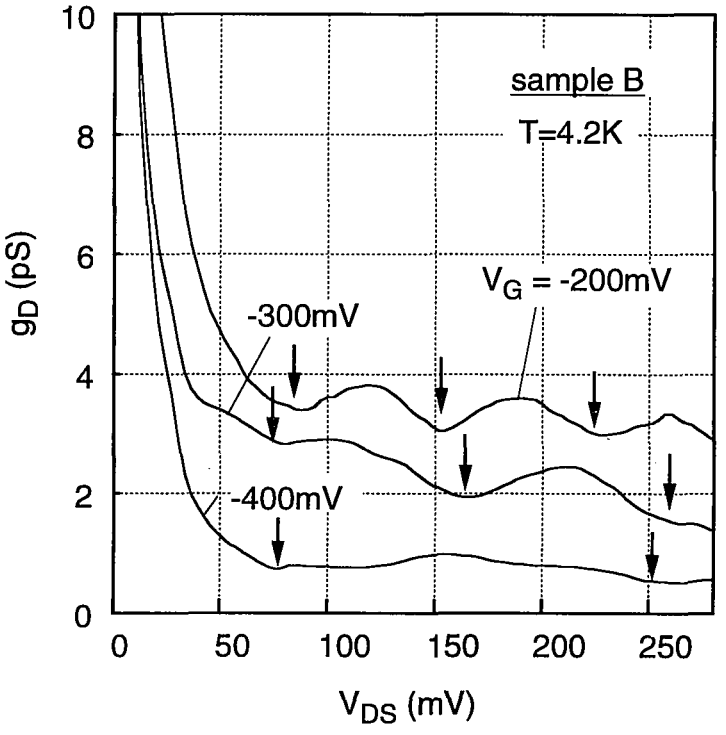
As shown in **Fig.7-8(b)**, the EBIC image exhibited a clear periodic pattern. The periodic pattern had the same periodicity as the fabricated grating structure, whereas no such pattern was observed in the SEM image in **Fig.7-8(a)**. The periodic-signal pattern was located in the M-S interface region, and it was confirmed that the dark and bright regions in the image correspond to the M-S interfaces with and without As-doped Si ICL, respectively. Since brighter regions correspond to regions with stronger electric fields, the observed EBIC image indicates that the M-S interface region without doped Si ICL should possess higher fields than those with Si ICL. Thus, the EBIC study directly confirmed that periodic variation of electrostatic potential on the nanometer scale could be produced at the M-S interface by using doped Si ICL stripes only 2nm thick.

7.5.2 *Drain conductance oscillation*

The fabricated LSSL devices showed reasonably good field-effect performance on a macroscopic scale, as shown by the drain current-drain voltage (I_{DS}-V_{DS}) characteristics of sample B shown in **Fig.7-9(a)**. Here, V_G denotes the gate-to-source voltage. However, periodic of dips are also recognized in the figure. The presence of dips is more clearly revealed in terms of the drain conductance g_D ($=\partial I_{DS}/\partial V_{DS}$), as shown in **Fig.7-9(b)** where oscillatory behavior of drain conductance is observed with the increase of V_{DS}. The period is of the order of 100meV, but its values change greatly with V_G. Similar drain conductance oscillation was also observed in samples C and D.

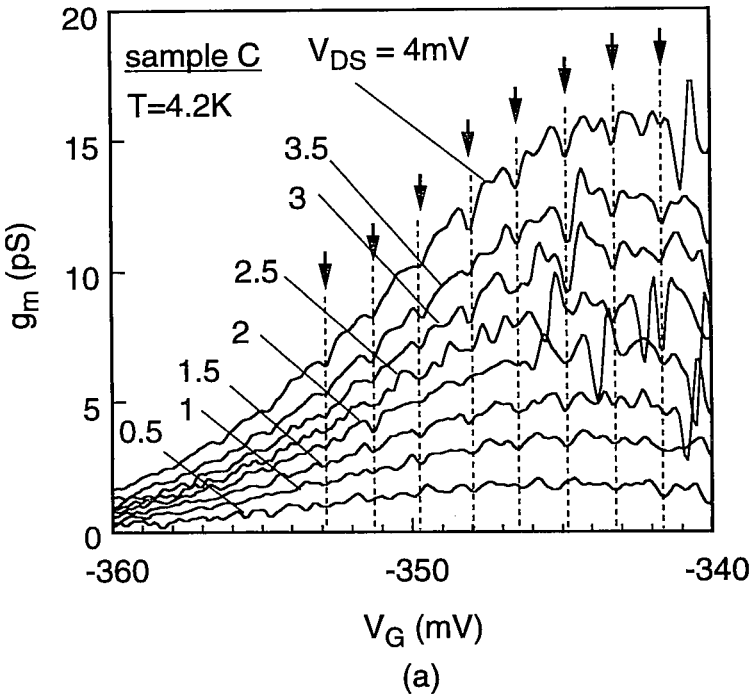


(a)

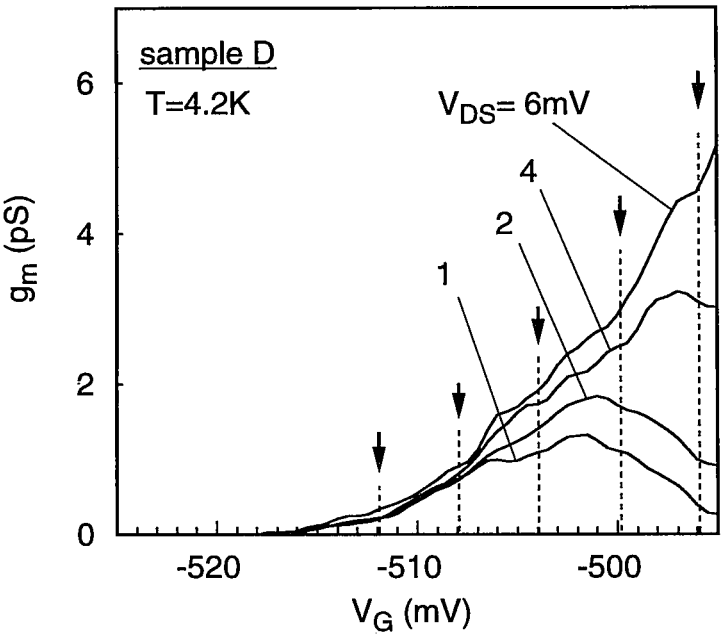


(b)

Fig.7-9. (a) Drain I-V characteristics and (b) drain conductance of sample B.



(a)



(b)

Fig.7-10. Transconductance characteristics of (a) sample C and (b) sample D.

7.5.3 *Transconductance oscillation*

Transconductance was measured under extremely small drain voltage V_{DS}, so that the effect of electric field in the direction of electron transport becomes negligible. **Figures 7-10(a)** and **7-10(b)** show the measured gate-voltage dependence of transconductance g_m ($=\partial I_{DS}/\partial V_G$) near the threshold voltage (V_{th}) of the channel pinch off for samples C and D, respectively. The observed characteristics are complex, but, again periodic occurrence of dips can be clearly observed, as indicated by dashed lines in **Fig.7-10**. The periods of the dips were determined by Fourier transformation and found to be independent of the drain voltage V_{DS} in both samples. The periodicity was about 2meV and 4meV for samples C and D, respectively.

7.5.4 *Temperature dependence of transconductance*

Figures 7-11(a), **7-11(b)** and **7-11(c)** show the observed temperature dependence of the transconductance of sample D. In this measurement, relatively large values of V_{DS} were used, and this resulted in more complex patterns than those for low V_{DS}. As seen in **Fig.7-11(a)**, at 2.5K, transconductance oscillation is clearly observed. At 10K, the shape of the oscillation pattern remained more or less the same, but the oscillation amplitude became smaller. The oscillation completely vanished at 77K. This temperature dependence suggests that the observed transconductance oscillation is due to quantum effects.

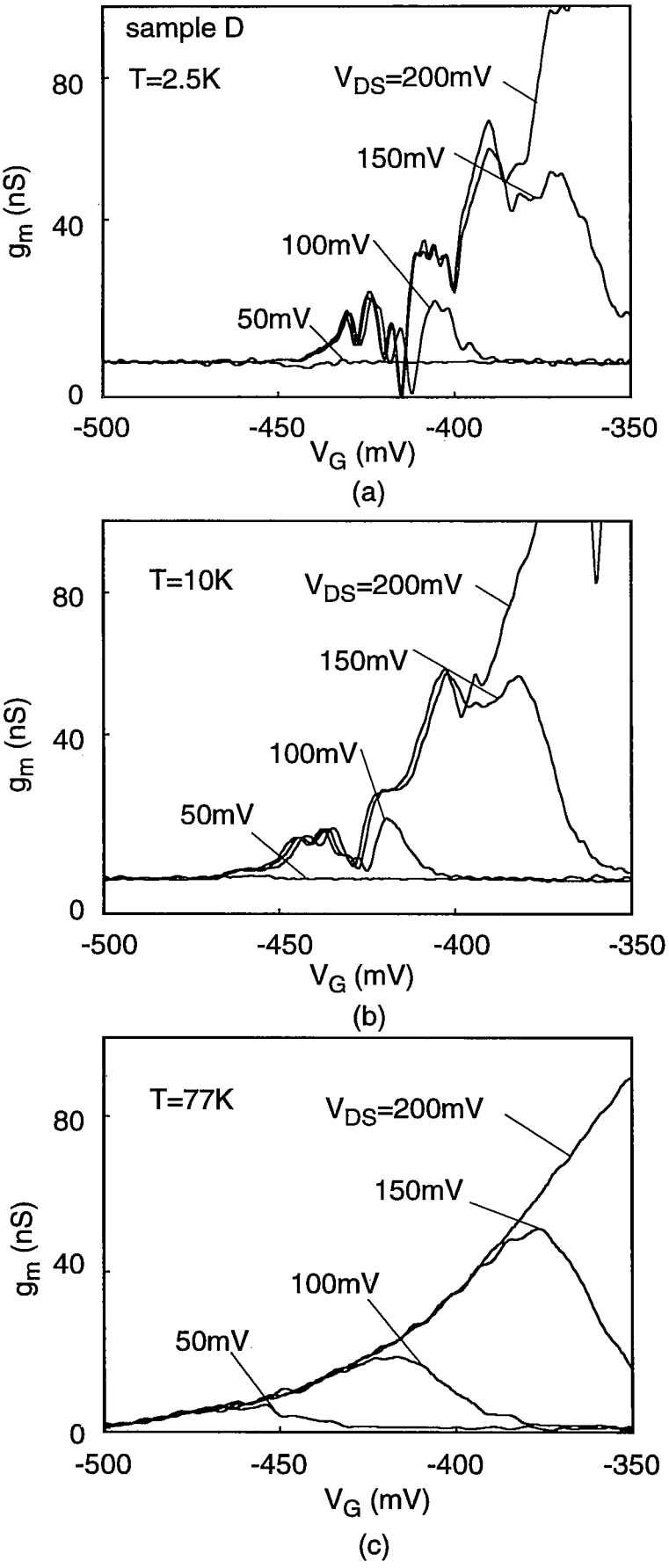


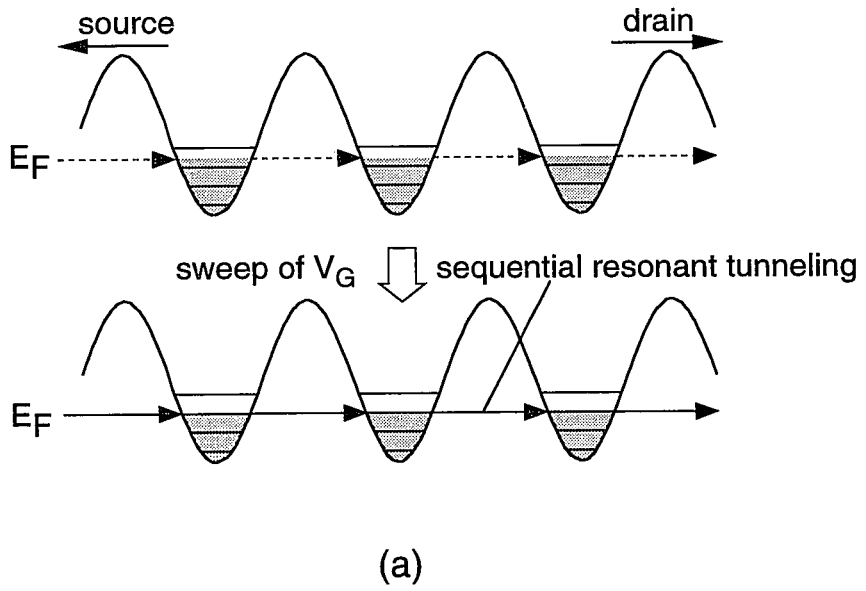
Fig.7-11. Temperature dependence of the transconductance oscillation of sample D.

7.6 Discussion

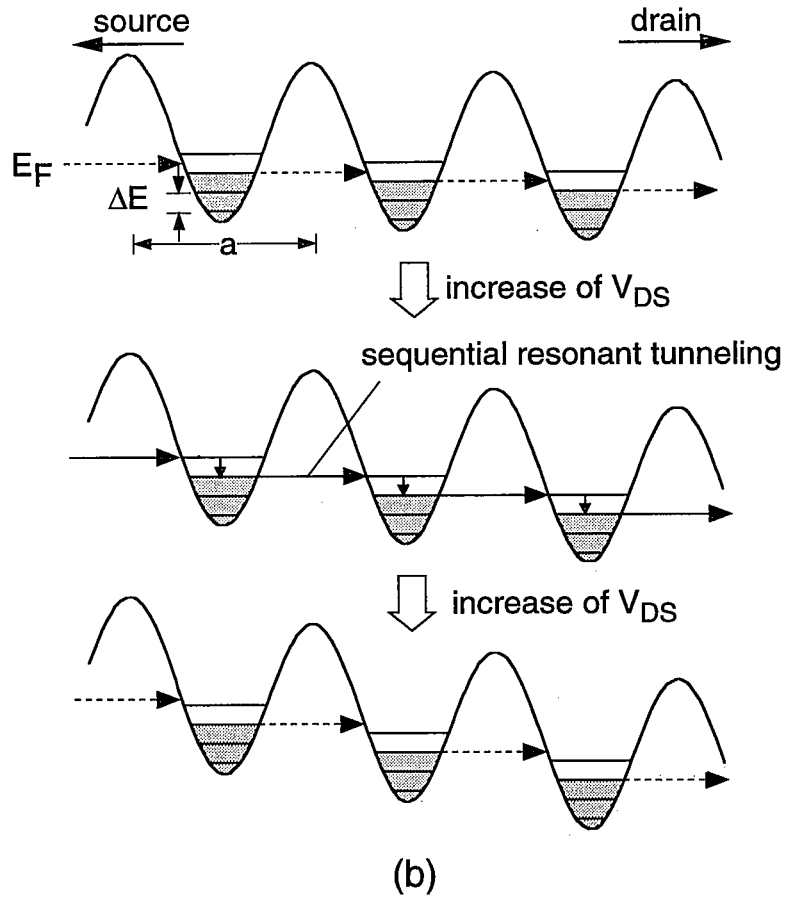
The fabricated novel LSSL devices consistently showed oscillatory behavior in their drain conductance and transconductance at low temperatures up to 10K. The origin of the two kinds of oscillatory behavior can be explained in terms of the sequential resonant tunneling model shown in **Fig.7-12**, which was suggested previously for split-gate LSSL devices.[4] The periodic variation of the potential results in the formation of multiple quantized levels, as shown in **Fig.7-12**, with the possible formation of narrow minibands. Since the period of the potential in the present device is longer than the Fermi wavelength and the scattering length, most of the current flows either by inelastic tunneling or thermal excitation process. However, it is assumed that some electrons do not lose phase information and are transported by the sequential resonant tunneling process.

Transconductance oscillation can be explained as follows according to **Fig.7-12(a)**. Since V_{DS} is sufficiently low in the I_{DS}-V_G measurement, the position of each quantized level in neighboring wells aligns horizontally. The Fermi level (E_F) also aligns horizontally and its position is controlled by V_G. Sweeping V_G, sequential tunneling takes place only when E_F agrees with one of the quantized levels with possible small broadenings. If such a condition is not met, the resonant tunneling cannot occur and the current is deduced, which produces a dip. Thus the conductance changes periodically due to sweeping V_G, resulting in the transconductance oscillation.

The drain conductance oscillation can be explained as shown in **Fig.7-12(b)**. Since measurements are performed under high V_{DS} condition, a quantized level in one well may align with an other quantized level in neighboring wells. Sequential resonant tunneling takes place with energy loss when the energy loss is equal to the energy difference between any two quantized levels. Thus, drain conductance



(a)



(b)

Fig.7-12. Sequential resonant tunneling model for the observed (a) transconductance and (b) drain conductance oscillation.

oscillation can be observed upon sweeping the source drain voltage.

On the basis of the above qualitative explanation, a more quantitative discussion can be given. A noteworthy feature of the observed transconductance oscillation in **Figs.7-10(a)** and **7-10(b)**, is the occurrence of regular periodic oscillation with a small gate voltage period of 2~4mV. In contrast, previous split-gate LSSL devices show more nonuniform gate voltages with larger periods about 8~15mV for the same value of a=200nm.[4] This difference can be understood in terms of the difference in the E_F-V_G relationship discussed earlier in **§7.3.2**. As compared with the split-gate device, E_F-E_{Cmin} of the present device changes more rapidly with V_G, and the relationship becomes remarkably linear near the pinch-off, as seen in **Fig.7-5(a)**. Thus, the regular occurrence of dips in **Figs.7-10(a)** and **7-10(b)** can be understood in terms of the linear sweeping of the Fermi level though equally spaced quantized levels. Then, using

$$\Delta E = \left(\frac{\partial E_F}{\partial V_G}\right)\Delta V_{G\,dip}, \tag{7.8}$$

where ΔV_{Gdip} is the gate voltage period of g_m dip, and the values of $(\partial E_F/\partial V_G)_{near\ pinch\text{-}off}\approx 0.7$, one can obtain the estimated values of ΔE shown in **Table 7-1** from the observed values of ΔV_{Gdip}.

In the case of drain conductance oscillation, ΔE should satisfy the following relation, on the basis of the model in **Fig.7-12(b)**.

$$\Delta E \sim q\Delta V_{DSdip} \cdot a / L_g = q\Delta V_{DSdip} / \text{finger} \tag{7.9}$$

ΔV_{DSdip} is the period of the drain conductance oscillation. Here, it is assumed that the electric field under the gate is uniform. Since the drain conductance oscillation was

observed in the saturation region, there is a possibility that ΔE may be overestimated due to concentrated electric field near the drain region. However, since ΔE in this study was estimated from the drain conductance by using the I-V curves near the drain current pinch-off, where the channel under the gate is almost uniform, such a concentration of electric field near the drain does not seem to be large. According to **Fig.7-9(a)**, the observed periodicity ΔV_{DSdip} of the oscillation decreased rapidly with increasing the gate voltage. Such a large change of periodicity with gate bias has not been observed to date in split-gate devices.[4,5] This difference can also be explained by the difference in the gate control characteristic. As seen in **Figs.7-4** and **7-5(a)**, the potential is more sensitively changed by V_G in the present device than in the split-gate device. The amplitude of the potential modulation, V_0, at the heterointerface changes more rapidly with increase of V_G in the present device. Reduction of V_0 reduces ΔE, which in tern reduces V_{DSdip}, according to **eq.(7.9)**. For comparison with the value of ΔE obtained from transconductance oscillation, ΔE was estimated from the drain conductance oscillation near pinch-off using **eq.(7.9)**. The result is given in **Table 7-1**. The difference in the SBHs ($\Delta\phi_B$) estimated from the values of ΔE using **Fig.7-4(b)** is also included in **Table 7-1**. Agreement between the two values of ΔE is good, confirming the interpretation given here. On the other hand, further work is necessary to understand the detailed complex patterns and the amplitudes of transconductance oscillation. Such work may reveal detailed features of quantum transport including the density of states in minibands. The remarkable linear E_F-V_G relationship of the present device suggests that it may be used as a spectrometer for quantum transport in LSSL devices. Such application is difficult for the split-gate structure because the highly nonlinear and complex relationship between ΔE, the Fermi level position and V_G.[21]

In terms of the SBH control capability achieved by Si ICL stripes, the value of $\Delta\phi_B$ is estimated to be $\Delta\phi_B$=70~150meV, as shown in **Table 7-1**. These values are

Table 7-1. Estimated ΔE from the transconductance and drainconductance oscillatioons and estimated $\Delta\phi_B$

	g_m oscillation		g_D oscillation		estimated
	ΔV_G	ΔE	ΔV_{DS}	ΔV_{DS}/finger	$\Delta\phi_B$
sample B	–	–	175meV	2.5meV	120meV
sample C	2meV	1.4meV	140meV	2.0meV	80meV
sample D	4meV	2.8meV	200meV	2.8meV	150meV

consistent with the clear contrast in the EBIC image shown in **Fig.7-8(b)**. The estimated value of $\Delta\phi_B$ is somewhat smaller than the expected value of $\Delta\phi_B$=200meV, but not unreasonable because it can be greatly affected by the details of Si ICL processing and metal deposition.

7.7 Conclusions

A novel LSSL device structure based on Schottky barrier height (SBH) control using Si interface control layers (Si ICL) was proposed and fabricated. The main conclusions are as below.

(1) Basic design considerations were determined by 2D computer simulation of potential.

(2) The appearance of a periodic EBIC signal directly confirmed SBH modulation by Si ICL stripes.

(3) Marked periodic oscillations of drain conductance and transconductance were observed at low temperatures up to 10K. Their detailed behavior was distinctly different from that of previous split-gate devices.

(4) The mechanism of these oscillations can be explained by the sequential resonant tunneling model. A quantitative analysis of the data indicated that SBH difference of 70~150meV was produced, which resulted in quantized levels with a separation of 2~3meV at the heterointerface.

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Chapter 8

Formation and Characterization of Quantum Nanostructures Utilizing III-V Compound Semiconductor Schottky In-Plane Gate and Wrap Gate

8.1 Introduction

The key issue concerning realization of next-generation quantum devices including quantum wave devices and single electron devices is how to fabricate defect-free quantum nanostructures. A standard practical nanolithography approach to form semiconductor nanostructures is combination of the electron beam (EB) lithography and dry etching. However, disadvantages of this approach are that the sizes of the nanostructures are usually not small enough, that the structure boundaries become very rugged in atomic scale and that the processing introduces damages into the nanostructures.

A known alternative approach to overcome above disadvantages of the standard fabrication technique is the split-gate technique. In this technique, quantum structures are formed by modulating potential of two dimensional electron gas (2DEG) at AlGaAs/GaAs heterointerface with planar Schottky split-gate patterns defined by standard EB lithography and metal-lift-off process. Damages are expected to be smaller since the structure are far away from the surface. Potential fluctuations at the lithographically defined rugged surface are smoothened by the long-range-isotropic nature of Coulomb force. However, the electron confinement obtainable by the split gate structure is extremely weak, and the quantum wire and single electron devices produced by this technique operate only in mK range.

To overcome this difficulty of the split-gate technique, novel quantum nanostructures based on potential modulation of 2DEG by Schottky in-plane gates (IPGs) is porposed.[1-5] This structure contains that Schottky gate contacts directly to

2DEG edge and directly control the potential in heterointerface, therefore abrupt and strong electron confinement potential can be realized. For formation of IPG with nanometer dimension, several techniques including high resistance gate by FIB irradiation and air gap gates are proposed.[6,7] Our group proposed Schottky in-plane-gate utilizing in-situ electrochemical process.[1-5] This process attract us due to the selectivity of metalization[3,8] and high Schottky barrier formation.[9] Metal plating by in-situ electrochemical process is carried out where the current is supplied. Therefore, Schottky In-plane-gate structure which contacts only to the side of channel where 2DEG locates can be conveniently obtained by in-situ electrochemical process.

For successful design and realization of such novel nanostructures utilizing Schottky IPGs and WPGs, a development of a suitable structural characterization technique is obviously desirable, since the depletion layer edges defining the quantum structure boundaries are buried in the structure and no directly visible by standard SEM observation.

In this chapter, attempt is made to characterize Schottky IPG and WPG-based GaAs quantum nanostructures by the electron beam induced current (EBIC) technique. A simple theory on EBIC signal from the basic Schottky/2DEG diode is developed and compared with experiments. The results indicate that the EBIC technique is a powerful means to detect electric field profiles in the buried depletion layers Then, the EBIC technique is applied to various Schottky IPG and WPG-based quantum nanostructures, including quantum wires, lateral superlattices and multi-quantum-dot chains, directly confirming successful formation of intended structures.

8.2 Principle and Basic design of IPG and WPG for quantum nanostructures

In the novel IPG structure, Schottky gates are formed on side edges of 2DEG as shown in **Fig.8-1(a)**. Strong lateral electric fields produced by the Schottky IPG push electrons in the direction parallel to 2DEG in the present structure which realizes strong confinement of electrons necessary for high temperature operation of quantum

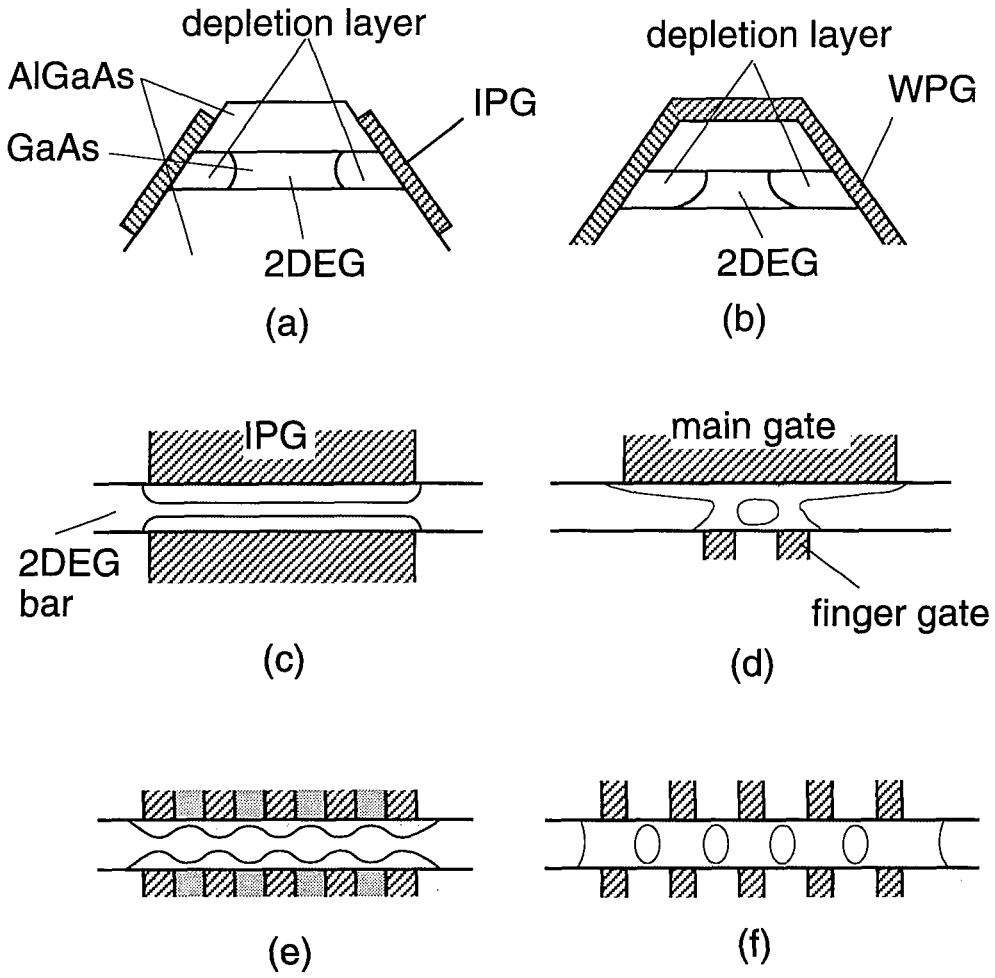


Fig.8-1. Novel Schottky (a) IPG and (b) WPG structures and possible quantum effect devices by IPG and WPGs, (c) quantum wire (QWR), (d) single-electron transistor, (e) lateral superlattice and (f) multiple-quantum dot chain.

seffect devices. A slightly modified cross structure, wrap gate (WPG) in **Fig.8-1(b)** is also obviously possible and may be more useful in some applications for devices. This technique can be used for formation of quantum wires, lateral superlattices and single and multi quantum dots whose sizes are voltage tunable as shown in **Figs.8-1(c)-8-1(f)**.

8.3 Analysis of IPG structures

8.3.1 Analytical model for Schottky IPG structure

Since a rigorous analysis of the complicated device structure in **Fig.8-1** requires a detailed three-dimensional potential analysis, only the basic Schottky IPG/2DEG diode is treated quantitatively here in order to compare with experiments. A simple model for the Schottky IPG structure used here is shown in **Fig.8-2(a)**, where a perpendicular IPG is formed at the edge of 2DEG. It is also assumed that the carrier supply layer to 2DEG is a δ-doped layer with a zero spacer thickness for simplicity. Then the longitudinal electric field distribution $E(x)$ along the x-axis and the depletion width $W_{dep}(V)$ of the basic Schottky IPG diode can be approximately described analytically by the following **eqs. (8.1a)** and **(8.1b)**, respectively.[11]

$$E(x) = -\frac{qn_S}{2\varepsilon_0\varepsilon_S} \ln\left(\frac{W_{dep} + \sqrt{W_{dep}^2 - x^2}}{W_{dep} - \sqrt{W_{dep}^2 - x^2}}\right) \tag{8.1a}$$

$$W_{dep}(V) = \frac{2\varepsilon_0\varepsilon_S(V_{bi} - V)}{qn_S} \tag{8.1b}$$

where n_s is the sheet carrier concentration of 2DEG, V is the gate voltage and V_{bi} is the built-in potential of the Schottky barrier. Then, the potential shape in x-direction is expressed as next equation.

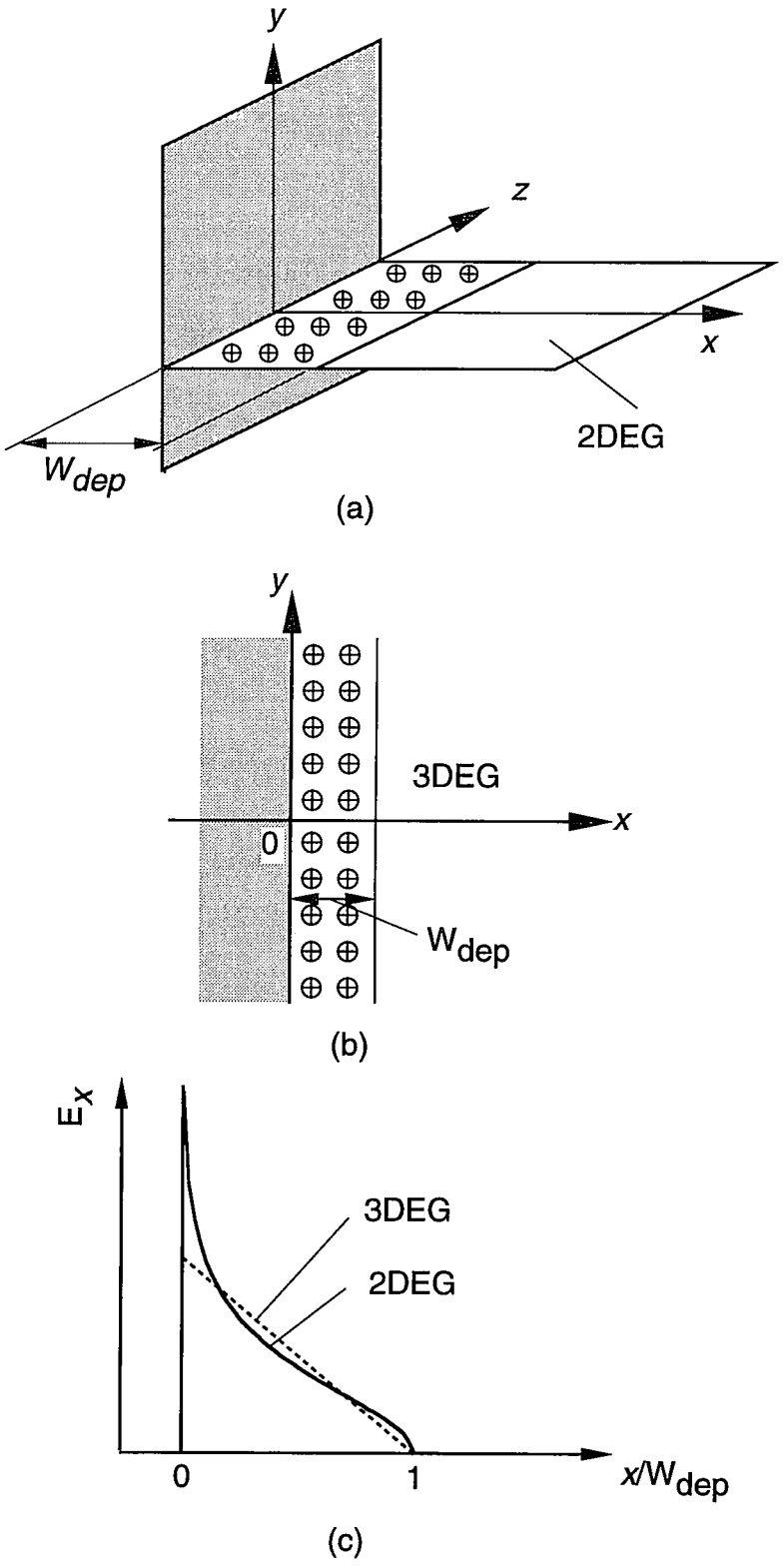


Fig.8-2. Simple model for (a) Schottky IPG to 2DEG, (b) planar Schottky contact on 3DEG and (c) field distributions of each contact.

$$V(x)=\frac{q\,n_S}{2\varepsilon_S}\left[x\ln\frac{W_{dep}+\left(W_{dep}^2-x^2\right)}{W_{dep}-\left(W_{dep}^2-x^2\right)}+2\,W_{dep}\,sin^{-1}\left(\frac{x}{W_{dep}}\right)\right] \qquad (8.1c)$$

These equations are to be compared with the following equations for a conventional planar Schottky contact on the three-dimensional electron gas (3DEG) shown in **Fig.8-2(b)**.

$$E(x)=\frac{qN(W_{dep}(V)-x)}{2\varepsilon_0\varepsilon_S} \qquad (8.2a)$$

and

$$W_{dep}(V)=\sqrt{\frac{2\varepsilon_0\varepsilon_S(V_{bi}-V)}{qN}} \qquad (8.2b)$$

where N is the ionized impurity concentration. Some example of the calculated field distributions are shown both structures in **Fig.8-2(c)** for comparison. It should be noted that the field strength is significantly large for the Schottky IPG/2DEG structure with the same value of (V_{bi}-V) and the depletion width in the IPG structure is controlled linearly with gate voltage V in. the IPG structure.

8.3.2 Computer simulation

A rigorous analysis of the complicated device structures in **Fig.8-1** was done by detailed two- or three-dimensional potential analysis. 2 or 3 dimensional Poisson's equation was solved numerically using the difference method and the successive over relaxation (SOR) method.

First, the 2-dimensional potential simulation is performed on the basic IPG-diode structures. The sample structure is shown in **Fig.8-3(a)**. This structure is closer to the experimental one than that of the analytical model. The top surface of the structure is semiconductor-free-surface and its surface potential is assumed to be fixed at 0.7eV

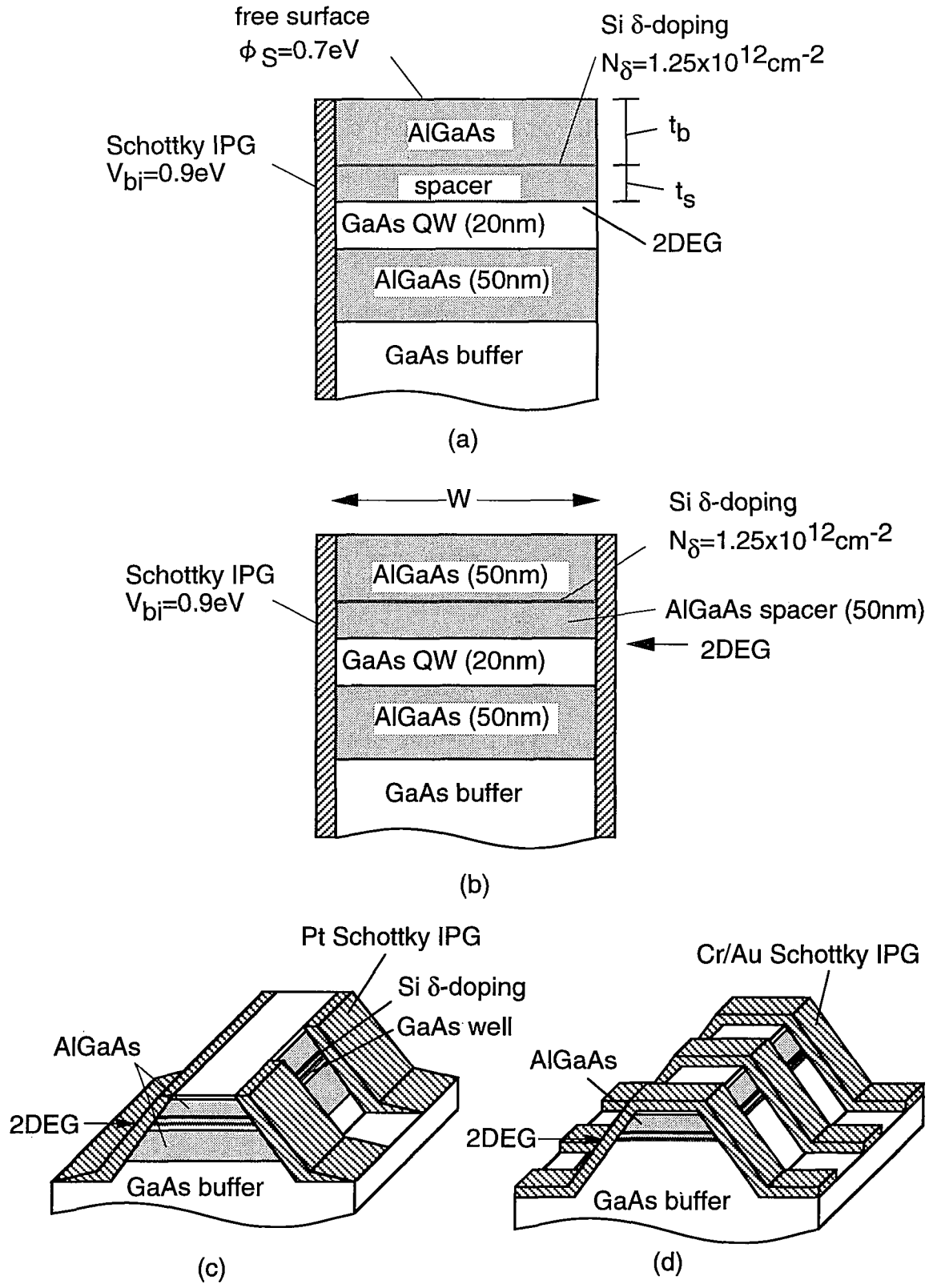


Fig.8-3. Sample structures for potential simulation. (a) Basic GaAs Schottky IPG structure. (b) GaAs IPG quantum wire (QWR). (c) GaAs IPG and (d) WPG single-dot SETs.

due to firm Fermi level pinning. The surface potential at the side-edge is the Schottky interface and it equals the Schottky barrier height of 0.9eV. The gate voltage is applied to this part. These values are conventional for GaAs. The side-edge of the structure is normal to the surface, then the shape of the structure is rectangle. 3-dimensional density of state (DOS) is applied to whole the structure, including the heterointerface. Calculation was done for structures having different AlGaAs-top barrier thickness and spacer thickness.

Figure 8-4(a) shows the simulated electric field distributions. Field distribution in the analytical model is also shown in this figure. When the AlGaAs top barrier is thin (50nm) and the spacer is thick (10nm), the field near the side-edge decays abruptly and the its tail in the edge of the depletion layer prolongs longer than that of the analytical model. However, when the structure is close to the analytical one, whose top barrier is thick and spacer is thin, the simulated field distribution well corresponds to that of the analytical model, because the effect of the surface potential on the top of the structure is reduced and the force lines from the top and the bottom of the structure balance with each other on 2DEG at the heterointerface. **Figure 8-4(b)** shows the calculated depletion-layer width as a function of the gate voltage. The depletion width changes linearly by the gate voltage as expected by the analytical model, even if the structure dimension is different. When the top barrier is thin, the depletion width at V_G=0 is wider than that of the other structures. This is due to the surface potential on the top surface reduces the carrier at the heterointerface and screens the force line from the IPG. Thus, reducing the effect of the surface potential on the top by the increase of the top-barrier thickness, the curve comes to corresponds to the curve of the analytical model.

8.3.3 Quantum nanostructures

Then, the potential simulation is applied to the quantum nanostructures by IPG/WPGs in order to get the idea for design of the devices. **Figure 8-5(a)** and **(b)** show the example of the cross-sectional potential at the heterointerface in the

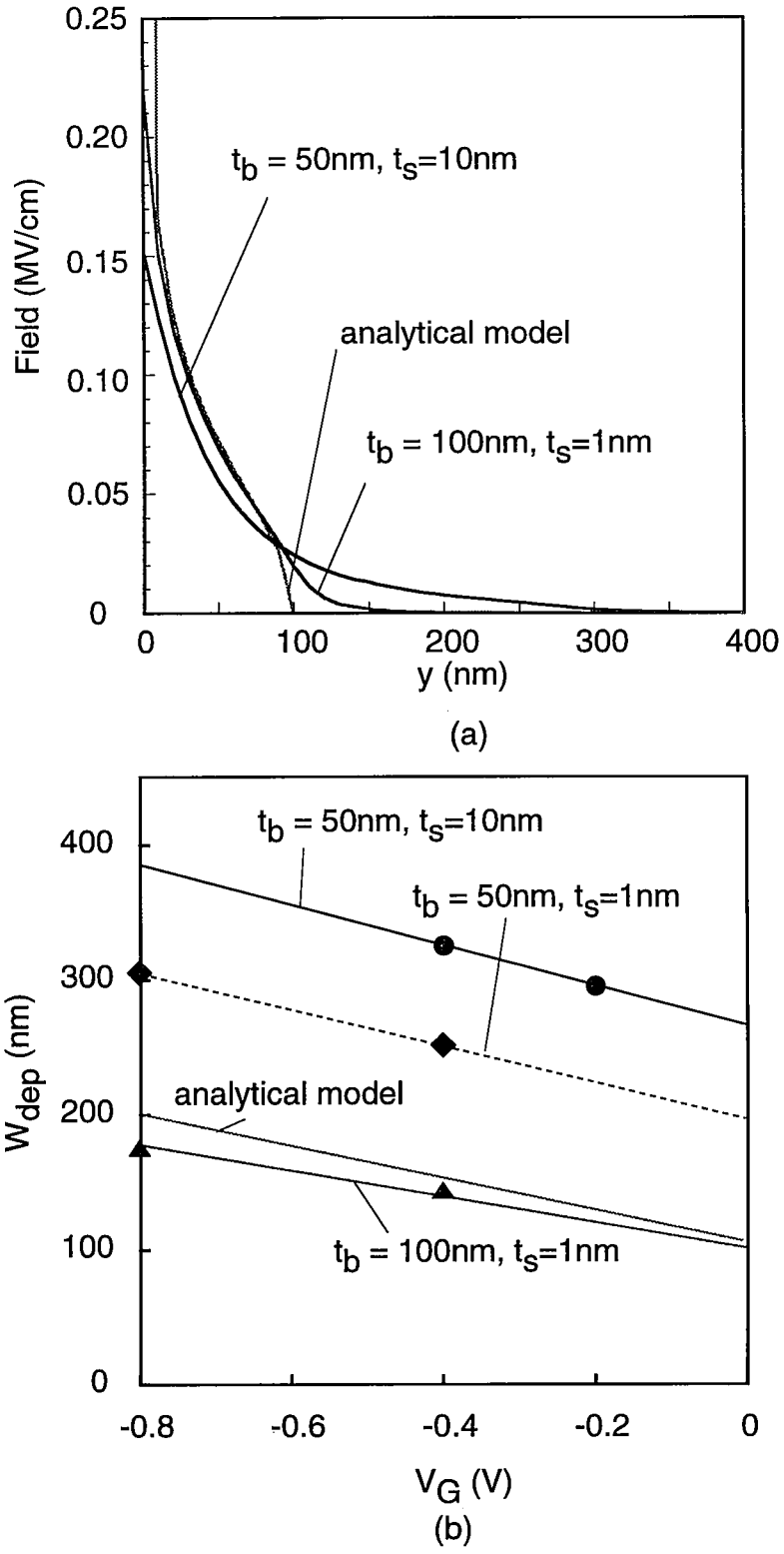


Fig.8-4. (a) Simulated field distributions and (b) depletion layer width as a function of gate voltage in basic Schottky IPG structures.

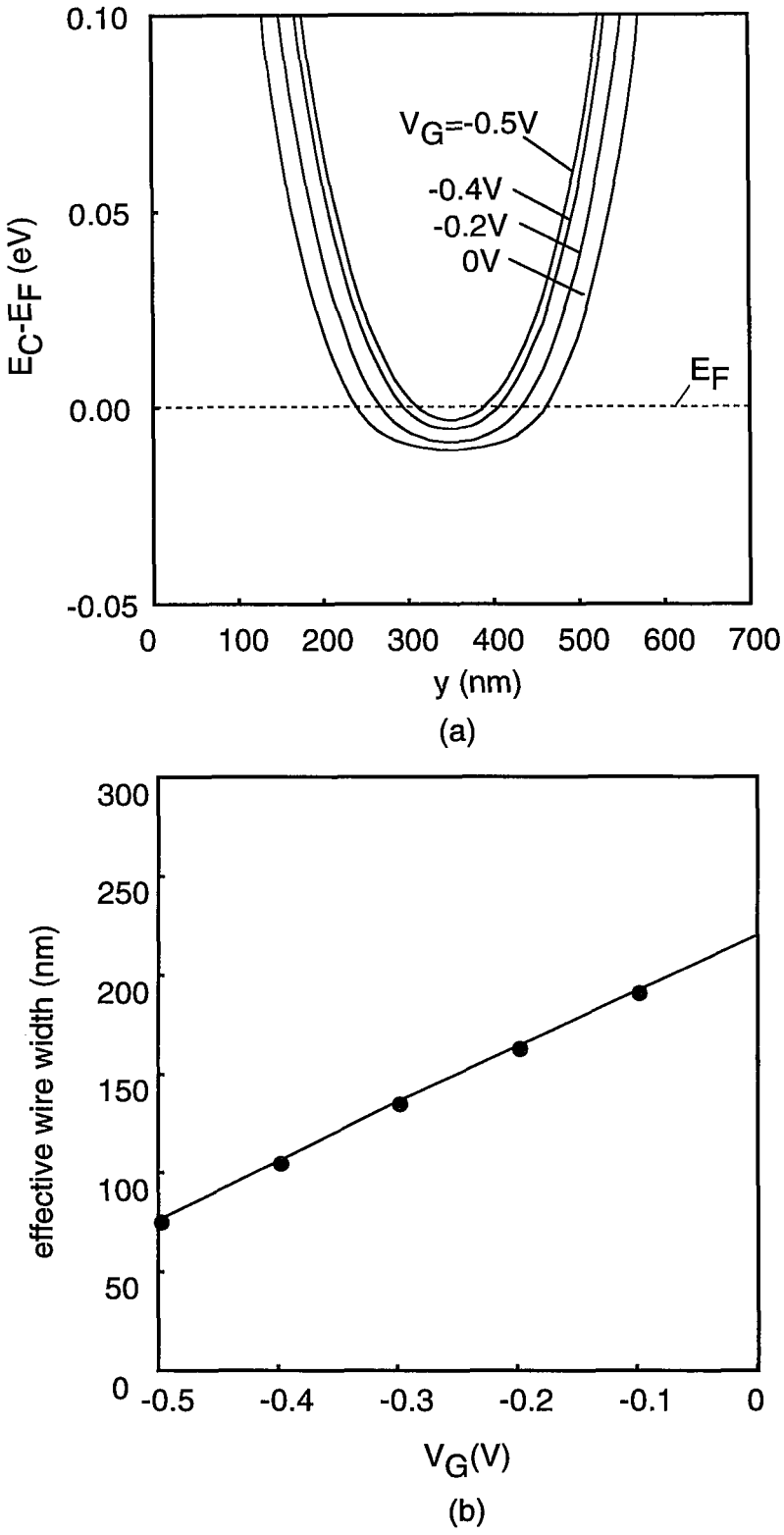


Fig.8-5. (a) Simulated potential at heterointerface and (b) the effective wire width as a function of gate voltage for a GaAs IPG quantum wire.

AlGaAs/GaAs IPG quantum wire as shown in **Fig.8-3(b)** and its effective wire width as a function of gate bias. The effective wire width is determined by the region that the conduction band edge is under the Fermi level. The wire width decreases linearly by the gate voltage and this change is two times of the change of the depletion width. The gate-controllability of the wire width is good and when the suitable voltage is applied to the gate, the wire becomes very narrow and is close to zero. The quantized-level spacing calculated numerically form the simulated potential shape is about 5~10meV. Concerning the change of the Fermi energy as a function of the gate voltage from the potential simulation, the quantized-conductance steps occur by 0.3~0.4V in the gate voltage, which well explains the experimental result described in **§8.6**.

Figure 8-6 and **8-7** compare the quantum-dot structures realized by Schottky IPG and WPG as shown in **Fig.8-3(c)** and **(d)**. Figure 8-6 shows the tunnel barrier shapes of these structures with same device dimensions. It is found that the quantum dot is formed by each structure. In the case of the IPG structure, tunnel barrier height changes slowly by the gate voltage. The dot is remained and electrons exit in the dot even if high gate voltage is applied. On the other hand, in the case of the WPG structures, the tunnel barrier shape is sharper than that of IPG structure and the change of the barrier height is sensitive to gate bias. This is because that the potential at the heterointerface is modulated not only from the side of the structure but also from the top surface. The top-surface potential also changes the carrier density of the heterointerface (n_s), and the potential modulation depth depends on the n_s. The combination of these two effects bring such a sharp and gate-voltage-sensitive tunnel barrier. **Figure 8-7** shows the simulated dot size and charging energy as a function of gate voltage of the IPG and WPG single-quantum-dot structures. The charging energy is estimated from the dot size. The dot size changes effectively by the gate bias in the IPG structure, since this structure has main gate as shown in **Fig.8-1(d)** which changes the transverse dot size. Thus, the charging energy becomes much larger than that of the WPG structure which does not have transverse-dot-size-control gate.

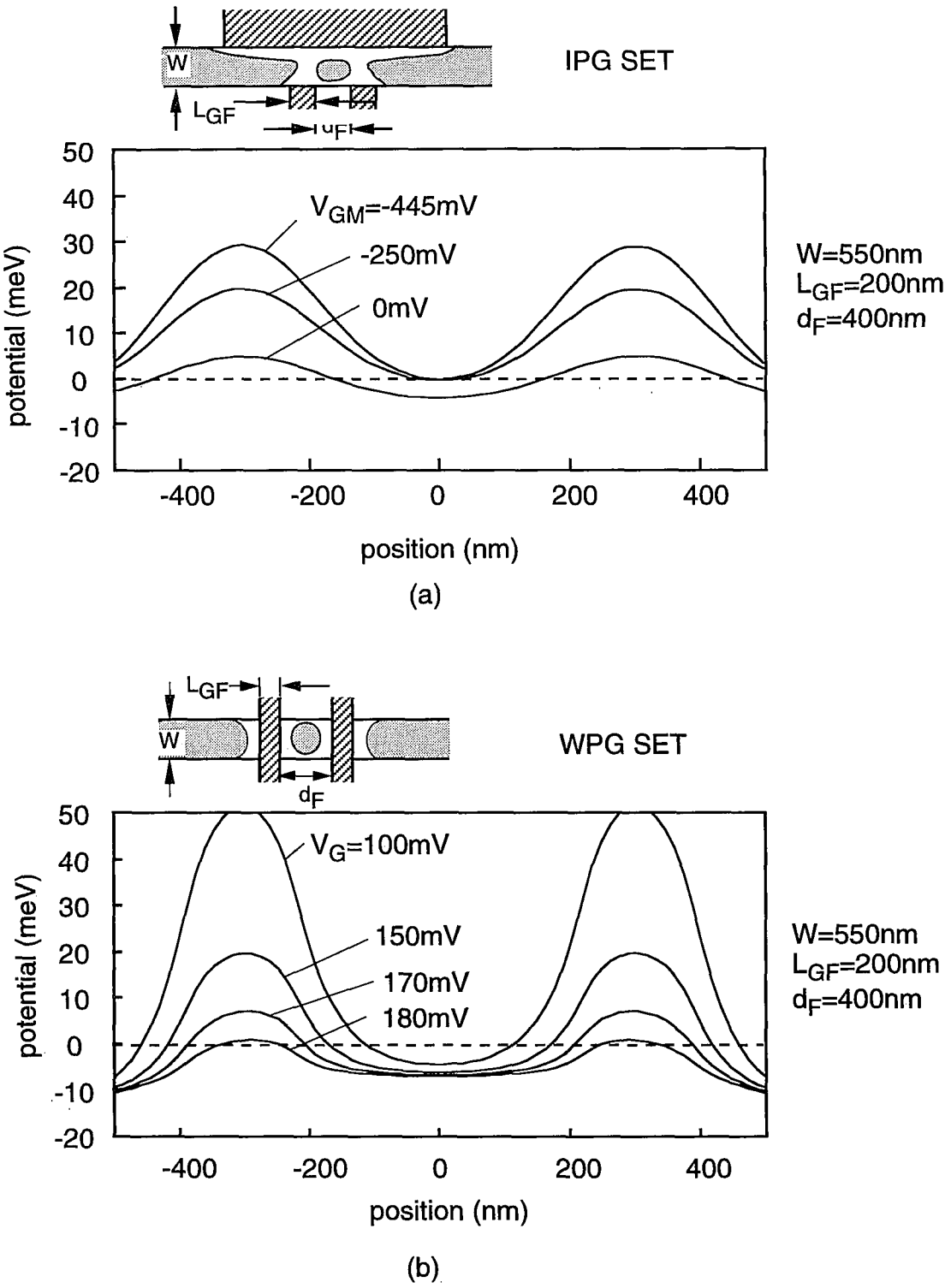


Fig.8-6. Simulated tunnel barrier shapes of (a) IPG single-dot SET and (b) WPG single-dot SET.

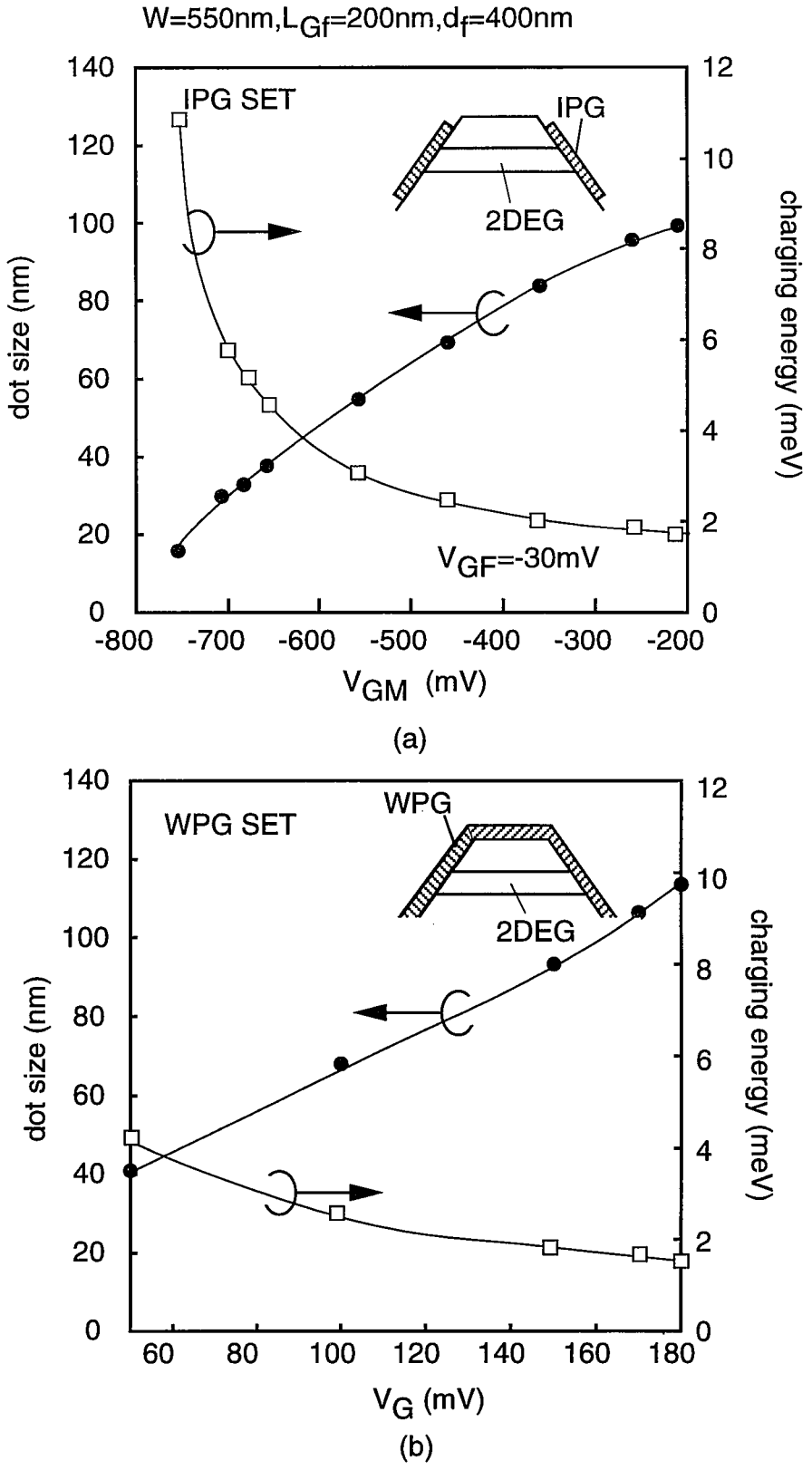


Fig.8-7. Simulated dot size and charging energy as a function of gate voltage for (a) IPG single-dot SET and (b) WPG single-dot SET.

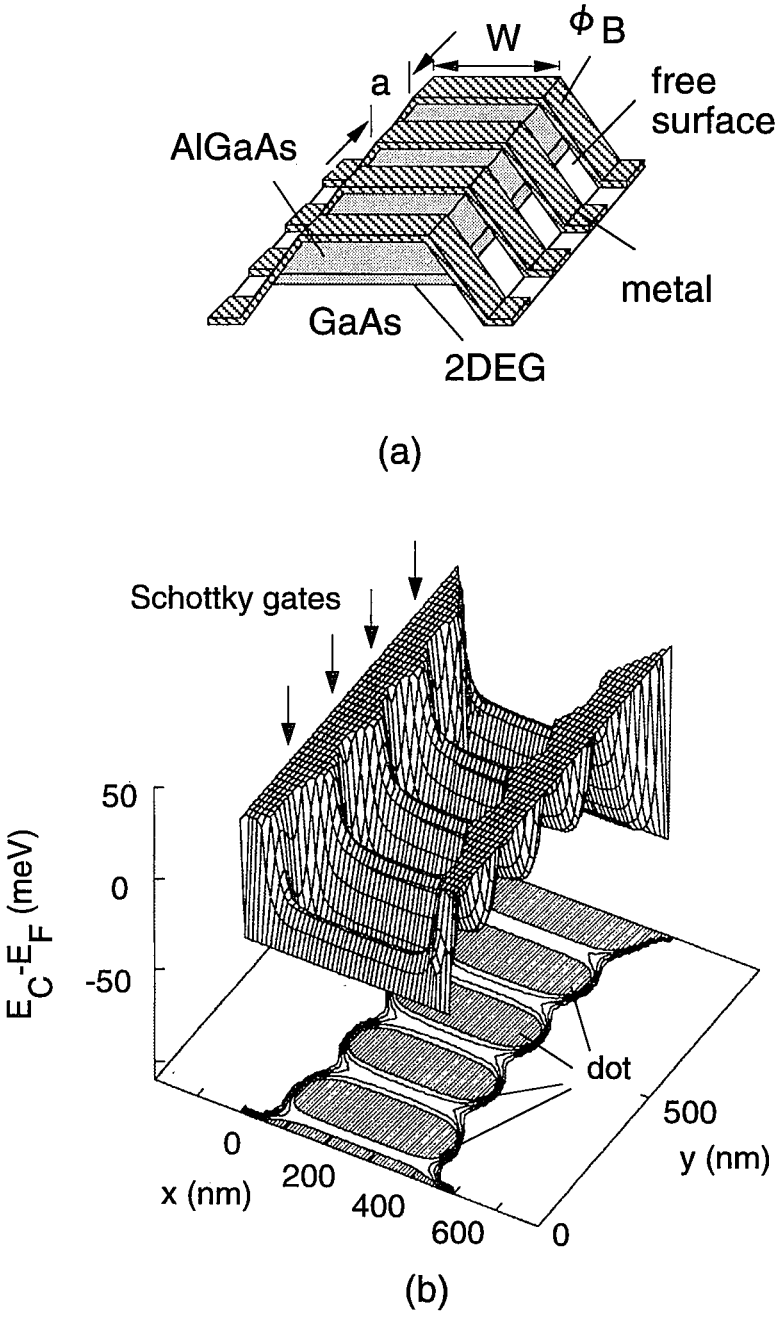


Fig.8-8. Example of potential simulation. (a) WPG mutiple-dot-chain structure and (b) calculated potential. Multiple-dot formation is clearly seen.

The example of potential simulation for WPG multiple-quantum dot chain is shown in **Fig.8-8**. The formation of quantum dots is clearly seen .

8.4 A theory for EBIC characterization of Schottky IPG structures

8.4.1 *Basic equations for EBIC analysis*

In the EBIC measurement, the charge carriers generated by an electron beam are collected and sensed as current in as external circuit. In particular, when a fine electron beam is irradiated at a position x, in the depletion layer with a width, W_{dep}, electron-hole pairs generated by irradiation of the electron beam are separated by the strong electric field in the depletion region, as shown in **Fig.8-9**. These electrons and holes then drift in opposite directions and produce a current in the external circuit, if all of them do not recombine in the depletion region. According to a previous work,[10] current $J(x)$ can be generally expressed by the following equation.

$$J(x)=qG\Sigma \quad \text{with} \quad G=I_B\frac{E_B}{E_{e-h}}(1-f) \tag{8.3}$$

where G is the electron-hole pair generation rate, q is electronic charge, I_B is the electron beam current, E_B is the electron beam energy, $E_{e\text{-}h}$ is the energy required for electron-hole pare generation, f is the surface reflectivity for electron beam and Σ is the collection efficiency. The value of the collection efficiency Σ is determined by the carrier dynamics in the depletion region. For example, for a depletion layer having a uniform field E, a carrier mobility μ and a SRH recombination lifetime τ,Σ is given by[10]

$$\Sigma=\frac{1-e^{-\gamma}}{\gamma} \quad \text{with} \quad \gamma=\frac{W_{dep}}{\mu E\tau} \tag{8.4}$$

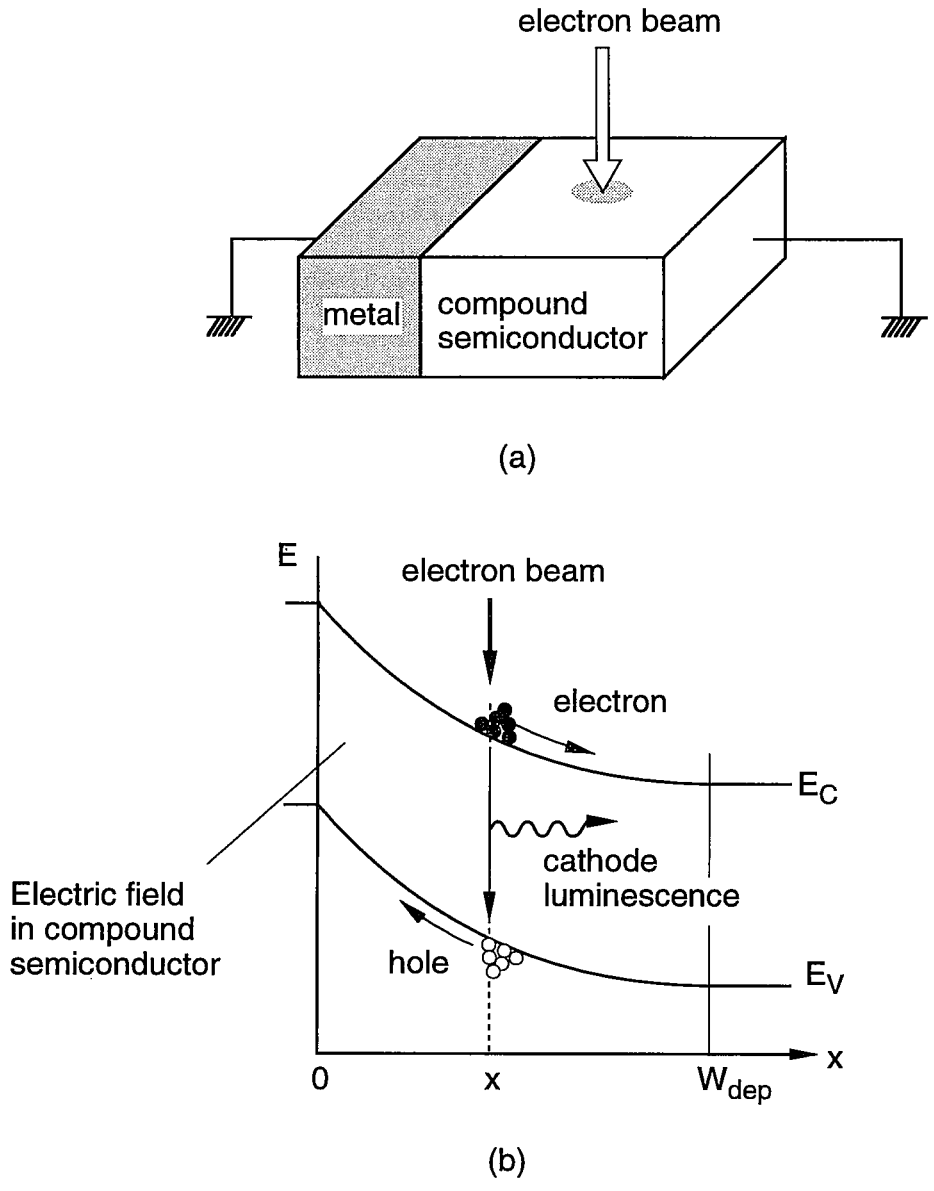


Fig.8-9. Principle of electron-beam-induced current.

where SRH recombination in the depletion layer is negligible, $\gamma \ll 1$ and **eq.(8.4)** gives $\sum=1$. Thus, $J(x)=G$, being independent of the field E. On the other hand, when SRH recombination is frequent, $\sum=\gamma^{-1}=\mu\tau E/W_{dep}$ and the current becomes proportional to E. In devices based on single crystalline Si, normally $\gamma \ll 1$, and one cannot get information concerning E from the EBIC signal. Thus, EBIC technique have been utilized for determination of diffusion length L and surface recombination velocity S.

In the case of GaAs, SRH recombination is similarly negligible. However, extremely strong radiative recombination takes place particularly due to its direct energy gap, producing cathode luminescence, as schematically shown in **Fig.8-9**. In this case, it is easy to show that $J(x)$ is given by the following equation.

$$J(x)=q\mu_n E(x)n_0 \quad \text{with} \quad n_0=\tau_n G \tag{8.5}$$

where τ_n is the effective radiative recombination time for cathode luminescence. This equation shows that the EBIC signal directly reflects the electric field in the structure if the generated equilibrium carrier density n_0 is the same everywhere. Thus, if one use an extremely high-resolution SEM system where the radius of the beam can be ignored, the signal gives potential distribution directly.

In practice, however, it is known that the area where electron-hole pairs are produced has a finite extension even if the radius of the electron beam is sufficiently small. This is due to the fact that the high energy electrons move within the material during electron-hole pair generation. A simplest way to take account of this effect is to make a superposition of **eq.(8.5)**. Then,

$$J(x) = \int_{-\infty}^{\infty} R_x(x'-x)\, n_0\, \mu_0\, E(x')\, dx' \tag{8.6}$$

where $R_x(x)$ is the distribution function of generated carriers. Assuming this distribution is Gaussian, the current is given by the next equation.

$$J(x) = \int_{-\infty}^{\infty} q\,\mu_0\,n_0\,exp\left(-\left(\frac{x'-x}{R_e}\right)^2\right)E(x')\,dx' \qquad (8.7)$$

where R_e is the electron range. It is known empirically that the value of R_e depends on energy of the electron beam, E_B,[10] as

$$R_e = \frac{4.28\times10^{-8}}{\rho}E_{EB}^{\ 1.75} \quad \text{(cm)} \qquad (8.8)$$

where ρ is the density of the sample (g/cm^3).

8.4.2 *EBIC Signal from basic Schottky IPG/2DEG diode*

For theoretical evaluation of EBIC signals using **eq.(8.7)**, one needs knowledge on the field distribution. A simple model for the Schottky IPG structure used here is shown in **Fig.8-2(a)**, where a perpendicular IPG is formed at the edge of 2DEG. **Figure 8-10(a)** shows the calculated normalized EBIC signals using **eqs.(8.1a)**, **(8.1b)**, **(8.2a)** and **(8.3b)** for the Schottky IPG/2DEG diode for different values of the electron beam energy, E_B. ρ =4.71g/cm^3 was used for GaAs. For comparison, calculated signals for a conventional Schottky contact are shown in **Fig.8-10(b)**. It is seen that use of higher acceleration voltages of the electron beam quickly broadens the EBIC signal.

Since the field profile is thus quickly broadened and distorted by the penetration effect of the electron beam, it is difficult to directly determine the depletion layer edge from the EBIC signal profile. Diffusion effects of carriers outside the depletion layer, which are ignored in the present simplified analysis may produce a long tail in the EBIC signal profile, and may cause farther difficulty in determining the edge position. This difficulty may be removed by theoretically relating to the effective width of the EBIC signal to the depletion width.

Figure 8-11 shows an example of the calculated relationship between the depletion layer width, W_{dep}, and the full width of half maximum (FWHM), ΔW, of the

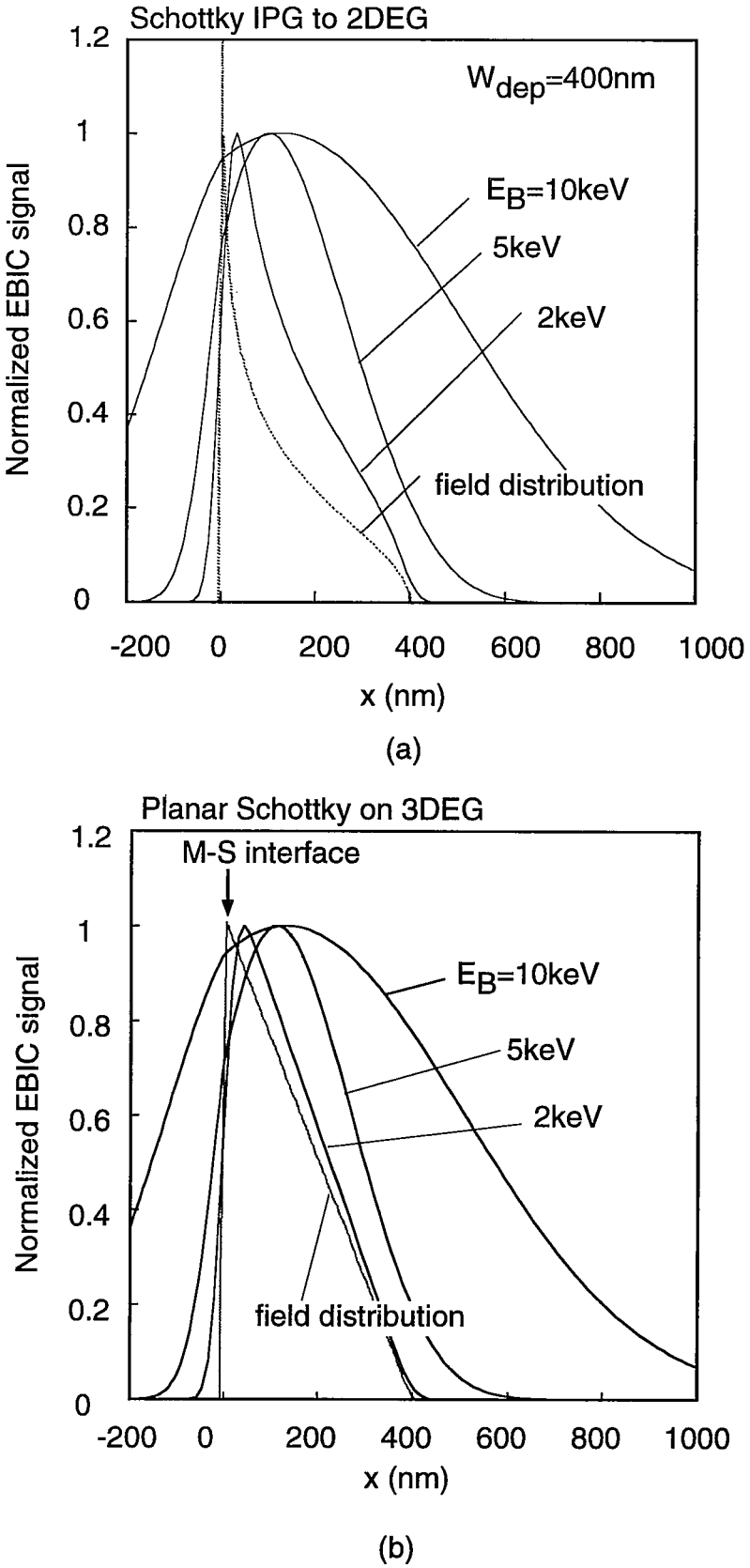


Fig.8-10. Calculated EBIC signals for (a) Schottky IPG and (b) planar Schottky contacts.

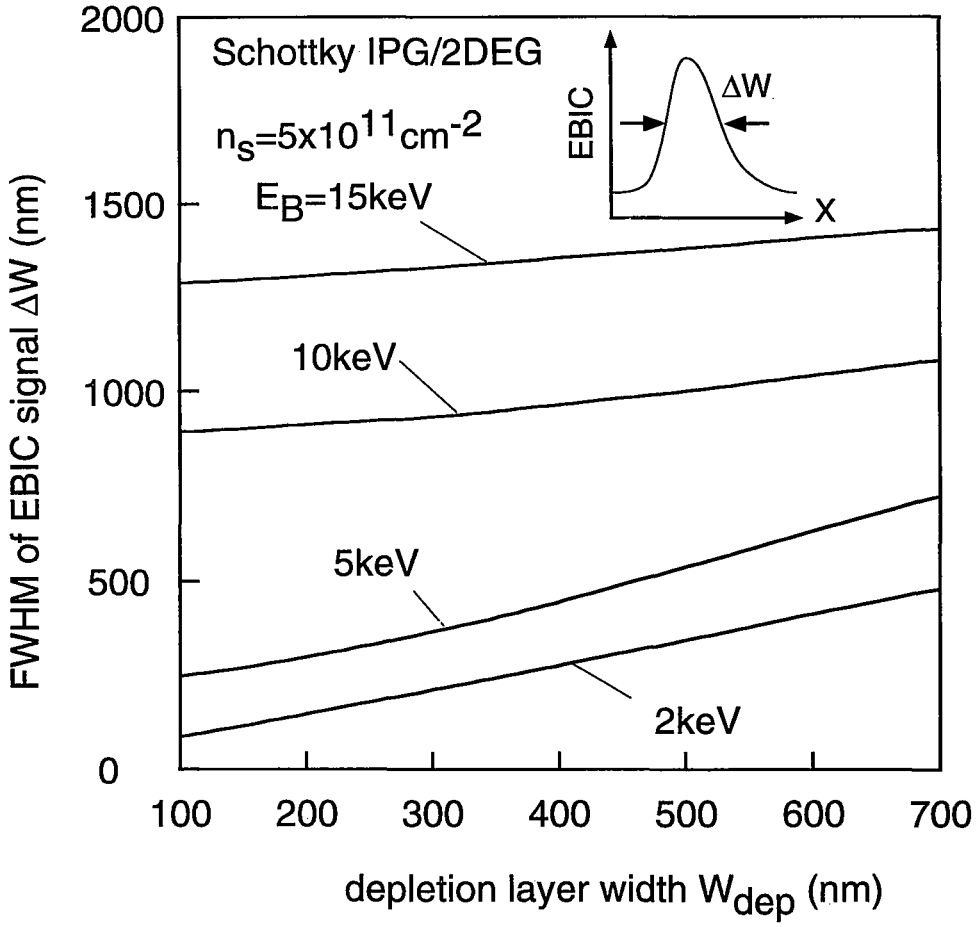


Fig.8-11. Calculated FWHM (ΔW) of EBIC signal as a function of depletion layer width (W_{dep}).

EBIC signal for the IPG Schottky contact. It is seen that ΔW increase almost linearly with the increase of W_{dep}. Using this relationship, the value of W_{dep} of the Schottky IPG structure can be estimated from the measured value of ΔW. For this purpose, the value of E_B should be kept reasonably small since the slope of the curve for a higher EB energy because smaller and less sensitive against variation of W_{dep}.

8.5 Experimental EBIC characterization of basic Schottky IPG structure

8.5.1 *Sample Structure and EBIC Measurement*

The experimental set-up and the sample structure used for EBIC characterization of the basic Schottky IPG structure is shown in **Fig.8-12**. The sample was fabricated as follow. First, an $Al_{0.3}Ga_{0.7}As$/GaAs double-hetero structure wafer with a GaAs well width of 20nm was grown by standard MBE growth at substrate temperature of 600°C. 2DEG was located at 60nm below the surface. Si atomic layer for δ-doping was formed at a position of 10nm above 2DEG. Then, the edge of the 2DEG was revealed by wet chemical etching down to 500nm. Subsequently, Schottky IPG electrodes were defined by photolithography or EB lithography and formed by Pt plating using an in-situ electrochemical process.[12] For EBIC measurement, Hitachi S4100 SEM equipment with a spatial resolution of 10nm was used. The beam voltage was varied in the range of 2~15keV. The EBIC measurement system attached to SEM had a bias-voltage application circuit to measure the bias dependence of the EBIC signal. The electron beam was scanned on the top surface or on the cross section of the samples, as shown in **Fig.8-12**.

8.5.2 *Observed EBIC signals and comparison with theory.*

The examples of the EBIC line-scan signal from the Pt/2DEG Schottky diode sample are shown for different bias voltages in **Fig.8-13(a)** and **8-13(b).** The value of the E_B was 5keV for **Fig.8-13(a)**, and 10keV for **Fig.8-13(b)**. By comparing **Fig.8-13**

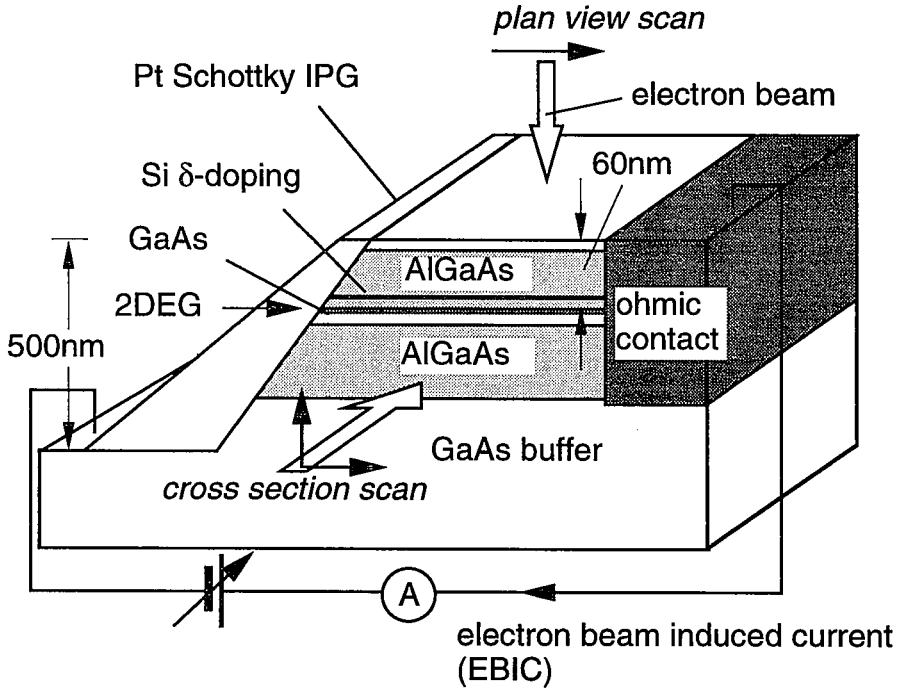
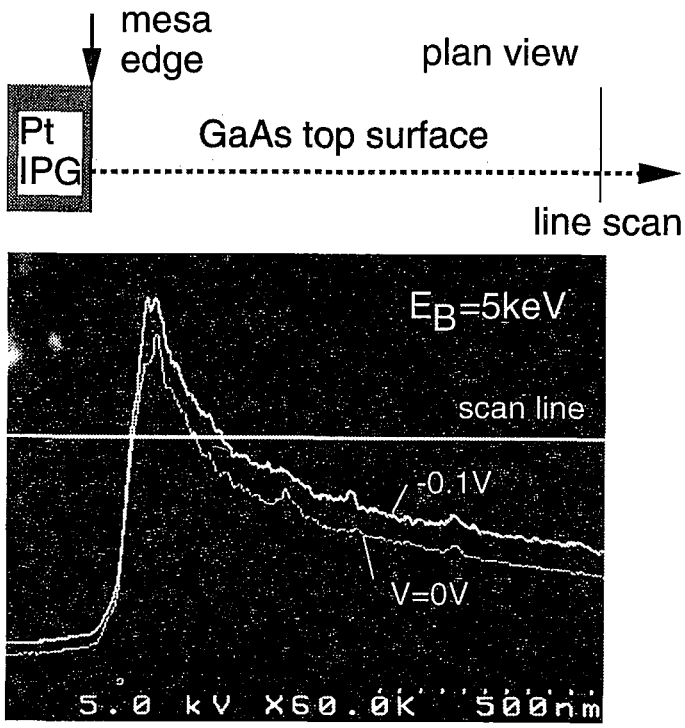
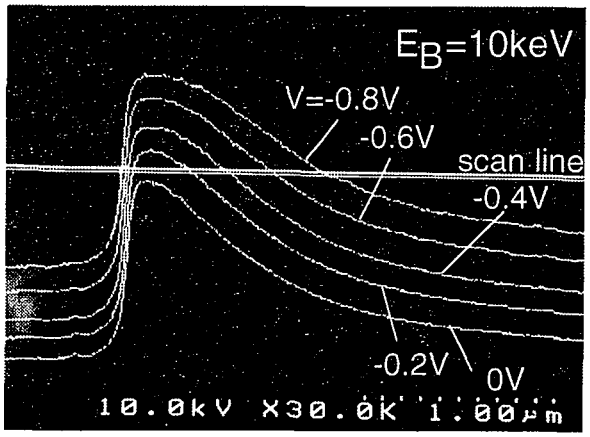


Fig.8-12. EBIC measurement system.



(a)



(b)

Fig.8-13. Example of line-scan EBIC signals from Pt/2DEG Schottky IPG diode, (a) electron beam energy E_B=5keV and (b) E_B=10keV.

with **Fig.8-13(b)**, it is found that experimentally observed signal shapes, their bias-voltage dependence and their beam-energy dependence qualitatively agree with those predicted by the theoretically calculation. However, quantitatively speaking, it is noted that the tail of the observed EBIC signal is somewhat more prolonged and maintains a higher level than the calculated one. This seems to be due to diffusion current components which are totally ignored in the present analysis. Moreover, 2-dimensional potential simulation performed for the experimental structures also indicated the tail of the electric field as shown in **Fig.8-4** which was slightly different from the analytical model.

For further quantitative comparison between theory and experiment, experimentally observed bias dependences of the FWHM of EBIC signal, ΔW, are plotted in **Fig.8-14(a)** for various values of the beam energy E_B. The theoretical curves n_s=5x10^{11}cm^{-2} and V_{bi}=0.7 eV confirmed by the Hall measurement and capacitance-voltage measurement,[3] are also shown in **Fig.8-14(a)**. It is seen that the theoretical curves agree excellently with the experimental results for each EB energy condition in spite of the aforementioned discrepancy in the tail portion of the EBIC signal. This indicates that the additional diffusion current components are not large enough to alter the main feature of the EBIC signal reflecting drift components.

In **Fig.8-14(b)**, the values of the estimated from the relationship between W_{dep} and ΔW in **Fig.8-6** are compared directly with the theoretical curves based on **eq.(8.7b)**. Again, an excellent agreement between theory and experiment is seen, showing an overall consistency. Therefore, the novel EBIC method is found to be extremely useful for not only qualitative but also quantitative characterization of the electric field and potential distributions controlled by the Schottky IPGs.

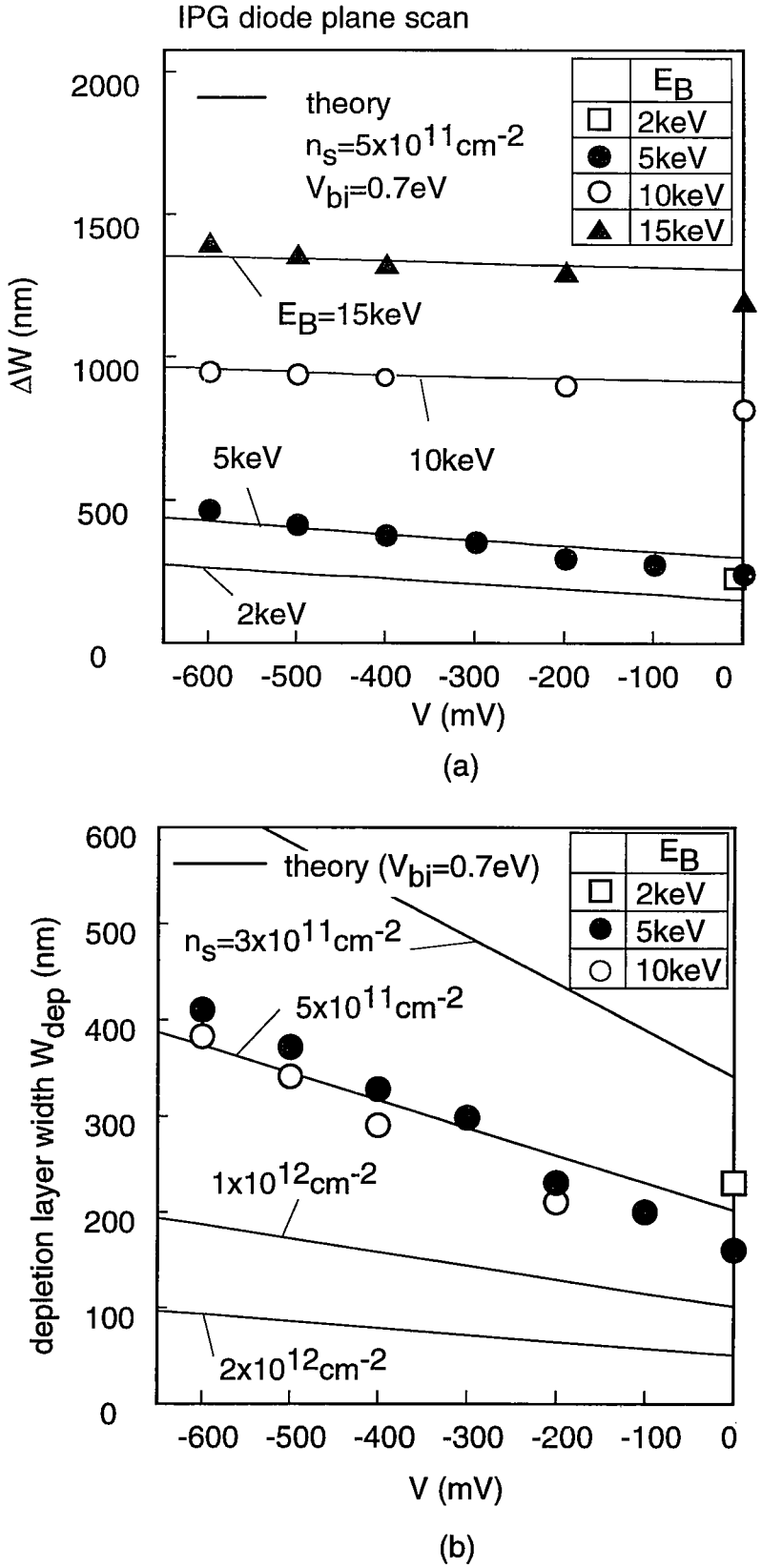


Fig.8-14. (a) FWHM (ΔW) of EBIC signal and (b) estimated depletion layer width (W_{dep}) as a function of applied voltage.

8.6 EBIC characterization of various quantum nanostructures based on Schottky IPGs

8.6.1 *Fabrication process of quantum nanostructures utilizing Schottky IPG and WPGs*

In this work, quantum wire (QWR), lateral superlattice (LSL) and multiple-dot chain devices utilizing Schottky IPG and WPG structures were fabricated as quantum nanostructures. The device fabrication process is shown in **Fig.8-15**. First, $Al_{0.3}Ga_{0.7}As$/GaAs double-heterostructure in **Fig.8-15(a)** was grown by standard MBE growth at the substrate temperature of 600°C. The thickness of undoped-AlGaAs barrier layer and spacer were 50nm and 10nm, respectively. Si δ-doping layer was inserted between these two layers. GaAs quantum well thickness was 20nm and lower AlGaAs barrier thickness was 50nm. On this structure, SiO_2 passivation layer was formed by using photo-CVD. After the formation of basic structures, 2DEG bars, source and drain pad regions were formed by EB lithography and wet chemical etching as shown in **Fig.8-15(b)**. Then, Au/Ge/Ni ohmic contacts were formed. Finally, Schottky IPG or WPG electrodes with a few hundred nm intervals were defined by EB lithography, and formed either by Pt plating using an in-situ electrochemical process for IPG structures in **Fig.8-15(c)** or by conventional Cr/Au lift-off process after removing SiO_2 layer for WPG structures in **Fig.8-15(d)**, respectively.

8.6.2 *Quantum wires*

With the present Schottky IPG approach, voltage-tunable quantum wire can be formed by the electrode arrangement shown in **Fig.8-1(c)**. A wire having a cross section of **Fig.8-1(a)** was fabricated and studied by EBIC method. The structure of the sample is shown in **Fig.8-16(a)**. The narrow wire-channel was presented by

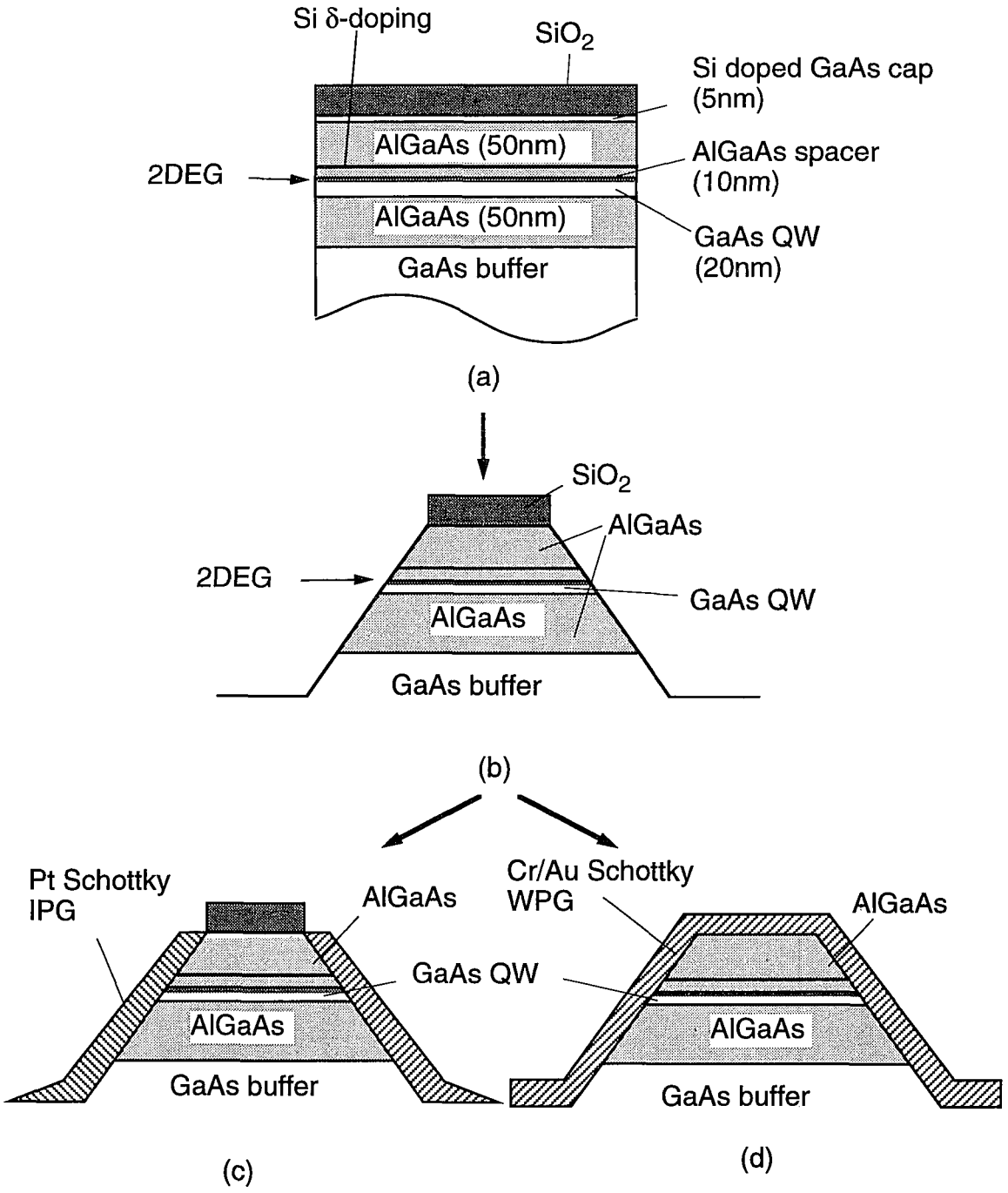


Fig.8-15. Schottky IPG and WPG structures fabrication process.

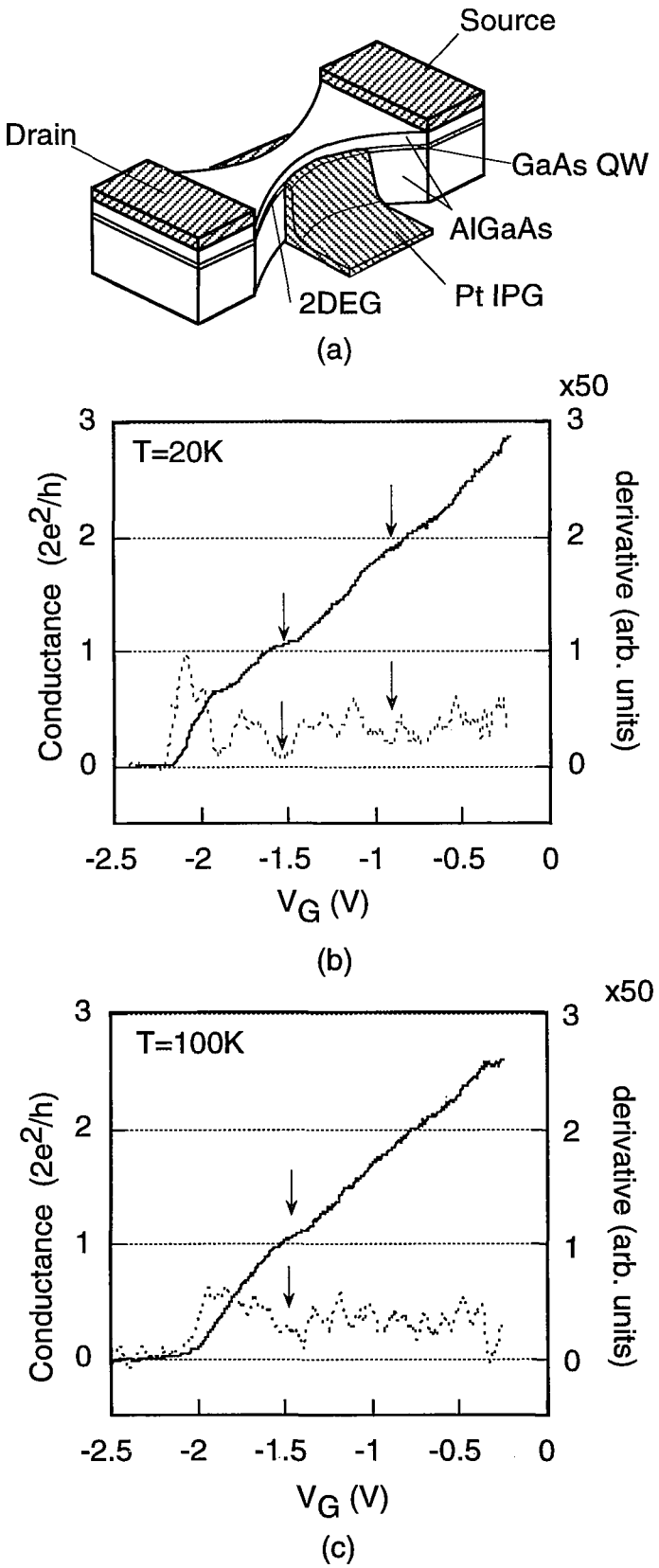


Fig.8-16. (a) Schematic view of the IPG-GaAs quantum wire (QWR) device. (b) and (c) are quantized conductance of the IPG-QWR. The conductance steps are visible up to 100K.

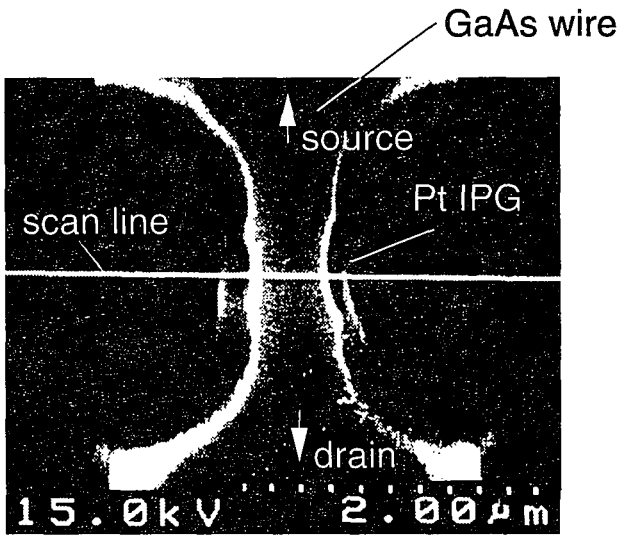
applying the EB lithography and wet chemical etching to an AlGaAs/GaAs QW wafer. This device showed the clear quantized conductance in a few Kelvin and, as shown in **Fig.8-16(b)**, it exhibited existence of first plateau of quantized conductance in units of $2e^2/h$ up to 100K in spite of its large waveguide length of more than 1,000nm.[2] This value is much higher than the value of 44K obtained with a AlGaAs/GaAs split-gate point contact formed by using much smaller dimensions,[13] and shows that a very strong confinement potential can be achieved by the present Schottky IPG structure. A plan view SEM micrograph of the sample is shown in **Fig.8-17(a)**. **Figure 8-17(b)** shows a line-scan EBIC signal taken on the SEM plan-view of the sample at zero bias. Two fine peaks were clearly observed at the edge of the wire, showing existence of depletion layers in the channel. This clearly demonstrates that the EBIC technique allows in this case non destructive characterization of buried depletion boundaries.

8.6.3 *Lateral superlattices and multiple-dot structures*

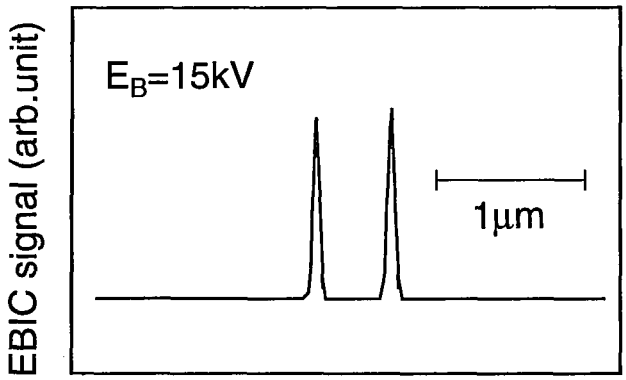
As shown in **Fig.8-1(e)** and **8-1(f)**, lateral superlattices and multi-dot chains can be easily realized by putting suitable Schottky IPG patterns to a 2DEG bar. Potential modulation can be achieved by gate bias, use of different Schottky barrier heights (SBHs), periodic insertion of air gaps etc. To find the feasibility of this novel approaches, samples shown in **Fig.8-18** were fabricated and characterized by the EBIC technique. The samples had a cross section shown in **Fig.8-1(b)**.

Figure 8-18(a) shows the fabricated lateral superlattice structure, utilizing a periodic arrays of Schottky IPGs with different SBHs, ϕ_{B1} and ϕ_{B2}. Due to the Fermi level pinning on GaAs and AlGaAs, realization of different SBHs by using metals with different work functions are almost impossible. Here, periodic insertion of As doped silicon interface control layer (Si ICL) was employed as shown in **Fig.8-19(a)** where doping-dipole formed in As-doped Si ICL reduces the SBH.[14]

EBIC images taken on the cross-section of the sample along the center line x-x' in **Fig.8-18(a)** are shown in **Figs.8-19(b)**. **Figure 8-19(b)** clearly and directly



(a)



(b)

Fig.8-17. (a) Plan-view SEM image and (b) line-scan EBIC signal of the Schottky IPG quantum wire.

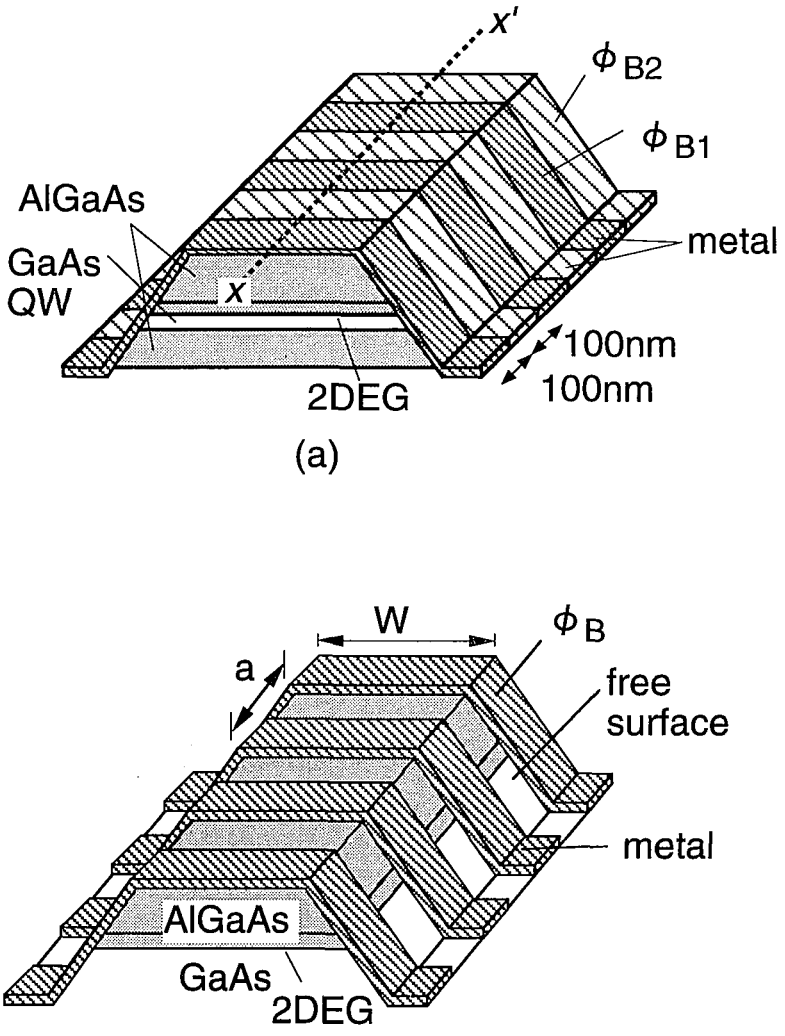
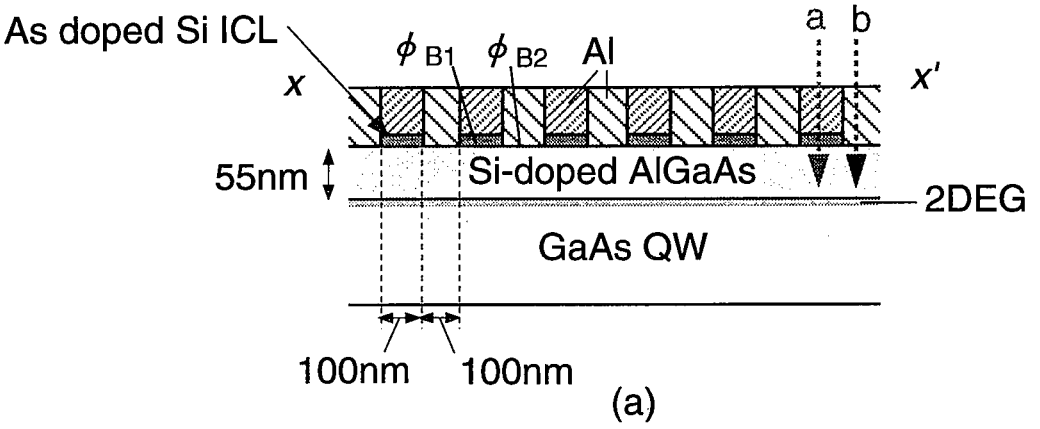
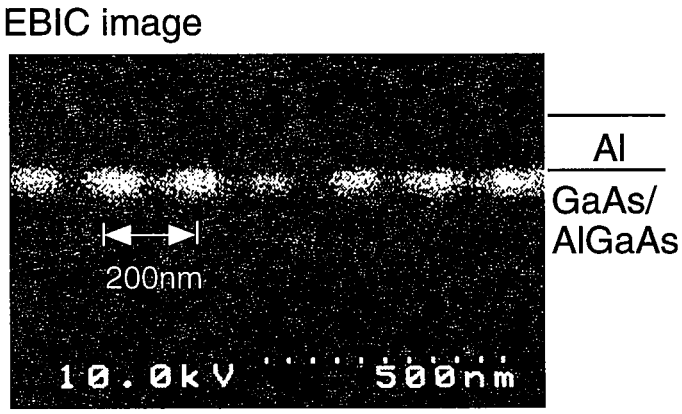


Fig.8-18. (a) Lateral superlattice (LSL) structure utilizing a periodic array of Schottky WPGs having different Schottky barrier height and (b) LSL with periodic WPGs and air-gaps.



(a)



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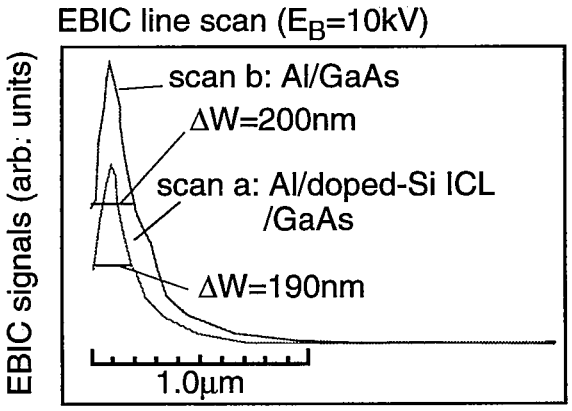


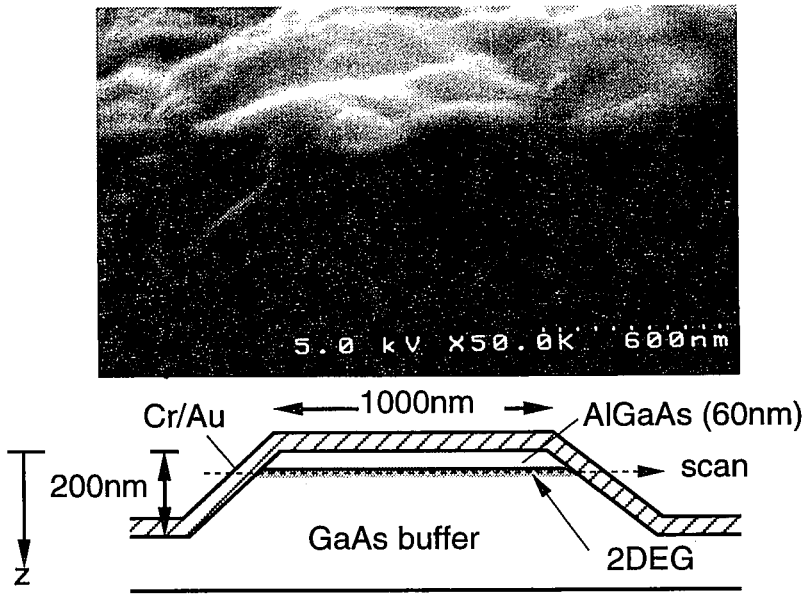
(c)

Fig.8-19. (a) Schematic view of cross section of the LSL device, (b) cross-sectional EBIC image of the LSL structure and (c) line-scan EBIC signal.

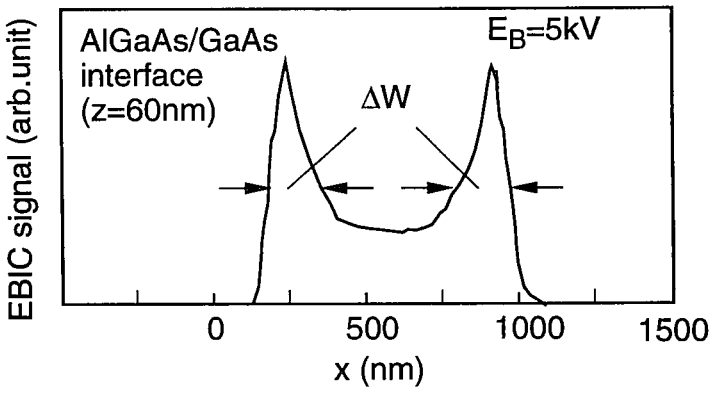
demonstrates that periodic variation of SBH is indeed realized by the insertion of Si ICL stripes. The result of EBIC line scans along lines, *a* and *b*, in **Fig.8-19(a)** is shown in **Fig.8-19(c)**. The difference in SBH can be seen more clearly seen here. A further quantitative analysis showed that SBH without Si ICL was 0.8eV and that with Si ICL was 0.6eV, that were consistent with the results of separate C-V measurements on Schottky diodes with larger dimensions. Thus, the EBIC allows direct analysis of buried field profiles of nanostructures. As reported elsewhere,[15] this type of lateral superlattice showed clear transconductance and drain conductance oscillations at low temperature.

Figure 8-18(c) shows yet another periodic structure utilizing periodic insertion of air gaps. This structure can be operated as lateral superlattices and multiple-dot chain, depending on the applied gate voltage. This structure was also fabricated by EB lithography, etching and deposition of the Cr/Au Schottky metal and was characterized by the SEM/EBIC technique.

The cross sectional SEM image and EBIC line-scan of the portion having a Cr/Au Schottky IPG is shown in **Fig.8-20(a)** and **(b)**. The top width of the 2DEG bar was 1μm and the height of the mesa pattern was 200nm. 2DEG was located at 60nm from the top M-S interface. The line scan of EBIC image near the heterointerface under zero bias shown in **Fig.8-20(b)**. From the value of ΔW of the EBIC edge peaks at E_B=5keV of about 250~300nm , the depletion width was estimated to be about 70~80nm using the present analysis. This value is reasonable, since the calculated value using **eq.(8.1b)** is 60nm with n_s=1.8x10^{12}cm^{-2} from Hall measurement. **Figure 8-20(c)** shows the plan-view SEM image of the fabricated structure having 38 stripes. Schottky IPG width was 40nm and the interval of the IPG gate was 160nm, corresponding to a gate periodicity of 200nm. As will be shown in **chapter 9**, this device have shown clear Coulomb oscillation characteristics near pinch-off up to 5.4K, in spite of a wide channel of 1300nm, indicating successful formation of multiple-dots. The maximum temperature for observation of Coulomb blockade oscillation is much higher than that for the usual split-gate SET devices, which show



(a)



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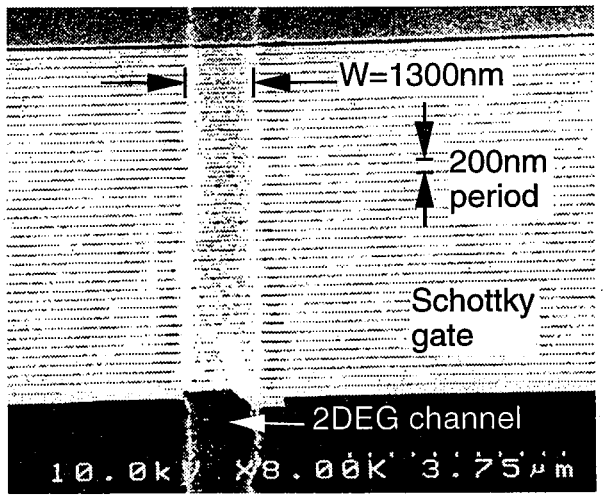

(c)

Fig.8-20. (a) Cross-sectional SEM image, (b) line scan EBIC signal of Schottky WPG structure and (c) plan-view SEM image of a mutiple-dot chain structure by Schottky WPGs.

the oscillation up to a few hundred mK. This result again shows that very effective confinement of electrons can be achieved by the Schottky IPG structure.

8.7 Conclusion

Attempts were made to characterize the depletion field profiles within the Schottky IPG based GaAs quantum nanostructures by the EBIC technique. Main conclusions are the following.

1) A simple theory on the EBIC signal from the basic Schottky IPG/2DEG developed here can explain the experimental results very well.

2) By taking account of the range of the electron beam, a direct, non-destructive and quantitative characterization of field profiles, depletion widths and Schottky barrier heights of the buried depletion layer becomes possible.

3) The results of applications of the EBIC technique to wires, lateral superlattices and multi-dot structures show the effectiveness of the Schottky IPG controls of 2DEG for realization defect-free compound semiconductor quantum nanostructures.

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Chapter 9

Fabrication and Characterization of Single-Electron Devices Utilizing GaAs Schottky In-Plane Gates and Wrap-Gates Structures

9.1 Introduction

With the recent rapid progress of fabrication techniques of nanostructures, various new phenomena related to single electron transport through single-quantum dot[1] and multiple-quantum dots[2-8] have been found and predicted. They are extremely interesting not only from the viewpoint of basic physics but also from the engineering viewpoint of constructing next generation electronics based on single electron devices with new system architectures.

For the latter purpose, high temperature operation of single electron devices seems to be one of the indispensable requirements. Recently, Si-based single-electron transistors (SETs) have made a great progress towards room temperature operation.[9,10] However, GaAs-based SETs reported so far operate mostly in mK range, in spite of the fact that first demonstration of feasibility of semiconductor SETs was made by them.[11,12] This is primarily because of the split-gate potential control used in GaAs-based SETs which produces a rather weak and gradual confinement potential with soft-wall potential boundaries. In contrast to this, the Si-SiO_2 interface used in Si SETs can produce large and sharp potential boundaries.

To overcome this problem, recently a novel GaAs SET based on Schottky in-plane-gate (IPG) control of two dimensional electron gas (2DEG) was proposed and fabricated.[13] In this structure, electric fields are perpendicular to the 2DEG edge and realize stronger confinement than the split gate geometry. The fabricated SET device

showed Coulomb blockade (CB) oscillation up to 20K.[13]

It is known that a quantum-dot chain is the most possible structure for the multi-function of SETs. However, researches on quantum-dot chain are not sufficient not only theoretically but also experimentally, yet.

In this chapter, the results of fabrication and characterization of single-dot and multiple-dot SETs based on control of 2DEG with novel Schottky gate geometries are described after brief introduction of single-electron physics. The previously proposed Schottky IPG and a newly introduced Schottky wrapped gate (WPG) geometries were used to realize 1, 2, 3, 18 and 37-dot SETs on AlGaAs/ GaAs heterostructures.

9.2 Single electron phenomena in a quantum dot

Figure 9-1(a) schematically shows the plan view of the quantum dot, which is formed by the Schottky split-gates, for example. The equivalent circuit of the system is shown in **Fig.9-1(b).** When a certain negative voltage is applied to the gates, constriction are formed and the induced potential barriers will strongly localize the electrons in the dot. Then the number of electrons in the dot is determined by an integer and can be changed one by one. The electrostatic energy $E_{e\to s}$ of the dot contains discrete number of electrons is written as

$$E_{e\to s}=\frac{(en-Q_0)^2}{2C} \qquad (9.1)$$

with

$$n=N-N_0$$
$$Q_0=C_L V_L+C_R V_R+C_G V_G$$
$$C=C_L+C_R+C_G$$

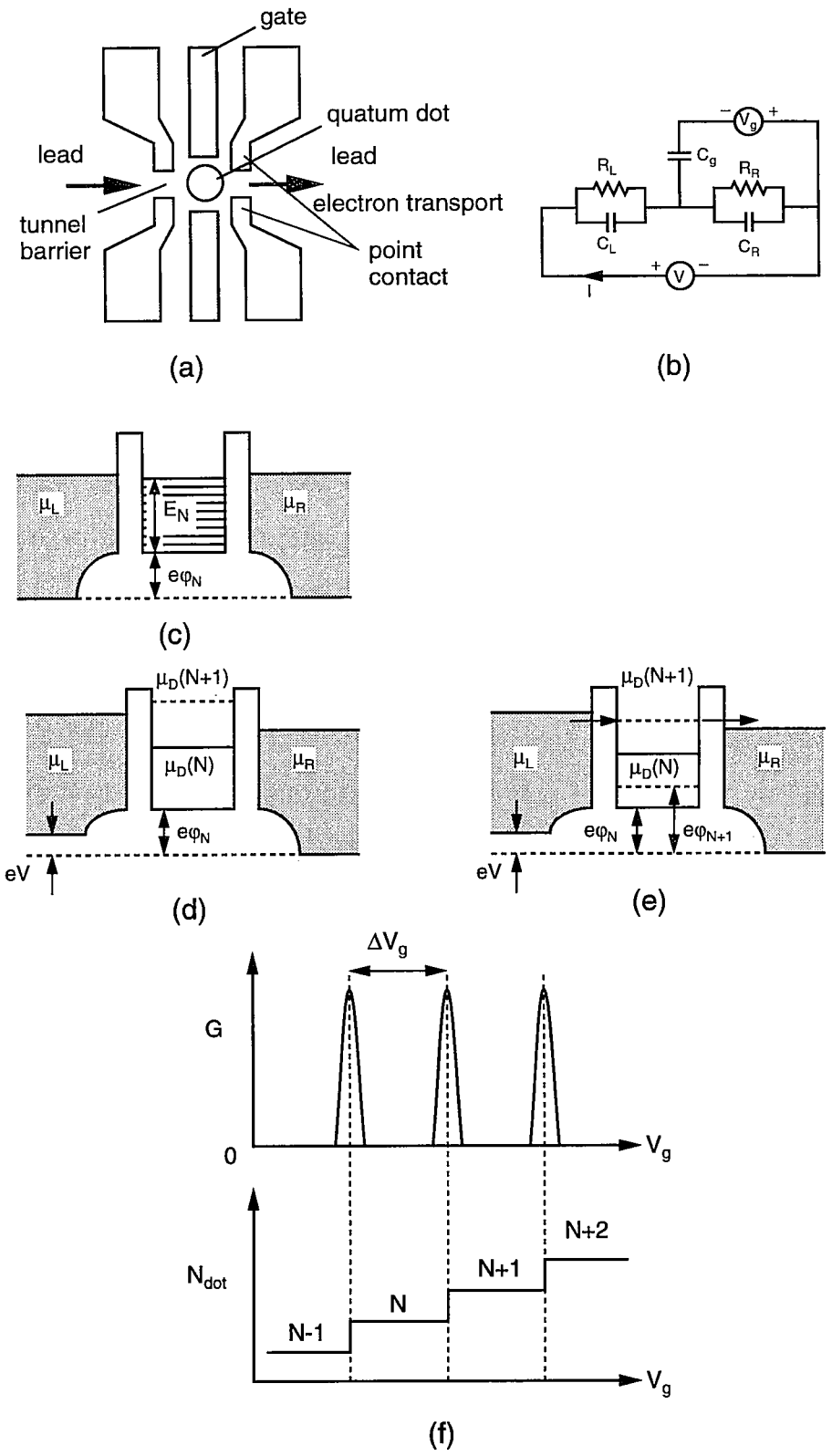


Fig.9-1. Basic feature of Coulomb blockade phenomena. (a) Schematic view of a SET structure by Schottky split gates, (b) equivalent circuit of the SET. (c) Energy diagram of the dot and reads, (d) Coulomb blockade is occurred and (e) is eliminated. (f) The number of electron in the dot as a function of V_G.

where, N is the number of electrons in the dot, N_0 is the number of electrons at gate bias V_G=0 (initial state), C_L and C_R are capacitances of left and right lead to the dot. C_G is gate capacitance, V_L and V_R are left and right read voltage, respectively. The integer part of the excess charge in the dot is $en=e(N-N_0)$, where e is the elementary charge. Q_0 represents the continuous part of the excess charge, which is induced by voltage differences V_L and V_R between the dot and the leads ($eV_L=\mu_L-\mu_D(N)$, $eV_R=\mu_D(N)-\mu_R$ where $\mu_D(N)$ is the electrochemical potential of the dot) and by the gate voltages. C is the total capacitance of the dot to ground. Note that in the case of n=1 and Q_0=0, **eq.(9.1)** gives the charging energy $e^2/2C$ for a single electron. However, it is more convenient to take $E_C=e^2/C$ as the unit for charging energy. Moreover, at zero bias voltage and at fixed gate voltage, the induced charge Q_0 can be compensated by tunneling of many electrons through the dot as required to reduce the total charge $en-Q_0$ smaller than e, so the electrostatic energy is minimized to less than e^2/C.

Here $Q_0=C_GV_G$ (V_G<0). The ground state energy for N electrons in the dot at zero temperature is the sum over the single particle energies E_p relative to the bottom of the conduction band, and the electrostatic energy given by

$$U(N)=\sum_{p=1}^{N} E_p + \frac{(en+C_GV_G)^2}{2C} \qquad (9.2)$$

From **eq.(9.2)**, the electrochemical potential is calculated which is needs to add N-th electron into the dot, which corresponds to $\mu_D(N)=U(N)-U(N-1)$,

$$\mu_D(N)=E_N+\frac{(2n-1)e^2}{2C}-e\frac{C_G}{C}V_G \qquad (9.3)$$

In a more familiar form $\mu_D(N)=\mu_{ch}(N)+e\varphi_N$, where $\mu_{ch}(N)=E_N$ and E_N is quantized energy due to electron confinement and the electrostatic potential $e\varphi_N$. When the number of electrons is changed by one, the resulting change in electrochemical potential in the dot at fixed gate voltage is given by

$$E_{gap}=\mu_D(N+1)-\mu_D(N)=E_{N+1}-E_N+e^2/C\,. \qquad (9.4)$$

Equation (9.4) implies that the electrochemical potential changes by a finite energy when an electron is added to the dot. $\mu_D(N+1)$-$\mu(N)$ becomes large if energy splitting between consecutive 0D-states is large, and/or if the capacitance is small. This energy gap E_{gap} can cause a blockade for tunneling of electrons into and out of the dot, as schematically shown in **Fig.9-1(c).** N electrons are localized in the dot and the N+1-th electron can not tunnel into the dot, because the electrochemical potential $\mu_D(N+1)$ is higher than the electrochemical potentials of the reservoirs. Thus, when $\mu_D(N)<\mu_L$, $\mu_R<\mu_D(N+1)$, the electron transport through the dot is blocked. This is known as Coulomb blockade. Transport is only possible by thermal activation or tunneling through virtual states. Note that the energy gap of **eq.(9.4)** takes place at the Fermi energy.

The Coulomb blockade is eliminated by changing gate voltage, when $\mu_L>\mu_D(N+1)>\mu_R$, as shown in **Fig.9-1(d)**. Now an electron can tunnel from the left reservoir into the dot, $\mu_L>\mu_D(N+1)$. The electrochemical potential in the dot increases by the amount given in **eq.(9.4)**, which is dominated by the increase of electrostatic energy $e\varphi_{N+1}$-$e\varphi_N=e^2/C$. Because $\mu_D(N+1)>\mu_R$, one electron can tunnel into the dot. This process is known as single charge tunneling where current is carried by successive discrete charging and discharging of the dot by one electron.

As the gate voltage is changed, the conductance of the quantum dot oscillates between zero (Coulomb blockade), and non-zero (no Coulomb blockade) as shown

in **Fig.9-1(e)**. This is Coulomb oscillation. In the case of the Coulomb blockade, the number of electrons in the dot is fixed. At a conductance maximum, this number oscillates by one electron, and the electrostatic potential oscillates by e^2/C. In between two conductance peaks, $e\varphi$ changes by E_{N+1}-E_N+e^2/C. From **eq.(9.3)** and the condition $\mu_D(N,V_G)=\mu_D(N+1, V_G+\Delta V_G)$, the period of the oscillations in gate voltage ΔV_G is given by

$$\Delta V_G=\frac{C}{C_G}\left(\frac{E_{N+1}-E_N}{e}\right)+\frac{e}{C_G} \qquad (9.5)$$

When quantized energy splitting by electron confinement is negligible, E_{N+1}-E_N~0, the usual voltage-capacitance relation for a single electron charge is obtained by $\Delta V_G=e/C_G$. When energy splitting due to size quantization is not negligible, it affect the period ΔV_G.

The Coulomb blockade can be removed by increasing the bias between the reservoirs V_{LR}. The energy interval $eV_{LR}=\mu_L$-μ_R determines the transport through the quantum dot. As long as the interval between μ_L and μ_R does not contain a charge state due to charging effect [$\mu_D(N)<\mu_R<\mu_L<\mu_D(N+1)$] as in **Fig.9-1(d)**, the current is zero. However, current starts to flow when either $\mu_L<\mu_D(N+1)<\mu_R$ or $\mu_L<\mu_D(N)<\mu_R$, depending on how the voltage drops across the two barriers. In this case, one can speak of opening a single charge channel, corresponding to either the $N\rightarrow(N+1)$ or the $(N-1)\rightarrow N$ transition. On further increasing V_{LR}, a second channel will open up when two charge states are contained between μ_L and μ_R, giving rise to a second increase of the current.

For a highly asymmetric quantum dot, for instance when the barriers are unequal, the voltage will mainly drop across one of the barriers. This keeps the electrochemical potential of one of the reservoirs fixed relative to the charge states in

the dot, which the electrochemical potential of the other reservoir moves in accordance with V_{LR}. In this asymmetric case, the current change are expected to appear in the *I-V* characteristics as pronounced steps. This is Coulomb staircase. The current steps ΔI occur at voltage intervals $\Delta V=e/C$. For a symmetric quantum dot, both μ_L and μ_R move relatively to the dot (one going up, the other going down), such that both electrochemical potentials are crossing charge states. This smears the steps in the Coulomb staircase yielding a more gradual; increase the threshold voltage to overcome the Coulomb blockade.

9.3 IPG and WPG SET structures and device fabrication process

9.3.1 *Basic structure and operation principle*

The basic structure and principles for single- and multiple-dot SET devices utilizing Schottky in-plane-gates (IPGs) and wrapped gates (WPG) geometries are schematically shown in **Fig.9-2(a)-(f)**. **Figure 9-2(a)** shows the cross section of the Schottky IPG structure. Schottky IPGs form direct contact to the edge of 2DEG and can control the electric field perpendicular to the edge of 2DEG plane. Then, they produce strong and efficient confinement of electrons. The quantum wire realized by Schottky IPG showed the quantized conductance up to 100K, which was higher than that of split-gate structures.[14-17] The Schottky WPG structure in **Fig.9-2(b)** is also obviously possible and may be more useful in some applications for SETs.

Various types of SETs utilizing Schottky IPGs and WPGs studied in this work are shown in **Fig.9-2(c)-(f)**. In these structures, dot sizes and tunneling barriers are voltage-tunable, allowing various conventional as well as "turnstile" operations. **Figure 9-2(c)** shows a single-dot IPG SET having two finger gates and one main gate. In this structure, tunnel barrier and dot size can be controlled by the finger gates and main gate, respectively. **Figure 9-2(d)** shows a double-dot SET. This device has three finger gates. By changing the middle finger gate voltage, the tunnel barrier between two dots can be controlled. The devices in **Fig.9-2(e)** and **9-2(f)** are 3-dot and multiple-dot WPG SETs, respectively, having multiple-finger gates for tunnel barrier control or dot size control. This device may be operated for example as a "single electron shift register". Other more complex functional devices seem to be feasible by proper design of 2DEG bars, IPGs and WPGs.

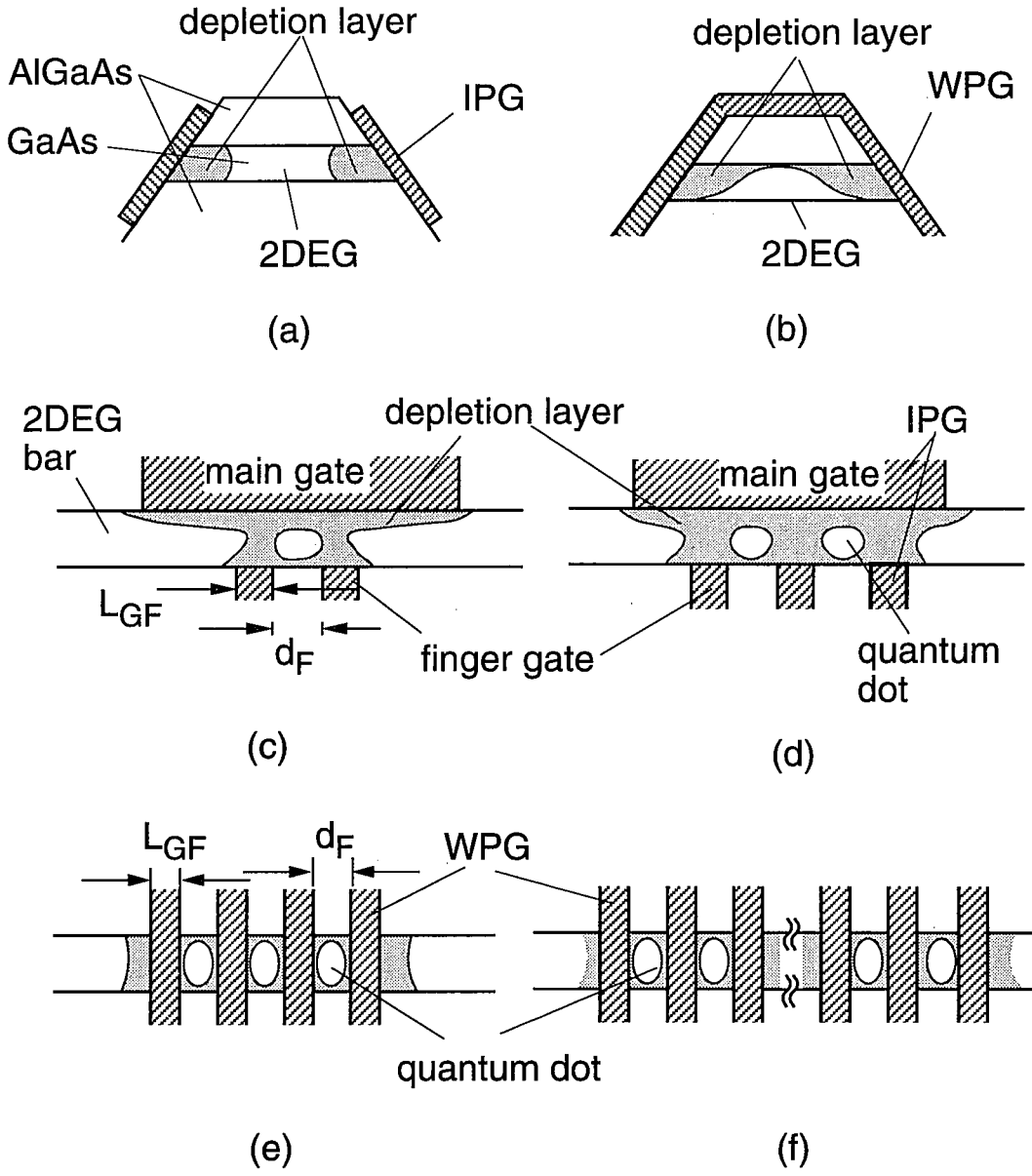
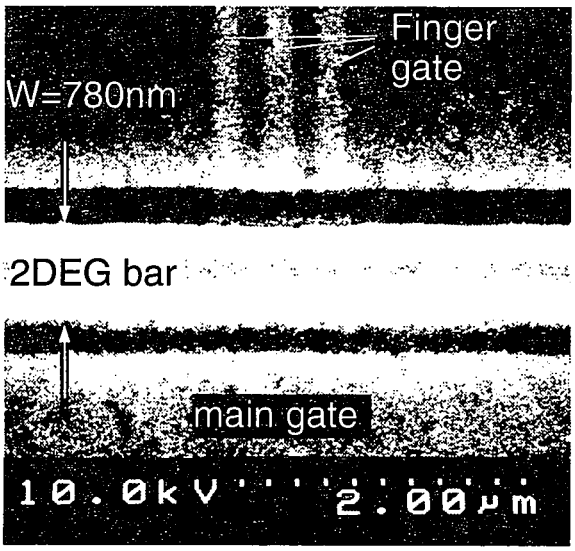


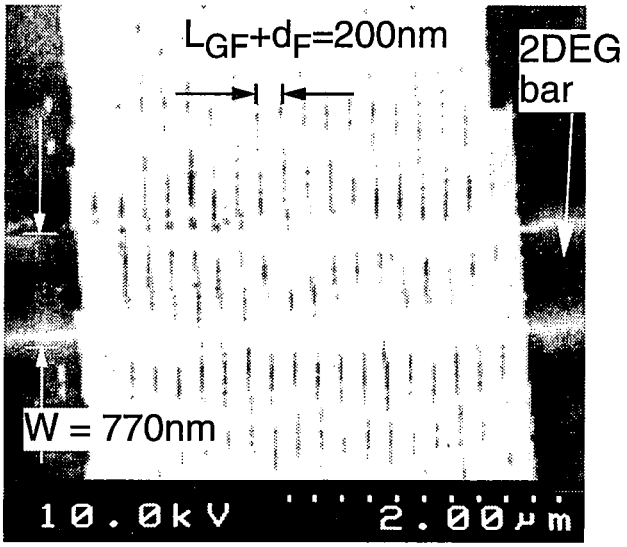
Fig.9-2. Principles and basic structures of SETs utilizing Schottky IPGs and WPGs.

9.3.2 *Device fabrication process*

In this study, single- and double-dot IPG SET and 3, 18 and 37 multiple-dot WPG SETs shown in **Fig.9-2(c)-(f)** were fabricated. First, $Al_{0.3}Ga_{0.7}As$/GaAs double-heterostructure was grown by standard MBE growth at the substrate temperature of 600°C. The thickness of undoped-AlGaAs barrier layer and spacer were 50nm and 10nm, respectively. Si δ-doping layer was inserted between these two layers. GaAs quantum well thickness was 20nm and lower AlGaAs barrier thickness was 50nm. On this structure, SiO_2 passivation layer was formed by using photo-CVD. After the formation of basic structures, 2DEG bars, source and drain pad regions were formed by EB lithography and wet chemical etching. Then, Au/Ge/Ni ohmic contacts were formed. Finally, Schottky IPG or WPG electrodes with a few hundred nm intervals were defined by EB lithography, and formed either by Pt plating using an in-situ electrochemical process for IPG structures [18] or by conventional Cr/Au lift-off process after removing SiO_2 layer for WPG structures, respectively. SEM micrographs of fabricated double-dot IPG SET and 18-dot WPG SETs are shown in **Fig.9-3(a)** and **9-3(b)**, respectively.



(a)



(b)

Fig.9-3. Plan-view SEM images of (a) double-dot IPG SET and (b) 18-dot WPG SET.

9.4 Experimentally observed transport characteristics of SETs

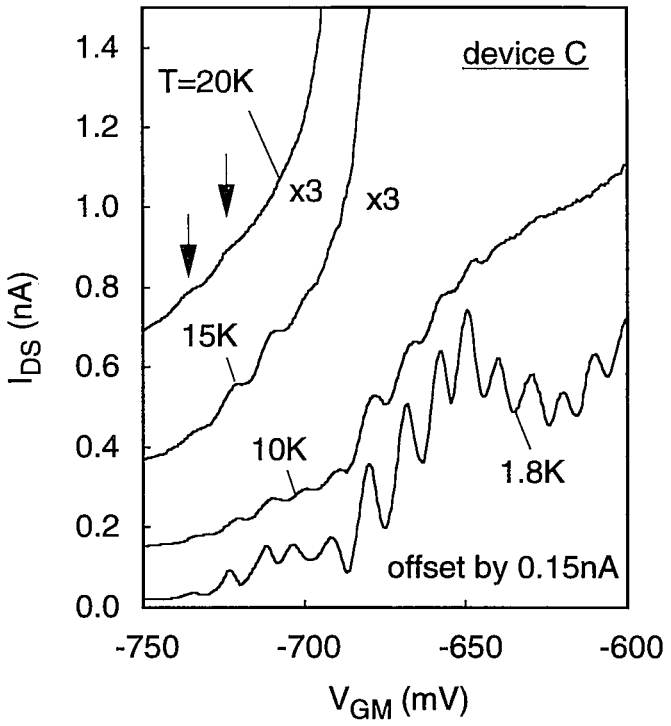
9.4.1 *Conductance oscillation characteristics in single-dot SETs*

The transport of single-dot SETs in **Fig.9-2(c)** with different device dimension, device A~D was characterized. The example of the observed conductance oscillations of device C and D are shown in **Figs.9-4(a)** and **9-4(b)**, respectively. All of the single-dot devices showed clear conductance oscillation characteristics. Conductance oscillation in device D with d_F=200nm was visible up to T_{max}=30K, which was much higher than that of the split-gate SETs. The observed Coulomb gap ΔV_Σ of the device D was 10mV, also corresponding to the observed T_{max} of 30K.

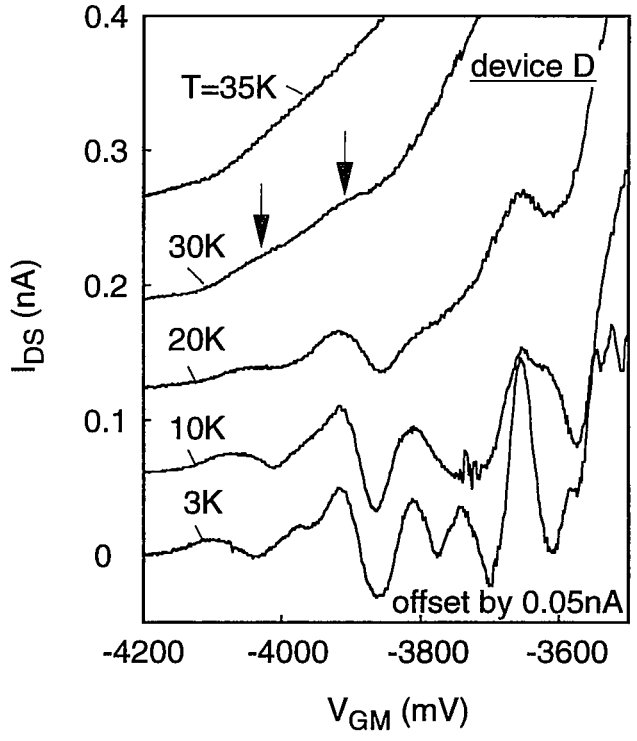
The observed conductance oscillation characteristics and device dimension are summarized in **Table 9-1**. The strong correlation between maximum temperature of conductance oscillation observation T_{max} and the device dimension was observed. T_{max} obviously increases with decrease of device dimension. Since the effective channel width can be change by control of main gate bias V_{GM}, then d_F directly reflects on dot size and charging energy U, as seen in simple relationship of k T_{max}~U=e^2/C_Σ~$1/d_F$. From the relationship, further reduction of finger gate spacing into 50 nm should realize 77-300 K operations of the novel SET devices.

9.4.2 *Conductance oscillation characteristics of multiple-dot SETs*

Figure 9-5(a) and **(b)** show the conductance oscillation on the double-dot SET in **Fig.9-3(a)** for different finger gate bias condition. In this device, 2DEG bar width W=780nm, finger gate spacing d_F=200nm and metal finger gate width L_{GF}=200nm were realized. It was seen that the behavior of the conductance oscillation was changed by changing gate bias condition. In the case of high negative finger gate



(a)



(b)

Fig.9-4. Conductance osicllations of single-dot IPG SETs

Table 9-1.
Device dimension and conductance oscillation characteristics of single-dot SET devices.

device	d_F (nm)	L_{GF} (nm)	W (nm)	ΔV_G (mV)	ΔV_Σ (mV)	T_{max} (K)
A	600	400	600	5~10	–	3.4
B	600	200	800	10~20	–	10
C	400	200	550	10~15	6	20
D	200	200	600	70~100	10	30

ΔV_G : conductance oscillation period
ΔV_Σ : observed Coulomb gap
T_{max} : maximum temperature of conductance oscillation observation

bias condition as shown in **Fig.9-5(a)**, the doublet peaks due to inter-dot coupling were observed, which corresponded to the behavior expected by classical capacitive charging model.[2] On the other hand, in lower negative finger gate bias condition as shown in **Fig.9-5(b)**, 4-pair peaks were observed near drain current pinch-off, which could not be explained by the classical model. This indicates the effect of quantization energy due to electron confinement. With increase of main gate bias V_{GM}, the oscillation behavior became stochastic. Sweeping middle finger gate bias V_{GF2}, position of each 4-pair peaks changed, but not monotonously.

Figure 9-6(a) shows the conductance oscillation characteristics of the 3-dot WPG SET device. The device dimension was W=1200nm, d_F=130nm and L_{GF}= 70nm. This device showed an unique characteristics. Fine conductance oscillation peaks with a period of 2.0~2.5mV were observed. 6 of these peaks seemed to be defined as a group with a period of about 10mV. This behavior could not be explained by the classical capacitive coupling model which predicted triplet peak separation by a 3-dot device.[2] The peaks in each group showed the nearly same amplitude of conductance. The amplitude decreased exponentially with decrease of gate voltage, such as $0.2e^2/h \rightarrow 0.1e^2/h \rightarrow 0.04e^2/h \rightarrow 0.02e^2/h$. **Figure 9-6(b)** shows the I_{DS}-V_{DS} characteristics of the 3-dot SET. In the curves, the voltage gaps seemed to be Coulomb gap could be clearly seen in certain gate bias. These gaps changed with increase of the gate voltage. The maximum value of the observed gap was about 5mV. The negative resistance characteristic was also observed when $|V_{DS}|$>5mV. This characteristic seems to be due to resonant tunneling.[19]

Conductance oscillation characteristics of 18-dot and 37-dot WPG SET devices are shown in **Figs.9-7(a)** and **9-7(b)**, respectively. Realized device dimensions were W=770nm, d_F=170nm and L_{GF}=30nm for the 18-dot device and W=1300nm, d_F=160nm and L_{GF}=40nm for the 37-dot device, respectively. These multiple-dot SETs showed clear and regular conductance oscillations rather than the 3-dot devices

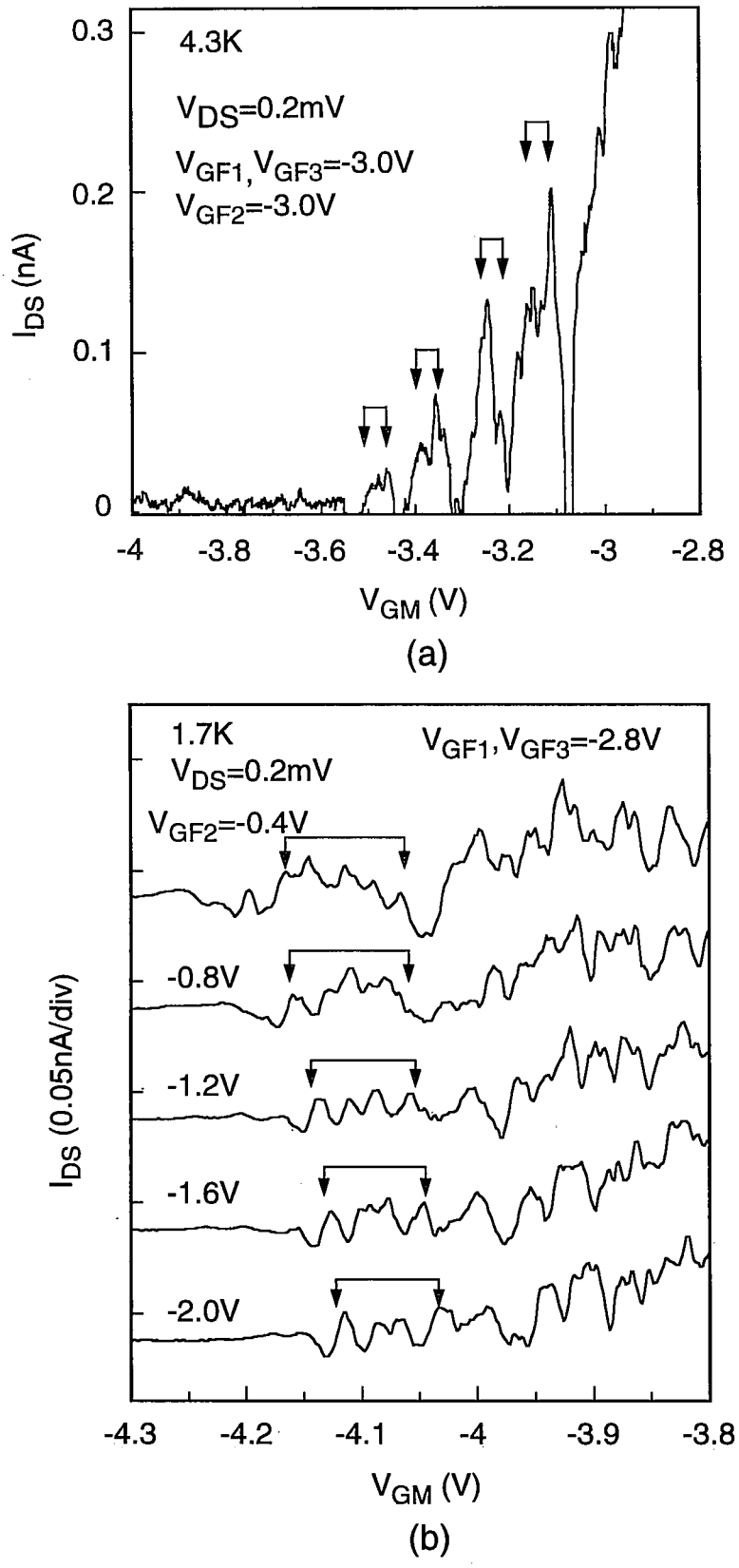


Fig.9-5. Conductance oscillations of double-dot IPG SET for different finger-gate bias conditions.

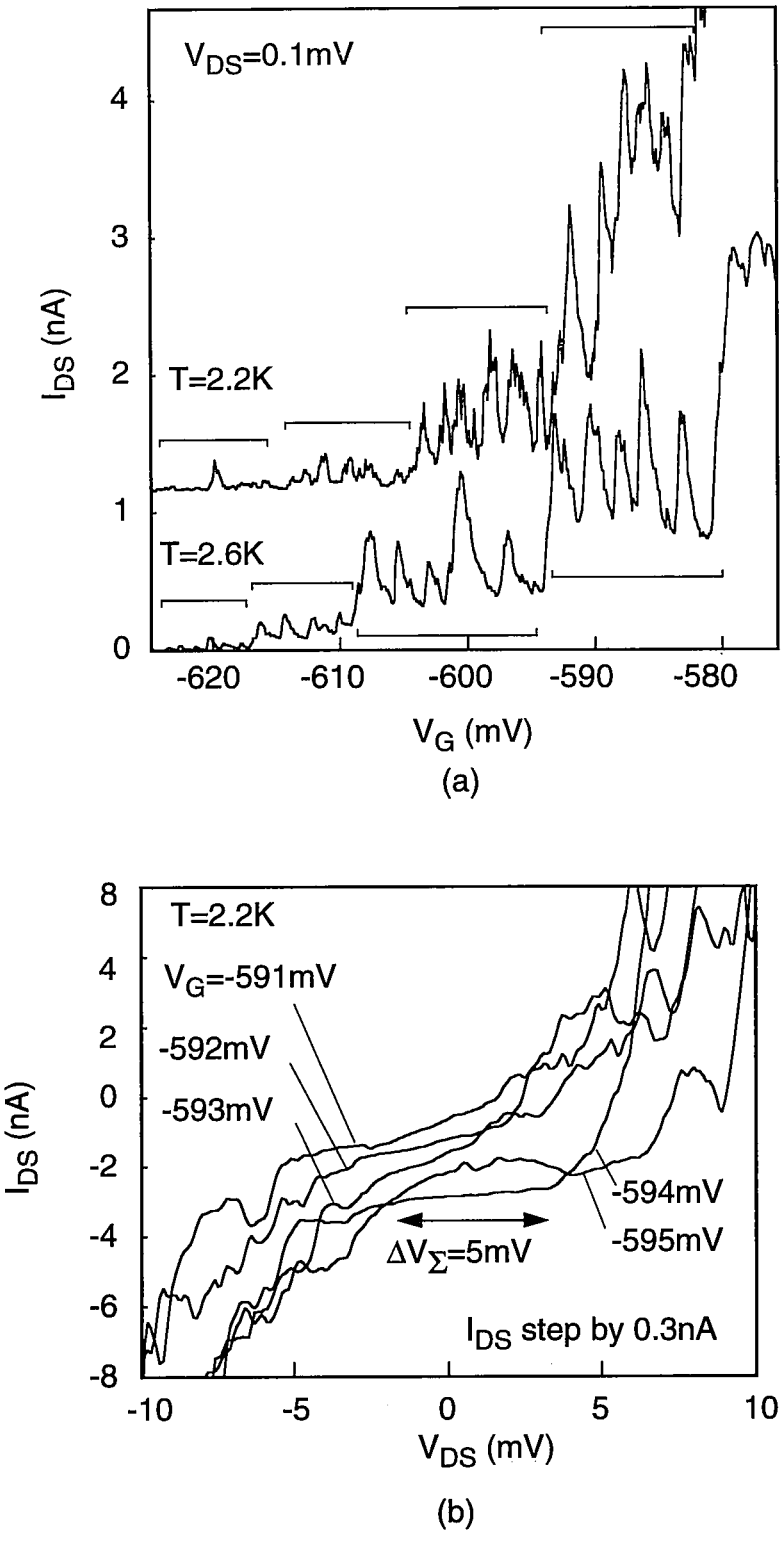


Fig.9-6. (a) Conductance oscillation and (b) I_{DS}-V_{DS} characteristics of 3-dot WPG SET.

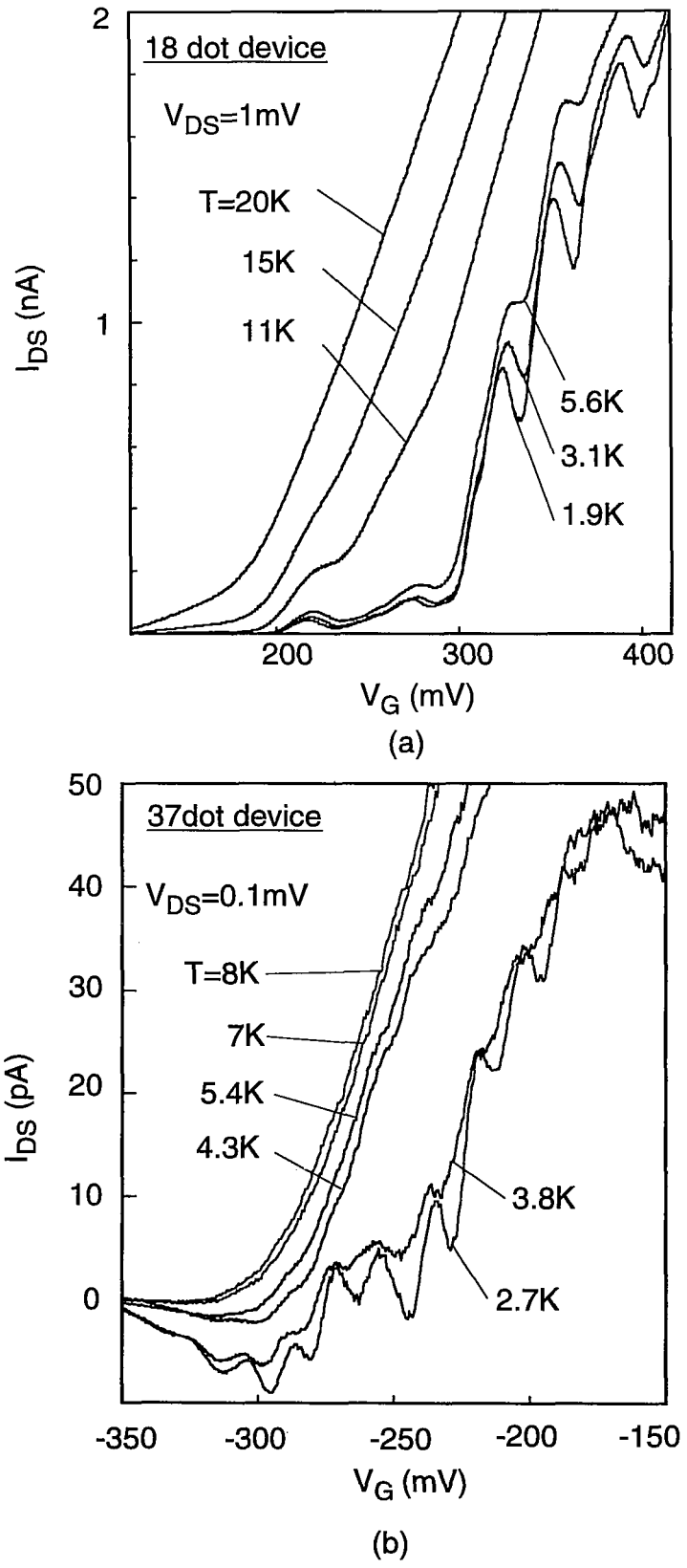


Fig.9-7. Conductance oscillation of (a) 18-dot and (b) 37-dot WPG SETs.

and behaved essentially like a single-dot SET device. The conductance oscillation of the 18-dot SET in **Fig.9-7(a)** was observed up to 15K even when V_{DS}=1mV. The conductance oscillation of the 37-dot SET in **Fig.9-7(b)** could be observed at 5K, even if the channel width W was as wide as 1300nm.

9.5 Simplified theoretical analysis and interpretation of experiments

9.5.1 *Simplified theoretical analysis of single-dot SET*

Quantitative analysis of Coulomb blockade characteristics of a single-dot SET was demonstrated by potential simulation with simple theory. Potential distributions in the Schottky IPG structures were calculated in the classical regime by solving 3-dimensional (3D) Poisson's equation with the successive over relaxation (SOR) method. The inset of **Figure 9-8(a)** shows the example of the plan view of calculated potential profile of the single-dot IPG SET, device C in **Table 9-1**. Formation of quasi-elliptic dot is clearly seen. The calculated dot size and charging energy as a function of main gate bias V_{GM} are shown in **Figure 9-8(a)**. The dot size was determined as the area of the dot equals to that of a circle whose radius was R. The dot capacitance C_Σ was estimated by $C_\Sigma=8\varepsilon R$, where ε is the permittivity.[12] It is found that the dot size comes to be 20nm and then charging energy reaches to 10meV with decrease of V_{GM}. However, this value is somewhat larger than the experimental result. The possible reason for this is that the tunnel barrier becomes large when V_{GM} far decreases and the electron tunneling becomes impossible before the dot size reaches to such a small size.

Peak intervals of the conductance oscillation for the single-dot SET device were also simulated by using the 3D potential calculation. The peak interval ΔV_G was calculated semi-classically using the next equation.

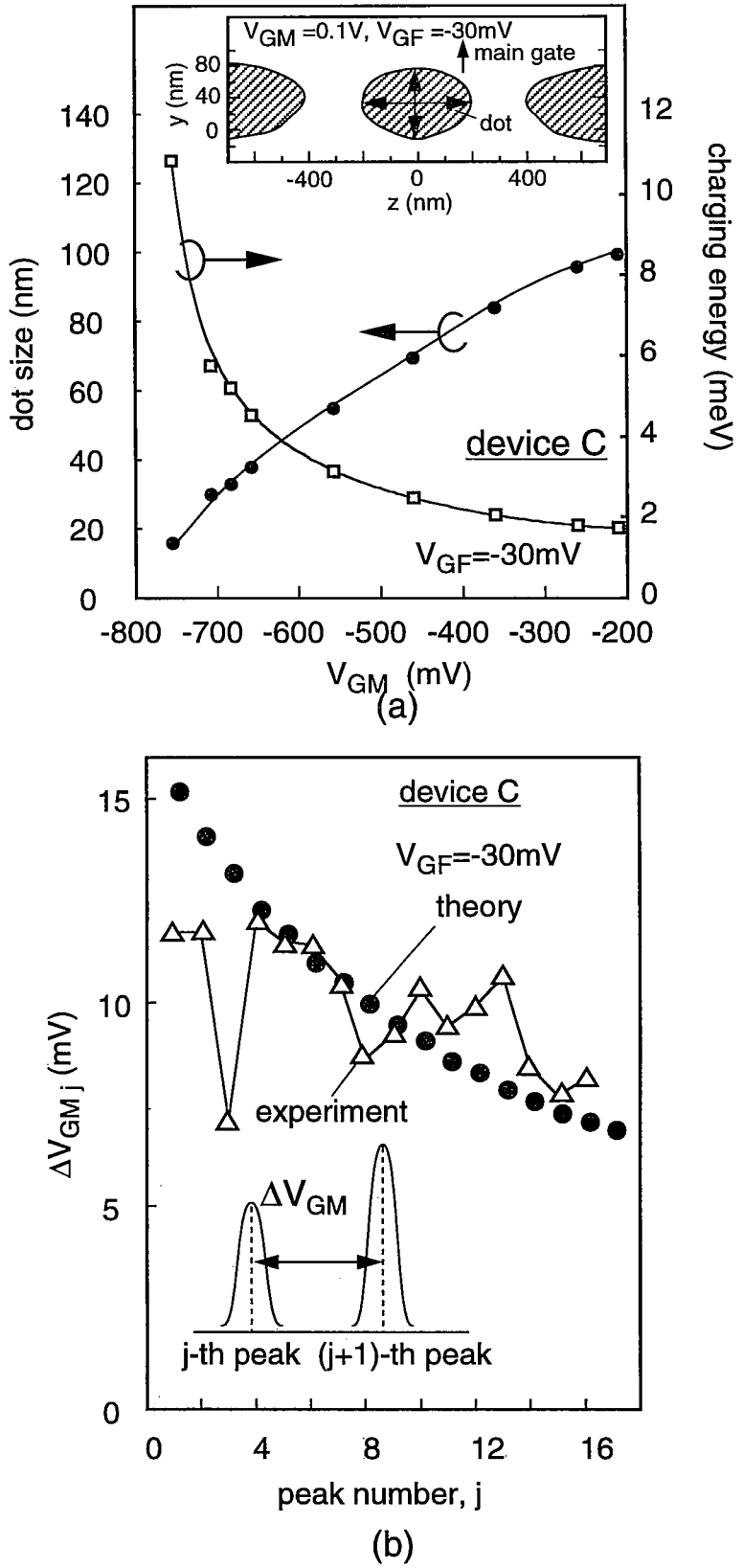


Fig.9-8. (a) Simulated dot size and charging energy of a single-dot SET. (b) Comparison of conductance peak separation between theory and experiment of the single-dot SET.

$$ne = \int_{-\infty}^{V_{G\,n-th}} C_G(V_G)\, dV_G \qquad (9.6)$$

where n is integer and C_G is the differential gate capacitance. C_G is given by

$$C_G(V) = \frac{\partial Q}{\partial V_G} = e\frac{\partial n_e}{\partial V_G} \qquad (9.7)$$

where n_e is the electron number in the dot. n_e is counted classically by applying the 3D density of states. The gate voltage that satisfies **eq.(9.6)** gives the n-th conductance peak. The relationship between ΔV_G and peak number, j, from experiment and theory for single-dot SET (device C) is shown in **Fig.9-8(b)**. Reasonably good semi-quantitative agreements were obtained between theory and experiment. However, some irregularity was seen in experimental data. This indicates that the effect of quantization energy due to electron confinement is revealed even when the gate spacing d_F=400nm. Such irregularity seems to occur when the quantized energy state that the electron passes through changes. Far more investigation including self-consistent analysis of quantum mechanical effect and electrical potential needs for full understanding of the experimental result.

9.5.2 *Interpretation of conductance oscillation in the multiple-dot SETs*

Double-dot IPG SET

Two different behaviors of conductance oscillation were observed in the double-dot IPG SET. This predicts that the transport mechanism is changed by the finger gate bias condition, which seems to correspond to two models in **Figs.9-9** for the conductance oscillation of double-dot SETs. **Figure 9-9(a)** schematically shows the classical capacitive charging model for peak splitting due to inter-dot coupling in

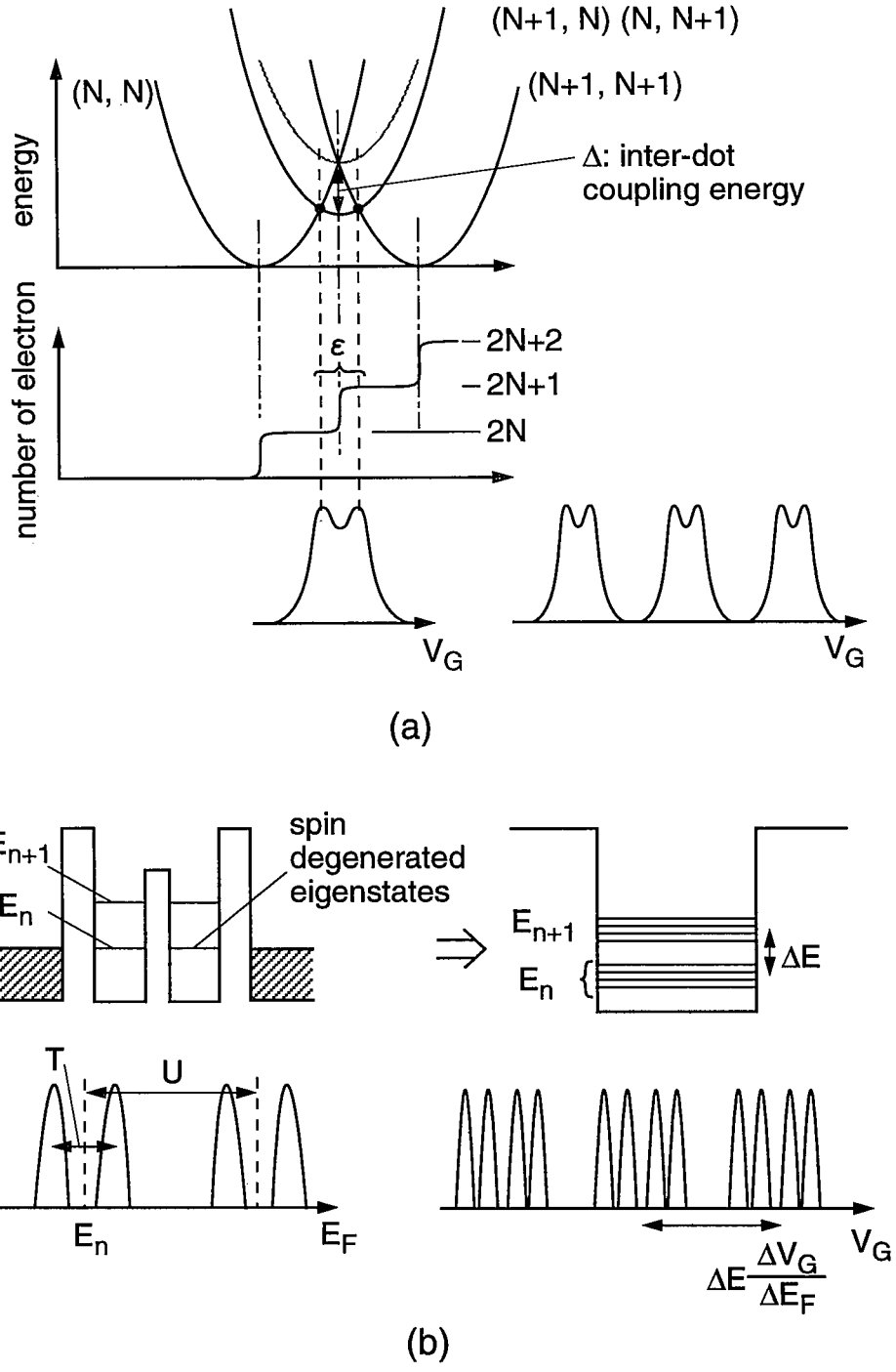


Fig.9-9. Transport models of a double-dot SET in the case of (a) U>ΔE and (b) U<ΔE.

a double-dot SET.[2] This model is applicable when charging energy U is larger than quantized energy ΔE due to electron confinement. Each zero inter-dot coupling eigenstate with definite particle number N on the each dot gives rise to a parabola. The center parabola corresponds to the condition that odd number of electrons are in the system, as indicated by $(N, N+1)$ or $(N+1,N)$ in **Fig.9-9(a)**, is shifted down by inter-dot coupling, then the degenerated states are split and the conductance peak splits into doublet peak as shown in **Fig.9-9(a)**. This model can explain the doublet peaks in **Fig.9-5(a)**. On the other hand, when the quantized energy is lager than the charging energy, the transport mechanism is switched. Conductance peak is dominated by quantized energy and it is corrected by charging energy as shown in the model in **Fig.9-9(b)**.[3-5] In the two dot system, quantized eigenstates due to electron confinement are degenerated in each quantized levels. The number of degenerated states equals to the multiplication of the number of dots and spin degeneracy, then this system can be treated as virtual one dot system having 4 fold degenerated states at each quantized level as shown in **Fig.9-9(b)**. The degenerated eigenstates in each dot are separated by inter-dot coupling and charging energy. Then, in the double-dot device, the conductance peak from each quantized levels splits into 4-pair peaks, which explains the result of 4-pair peaks in the **Fig.9-5(b)**.

From the gate bias condition, the dot size in **Fig.9-5(a)** was expected to be smaller than that in **Fig.9-5(b)**.[13] Then, it seemed that quantized effect became more dominant in **Fig.9-5(a)**. However, as shown in **Fig.9-8(a)**, when the dot size becomes small enough, it is possible that the charging energy becomes larger than quantized energy. Thus, the oscillation characteristics in **Fig.9-5(a)** is dominated by charging effect and then the behavior seems to be close to that expected by the classical model in **Fig.9-9(a)**. The shift of each peak in the pair observed in **Fig.9-5(b)** was not monotonous with the change of middle gate bias V_{GF2}. However, in the present double-dot SET structure, the dot size was also changed by decrease of V_{GF2}.

It was reported that the inter-dot coupling energy T also depended on the dot size and indicated that T increased with decrease of dot size.[3] Because the position of each peak was determined by the balance between the charging energy U and T ,[3-5] observed behavior of peak positions seemed to be possible.

3, 18, 37-dot WPG SET devices

In the present 3, 18 and 37-dot WPG SETs with the structure shown in **Fig.9-2(e)** and **9-2(f)**, the gate spacings d_F were narrow such as 130~170nm. And these devices did not have main gates which control effective wire width, then the dot size could not be small compared with the present single and double-dot IPG SETs. Thus, in the case of the present 3, 18 and 37-dot WPG SETs, quantized energy spacing ΔE is expected to be over the charging energy U.

The grouping of conductance oscillation peaks in the 3-dot SET is considered to be brought by the situation that the quantized energy is over the charging energy. In this case, based on the model in **Fig.9-9(b)**, the 3-dot system can be treated as virtual one dot system having 6 fold degenerated states. The degenerated states are separated by charging energy and inter-dot coupling and this results in 6 peaks in one quantized level as shown in **Fig.9-10**. Nearly same amplitude of the peaks in each group indicates that the transition probability depends strongly on the quantized energy level as schematically shown in **Fig.9-10**. The difference of dot to lead transition probability for each quantized levels seems to cause such a situation.

For detail analysis of the oscillation behavior of multiple-dot WPG SETs under the condition of $\Delta E>U$, we calculated peak separation due to inter-dot coupling and charging effects by the Hubbard model,[3-5] using Hamiltonian, H, taking account of charging effect and inter-dot coupling. The exact solution of the Hamiltonian shows that the conductance based on one quantized energy level has two groups separated by roughly the charging energy U which correspond to Hubbard band, and each

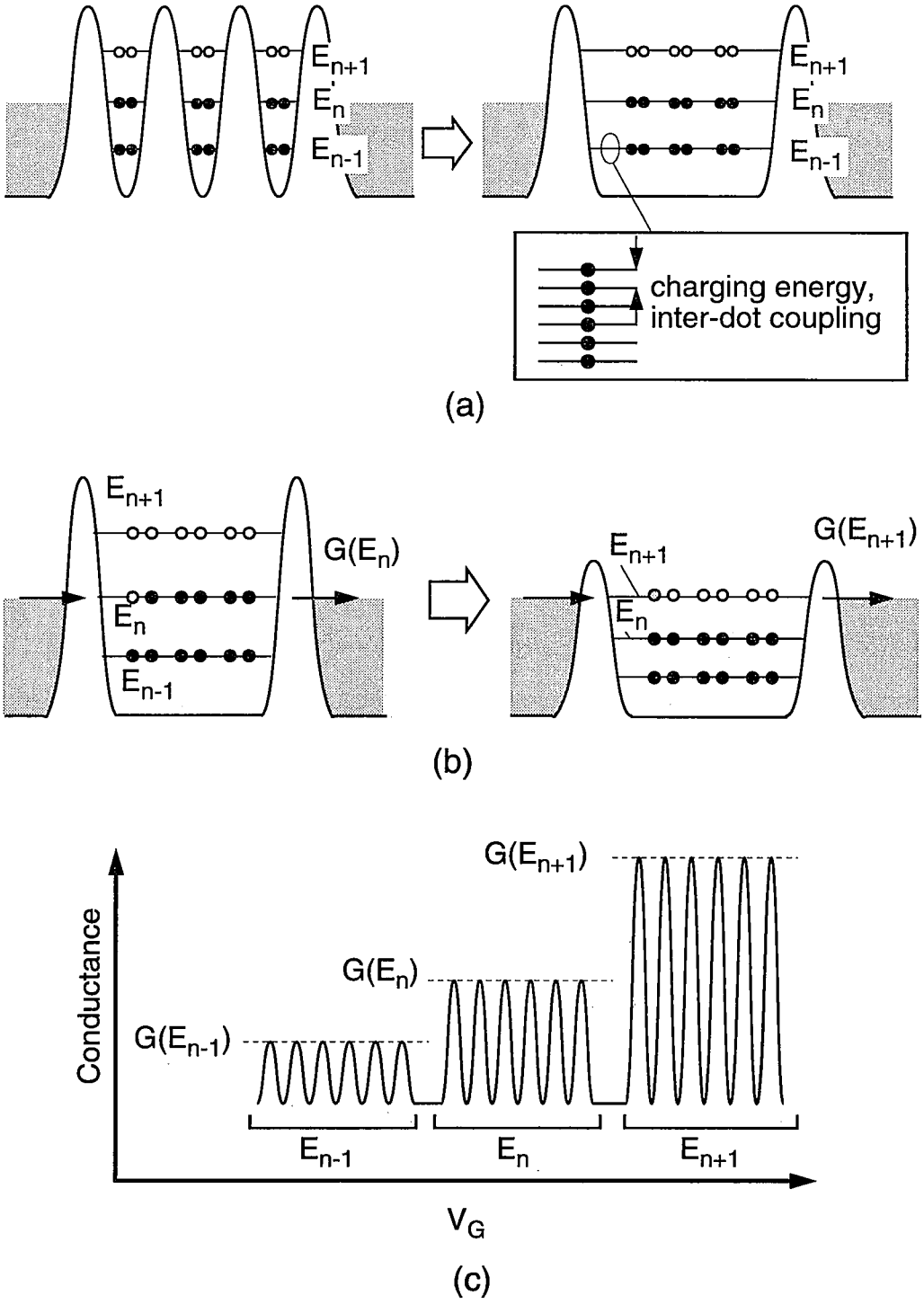


Fig.9-10. The conductance oscillation model of the 3-dot WPG SET.

group has a number of peaks by inter-dot coupling energy T equals to the number of dots, when $U>T$.[4] Therefore, only the next equation have to be evaluated for estimation of peak separation by inter-dot coupling effect, assuming $U>T$.

$$\det|H-E|=\begin{vmatrix} E_n-E & T & 0 & \cdots \\ T & E_n-E & T & \cdots \\ 0 & T & E_n-E & \cdots \\ \vdots & \vdots & \vdots & \ddots \end{vmatrix}=0 \qquad (9.8)$$

where E is the eigenenergy and E_n is the n-th quantized energy. The number of column and low corresponds to the number of dots in an array. For example, including the charging energy U, all of the eigenstates are $E=E_n \pm T, E_n+U\pm T$ for two-dot system and $E=E_n$, $E_n \pm T\sqrt{2}$, E_n+U, $E_n+U\pm T\sqrt{2}$ for three-dot system.

From the observed Coulomb gap and potential simulation of the 3-dot SET device, the charging energy U is estimated about 1~2meV. Inter-dot coupling energy can be estimated by using $T\sim 4h^2/m^*d^2$, where m^* is the effective electron mass and d is the dot size.[3] Estimated T is about 0.3~0.4meV, which is about 1/3~1/5 of charging energy. These estimated values can be explain nearly equal spacing of the fine peaks in Coulomb oscillation of the 3-dot SET. **Figure 9-11** shows the calculated peak separation from a quantized energy level by charging energy and inter-dot coupling for various numbers of dots using **eq.(9.8)** when $U:T$=1:0.4. As shown in this figure, the larger the number of dots becomes, the narrower separation of peaks becomes with the same inter-dot coupling energy. The peak separation can be observed when the peak interval is larger than thermal broadening kT. When T is 0.3~0.4meV, the peak separation can be observed in a few Kelvin for 3-dot SET, but not for 18 and 37 dot SETs. Therefore, in multiple-dot SETs having large number of dots, the fine peaks due to inter-dot coupling are smeared out and conductance oscillation may be

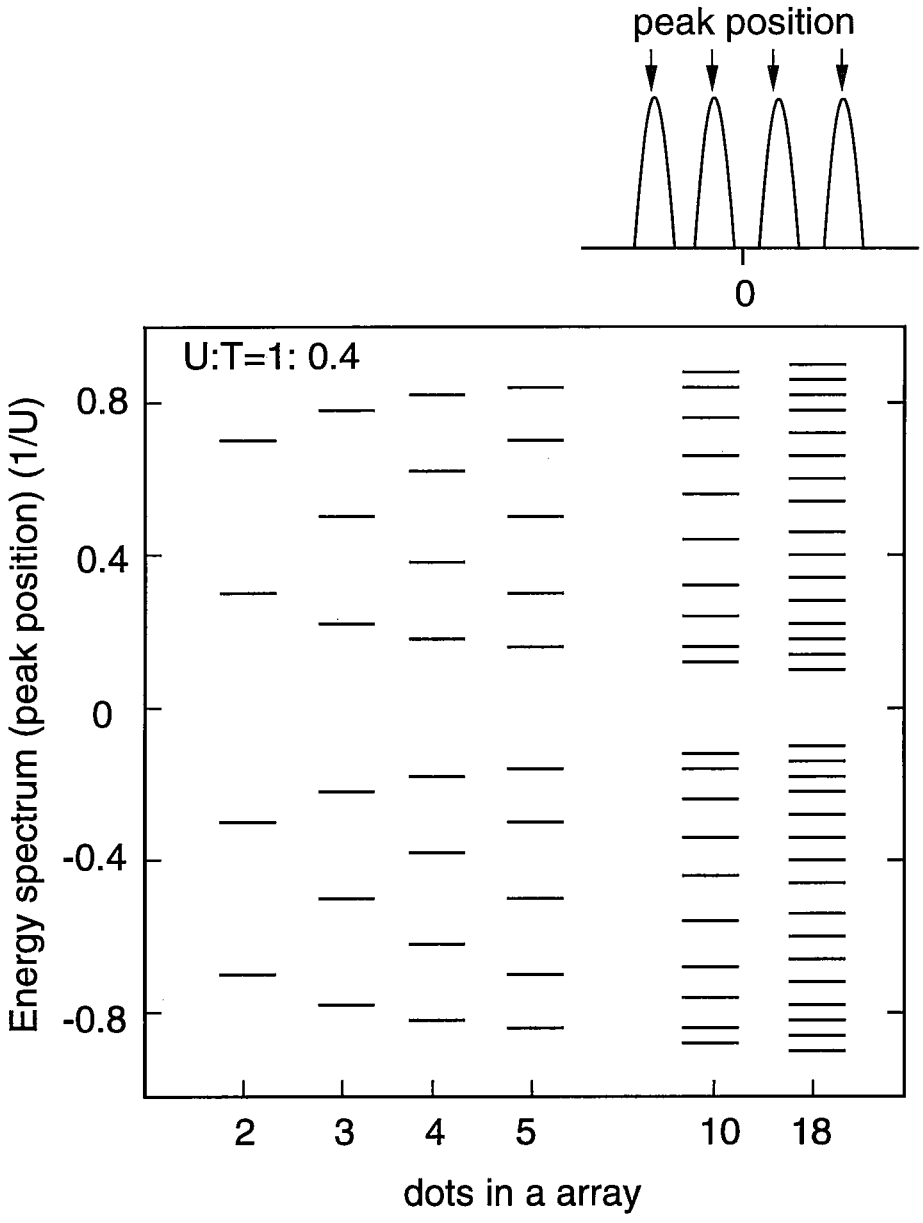


Fig.9-11. Calculated energy spectrum (peak position) caused by inter-dot coupling and Coulomb interaction for various number of dots in a quantum-dot array.

simplified rather than that of the 3-dot SET. However, if we can control the inter-dot coupling and charging energy, it will be possible to observe more interesting peak separation behavior in the conductance oscillation of the multiple-dot SETs.

9.6 Conclusions

Single-dot and multiple (2,3,18 and 37)-dot SETs based on the control of 2DEG with Schottky in-plane gate (IPG) and wrapped gate (WPG) geometries were fabricated on AlGaAs/GaAs heterostructures by EB lithography and their transport properties were characterized. Main conclusions are listed below.

(1) All the fabricated SETs showed Coulomb blockade like conductance oscillation with the gate voltage.

(2) Single-dot SET devices realized by Schottky IPG could be operated in high temperatures up to 30K. Fabricated single-dot SETs shows the strong correlation between device dimension and temperature limit of conductance oscillation, which predicts more higher temperature operation can be achieved by optimization of the device dimension.

(3) Simplified theoretical analysis based on computer simulation was done for a single-dot SET and semi-quantitative agreements were obtained between theory and experiment. Some irregularity in the experiment indicates the interplay between quantization energy due to electron confinement and charging effect.

(4) The double-dot SET showed the peak separation due to inter-dot coupling in the conductance oscillation. Doublet or 4-pair peaks were observed by changing gate bias condition. This indicates that the relationship between charging energy and quantized energy was changed by the gate bias condition.

(5) The 3-dot SET with reduced inter-gate dimension of 130nm showed six peak pairs in conductance oscillation indicating dominance of quantized energy by

electron confinement over charging energy. On the other hand, 18 and 37-dot SET behaved essentially like single-dot devices above 1.9K due to smearing out of fine energy separations by thermal broadening.

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Chapter 10

Summary and Conclusions

The purpose of this work is to find and establish a systematic method of control of III-V compound semiconductor Schottky barrier and to apply these Schottky barriers to quantum effect devices.

Summary and conclusions of the present work are the following:

In **chapter 3**, in order to control Schottky barrier of III-V compound semiconductor precisely, the theoretical analysis of control of Schottky interface, mainly for the method using an interface control layer (ICL), was done from the point of view not only Schottky barrier height (SBH) but also forward and reverse current transport. The main conclusions are listed below:

(1) Metal/semiconductor interfaces with and without ICLs were modeled and interface index S was calculated by using the DIGS model. S was modified by inserting an ICL, which depended on the ICL material.

(2) SBH controlled by Si ICL was calculated by the numerical potential simulation taking account of the band gap narrowing by strain and interface state effect. It was found that these effects limited the range of the SBH control. For sufficient control of SBH, it needs that the factor $N_{ICL}/\varepsilon_{ICL}$ is more than 10^{19} cm$^{-3}/\varepsilon_0$, and interface state density N_{SS} at ICL/semiconductor interface is less than 10^{12}cm^{-2}eV^{-1}.

(3) The Richardson constant A^{**} reduced anomalously even if the thickness of the ICL was less than 10Å and deteriorate the forward current transport. Such a reduction could not be caused by the use of Si ICL.

(4) Reverse leakage current was investigate using the DIGS model. The low permittivity of ICL and low N_{SS} at ICL/semiconductor interface caused large leakage current. Such a current could be suppressed by using a material having large

permittivity which is more than $10\varepsilon_0$.

(5) From these results, the requirements of ICL material are found to be moderate band gap and band line-up with the semiconductor, thin film, high doping concentration more than $10^{20}cm^{-3}$, high permittivity and low N_{SS}.

In **chapter 4**, for control of metal/III-V compound semiconductor interfaces of GaAs and InP by an interface control layer (ICL), optimization of ICL including thin and thick oxide ICLs and Si ICL is studied and discussed from the points of view not only Schottky barrier height but also current transport through the interfaces. The main conclusions are listed below:

(1) With oxide ICL, unintentional interface reaction was caused by formation of metal and it brought complex interface structure, which produces uncontrollablility and instability of Schottky barrier. M-S interface with Si ICL gives simple and coherent interface structure.

(2) Richardson plots show that the Si ICL does not block thermionic emission current transport. Richardson constants with oxide ICLs are anomalous reduced and the ICLs block the current transport even if the thickness is about a few 10Å.

(3) Poor reverse leakage current properties are observed in Schottky diodes with thick oxide ICLs. This correlates strongly with interface states density at ICL/semiconductor interface and the permittivity of ICL. Such a current is suppressed by using Si ICL.

In **chapter 5**, the Schottky barrier height (SBH) control technique for metal/ GaAs and InP interfaces by Si interface control layer (Si ICL) is discussed experimentally. And the method to spatially control SBH using FIB for its application to quantum nanostructures. The main conclusions are listed below:

(1) The SBH can be systematically controlled by doping into the Si ICL in the range

of about 300meV for GaAs and 400meV for InP. And precise and continuous control can be achieved by changing doping concentration into the Si ICL until Si layer is psuedomorphic on the substrate semiconductor.

(2) As doping and B doping is effective, but Ga, Al doping is not.

(3) The experimentally observed behavior can be explained by theoretical models including ideal and relaxed cases, with the latter taking into account the effect of the interface state at the ICL/semiconductor interfaces.

(4) To achieve high-performance diodes with controlled and reproducible barrier heights, Si ICL should be kept pseudomorphic with GaAs.

(5) By FIB irradiation on Si ICL, SBH of Al/doped Si ICL/n-GaAs changes by 300meV and this method is found to be possible for spatial control of SBH in nanometer order. SBH depends on dose of FIB and this result indicates that the interface state is induced by FIB irradiation at Si ICL/GaAs interface and its density depends on the dose of FIB.

In **chapter 6**, InP Schottky diodes were fabricated by in-situ electrochemical process. Pt/n-InP Schottky diodes with high barrier heights (SBH=0.86eV) have been reproduciblly obtained for the first time by the novel in situ electrochemical process. This ideality factor is near unity. This novel high SBH process has led to the first realization of well-behaved InP MESFETs. Good gate control of drain current and an effective channel mobility of 1,840 cm^2/Vs have been achieved. The present InP MESFET operates even under the positive bias condition. Thus, the present in situ electrochemical process appears to be useful for realization of high-speed, low-power as well as high-power InP-based devices and integrated circuits.

In **chapter 7**, novel LSSL device structure based on Schottky barrier height (SBH) control using Si interface control layers (Si ICL) was proposed and fabricated. The main conclusions are as below.

(1) Basic design considerations were determined by 2D computer simulation of potential.

(2) The appearance of a periodic EBIC signal directly confirmed SBH modulation by Si ICL stripes.

(3) Marked periodic oscillations of drain conductance and transconductance were observed at low temperatures up to 10K. Their detailed behavior was distinctly different from that of previous split-gate devices.

(4) The mechanism of these oscillations can be explained by the sequential resonant tunneling model. A quantitative analysis of the data indicated that SBH difference of 70~150meV was produced, which resulted in quantized levels with a separation of

In **chapter 8**, attempts were made to characterize the depletion field profiles within the Schottky IPG based GaAs quantum nanostructures by the EBIC technique. Main conclusions are the following.

1) A simple theory on the EBIC signal from the basic Schottky IPG/2DEG developed here can explain the experimental results very well.

2) By taking account of the range of the electron beam, a direct, non-destructive and quantitative characterization of field profiles, depletion widths and Schottky barrier heights of the buried depletion layer becomes possible.

3) The results of applications of the EBIC technique to wires, lateral superlattices and multi-dot structures show the effectiveness of the Schottky IPG controls of 2DEG for realization defect-free compound semiconductor quantum nanostructures.

In **chapter 9**, Single-dot and multiple(2,3,18 and 37)-dot SETs based on the control of 2DEG with Schottky in-plane gate (IPG) and wrapped gate (WPG) geometries were fabricated on AlGaAs/GaAs heterostructures by EB lithography and their transport properties were characterized. Main conclusions are listed below.

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(3) Simplified theoretical analysis based on computer simulation was done for a single-dot SET and semi-quantitative agreements were obtained between theory and experiment. Some irregularity in the experiment indicates the interplay between quantization energy due to electron confinement and charging effect.

(4) The double-dot SET showed the peak separation due to inter-dot coupling in the conductance oscillation. Doublet or 4-pair peaks were observed by changing gate bias condition. This indicates that the relationship between charging energy and quantized energy was changed by the gate bias condition.

(5) The 3-dot SET with reduced inter-gate dimension of 130nm showed six peak pairs in conductance oscillation indicating dominance of quantized energy by electron confinement over charging energy. On the other hand, 18 and 37-dot SET behaved essentially like single-dot devices above 1.9K due to smearing out of fine energy separations by thermal broadening.