Optimization and Interface Characterization of a Novel Oxide-Free Insulated Gate Structure for InP Having an Ultrathin Silicon Interface Control Layer

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Attempts were made to characterize and optimize the novel oxide-free insulated gate structure for InP, having an ultrathin Si interface control layer (Si ICL). An *in situ* X-ray photoelectron spectroscopy (XPS) study indicated that P deficiency took place on the InP surface by the irradiation of a high-energy Si beam during the MBE growth of Si ICL. Based on this, a modified gate structure having an $In_{0.53}Ga_{0.47}As$ cap layer on the InP surface for prevention of phosphorus loss was proposed and its interface properties were investigated. A careful design for quantum state control indicated that the Si ICL thickness should be reduced down to 0.5 nm for the InGaAs cap thickness of 3 nm. *In situ* XPS spectra showed that no pronounced desorption of As or P took place from the surface in the new gate structure. In situ contactless *C-V* measurement showed a low and wide interface state density distribution with a minimum of 2×10^{11} $cm^{-2}eV^{-1}$. An InP MISFET test device with a gate length of 2 μm exhibited a maximum g_m of 123 mS/mm and a high drain current of 389 mA/mm. These results indicated the effectiveness of the novel oxide-free insulated gate structure for application to InP power MISFETs as well as to surface passivation.

KEYWORDS: InP, InGaAs, surface passivation, MISFET, XPS, UHV contactless *C-V*

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1. Introduction

InP has a higher electron saturation velocity and a higher thermal conductivity than GaAs. It has always been considered to be an excellent candidate for the channel material of high-power microwave and millimeter wave semiconductor field effect transistors (FETs). However, metal-semiconductor FETs (MESFETs) are difficult to realize due to low and unstable Schottky barrier heights. InP metal-insulator-semiconductor FETs (MISFETs) utilizing various native and deposited oxides have shown great promise in the past, but they suffered from severe drain current drifts due to the inclusion of chemically unstable In-oxide components.[1-2] MISFET devices using more stable oxide-free insulators such as Si_3N_4 showed low transconductance values due to high-density interface states at the insulator-InP interface.[3-4] These problems could be attributed generally to the poor interface control inherent in the conventional passivation structure where unexpected and unwanted reactions between InP and insulator materials produce defects, disorder and random strain, and it seriously hinders its exploitation. Thus, a new type of interface engineering is needed to achieve a high-quality insulator-InP interface for the realization of high-performance InP MISFETs.

A new approach using a Si interface control layer (Si ICL) has been proposed to passivate compound semiconductor surfaces.[5] According to this concept, an ultrathin Si layer inserted between the compound semiconductor and the outer insulator plays the role of terminating the surface bonds of the compound semiconductor and transferring bonds smoothly to those of a Si-based dielectric. This passivation method has been successfully applied for the fabrication of InGaAs MISFETs[6-7] and surface passivation of near-surface quantum wells[8] and quantum wires[9] for photoluminescence enhancement. Recently, we have used the passivation method to form an oxide-free insulated gate structure on InP[10]. Using this structure, stable operation of MISFETs with good gate control in both enhancement and depletion modes has been realized.[11] However, there was a problem that the reproducibility of successful processing was poor, being accompanied by a small transconductance (g_m) value which was smaller than the value expected from the Hall mobility measured before the fabrication of MISFETs.

The purpose of this paper is to clarify the reasons for the above problems in InP MIS structures having an ultrathin Si ICL and to solve them by a suitable gate-structure modification. In this study, an ultrahigh-vacuum (UHV)-based sample preparation and fabrication system was used. A detailed *in situ* XPS study was performed for chemical analysis of each step of the sample fabrication.

Electronic properties of the interface were examined by *in situ* XPS band-bending measurements, *in situ* UHV contactless *C-V*[3] and standard MIS *C-V* measurements as well as via fabrication of InP MISFET test devices. On the basis of the analysis, a modified insulated gate structure inserting an $In_{0.53}Ga_{0.47}As$ cap layer was proposed and it was found that this led to excellent interface properties for high-power InP MISFETs.

2. Experimental

Figure 1(a) shows schematically the UHV-based growth/processing/characterization multichamber system used in this study for the fabrication and characterization of samples. The structure of the novel oxide-free insulated gate for InP with an ultrathin Si ICL which we have been using is shown in Fig. 1(b). The sequence of sample fabrication and characterization is shown in Fig. 2. First, cleaned wafers were loaded into the gas-source molecular beam epitaxy (GSMBE) chamber. Before the growth of n-InP, the substrate temperature was generally increased up to 490^{o}C under a phosphorus gas ambient to remove the natural oxide. Then, a Si-doped n-InP epitaxial layer was grown using tertiarybutylphosphine (TBP) as P source. This was followed by MBE growth of an ultrathin (1 nm) Si ICL. The Si cell temperature was 1208^{o}C with a growth rate of ~1 nm/h. The reflection high-energy electron diffraction (RHEED) pattern was monitored during the growth.

Then, the samples were transferred into an electron cyclotron resonance-chemical vapour deposition (ECR-CVD) chamber through a UHV transfer chamber and partial nitridation of the Si surface was performed for 5 s at room temperature with a microwave power of 50 W and a typical nitrogen pressure of 10^{-4} Torr. This produces an ultrathin SiN_x film with a thickness of 0.4 nm and an average x value of 0.87 according to our previous *in situ* XPS study.[10] Although the film has a nonuniform and Si-rich composition, it functions well as an interfacial layer. After the growth of this SiN_x film, a thick Si_3N_4 film (12 nm) was deposited as the main gate dielectric at 300^{o}C in the ECR-CVD chamber using N_2 and SiH_4 gases and an rf power of 120 W.

At each step of fabrication, the sample was transferred to the XPS chamber and to the UHV contactless *C-V* chamber in order to investigate the surface and interface properties. *In situ* XPS analysis was carried out using a Perkin-Elmer PHI 1600 spectrometer with a spherical capacitor analyzer (SCA) under monochromatic Al Kα radiation at 1486.6 eV. The details of the *in situ* UHV contactless *C-V* technique have been described previously[12]. Contactless MIS *C-V* measurement was accomplished by utilizing a constant UHV gap of a few hundred nm as insulator. The gap is

maintained between the sample surface and the field plate by piezoelectric-control and capacitance feedback.

InP MISFET test devices were fabricated by forming an Al gate electrode and Au/Ge/Ni source drain ohmic contacts on the Si ICL-passivated wafer by the standard photolithography, vacuum deposition and lift-off processes.

3.Results and Discussion

3.1. RHEED observation and in situ XPS study

Prior to the MBE growth of InP, a clear (2×4) pattern shown in Fig. 3(a) appeared on the InP substrate surface under phosphorus overpressure when the substrate temperature was raised to 490^{o}C. This clear pattern not only indicates the removal of the natural oxide from the surface, but also the formation of a well-defined clean surface for the growth of an n-InP epitaxial film on the top. The (2×4) RHEED pattern was always maintained during the growth of the n-InP epitaxial film surface at the substrate temperature of 460^{o}C.

The growth of the Si ICL was performed at a substrate temperature of 270^{o}C. Although the phosphorus source was shut off during the Si growth, a high residual phosphorus pressure of 3 - 4 × 10^{-7} Torr persisted. After the start of Si beam supply, the RHEED pattern gradually changed to the (1×1) pattern. After the growth of a 1 nm-thick Si ICL, a sharp (1×1) RHEED pattern was maintained as shown in Fig. 3(b). This is a clear evidence that the growth of an ultrathin Si ICL occurs in a pseudomorphic fashion on the InP.

The interface chemistry of the InP surface for both before and after the growth of Si ICL was investigated by *in situ* XPS measurements. The chemical assignment of XPS peaks in both samples was simple. There was no O 1*s* peak (531 eV) and peaks of related oxidized components of other elements within the experimental detection limit. The angle-resolved XPS spectra of In $3d_{5/2}$ and P 2*p* core levels for the InP surface before and after the growth of Si ICL are shown in Fig. 4. After the growth of the Si ICL, In $3d_{5/2}$ and P 2*p* peaks showed no change in the shape and the peak width as shown in Fig. 4. At the same time, the energy positions of In $3d_{5/2}$ and P 2*p* shifted to the low-energy side by 100 meV after the Si ICL growth, indicating the reduction of band-bending. Unexpectedly, it was also clearly observed in Fig. 4 that the P 2*p* signal decreased markedly with respect to the In 3*d* signal after the growth of the Si ICL.

The relative concentrations of the surface atoms can be estimated from the integrated

intensities of XPS peaks and the values of the atomic sensitivity factor[13]. From this analysis, P/In atomic concentration ratios were found to be 0.98 and 0.78 for the InP surface before and after the growth of the Si ICL, respectively. Thus, the surface stoichiometry markedly changed during the Si ICL formation. This is most likely due to preferential desorption of P atoms from the InP surface.

It is known that phosphorus readily desorbs from the InP surface during thermal treatment even at low temperatures such as 200^{o}C due to its high volatility. Thus, in spite of the presence of a high residual phosphorus pressure, the main reason for the change of surface stoichiometry after Si ICL growth is thermal desorption of phosphorus which is possibly enhanced by direct irradiation of a high-energy Si beam on the InP surface. The observed deficiency of P on the InP surface should be the dominant cause for the poor process reproducibility and small g_m values of InP MISFETs with Si ICL in the previous study using the structure shown in Fig. 1(b).

3.2. A modified gate structure and its design

To suppress phosphorus desorption from the InP surface during MBE growth of Si ICL, a modified gate structure having an $In_{0.53}Ga_{0.47}As$ cap layer was investigated. The new structure is shown in Fig. 5. Here, an $In_{0.53}Ga_{0.47}As$ cap layer is used to cover the InP surface to prevent phosphorus loss.

However, since InGaAs has a much smaller band gap than InP, a careful design for quantum state control is required. For this purpose, the band line-up was calculated for the new gate structure using the model-solid theory[14]. The results are shown in Fig. 6(a). It is observed that extremely large band-gap narrowing of Si takes place due to the tensile strain. Based on these band line-ups, the energy position of the qualitized states in the Si ICL could be obtained by solving the Schrödinger equation. Figure 6(b) shows the calculated quantized energy levels for electrons and light holes in the Si ICL as a function of the Si ICL thickness for the new gate structure having an InGaAs cap layer of 3 nm thickness. It was found that the quantum well states of electrons can be completely removed by decreasing the Si ICL thickness to 0.5 nm.

From a practical point of view, delicate thickness control could only be realized by partial nitridation of the Si ICL surface at an ECR-excited nitrogen plasma.[10]

3.3. In situ characterization of the new gate structure

In situ XPS was used to examine the surface of a modified gate structure having an InGaAs cap layer. Figure 7 shows In 3*d* and As 2*p* core level spectra obtained from the surface before and after

Si ICL growth at 270°C. Similar peak shifts of In 3*d* and As 2*p* were observed after the growth of the Si ICL, although they are not clearly shown in Fig. 7 to directly compare the shapes and heights of peaks.

In contrast to the growth of Si ICL on InP, there was no change in the As 2*p* signal with respect to the In 3*d* signal before and after the growth of Si ICL. This means that no pronounced desorption of As took place during the Si ICL growth. This result could be attributed to the fact that the desorption of As from the InGaAs surface is more difficult than that of P from the InP surface. Additionally, by inserting an InGaAs cap layer, MBE growth of the Si ICL will not affect the surface of the important InP channel layer, and possible complex interface reactions are avoided.

The electronic properties of the interface of the new gate structure were investigated using the *in situ* UHV contactless *C-V* method. The measured contactless *C-V* curve of the Si ICL/InGaAs/InP structure after partial nitridation of the Si ICL surface using an ECR-excited nitrogen plasma is plotted in Fig. 8(a). The measured frequency was 500 KHz. A large variation of capacitance was obtained, being close to the calculated ideal *C-V* curve. This indicates that the surface Fermi level could be moved almost over the entire band gap of InP. The *C-V* curves were shifted to the positive side compared to the ideal curve. This could be due to the workfunction of the gate metal, interface state charge and fixed charge. A quantitative analysis has revealed that this is most likely due to the existence of negative fixed charge in the Si-rich SiN_x film. By using Terman's method[15], the interface state density (N_{SS}) distribution was calculated as shown in Fig. 8(b). A very wide Nss distribution with a low N_{SSmin} value of 2×10^{11} $cm^{-2}eV^{-1}$ was realized for the new gate structure. A similar Nss distribution was obtained in air by standard MIS C-V measurements on a MIS sample having a thick Si_3N_4 layer and Al field electrode. The N_{SSmin} value obtained in this study is larger than the N_{SSmin} value of 2×10^{10} $cm^{-2}eV^{-1}$ in the previous Si_3N_4/Si ICL/InP structure.[10] However, the width of the Nss distribution is much larger, allowing a full swing of the Fermi level over the entire energy gap. This is much more important for MISFET applications. The result was also much more reproducible than that in the previous study.

3.4. I-V characteristics of InP MISFET test devices

A schematic illustration of fabricated InP MISFETs test devices with a gate length of 2 μm is shown in Fig. 9(a). The measured I-V characteristics of an InP MISFET are shown in Fig. 9(b). Unfortunately, the Si_3N_4 film in this MISFET test device had a small breakdown voltage, and the device could be operated in the linear region. In spite of this, the device having a new gate structure

with an InGaAs cap layer showed a high g_m of 123 mS/mm and a high drain current level of 389 mA/mm. As compared with the previous InP MISFETs without the InGaAs cap layer[11], the g_m value was enhanced by a factor of 4. We believe that this is due to the improvement of the interface properties of the modified insulated gate structure. The nonsaturation of the drain current in Fig. 9(b) comes from the poor insulating property of the PCVD Si_3N_4 film. Although these results obtained are at a preliminary stage, they indicate the potential of the present InP insulated gate technology for high-power applications.

4. Conclusions

Attempts were made to characterize and optimize the novel oxide-free insulated gate structure for InP, having an ultrathin Si ICL. For the original insulated gate structure having a metal/SiN_x/Si ICL/InP configuration, an *in situ* XPS study indicated that deficiency of P took place on the InP surface through the irradiation of a high-energy Si beam during MBE growth of the Si ICL. A modified gate having an $In_{0.53}Ga_{0.47}As$ cap layer was then proposed. The *in situ* XPS study showed that it prevents desorption of As and P from the surface. The *in situ* contactless *C-V* method showed a low and wide interface state density distribution with a minimum density of 2×10^{11} $cm^{-2}eV^{-1}$. An InP MISFET test device with a gate length of 2 μm exhibited a maximum g_m of 123 mS/mm and a high drain current of 389 mA/mm, showing the potential for power MISFET applications.

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Fig. 1 (a) A UHV-based growth/processing/characterization multichamber system and (b) the original structure of an oxide-free insulated gate structure for InP with a Si ICL.

Fig. 2 Sequence of sample fabrication and characterization.

Fig. 3 RHEED patterns of MBE-grown InP surface (a) before and (b) after the growth of Si ICL .

Fig. 4 (a) In 3*d* and (b) P 2*p* XPS spectra from InP surfaces before and after the growth of Si ICL.

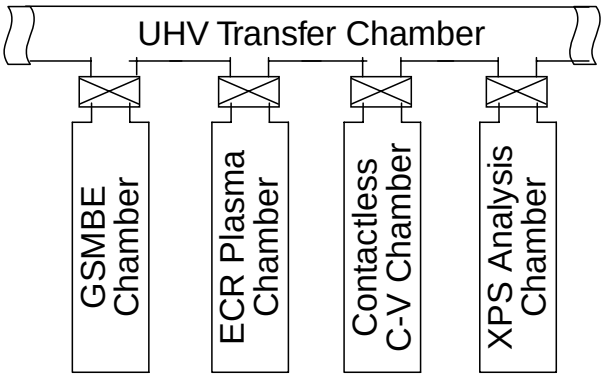
Fig. 5 A modified version of the oxide-free insulated gate structure for InP with Si ICL.

Fig. 6 (a) Band line-up of Si_3N_4/Si/InGaAs/InP insulated gate structures calculated by model-solid theory and (b) positions of quantum-confined ground state levels for electrons in the Si quantum well measured from the bottom of the InP conduction band.

Fig. 7 (a) In 3*d* and (b) As 2*p* XPS spectra from the InGaAs cap layer before and after the growth of Si ICL .

Fig. 8 (a) A UHV contactless *C*-*V* curve of the Si/InGaAs/InP structure and (b) N_{SS} distribution calculated by the Terman's method.

Fig. 9 (a) A schematic view and (b) *I*-*V* curves of a novel oxide-free InP MISFET test device with Si ICL.



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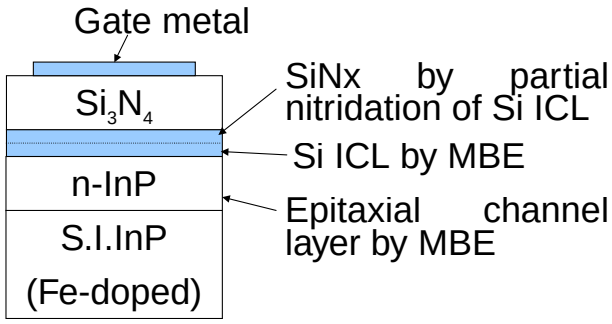

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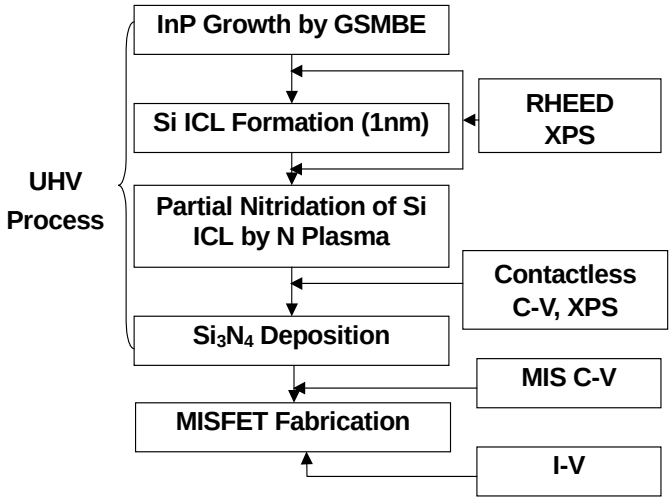

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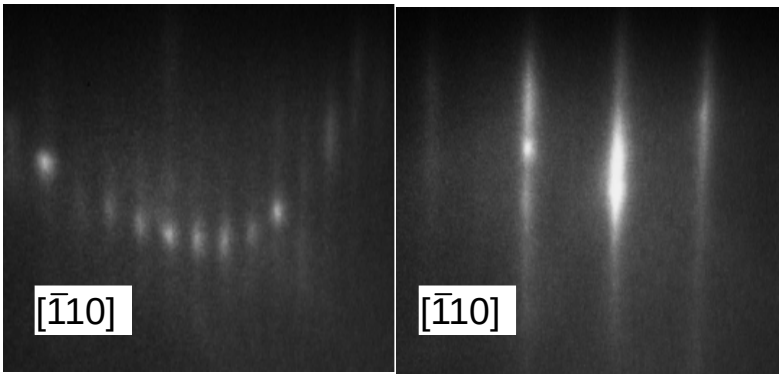

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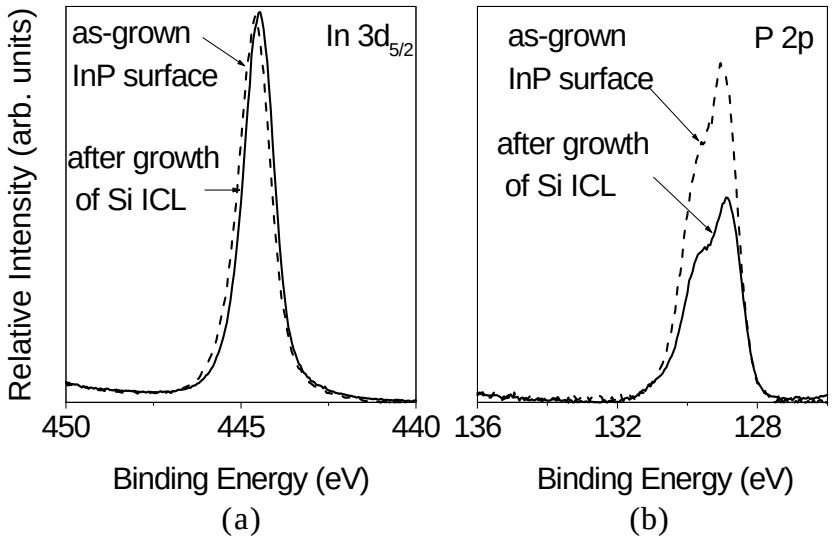

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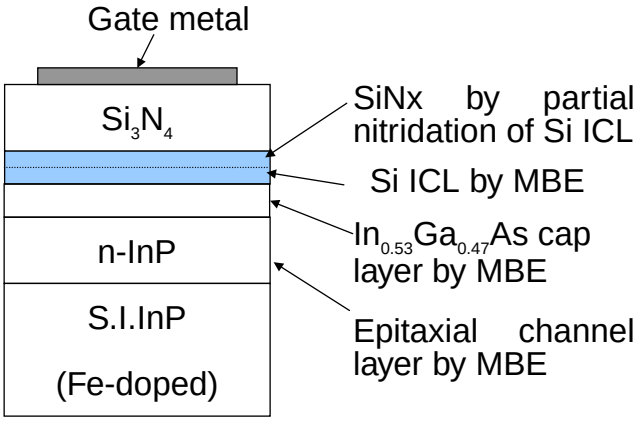

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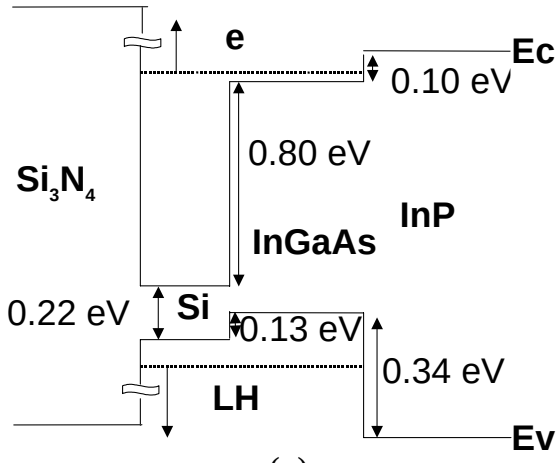

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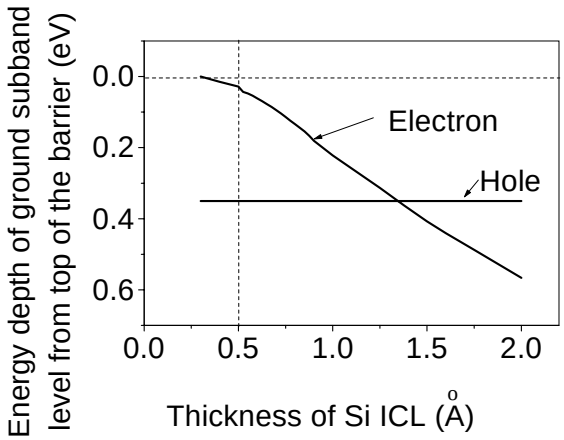

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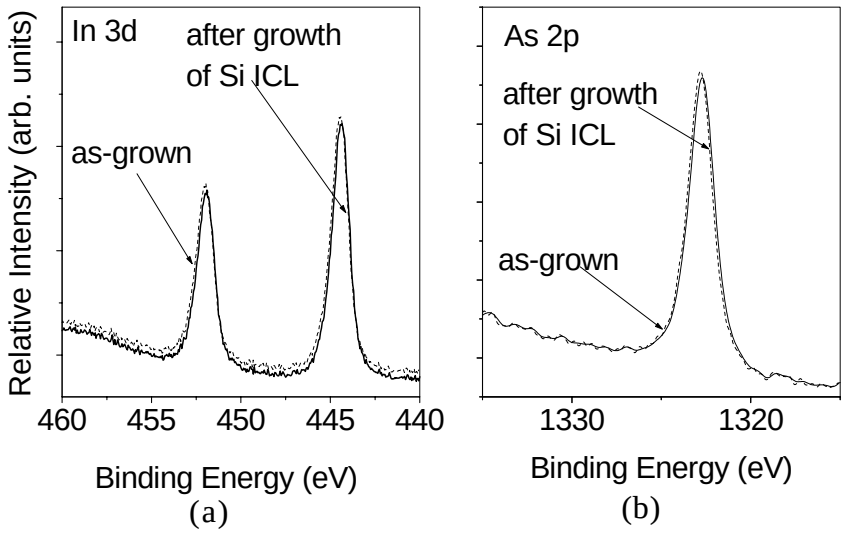

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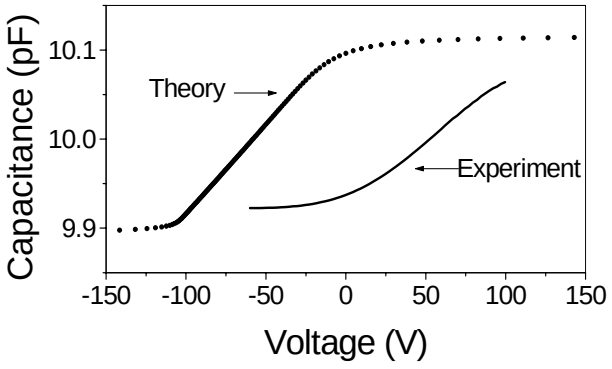

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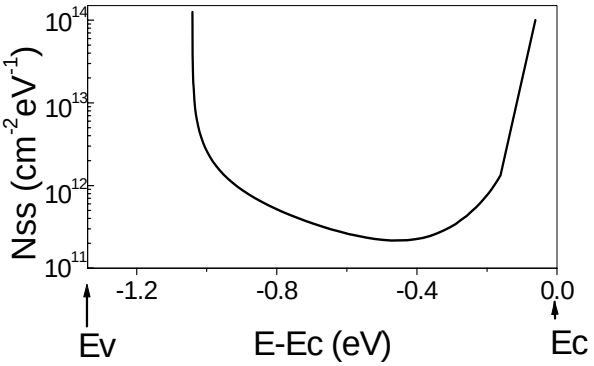

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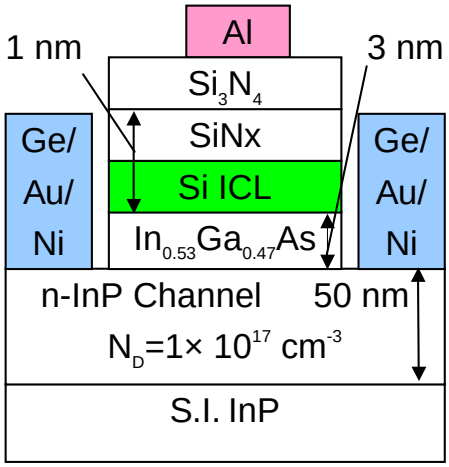

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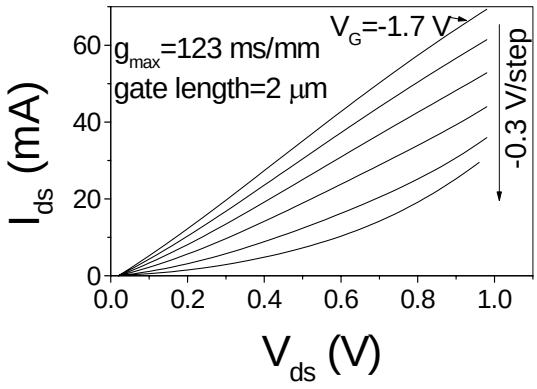

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