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The 8th International Micro-Process Conference July 17-20, 1995 Sendai, Japan

Transport Characterization of Schottky In-Plane Gate $Al_{0.3}Ga_{0.7}As$/GaAs Quantum Wire Transistors Realized by In-Situ Electrochemical Process

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The low-temperature transport properties of the novel $Al_{0.3}Ga_{0.7}As$/GaAs Schottky in-plane gate (IPG) quantum wire transistor realized by the in-situ electrochemical process were studied. The device showed good field-effect transistor (FET) characteristics with excellent gate control and complete pinch-off. Quantized conductance in the units of 2e2/h was clearly seen at 4K. The first plateau persisted up to 40K. Shubnikov-de Haas oscillation measurements showed an extremely weak dependence of the carrier density on the gate bias, indicating that the Schottky IPG controls the wire width without changing the sheet carrier density. Application of a magnetic field widened the conductance plateaus. Under harmonic approximation for the electrostatic confinement potentials, a subband spacing of hw0=4-5 meV was obtained.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Scanning Tunneling Microscope Study of (001) InP Surface Prepared by Gas Source Molecular Beam Epitaxy

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(001) InP surface prepared by gas source molecular beam epitaxy (GSMBE) using tertiarybutylphosphine (TBP) as P source was studied by ultrahigh-vacuum scanning tunneling microscope (UHV-STM), reflection high-energy electron diffraction (RHEED) and X-ray photoelectron spectroscopy (XPS). It was found that the P-stabilized (2×4) reconstructed (001) InP surfaces can be obtained by annealing the (2×1) reconstructed surface which contains excess phosphorus. (2×4) reconstructed surfaces were found to possess the missing-dimer arrangements with at least two microscopic structures, a phase with two missing-dimer

rows and b phase with one missing-dimer row, depending on the annealing temperature of the (2×1) surface. The (2×4)a phase is more stable with a wider range of annealing temperature, whereas the (2×4)b phase was obtained by annealing only near 330°C. The (2×4) a phase was observed even on a partially oxidized surface having many oxide patches, showing its remarkable stability.

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the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

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Photoluminescence and Cathodoluminescence Investigation of Optical Properties of InP-Based InGaAs Ridge Quantum Wires Formed by Selective Molecular Beam Epitaxy

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Optical properties of InP-based InGaAs ridge quantum wires formed by selective molecular beam epitaxy (MBE) growth were characterized in detail by using cathodoluminescence (CL) and photoluminescence (PL). Both the CL and PL spectra had strong emission peaks with narrow widths. Spot-excited CL images confirmed that these peaks originated from ridge quantum wires. Depending on the excitation power, emission peaks showed energy shift and half-width change due to band filling. Temperature dependence of the PL emission peak followed that of the energy gap. The PL intensity decreased with increasing temperature, but was still fairly intense at room temperature. The behavior of PL intensity change with temperature was found to be the same for wires and reference wells, indicating the presence of a common nonradiative recombination mechanism.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Fabrication and Characterization of A Novel Lateral Surface Superlattice Structure Utilizing Schottky Barrier Height Control by Doped Silicon Interface Control Layers

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A novel lateral surface superlattice (LSSL) device structure based on Schottky barrier height (SBH) difference produced by periodic insertion of Si interface control layer (Si ICL) stripes is proposed, fabricated and characterized.

Two-dimensional computer simulation was performed first to gain information on basic design considerations. An electron beam induced current (EBIC) study on the fabricated device directly confirmed SBH modulation by Si ICL stripes. The devices showed periodic oscillations of drainconductance and transconductance at low temperatures up to 10K whose behavior was distinctly different from that of previous split-gate devices. The mechanism of these oscillations was explained by a sequential resonant tunneling model. According to a quantitative analysis of the data, SBH difference of 70-150 meV was produced at the metal-semiconductor interface and it produced quantized levels with the separation of 2-3 meV at heterointerface.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Novel GaAs-Based Single-Electron Transistors with Schottky In-Plane Gates Operating up to 20K

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In an attempt to enhance the operation temperature of GaAs-based single-electron transistors (SETs), a novel Schottky in-plane gate (IPG) SET based on voltage-controlled depletion of two-dimensional electron gas (2DEG) was proposed, fabricated and characterized. For

device fabrication, EB lithography and the in-situ electrochemical process were applied to a MBE-grown AlGaAs/GaAs 2DEG wafer, and narrow Pt IPGs with 200 nm length were realized on the side walls of 2DEG. The fabricated SETs clearly showed Coulomb oscillations with a Coulomb gap and Coulomb staircase at low temperatures. Coulomb oscillation was observed up to 20K which is much higher than the operation temperature of split-gate devices having similar dimensions of several hundred nm. The small capacitance values as well as the observed strong bias dependences of device characteristics are explained in terms of the depletion characteristics of 2DEG with the Schottky IPG. The current leakage within the Coulomb gap is compatible with the cotunneling theory.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Deep Levels and Conduction Mechanism in Low-Temperature GaAs Grown by Molecular Beam Epitaxy

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Deep levels in low-temperature (LT) GaAs layer grown by molecular beam epitaxy were investigated by deep level transient spectroscopy (DLTS), photocapacitance and photoluminescence (PL) techniques. For the LT-GaAs layers grown at 350C, five electron traps were detected, and the trap concentration of the dominant deep level (S1) was found to be 1.8×10^{16} cm^{-3} with an activation energy of 0.64 eV. The S1 level showed remarkable photoquenching behavior. The electrical conduction in LT-GaAs seems to be governed by these traps with high density.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

0.86 eV Platinum Schottky Barrier on Indium Phosphide by In Situ Electrochemical Process and Its Application to MESFETs

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Pt Schottky barrier diodes (SBDs) with a high Schottky barrier height of 0.86 eV and an ideality factor of near unity were successfully realized by a novel in situ electrochemical process. Applying this novel technique to InP metal semiconductor field effect transistors (MESFETs), good gate control of drain current with pinch-off, an effective channel mobility of 1,840 $cm^2V^{-1}s^{-1}$ and no drain current drift behavior were achieved. The InP MESFET operates even under a positive gate bias, showing feasibility of enhancement-mode operation as well as depletion-mode operation.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Contactless Characterization of Thermally Oxidized, Air Exposed and Hydrogen-Terminated Silicon Surfaces by Capacitance-Voltage and Photoluminescence Methods

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Contactless and nondestructive characterization of the electrical properties of the free surfaces of single-crystalline silicon wafers is accomplished for the first time by combined use of the contactless metal-insulator-semiconductor (MIS) capacitance-voltage (C-V) technique and the photoluminescence surface state spectroscopy (PLS^3) technique. The thermally oxidized, air-exposed and hydrogen-terminated silicon (111) surfaces were investigated. Thick thermally oxidized surfaces showed well-behaved characteristics with a minimum of a broad U-shaped interface state density (Nss) distributions in a range of 10^{10} $cm^{-2}eV^{-1}$. On the other hand, the air-exposed Si surface exhibited a GaAs MIS-like behavior with strong Fermi level

pinning near the charge neutrality level E_{HO} caused by a narrow U-shaped state distribution. Surprisingly, hydrogen-terminated surfaces showed even stronger Fermi level pinning at E0= Ec-0.53 eV due to high density of amphoteric discrete state which may be due to silicon dangling bonds.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Optical Characterization of InAs Quantum Dots Fabricated by Molecular Beam Epitaxy

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Optical characterization were performed on patterned InAs dots based on InAs/InAlAs hetero-structure and the self-assembled InAs dots grown on GaAs. Unexpectedly high peak energy shift in photoluminescence (PL) and cathode luminescence (CL) was observed from InAs dots based on InAs/InAlAs heterostructure. PL results of self assembled InAs dots grown on GaAs also showed unexpectedly high peak energy. CL spectra from each single InAs dot suggested luminescence from highly strained dots contribute to shift the average luminescence peak towards high energy. According to these optical characterization, the inherent strain distribution is found to play an important role in the analysis of luminescence from dots of strained material systems.

the 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Regular Array Formation of Self-Assembled InAs Dots Grown on Patterned (111)B GaAs Substrate by MBE

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We report, for the first time, self-assembled molecular beam epitaxial (MBE) growth of InAs dots on patterned (111)B GaAs substrates by Stranski-Krastanow growth mode. (111)B

GaAs substrates were patterned by using conventional optical lithography process and wet-chemical etching. Self-assembled InAs dot growth was performed on both tetrahedral etch-pit pattern and trapezoidal grooves. InAs dots were found to be selectively grown on the bottom of the tetrahedral etch-pit with appropriate growth conditions. As for the growth on trapezoidal grooves, InAs dots were found to be periodically arrayed on the middle of one side of the slope of grooves patterned along [211] direction and on the top and the bottom surface of grooves patterned along [011] direction. The observed periodic distributions of InAs dots on the patterned substrates are presumably caused by the periodic lattice strain distributions on the patterned surface at the initial stage of highly strained layer growth.

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A High Performance p-Channel Transistor : β-MOS FET

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We have fabricated a β (Bipolar Enhanced Transistor Action) MOS FET device which operates in combined FET and bipolar modes, while perfectly maintaining the MOSFET circuit configuration with extended operational voltage up to-4 volts due to gate-voltage-controlled base resistance of the parasitic lateral bipolar transistor. Three types of gate-to substrate contact were investigated including ultrathin tunnelling barriers. The p-channel β-MOS FET showed dramatic improvements in transconductance by a factor of 4 while maintaining the same threshould voltage compared with conventional MOS structures.

Third International Symposium on New Phenomena in Mesoscopic Structures December 4-8, 1995 Hyatt Regency Maui, Hawaii, USA

Quantum Transport in A Schottky In-Plane-Gate Controlled GaAs/AlGaAs Quantum Well Wires

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Abstract

Transport properties of the novel GaAs/AlGaAs quantum well wires (QWWs) with Schottky in-plane gates realized by a combination of a electron beam lithography and the in-situ electrochemical technology were investigated. Clear quantized conductance in units of 2e2/h was observed up to 100K. Nonlinealities are found in the current-voltage characteristics at a small applied voltage, resulting in conductance deviation from the value of the quantized conductance. From the breakdown voltage of conductance quantization, a subband energy separation is estimated to be 10meV or higher.

Third International Symposium on New Phenomena in Mesoscopic Structures December 4-8, 1995 Hyatt Regency Maui, Hawaii, USA

Design and fabrication of GaAs/AlGaAs single electron transistors based on in-plane Schottky gate control of 2DEG

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A novel GaAs-based single electron transistor (SET) based on in-plane Schottky gate control of 2DEG is designed and fabricated to achieve SET operations at higher temperatures than split-gate devices. Coulomb oscillation is observed up to 20K in the novel device.

23rd Conference on the Physics and Chemistry of Semiconductor Interfaces January 21-25, 1996 La Jolla, California, USA

Contactless capacitance-voltage and photoluminescence characterization of ultrathin oxide-silicon interfaces formed on hydrogen terminated (111) surfaces

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Electronic properties of the interfaces between Si and ultrathin (<10Å) oxides formed by various low-temperature processes were characterized in contactless fashion, using contactless capacitance-voltage (C-V) and photoluminescence surface state spectroscopy (PLS^3) techniques together with X-ray photoelectron spectroscopy (XPS) measurement. Hydrogen (H)-terminated Si (111) surfaces were used as the initial surface. Ultrathin oxides were formed at low temperatures by chemical oxidation processes (hot HNO_3, $H_2SO_4+H_2O_2$), long-time air exposure and low-temperature oxidation processes below 350°C.

The initial H-terminated surfaces showed presence of Fermi level pinning at $E_0=Ev+0.65$ eV due to high density of amphoteric discrete state probably originating from Si dangling bonds. On the other hand, all the ultrathin oxide-Si interfaces exhibited very limited capacitance variations with voltage at low capacitance levels similar to GaAs MIS systems, and indicated that Fermi level is pinned near the charge neutrality level E_{HO} due to presence of interface states with narrow U-shaped continuous distributions. Low-temperature oxidation at 350°C slightly weakens such pinning. The present work indicates difficulty of realizing unpinned ultrathin oxide-silicon interface by low-temperature processes.

23rd Conference on the Physics and Chemistry of Semiconductor Interfaces
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Surface Passivation of $In_{0.53}Ga_{0.47}As$ Ridge Quantum Wires Using Silicon Interface Control Layers

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Surface state effects in $In_{0.53}Ga_{0.47}As$ one-dimensional quantum wires and the effectiveness of the Si interface control layer (SiICL)-based passivation technique are investigated using photoluminescence as the probe. Scanning electron microscope (SEM) and x-ray photoelectron spectroscopy (XPS) measurements were made to characterize the structure and the interface properties. The $In_{0.53}Ga_{0.47}As$ quantum wires embedded in $In_{0.52}Al_{0.48}As$ barrier material were fabricated by selective molecular beam epitaxy (MBE) growth on patterned InP substrates.

Unpassivated near-surface quantum wires showed an exponential decrease of PL intensity with reduction of surface-to-well distance, tws, similarly to the near-surface quantum wells. By applying the SiICL based passivation, a nearly complete recovery of PL intensity was achieved with an observed maximum recovery factor of 250 for the InGaAs quantum wire directly passivated with SiO2/SiICL (tws=0). The mechanism for the PL recovery is explained in terms of suppression of surface states by passivation.

8th International Conference on Indium Phosphide and Related Materials April 21-25, 1996 Convention Center " Stadtgarten " Schwabisch Gmund, Germany

SURFACE PASSIVATION OF InP-BASED $In_{0.53}Ga_{0.47}As$ QUANTUM WIRES USING SILICON INTERLAYER-BASED PASSIVATION TECHNIQUE

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Surface control of compound semiconductor quantum structures is one of the key issues for realizing quantum LSIs, since such structures should be placed near the surface. For example, presence of severe surface effects on photoluminescence (PL) properties of quantum structures have been reported so far by several groups. According to these reports, PL intensity from near-surface quantum wells (QWs) and that from QW-based etched quantum wires (QWRs) decreased rapidly with reducing the well-to-surface distance and the lateral dimension of the wire, respectively, due to rapid nonradiative recombination process at the compound semiconductor surfaces.

Recently, we proposed a new passivation layer for compound semiconductor including a Si interface control layer (SiICL) between compound semiconductor substrate and outer SiO_2 and succeeded in a complete suppression of the surface effect on the near-surface QWs. In this paper, the SiICL technique was applied to an $In_{0.53}Ga_{0.47}As$ QWRs fabricated by using selective molecular beam epitaxy (MBE) with different values of the wire-to-surface distance (tws). The surface effects and the effectiveness of passivation were investigated by PL method. X-ray photoelectron spectroscopy (XPS) measurements were also made to characterize the interface properties of the samples.

8th International Conference on Indium Phosphide and related Materials April 21-25, 1996 Schwabisch Gmund, Germany

GROWTH TEMPERATURE DEPENDENCE OF COMPOSITION IN In1-xGaxP ALLOY SYSTEM GROWN BY GSMBE USING TERTIARYBUTYLPHOSPHINE

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$In_{1-x}Ga_xP$ is a promising material for optoelectronic devices in the visible wavelength and long wavelength ranges as well as for use in high-speed electronic devices such as hetero-bipolar transistors (HBTs) and high electron mobility transistors (HEMTs). However its controlled epitaxial growth is known to be difficult because that the alloy composition x of $In_{1-x}Ga_xP$ strongly depends on the growth temperature Tg. In the case of gas source molecular beam epitaxy (GSMBE) growth of In1-xGaxP, there has been no report on the relationship between x and Tg.

The purpose of the present paper is to investigate growth-temperature dependence of growth rate and composition for GSMBE growth of $In_{1-x}Ga_xP$ using tertiarybutylphosphine (TBP) and to clarify the underlying mechanism. TBP is a promising substitute for PH_3 due to its relatively low toxicity.

the 1996 International Conference on Indium Phosphide and Related Materials April 21-25, 1996 Convention Center " Stadtgarten ", Germany

Fabrication of high-performance InP MESFETs with in-situ pulse-plated metal gates

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Although InP has higher saturation velocity and higher thermal conductivity than GaAs, its use in the active channel of electron devices has been limited by lack of suitable Schottky gate

technology. The purpose of this paper is to demonstrate that high-performance InP MESFETs with Schottky barrier heights (SBHs) = 0.85-0.89 eV can be realized by the novel in-situ electrochemical etching/plating technique.

Previously, direct metal contacts were formed on InP by conventional techniques. But this results in low SBHs of about 0.4 eV, being independent of metal workfunctions (Fermi level pinning). Such low Schottky barriers make it difficult to use them as the gate of practical MESFETs. To overcome this difficulty, many attempts have been made to enhance SBHs on n-type InP, including incorporation of a thin interfacial oxide layer at the metal/InP interface, incorporation of a p^+ planar-doping layer near the interface and modification of surface properties by plasma treatments. However, such Schottky barriers having various interfacial oxide layers suffer from instability and poor reproducibility due to complex interfacial reactions. Furthermore, MESFETs utilizing Schottky barriers with interlayers generally exhibited drain current fluctuation, kinks and poor pinch-off.

On the other hand, InP Schottky barriers produced by the in-situ electrochemical process used in this paper are free of interfacial oxides and removes Fermi level pinning, realizing workfunction-dependent SBHs. High-barrier height, low-leakage and stable InP MESFETs are realized for the first time using this process.

38th Electronic Materials Conference June 26-28, 1996 University of California Santa Barbara California, USA

Dominant Deep Level and Its Photocapacitance Quenchingin LT-GaAs Grown by MBE

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Undoped GaAs layers grown by molecular beam epitaxy (MBE) at low substrate temperatures (LT-GaAs buffer) possess unique semi-insulating properties that are useful for elimination of side-gating in MESFETs and HEMTs. They are also useful for ultra-fast optoelectronic switching. However, the mechanism for their semi-insulating properties have not been clarified yet, being disputed between two models, i. e, the deep level compensation model and the As-precipitate-induced Fermi level pinning model. The purpose of this paper is to investigate deep level properties of LT-GaAs layers by using deep level transient spectroscopy (DLTS) and photocapacitance (PHCAP) techniques. Si-doped conductive LT-GaAs layers were grown at 300-400°C so as to directly apply the DLTS and PHCAP techniques to the LT-GaAs layer.

38th Electronic Materials Conference June 26-28, 1996 University of California Santa Barbara California, USA

AlGaAs/GaAs Narrow Quantum Wires Produced by Schottky In-Plane Gate Technology

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The key point of the fundamental devices for future quantum electronics is formation of scattering-free one-dimensional electron waveguide with gate control. A promising approach is to confine two-dimensional electron gas (2DEG) into one dimension by utilizing voltage-adjustable depletion layers. The in-plane-gate (IPG) device utilizes electric field parallel to the 2DEG plane and seems to be potentially more effective for realization of quantum devices working at high temperatures due to strong and efficient electron confinement. The purpose of the present paper is to report transport properties of the novel Schottky-IPG controlled $Al_{0.3}Ga_{0.7}As$/GaAs quantum well wires (QWWs). IPGs were realized by formation of Schottky contacts to the edges of the 2DEG plane by applying a novel in-situ electrochemical process.

38th Electronic Materials Conference June 26-28, 1996 University of California Santa Barbara California, USA

Self-assembled InAs Quantum Dots Grown on Patterned GaAs Substrates

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We report on the growth of self-assembled InAs quantum dots on two-dimensionally arrayed tetrahedral etch-pits and trapezoidal V-grooves patterned on (111)B GaAs substrates by MBE. GaAs (111) B substrates were patterned by using conventional optical lithography process and wet-chemical etching. MBE growth of InAs dots were performed at substrate temperature ranging from 510°C and 540°C. Many InAs dots formed on the etched wall at substrate temperature of 510°C. indicate insufficient surface migration of indium atoms on the surfaces. InAs dots were selectively grown on the bottom of the tetrahedral etch-pit when the

growth temperature of 530°C was chosen. No InAs dot was observed on the surface of the sample grown at 540°C indicating re-evaporation of indium atoms from the substrate at this growth temperature.

On the grooves which align to [211] direction, InAs dots were found on the middle of one of the slopes. No InAs dots was found on the other side of the slope. Furthermore, the InAs dot were distributed periodically along the line direction. On the other hand, on the grooves aligned to [011] direction, the InAs dots were formed only on top of the ridge and on bottom of the valley. The InAs dots on the top and bottom of the grooves distributed also periodically along the line direction. The shape of the InAs dots on the grooved substrates looks hexagonal in its top view, and column shaped in its side view. The bulky shape of the dots on the patterned substrates makes clear contrast with InAs (or InGaAs) dots (or rather disks) on flat substrates. The dot distribution along the slope concentrating near mid-point of the slope in trapezoidal grooves aligned to [211] direction with total width of approximately 3.5 μm. The average position was 1.53 μm measured from the top (ridge) toward the valley and its standard deviation was 0.46 μm. The histogram of the distance between the nearest neighbor InAs dots on the slope, on the ridge, and on the bottom of the valley, along the line direction shows narrower distribution compared with totally random Poisson distributions with the same average distance as the real dot distribution. The periodic strain distribution at the initial stage of the highly strained growth of the wetting layer was suggested to account for the periodic nature of the InAs dot distribution.

9th International Conference on Hot Carriers in Semiconductors, Chicago, USA, 1995

Anomalous Blue-shift in Photoluminescence from Strained InAs Quantum Dots Fabricated by MBE

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We have fabricated and characterized strained InAs quantum dots grown by MBE on InP substrate. InAs quantum dots showed anomalously large blue-shifts compared with the calculation which only takes acount of the quantum size effect due to lateral confinement. Cathode luminescence analysis suggested that the average luminescence peak energy of the 2D quantum well falls into the lowest energy of the possible variations caused by the non-uniform strain distribution through exciton diffusion, whereas luminescence from quantum dots contains all possible energy variations.

1995 International Semiconductor Device Research Symposium, Charlottesville, USA, 1995

β-MOS FET: a Novel High Performance Transistor

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We have fabricated a β (Bipolar Enhanced Transistor Action) MOS FET device which operates in combined FET and bipolar modes with extended operational voltage up to -4 volts due to gate-voltage-controlled base resistance of the parasitic lateral bipolar transistor. The p-channel β-MOS FET showed dramatic improvements in transconductance by a factor of 4 while maintaining the same threshould voltage compared with conventional MOS structures. This result of 1.3 μm β-MOS FET is favorably compared with one tenth of a micron p-MOS FET.

1995 International Semiconductor Device Research Symposium, Charlottesville, USA, 1995

A Novel Method of InAs Dot Array Formation for Nanostructure Devices

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Self-organized MBE growth of InAs dots on GaAs by Stranski-Krastanow growth mode is drawing much attention for possible nanostructure device applications. However, lack of spacial control of InAs dots of this method tend to place the constraints on the possible applications of quantum dots in electronic and optical devices. In this paper, we showed regularly arrayed InAs quantum dots grown on tetrahedral etch-pits and trapezoidal V-grooves patterned on (111)B GaAs substrates by strain effect. The shape of the InAs dot was found to have facets and its shape being close to truncated hexahedron, which is more like a bulky ball as compared with very short dots (disks) grown on a flat surface.

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In Situ Optical Characterization Method for Selective Area MOCVD

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A novel *in-situ* optical monitoring method for selective area metalorganic chemical vapor deposition (MOCVD) on masked substrates is described, and demonstrated on the growth of 2 μm wide GaAs wire structures. A beam of 488 nm Ar^+ laser light irradiated a GaAs (001) surface covered with a mask having line and space patterns during growth. In this technique the reflected light intensity decreases and displays oscillatory behavior as the growth proceeds, due to the interference between the reflected light from the top of the wires with trapezoidal cross-sections and that from the masked areas of the substrate. From the peak and the valley positions in the reflected light intensity, we can estimate the growth thickness of the wire structures. Thicknesses measured using this technique agree well with those obtained from cross-sectional scanning electron microscopy.

The 1995 International Conference on Solid State Devices and Materials August 21-24, 1995, Osaka, Japan

Simulation and observation of the step bunching process grown on GaAs (001) vicinal surface by metalorganic vapor phase epitaxy

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The step bunching processes on GaAs (001) vicinal surface grown by metalorganic vapor phase epitaxy (MOVPE) are investigated by the experimen and the simulation method. In the early stage of the growth, the step bunching height and the terrace widths increase linearly, and saturate as increasing the growth thickness. The step bunching height and the terrace widths are estimated by the Monte Carlo simulation. From the fitting of simulation value to the experimental data, the activation energy to the up-side and down-side step sites compared with that to the terrace sites are obtained. Furthermore, the terrace width saturation mechanism are also clarified.

The 8th International Conference on Metal Organic Vapour Phase Epitaxy 9-13 June, 1996, Cardiff, Wales, UK

Formation and Characterization of InGaAs Strained Quantum Wires on GaAs Multiatomic Steps Grown by Metalorganic Vapor Phase Epitaxy

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We investigated the formation of self-organized InGaAs quantum wires (QWRs) on coherent GaAs multiatomic steps grown on vicinal GaAs substrates by metalorganic vapor phase epitaxy. We clarified that thin InGaAs with less than 0.15 In content grows *in step flow growth mode* from the edge of GaAs multiatomic steps, while that with more than 0.2 In content grows *in three-dimensional nucleation and growth mode* at the edge of steps due to the strain effect. Next, we fabricated InGaAs/GaAs strained QWRs at the edge of coherent GaAs multiatomic steps. Locally thick InGaAs QWR structures are observed by a transmission electron microscope. Photoluminescence spectra of InGaAs QWR samples show lower energy shift (red-shift) by about 30meV compared to those of quantum well ones due to the formation of InGaAs QWRs at the edge of coherent GaAs multiatomic steps.

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Optical Characterization of InGaAs Strained Quantum Wires Formed on GaAs Multiatomic Steps

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In the present investigation, we characterized photoluminescence properties of InGaAs strained quantum wires (QWRs) on coherent GaAs multiatomic steps grown on vicinal GaAs substrates by metalorganic vapor phase epitaxy. First, we clarified that thin InGaAs with less than 0.15 In content grows *in step flow growth mode* from the edge of GaAs multiatomic steps, while that with more than 0.2 In content, grows *in three-dimensional nucleation and growth*

mode at the edge of multiatomic steps due to the strain effect. Next, we fabricated InGaAs/GaAs strained QWRs at the edge of coherent GaAs multiatomic steps. Locally thick InGaAs QWR samples show low energy shift (red-shift) by about 30 meV compared to those of quantum well ones due to the formation of InGaAs QWRs at the edge of coherent multiatomic steps.

The 8th International Conference on Metal Organic Vapour Phase Epitaxy 9-13 June, 1996, Cardiff, Wales, UK

Formation and Characterization of Coupled Quantum Dots (CQDs) by Selective Area Metalorganic Vapor Phase Epitaxy

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We have demonstrated novel GaAs quantum dot arrays coupled to quantum wire networks, that is coupled quantum dots (CQDs) formed by selective area metalorganic vapor phase epitaxy (SA-MOVPE). First, GaAs buffer layers are grown on GaAs (001) substrates with SiNx square masks in 400 nm periodicity to [100] and [010] directions. GaAs cross-wire structures with pyramids at the corners are obtained. Next, GaAs/AlGaAs quantum wells are overgrown on top of these structures. Quantum dots (QDs) and quantum wires (QWRs) are formed at the top portions of the pyramids and at the ridges of wires, respectively. The cathodoluminescence (CL) image shows strong emission from the top portions of the pyramids, which suggests that high quality CQD structures are formed by SA-MOVPE.

Fourth China-Japan Symposium on Thin Films 24-28 October, 1995, Jiande Zhejiang, China

Investigation and Application of Multiatomic Steps on (001) GaAs Vicinal Surfaces Grown by Metalorganic Chemical Vapor Deposition

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We report on formation of coherent multiatomic steps on GaAs vicinal surfaces by

metalorganic chemical vapor deposition (MOCVD) and its application to self-organizing quantum well wires (QWWs). Uniform multiatomic steps with equal spacing terraces were formed on GaAs grown at 600C-700C. The detail of the step bunching mechanism are investigated using Monte Carlo simulation for the atomic motion on the terrace and step, and the activation energies to the step sites were estimated by the fitting of the simulation and experiment. QWW structures were grown on GaAs layer with coherent multiatomic steps. PL peak energies of the QWWs were smaller than those of the QWs formed on (001) exactly oriented GaAs substrates. These peak energy shifts indicates that locally thick quantum well wire like structures were successfully formed at the corner of multiatomic steps. These results suggest that self-organized QWWs can be fabricated uniformly on coherent multiatomic steps.

22nd International Symposium on Compound Semiconductors August 28-September 2, 1995, Cheju Island, Korea

Coherent multiatomic Step Formation on GaAs (001) Vicinal Surfaces by MOVPE and Its Application to Quantum Well Wires

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We observed the surface morphology of vicinal GaAs (001) after thermal A novel quantum well wire (QWW) fabrication using coherent multiatomic steps on vicinal surfaces is demonstrated by metalorganic vapor phase epitaxy (MOVPE). Uniform multiatomic steps with equal spacing terraces were formed on GaAs grown at 600C-700C. Similar multiatomic steps also appeared after thermal treatment under AsH3 atmosphere. The detail of the step bunching mechanism were investigate using Monte Carlo simulation for the atomic motion on the terrace and at the step. QWW structures were grown on GaAs layer with coherent multiatomic steps. PL peak energies of the QWWs were smaller than those of the QWs formed on (001) exactly oriented GaAs substrates. These peak energy shifts indicates that locally thick quantum well wire like structures were successfully formed at the corner of multiatomic steps.

The 8th International Micro-Process Conference July 17-20, 1995, Sendai, Japan

Coherent Multiatomic Step Formation on GaAs (001) Vicinal Surface by Thermal Treatment in AsH3/H2 Atmosphere

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We observed the surface morphology of vicinal GaAs (001) after thermal treatment in AsH3/H2 atmosphere by atomic force microscopy (AFM). Clear multiatomic steps were formed under the high temperature thermal treatment. Next we investigated the mechanism of step bunching during thermal treatment by two experiments from the view point of Ga atom evaporation. One is the selective thermal treatment using a partially masked GaAs wafer, and the evaporation of Ga atoms was estimated by AFM. The other is the investigation of photoluminescence (PL) peak energy shifts for AlGaAs GaAs single quantum wells with a thermal treatment process at the top of the GaAs quantum well layer, compared to those without thermal treatment. These results indicate that the evaporation hardly occurs during the thermal treatment process. Therefore, step bunching phenomena on GaAs (001) vicinal surfaces during thermal treatment are probably caused by migration of the atoms detached from upside steps and their re-incorporation to downside steps.

Third International Symposium on " New Phenomena in Mesoscopic Structures " December 4-8, 1995, Maui, Hawaii, USA

Theoretical and Experimental Investigation of an Electron Interference Device Using Multiatomic Steps on Vicinal GaAs Surfaces

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We propose a new, lateral surface superlattice (LSSL) type of electron interference devices, where the period of LSSL is typically 60 nm, by utilizing multiatomic steps on a vicinal GaAs (001) surface. The conductivity of the device is theoretically studied by taking the effect of randomness in the LSSL into account. We also investigate its drain and transconductance characteristic experimentally at low temperatures, and found clear oscillations in gm-

VG characteristics, which were ascribed to the electron interference effect.