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| Author(s)        | Shiratori, Yuta; Kasai, Seiya                                                                                                                    |
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# Effect of Size Reduction on Switching Characteristics in GaAs-Based Schottky-Wrap-Gate Quantum Wire Transistors

Yuta Shiratori<sup>1\*</sup> and Seiya Kasai<sup>1,2</sup>

<sup>1</sup> Research Center for Integrated Quantum Electronics, and Graduate School of Information Science and Technology, Hokkaido University, North 13, West 8, Sapporo 060-8628, Japan

<sup>2</sup> PRESTO, Japan Science and Technology Agency, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan

The effect of size reduction on switching characteristics is investigated experimentally for the low-switching-power operation of GaAs-based quantum wire transistors (QWRTr's) utilizing etched AlGaAs/GaAs nanowires controlled by Schottky wrap gates (WPGs). WPG QWRTr's in which the wire width,  $W$ , and gate length,  $L_G$ , were systematically changed are fabricated and characterized with respect to operation temperature, switching voltage,  $\Delta V_G$ , gate voltage to Fermi energy scaling factor,  $\alpha$ , and power-delay product, PDP. When  $W$  is less than 200 nm, more than 80% of the fabricated devices exhibit quantized conductance at 30 K. The device with  $W=40$  nm shows a large  $\alpha$  of 0.7. Decreasing  $L_G$  into the sub-100-nm range was found to be effective for improving power consumption, since the short channel effect was suppressed by tight potential control in the WPG structure.

KEYWORDS: quantum wire transistor, GaAs, Schottky wrap gate, power consumption, switching voltage, operation temperature

\*E-mail address: [siratori@rciqe.hokudai.ac.jp](mailto:siratori@rciqe.hokudai.ac.jp)

## 1. Introduction

The reduction of power consumption has been an inevitable issue for logic LSIs in which device size is decreased into the sub-100-nm range. A fundamental method of reducing active power consumption is to decrease the number of electrons for each bit manipulation.<sup>1)</sup> The quantum wire transistor (QWRTr's) is one of the devices that can be used for this purpose. Our research group has proposed and fabricated a novel ultra low-power logic circuit integrating QWRTr's or single-electron transistors (SETs), that is the hexagonal binary decision diagram (BDD) quantum circuit.<sup>2,3)</sup> Passive circuit operation without gain provides the opportunity to use quantum devices, resulting in ultra low-power consumption. Increasing the temperature at which quantum transport occurs still remains an unresolved issue. Commonly, it is understood that both a reduction in power consumption and an increase in operation temperature can be achieved by size reduction. However, no systematic research has been carried out on this subject yet. This is mostly because of the immature fabrication technology of quantum devices, which does not allow systematic position and size control in a reproducible way. Therefore, the performance of QWRTr's has not been clarified experimentally yet.

The purpose of this study is to investigate the effects of a size reduction on the power consumption and operation temperature in GaAs-based QWRTr's utilizing etched AlGaAs/GaAs nanowires controlled by nanometer-scale Schottky wrap gates (WPGs). These devices are fabricated by mature top-down process techniques, and well-defined fine structures can be realized.

## 2. Device Structure and Fabrication

The device structure used in this study is schematically shown in Fig. 1(a). It has a GaAs-based nanowire with a conventional AlGaAs/GaAs HEMT structure wrapped by a nanometer-scale Schottky WPG.<sup>4)</sup> By applying a suitable gate voltage,  $V_G$ , to the WPG, the channel is squeezed electrostatically and a quantum wire is formed. In a quantum transport regime, a few-electron switching can be performed using the 1st step of quantized conductance, as shown in Fig. 1(b). The WPG structure is suitable for planar integration because of its simple lateral structure and precise size and position control utilizing the top-down fabrication process. In addition, this structure can realize stronger quantum confinement than a conventional quantum point contact (QPC) structure. In addition to the high gate

controllability resulting from the three-dimensional (3D) gate configuration, excellent electron transport in the AlGaAs/GaAs heterointerface is important for low-power consumption.

GaAs-based nanowires were formed by the electron beam (EB) lithography and wet chemical etching of an AlGaAs/GaAs heterostructure wafer using a sulfuric acid-based etchant. Then, Ni/Ge/Au/Ni/Au Ohmic contacts for source and drain electrodes were formed. Then, Cr/Au Schottky WPGs were formed using EB lithography, vacuum deposition and the lift-off process. The mobility and carrier density of the two-dimensional electron gas (2DEG) at 77 K were  $1.1 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $1.0 \times 10^{12} \text{ cm}^{-2}$ , respectively. The electron mean free path at 77 K was 1.8  $\mu\text{m}$ . Geometrical wire width,  $W$ , and gate length,  $L_G$ , were systematically changed from 40 to 600 nm at 50 nm intervals and 100 to 800 nm at 100 nm intervals, respectively. Fabricated devices were characterized by current-voltage ( $I$ - $V$ ) measurement using an Agilent 4156C semiconductor parameter analyzer in a low-temperature probe station. In this study, we focused on four major parameters, operation temperature, switching voltage,  $\Delta V_G$ , gate voltage to energy scaling factor,  $\alpha$ , and power-delay product, PDP. Here,  $\Delta V_G$  is defined as shown in Fig. 1(b). In QWRTr's, the scaling factor directly relates to the switching voltage according to the following formula:<sup>5)</sup>

$$\Delta V_G = \frac{4kT}{e\alpha}, \quad (1)$$

where  $k$  is the Boltzmann constant,  $T$  is the temperature, and  $e$  is the elementary charge.  $\alpha$  is defined as follows:

$$\alpha = \frac{\Delta E_F}{\Delta V_G}. \quad (2)$$

$\alpha$  has a value less than unity. A small  $\Delta V_G$  and a large  $\alpha$  are necessary for low-power switching.

### 3. Experimental Results

#### 3.1 Basic characteristics and operation temperature

A scanning electron microscopy (SEM) image of one of the fabricated devices is shown in Fig. 2. Nanowires were fabricated along the  $\langle 110 \rangle$  direction and trapezoidal cross sections with smooth (111)B side facets were formed. Via the device fabrication process used in this study, nanowires with a  $W$  less than 100 nm can be fabricated reproducibly. In order to

investigate the structure size dependence of the switching characteristics, we fabricated and measured more than 330 devices, in which  $W$  and  $L_G$  were systematically changed. The measured  $L_G$  dependence of the threshold voltage,  $V_{th}$ , at 30 K is shown in **Fig. 3**.  $V_{th}$  systematically changed depending on  $L_G$  and  $W$ . This result confirmed that our fabrication process was highly reproducible even for structure-sensitive quantum nanodevices. A short channel effect in which  $V_{th}$  shifted with a decrease in  $L_G$  was observed. However, the effect was suppressed by reducing wire width owing to tight potential control in the 3D gate configuration of the WPG.

Examples of the conductance characteristics of different structure size devices are shown in Fig. 4. In the device with  $W=610$  nm and  $L_G=300$  nm, conductance quantization was observed at 30 K, as shown in Fig. 4(a). In a narrower wire device with  $W=200$  nm and  $L_G=500$  nm, clear conductance steps were observed even at 100 K as shown in Fig. 4(b). To our knowledge, this is the highest temperature ever reported for gate-control-type QWRTr's and QPCs.<sup>6-8)</sup> Assuming  $\Delta E = 3kT$ , the sub-band spacing,  $\Delta E$ , induced by lateral confinement was estimated to be 30 meV. The obtained result clearly indicated that a reduction in geometrical wire width was effective for increasing the operation temperature.

From an engineering viewpoint, it is necessary to obtain conductance quantization reproducibly. The  $W$  and  $L_G$  dependences of the appearance rate of conductance quantization at 30 K was evaluated. The result is summarized in Fig. 5. The total number of measured samples was 336. In the case of  $W < 200$  nm, 18 devices were characterized for each element of the matrix. The appearance of the conductance quantization was judged from the oscillation in the derivative of the conductance. It was clearly seen that the appearance rate strongly depended on the wire width. A high appearance rate of more than 80% was obtained when  $W < 200$  nm. This result shows that reducing geometrical wire width is necessary to increase operation temperature, even though the effective wire width can be reduced electrostatically by gate voltage. On the other hand, the rate did not depend on the gate length. This was because the gate length of the fabricated devices was shorter than the mean free path of 1.8  $\mu\text{m}$  at 30 K.

To confirm the cause of abrupt the rate increase when  $W < 200$  nm, 3D potential simulation solving Poisson's equation numerically was carried out and sub-band spacing,  $\Delta E$ , was evaluated. The simulation showed that the confinement potential had a parabolic shape and that the effective wire width was smaller than the geometrical one by side depletion, as shown in the inset of Fig. 6. Then sub-band spacing was evaluated using a parabolic potential approximation. The calculated sub-band spacing in the 1st conductance step as a function of

geometrical wire width is plotted in Fig. 6. The obtained value was larger than that from a rectangular well with a geometrical wire width and exceeded the thermal energy at 30 K when  $W \leq 200$  nm. This value could explain the critical size for the high appearance rate of conductance quantization in Fig. 5.

### 3.2 Switching voltage and scaling factor

Figure 7 shows the temperature dependence of switching voltage in the quantum transport regime for the devices with various wire widths. A theoretical curve for the ideal case is also plotted with a broken line. Experimental data showed a linear dependence on temperature, which corresponds to the theory. It was clearly seen that switching voltage decreased with a decrease in the wire width and came close to the ideal curve. On the other hand, when  $W \geq 540$  nm, the experimental curve was offset at 0 K. The offset energy was estimated to be 5 meV from  $\alpha \Delta V_G$ . One of the possible reasons is the smoothing of the one-dimensional (1D) density of state (DOS) in the wires caused by fluctuations in structure and impurities.<sup>9)</sup> When the widening of the 1D DOS becomes larger than  $kT$ , the shape of the conductance step edge is defined by the DOS and  $\Delta V_G$  has a finite value even at 0 K. The scaling factor was also evaluated from the slopes and obtained values are indicated in Fig. 7. By decreasing  $W$ ,  $\alpha$  was found to clearly increase, corresponding to a decrease in  $\Delta V_G$ , as explained by eq. (1).

The wire width dependence of  $\alpha$  was evaluated for 400-nm-gate devices and the result is shown in Fig. 8.  $\alpha$  was calculated using eq. (1) and the measured switching voltage. Experimental data showed that  $\alpha$  increased with a decrease in wire width. This is simply because the field effect becomes strong when the distance between carriers and the gate becomes small. An  $\alpha$  of 0.5 was experimentally obtained when  $W=40$  nm. This value agreed reasonably well with the theory from the 3D potential simulation with eq. (2). The theory also indicated that  $\alpha$  reaches unity when  $W$  is 20 nm. The obtained results confirm that a decrease in the wire width results in a decrease in switching power consumption.

Figure 9 shows the gate length dependence of  $\alpha$  for devices with various wire widths. Theoretical curves from the 3D potential simulation are also plotted. When  $W > 80$  nm, the experimentally obtained  $\alpha$  remained at approximately 0.3 even for varying gate lengths. This result was reproduced by the theory using the 3D potential simulation. On the other hand, when  $W=40$  nm, experimental  $\alpha$  increased rapidly and an  $\alpha$  of 0.7 was obtained when  $L_G=300$  nm. The theory also indicated a similarly large  $\alpha$ . However, the experimental data in several

devices with  $W=40$  nm were unexpectedly smaller than the theoretical values. The discrepancy between the experimental and theoretical results is partly because of the wire width fluctuation,  $\Delta W$ . The estimated  $\Delta W$  determined from the difference between the theoretical and experimental values at  $W=40$  nm was roughly 10 nm, which agreed reasonably well with the  $\Delta W$  of 10 nm determined from SEM images of fabricated devices. In addition, the small  $\alpha$  in the short gate devices was likely also caused by the short channel effect. Further study is necessary for more precise control and the optimization of the gate length in WPG QWRTr's.

### 3.3 Power-delay product

As a standard figure of merit for switching devices, power-delay product, PDP, was evaluated. In this study, PDP was calculated using the following formulas and device parameters from DC measurement at 30 K and device dimensions:

$$PDP = C_G \Delta V_G^2, \quad (3)$$

$$C_G = \frac{\Delta Q_G}{\Delta V_G} = \frac{e \Delta n_{1D} L_G}{\Delta V_G}, \quad (4)$$

where  $C_G$  is the gate capacitance,  $n_{1D}$  is the 1D electron density in the nanowire.  $\Delta n_{1D}$  was obtained by integrating 1D DOS in the 1st conductance step edge. The obtained result is shown in Fig. 10. It was found that PDP decreased as  $W$  and  $L_G$  decreased. We also estimated PDP theoretically using the following formula:

$$PDP = \frac{8\sqrt{2m_e(kT)^3}}{\pi\hbar} \cdot \frac{L_G}{\alpha}, \quad (5)$$

where  $m_e$  is the effective mass of electrons and  $\hbar$  is Plank's constant.  $\alpha$  was obtained from the 3D potential simulation. Theoretical curves are plotted with solid lines. The thermal and quantum limits of PDP are also plotted with broken lines. Since  $\alpha$  depends on  $W$ , theoretical PDP values also decreased with decreases in  $W$  and  $L_G$ . The experimental data agreed well with the theoretical results. It should be also mentioned that the PDP of the fabricated QWRTr with  $W=40$  nm and  $L_G=300$  nm was two orders of magnitude smaller than that of a 20-nm-gate MOSFET at 30 K estimated from data from ITRS 2006.<sup>10)</sup> The minimum PDP in the fabricated devices was still 10 times larger than the thermal limit. The theory indicated that PDP decreased with a decrease in  $L_G$ , since the gate capacitance decreases linearly depending on  $L_G$  and the increase in  $\Delta V_G$  induced by the short channel effect was weak in the present devices. In addition,  $\alpha$  increased with a decrease in  $W$ , as discussed in the previous subsection.

Therefore the size reduction in both  $L_G$  and  $W$  results in a decrease in PDP. It is expected that QWRTr's with  $W=20$  nm and  $L_G=50$  nm can reach the thermal limit at 30 K, which is higher than the quantum limit with a delay time of 1 ps.

#### 4. Conclusions

The effect of size reduction on switching characteristics was investigated experimentally in GaAs-based quantum wire transistors (QWRTr's) utilizing AlGaAs/GaAs etched nanowires controlled by Schottky wrap gates (WPGs). Devices QWRTr's in which wire width,  $W$ , and gate length,  $L_G$ , were systematically changed were fabricated and characterized with respect to operation temperature, switching voltage,  $\Delta V_G$ , gate voltage to Fermi energy scaling factor,  $\alpha$ , and power-delay product, PDP. By reducing structure size, clear conductance steps were obtained at 100K. When  $W$  was less than 200 nm, more than 80% of the fabricated devices exhibited quantized conductance at 30K. The device with  $W=40$  nm showed a large  $\alpha$  of 0.7. The obtained results can reasonably be explained by the theory based on three-dimensional potential simulation. Decreasing  $L_G$  into the sub-100-nm range was found to be effective for improving power consumption, since the short channel effect was suppressed by tight potential control in the WPG structure. The possibility that WPG QWRTr's with  $W=20$  nm and  $L_G=50$  nm could achieve a small PDP close to the thermal limit at 30 K was pointed out.

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## Figure captions

**Figure 1** (a) Basic structure of WPG quantum wire transistor and (b) its switching operation.

**Figure 2** SEM image of fabricated WPG QWRTr.

**Figure 3** Gate length dependence of threshold voltage at 30 K.

**Figure 4** Conductance characteristics of fabricated WPG QWRTr's with (a)  $W=610$  nm and  $L_G=300$  nm at 30 K, and (b)  $W=200$  nm and  $L_G=500$  nm at 100 K.

**Figure 5** Wire width and gate length dependences of appearance rate of conductance quantization at 30 K.

**Figure 6** Sub-band energy in QWRTr's as function of geometrical wire width.

**Figure 7** Temperature dependence of switching voltage in quantum transport regime.

**Figure 8** Wire width dependence of gate voltage to Fermi energy scaling factor.

**Figure 9** Gate length dependence of scaling factor.

**Figure 10** Wire width dependence of PDP.

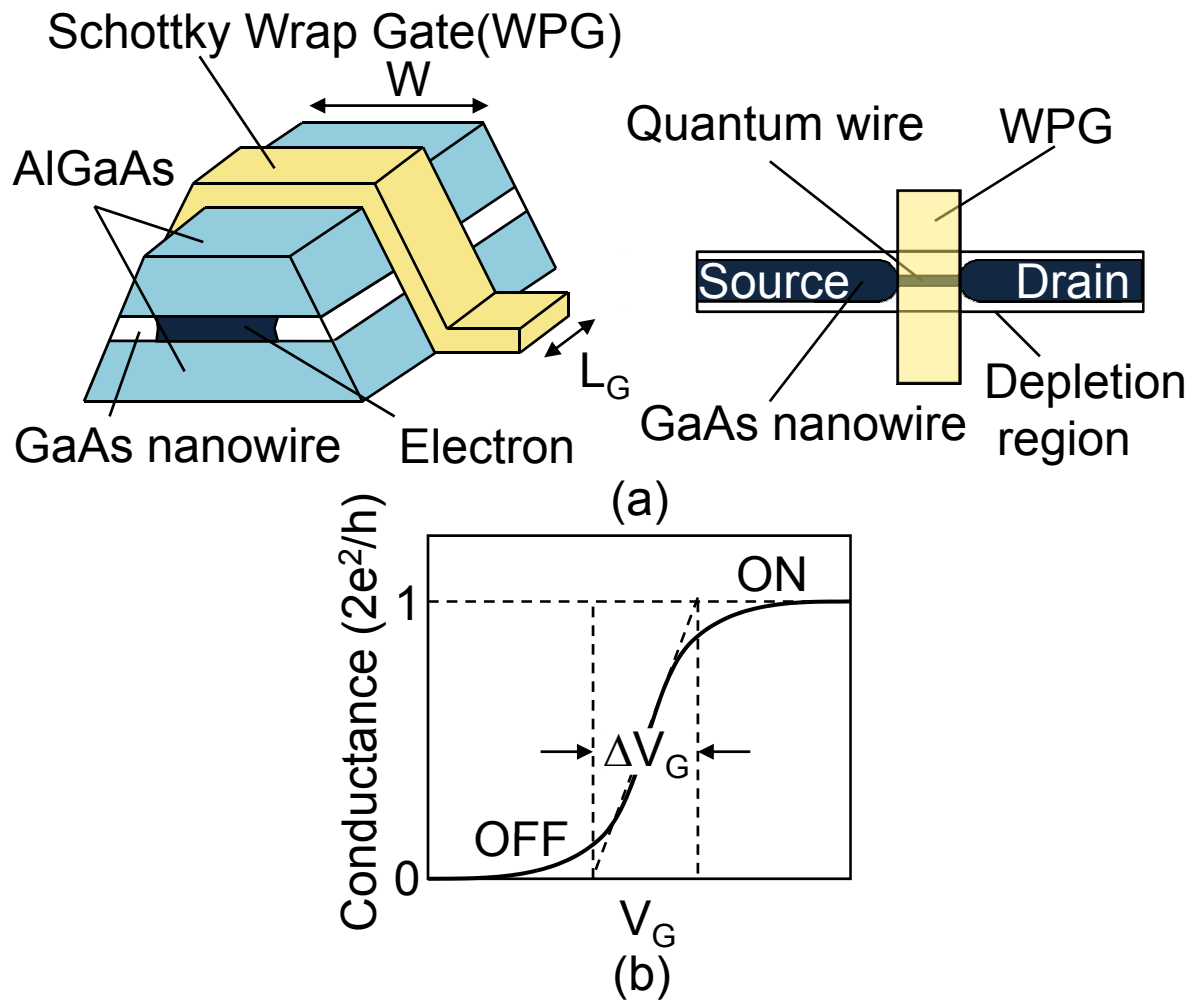


Fig. 1 Shiratori et al.

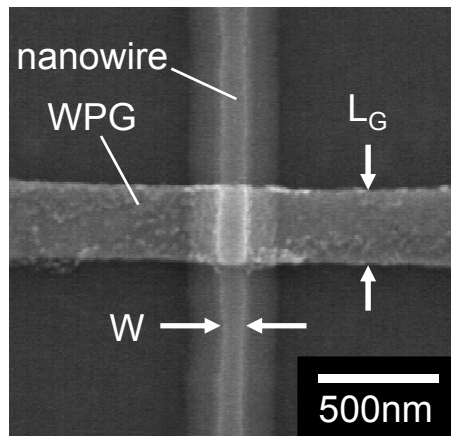


Fig. 2 Shiratori et al.

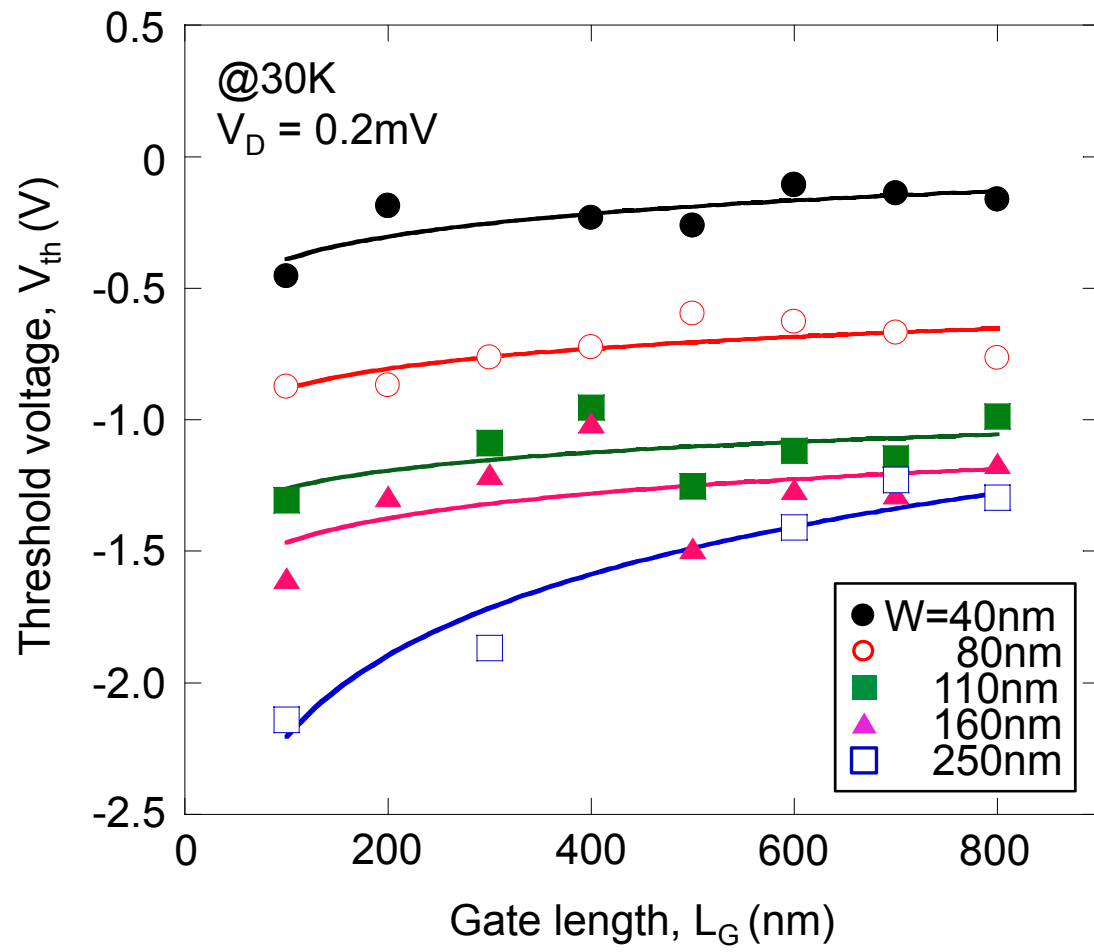
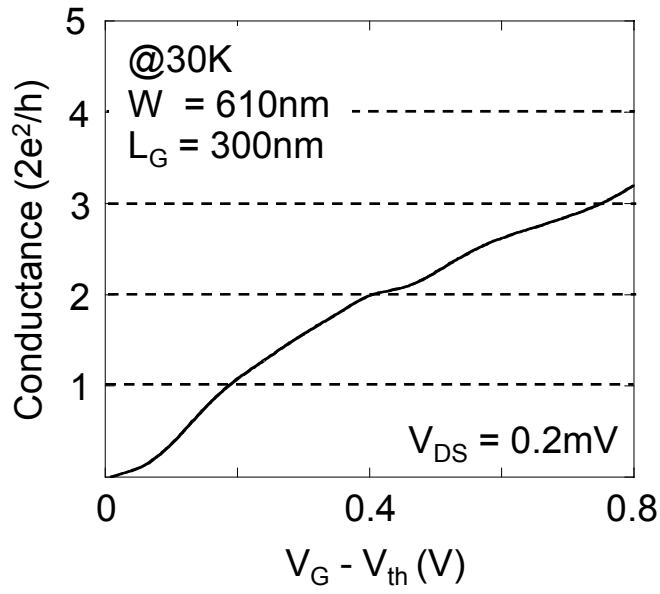
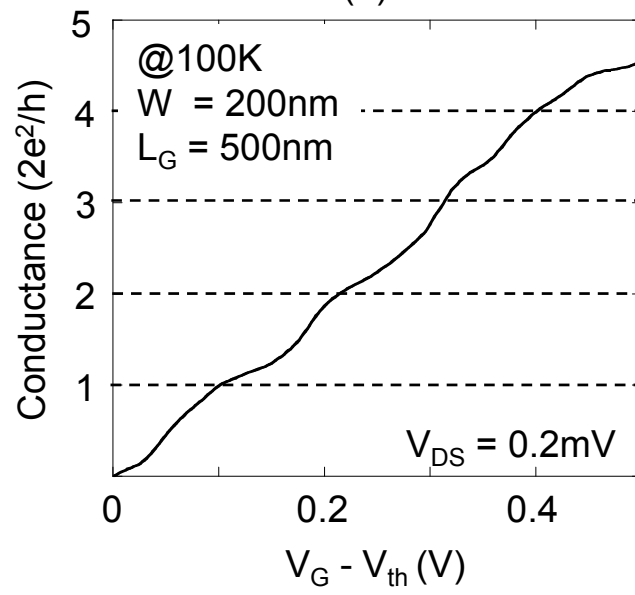


Fig. 3 Shiratori et al.



(a)



(b)

Fig. 4 Shiratori et al.

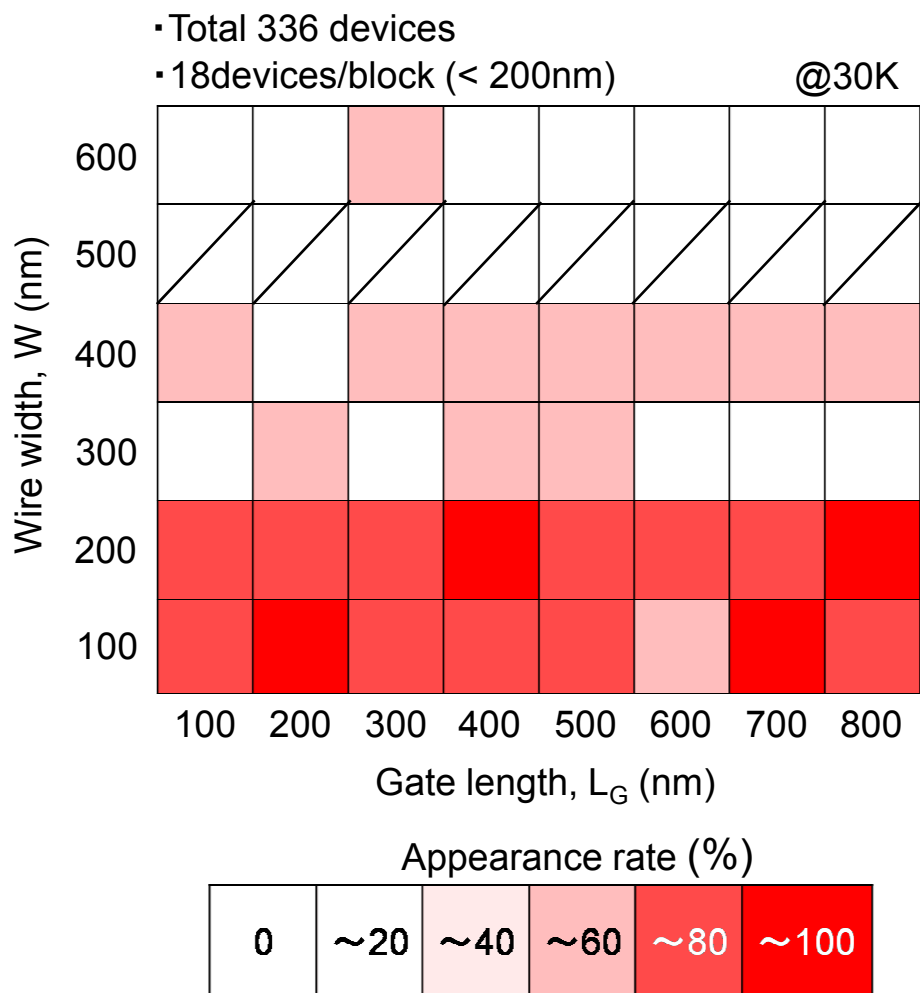


Fig. 5 Shiratori et al.

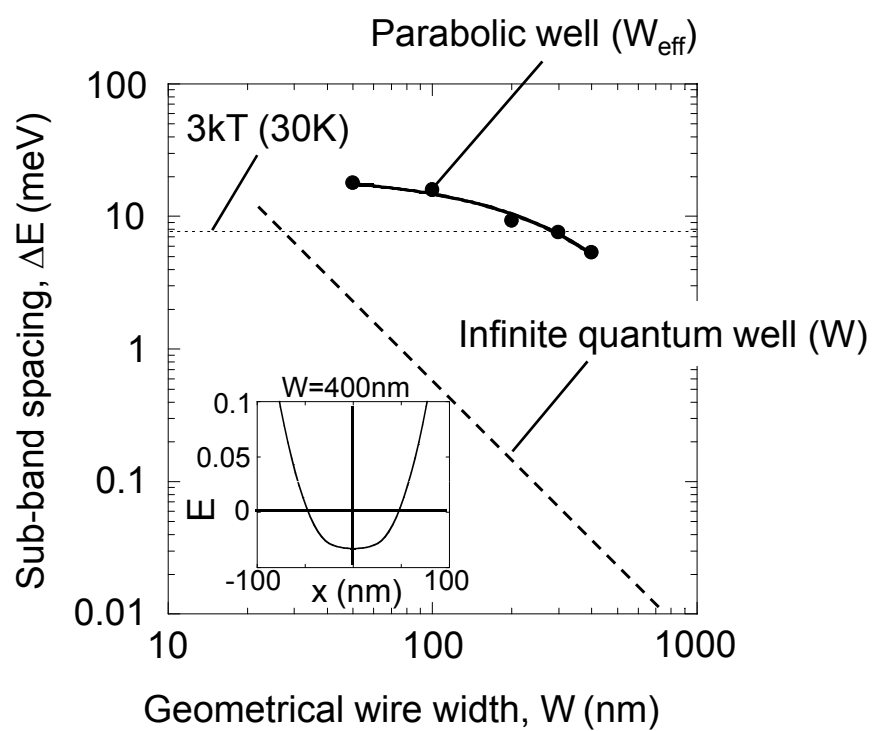


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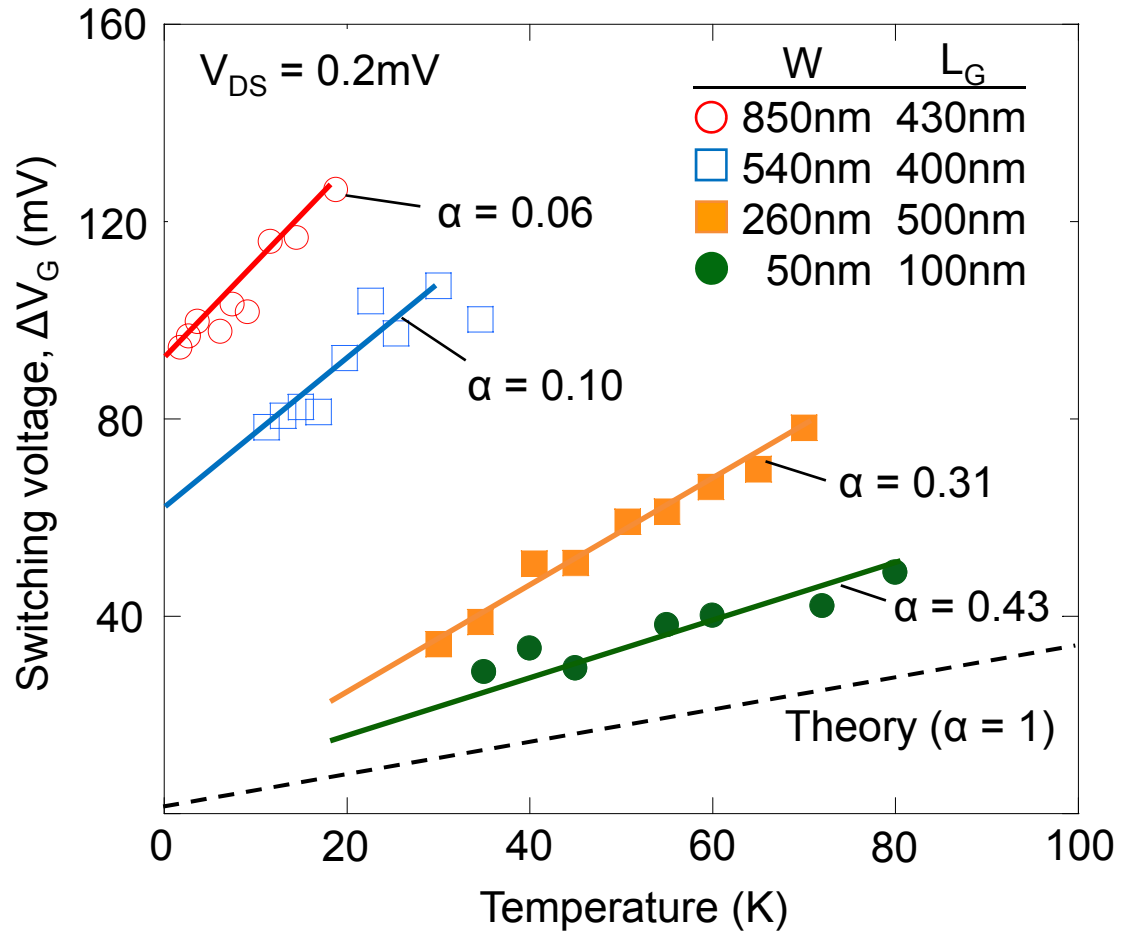


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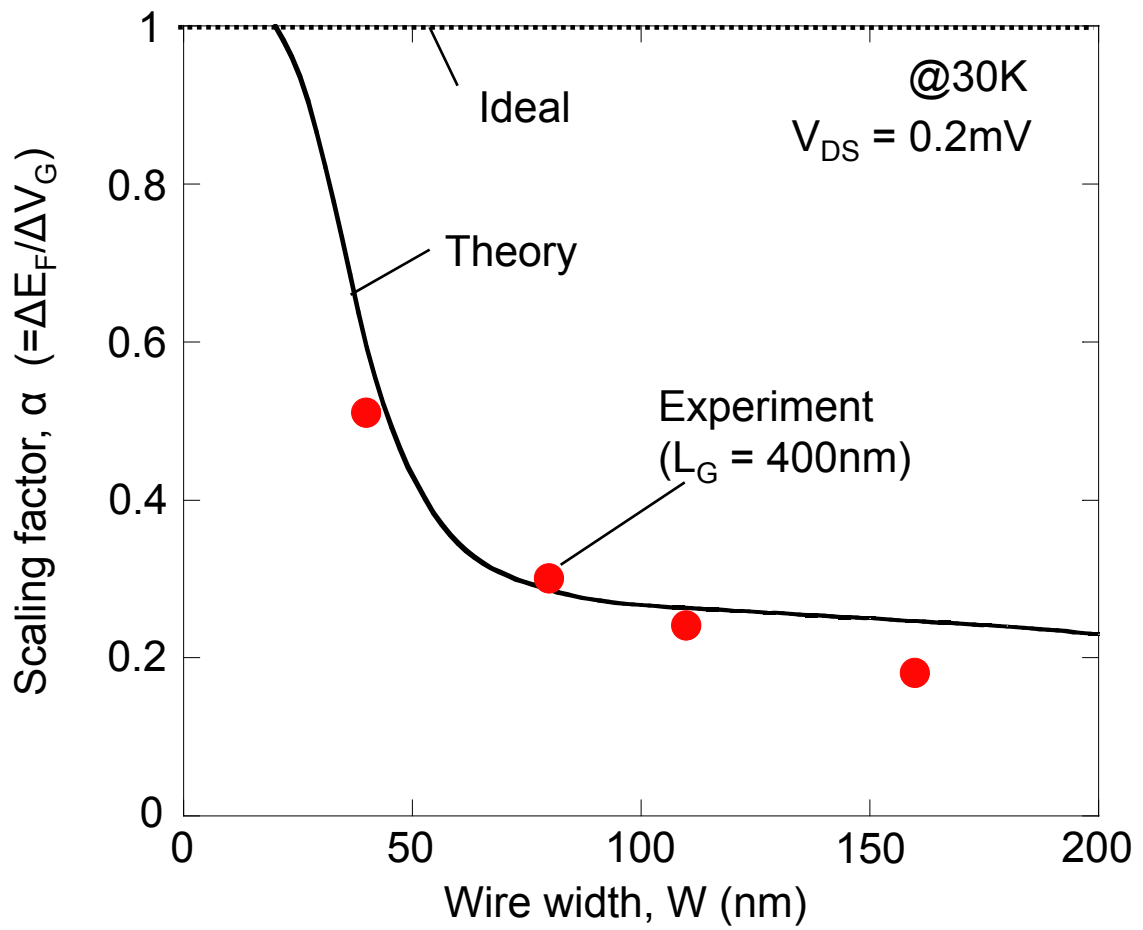


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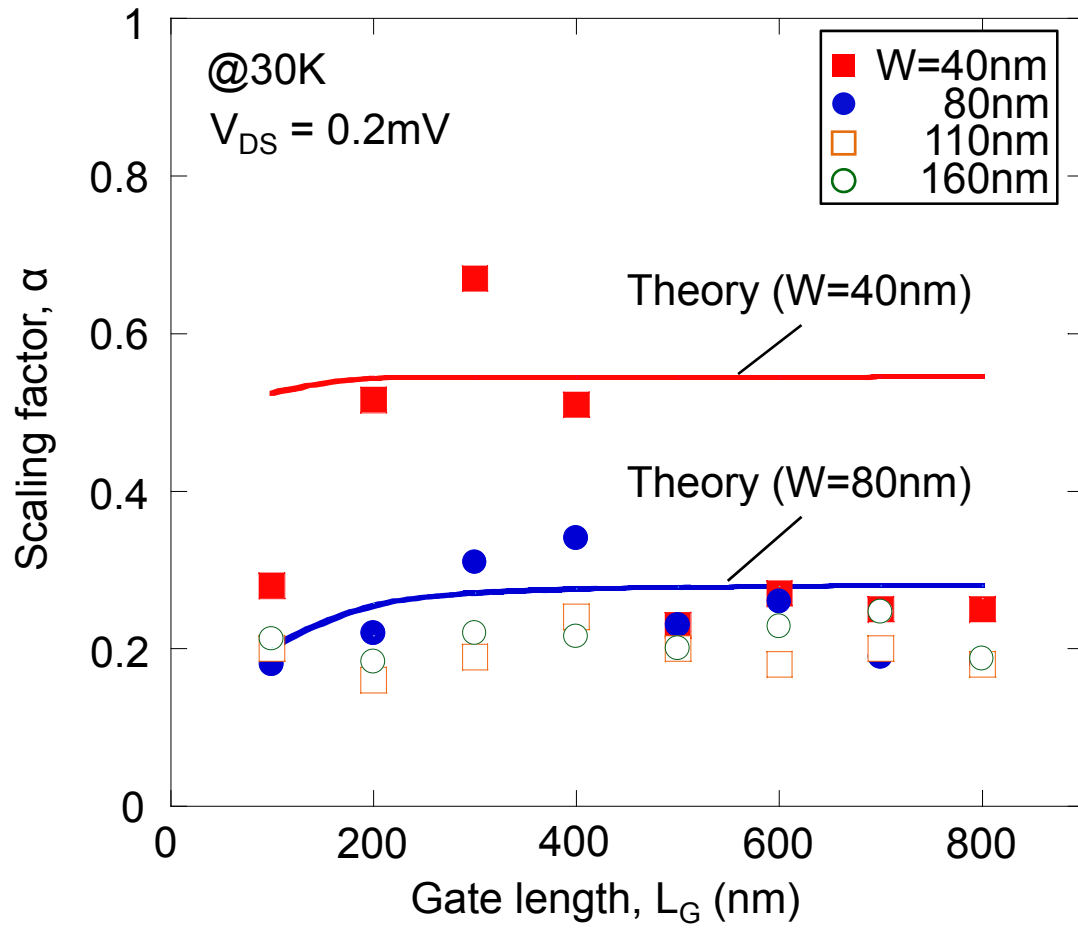


Fig. 9 Shiratori et al.

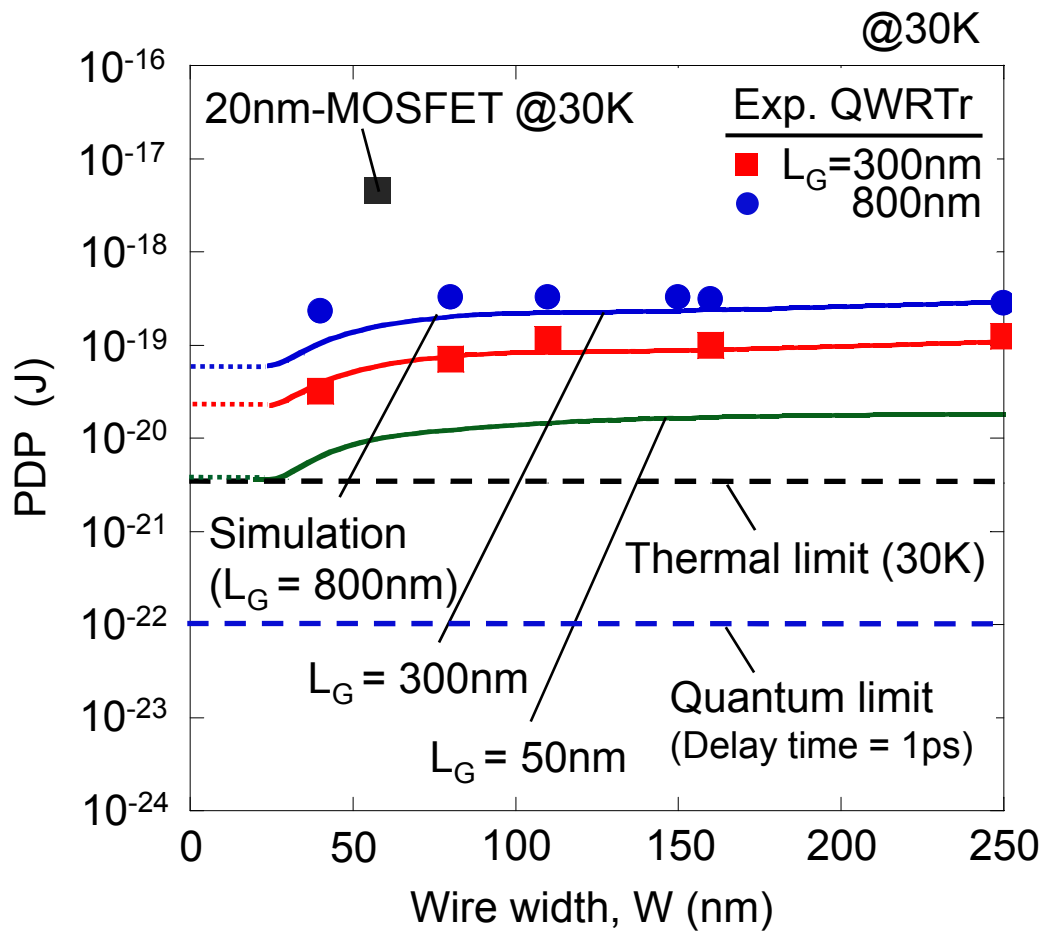


Fig. 10 Shiratori et al.