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Fast SPT-Term Allocation and Efficient FPGA Implementation of FIR Filters for Software Defined Radio Applications

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***Abstract*—This paper presents a fast SPT-term allocation scheme and an efficient FPGA implementation of FIR filters for Software Defined Radio (SDR) applications. Direct conversion method based on RF direct sampling is nowadays widely used in SDR applications. Fast and accurate digital filters are required for RF direct sampling and processing in direct conversion, however such filters often require large digital circuit area. Signed-Power-of-Two (SPT) terms will be suitable for fast processing and efficient implementation of FIR filters. This paper first aims at developing a fast SPT-term allocation scheme for designing FIR filters, and then tries to efficiently implement FIR filters on FPGA. Performance of SPT-term allocation and FPGA implementation is evaluated through computer simulation and hardware implementation.**

I. INTRODUCTION

Mobile communication system is developping toward so-called 4th-generation technology, and Software Defined Radio (SDR) will play an important role for such systems. SDR systems can correspond to various applications only by updating software while using common hardware [1]. Since existing SDR technology uses slow AD converter that wasn't able to directly sample RF signals, general versatility of a radio receiver has been reduced. However, as fast AD converter has already commonly used, Direct Sampling method that directly samples RF signal using fast AD converter is suggested [2].

In Direct Sampling system, RF signal is very quickly sampled by fast AD converter, and then a massive amount of data is derived due to very high sampligh frequency. Here the sampling rate conversion circuit and digital filter are required to enable downsampled baseband prcessing from the input data. Also hardware cost for digital filter becomes large when implementing SDR system on digital hardware. To resuce the computational cost of digital filters, Signed-Power-of-Two (SPT) terms are used which can replace multiplication by shift-add operation [3]-[7], and it finally leads smaller software and hardware cost. However it takes time to determine the allocation of SPT terms for filter coefficients. Moreover, it is not discussed if digital filters using SPT terms are friendly with FPGA implementaion.

This paper presents a fast SPT-term allocation scheme and an efficient FPGA implementation of FIR filters for SDR applications. First we aim at developing a fast SPT-term allocation scheme for designing FIR filters, and then tries to efficiently implement FIR filters on FPGA. Performance of SPT-term allocation and FPGA implementation is evaluated through computer simulation and hardware implementation.

II. FIR FILTER USING SPT COEFFICIENTS

This section summarizes conventional FIR filter design using SPT coefficients. SPT means a binary with sign, And SPT number is the number of "1" bits when coefficient is transformed to a binary. SPT number also means same addition and shift operation's number when we calculate multiplication. FIR filter using SPT coefficient, is shown in (1)-(3), indicated common FIR filter's coefficients to binary[4].

Filter response of m-tap FIR filter is given by

$$H(\omega) = \boldsymbol{h}^T \boldsymbol{C}(\omega)\boldsymbol{h} = [h(1), ..., h(m)]^T \tag{1}$$

$$\boldsymbol{h} = [h(1), ..., h(m)]^T$$

where $\boldsymbol{C}(\omega)$ is an appropriate cosine function vector. SPT coefficient of filter is expressed as

$$h(n) = \sum_{i=1}^{bit} s_{i,n} 2^{-i} \qquad s_{i,n} \in 0, 1 \tag{2}$$

where bit is the bit length of the coefficient and $s_{i,n}$ is the existence of 1 at i bit of n-tap. Finally, total SPT number of filter coefficient SPT is given by

$$SPT = \sum_{n=1}^{m} \sum_{i=1}^{bit} s_{i,n}. \tag{3}$$

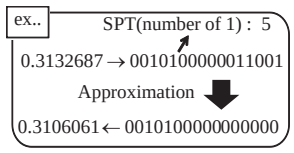

Fig. 1. SPT coefficient's approximation

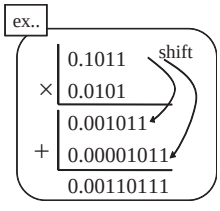

Fig. 2. SPT multiplication by addition and shift operation

This filter's main characteristics are as follows; SPT coefficient's quantization and approximation are easy. for example, it just needs to cut off an ineffective information of backward SPT coefficients for approximation as Fig. 1. Second, it is

possible to calculate the multiplication by addition and shift operation, as Fig. 2.

In digital filter FPGA implementation, if multiplier is used to calculate convolution of coefficients, the operation speed gets faster although the circuit area gets bigger. However, if the addition and shift operation are using SPT calculation filter on FPGA implementation, the circuit area can be reduced since the multiplier is not necessary. Additionally, as addition number can be controlled by SPT number, the circuit area also can be controlled by SPT number. From these reasons, lower circuit area based on FPGA can be expected by using SPT terms.

III. SPT ALLOCATION SCHEME OF FIR FILTER WITH SPT COEFFICIENTS

In previous section, it is introduced that multiplication using SPT can be calculated by addiction and shift operation. In this section, by a new SPT allocation scheme, we redesign standard filter to the filter with SPT coefficients. Design order is as following; First, we prepare standard filter. Next, coefficient of standard filter is allocated to SPT coefficient by using evaluation function and searching algorithm.

A. Preparation of standard FIR filter

At first, we need to prepare a standard filter, since filter with SPT coefficient can be designed by allocating a standard filter's coefficient to SPT term. Standard filter, which is set to design SPT coefficient, can be any filter, if coefficients of the filter is known.

B. SPT allocation scheme of filter coefficient

The coefficient of standard filter is transformed to SPT coefficients by SPT allocation. This allocation scheme is a new and fast method for allocating different number of SPT terms to each coefficient value keeping the total number of SPT terms fixed.

For the reason of controling the SPT number, if filter coefficients are transformed SPT coefficient directly by a binary transform, it includes ineffective information of backward coefficient. For example, SPT coefficient is '$01001101_{(2)}$', the last '1' means $1 \times 2^{(-8)}$ which is not effective to the filter response. Therefore, unnecessary calculation and circuit area can be reduced by allocating such a information.

The design of FIR filter using SPT term is proposed [4], which used the evaluation function on the basis of NPR, and optimal algorithm to design filter. However, in this paper, since we redesign a standard filter to the filter with SPT coefficients, maintaining the filter response from a standard filter and reducing circuit area on FPGA are required to design filter. This design feature is as following; First, standard filter characteristic, such as null point, is maintained, as allocatted filter converge standard filter. Second, although there are a few information of standard filter except to coefficient, it can be allocated SPT coefficient. This design method is a high applicability, as it can be applied to existing filters.

To allocate the SPT coefficient, we research an optimum SPT coefficient of standard filter by using algorithm and evaluation function, which is presented by section Ⅲ. C.

C. ALGORITHM of SPT allocation

Filter coefficient is allocated to SPT term by using algorithm and evaluation function. When we set the total SPT number, algorithm that searching a optimum SPT coefficient is indicated following three steps. ; First, in STEP 1, the SPT number is searched for all number which can be used filter coefficient. Next, in STEP 2, each coefficient of standard filter is allcated optimum SPT coefficient for each SPT number by using a result of STEP. 1 and evaluation function. Finally, in STEP 3, by using the result of STEP 2's SPT coefficient, the SPT coefficients of the filter are determined on a total SPT number.

STEP 1: First, the SPT number is searched for all number which can be used to the filter coefficient. Since we design a filter of 8-tap $\times$ 16-bit, the number which can be used to the filter coefficient is 0 to $2^{16bit} - 1$. In STEP 1, we find a SPT number of each number which is shown in Table I.

TABLE I
STEP 1: SEARCH THE SPT NUMBER FOR ALL NUMBER.

Number	SPT term	SPT number
	$\overbrace{00\cdots000}^{bit}$	
0	$00\cdots000$	0
1	$00\cdots001$	1
2	$00\cdots010$	1
3	$00\cdots011$	2
$\vdots$	$\vdots$	$\vdots$
$2^{bit}-1$	$11\cdots111$	bit

STEP 2: In STEP 2, each coefficient is allocated to the optimum SPT coefficient for each SPT number by using the result of STEP 1 and the minimum of evaluation function. Evaluation function, which is presented in (4), shows how different coefficient of standard filter and filter allocated SPT are.

$$F = |h(n) - h^*(n)| \tag{4}$$

For example, when the coefficient of standard filter is 00111001, the optimum SPT coefficient is 01000000 when SPT = 1, and 01110000 when SPT = 3. As in the example given above, if a coefficient of standard filter is known, the optimum SPT coefficient of each coefficient on each SPT number can be determined. This process makes STEP 3 without searching all number and calculation amount can be reduced. Simple overview of STEP 2 of 8-tap $\times$ 16-bit filter is shown in Table Ⅱ.

STEP 3: In STEP 3, an optimum filter coefficient of total SPT number is calculated. By using the result of STEP 2, if the SPT number of each coefficient is determined, the optimum SPT coefficient is also decided. Thus, when we set the total SPT number, by calculating evaluation function in all case of SPT number on each coefficient and searching minimum evaluation function, SPT number of each coefficient and the

TABLE II
STEP 2: ALLOCATED TO THE OPTIMUM SPT COEFFICIENT FOR EACH COEFFICIENT.

$h(1)_{Standard}$		0000000000010010
$h(1)_{minF}$	SPT=0	0000000000000000
	SPT=1	0000000000010000
	SPT=2	0000000000010010
$h(2)_{Standard}$		0001001011000110
$h(2)_{minF}$	SPT=0	0000000000000000
	SPT=1	0001000000000000
	SPT=2	0001001000000000
	SPT=3	0001001100000000
	⋮	⋮
⋮	SPT=6	0001001011000110
$h(m)_{Standard}$		⋮

optimum SPT coefficient can be decided. Evaluation function used STEP 3, which is presented in (5), is a sum of each coefficient of (4). Simple overview of STEP 3 is shown in Table Ⅲ.

TABLE III
STEP 3: DETERMINE THE SPT NUMBER OF EACH COEFFICIENT FROM TOTAL SPT NUMBER.

Ex. $SPT_{total} = 8$
$SPT_{h(1)} = 0 \sim 8$
$SPT_{h(2)} = 0 \sim 8 - SPT_{h(1)}$
$SPT_{h(3)} = 0 \sim 8 - SPT_{h(1)} - SPT_{h(2)}$
⋮ ⋮
$SPT_{h(m)} = 0 \sim 8 - \sum_{n=1}^{m-1} SPT_{h(n)}$
⇓⇓
Select SPT and match h(n) from STEP. 2
⇓⇓
minF_{total}

$$F_{total} = \sum_{n=1}^{m} |h(n) - h^*(n)| \tag{5}$$

Computational Cost amount of Algorithm: The reason of three step processes algorithm is to reduce searching calculation, since it needs a huge amount of calculation that all case of total SPT number is iterated on computer. All case of total SPT number, which is same as the number of Evaluation function's iteration times, is given by

$$(2^{bit})^m \tag{6}$$

where bit is the bit length of coefficient and m is the filter length.

However, by using the three step processes, the number of calculating evaluation function can be reduced to

$$(2^{bit}) \times m + \prod_{i}^{m} SPT_{h(i)} \tag{7}$$

where $SPT_{h(i)}$ is the SPT number of $h(i)$. If the standard filter is linear phase FIR filter, m can be replaced to the $m/2$.

D. Result of filter response and coefficient by SPT allocation

At this time, the standard filter is to redesign lower circuit area filter used by multilevel decimation of [2]. The design condition of the filter is as following ; First, designing filter is a 8-tap linear phase FIR filter since lower circuit area and high process speed are required by using 912MHz of fast sampling frequency. Second, null at $f_s/4$ is requirement to avoid effect of DC offset in AD converter. Finally, Frequency sampling design is used by filter design method.

The result of standard filter response is shown in Fig. 3. And the result of SPT allocation of standard filter using the three steps algorithm is also indicated in Fig. 3. The total SPT numbers of filter with SPT coefficient, which are presented in Fig. 3, are 6, 14, 20. The standard filter coefficient and the coefficient when SPT = 20 are shown in (8) and (9).

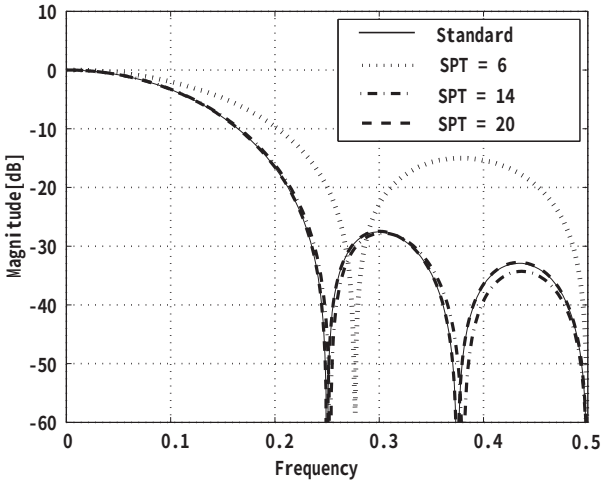

Fig. 3. FIR filter response of approximated SPT coefficient

$$h_{standard} = \begin{bmatrix} 0.0003 \\ 0.0733 \\ 0.1767 \\ 0.2497 \end{bmatrix} = \begin{bmatrix} 0.000000000001001_{(2)} \\ 0.000100101100011_{(2)} \\ 0.001011010011100_{(2)} \\ 0.001111111110110_{(2)} \end{bmatrix} \tag{8}$$

$$h_{SPT=20} = \begin{bmatrix} 0.000000000000000_{(2)} \\ 0.000100101100000_{(2)} \\ 0.001011010100000_{(2)} \\ 0.010000000000000_{(2)} \end{bmatrix} = \begin{bmatrix} 0 \\ 0.0732 \\ 0.1768 \\ 0.2500 \end{bmatrix} \tag{9}$$

According to the result of Fig. 3, as the SPT number increases, the filter coefficients converges closer to that of the existing standard filter. When the coefficient is SPT = 20, the difference between standard filter and the each coefficient are less then 0.0005, which also corresponds to filter response. The simulation run time of SPT = 20 is about 30 seconds on core2 duo 2.4GHz computer.

IV. Efficiency of using SPT term based on FPGA implementation

In section Ⅱ, it is introduced that multiplication using SPT can be calculated by addiction and shift operation, and this feature makes to reduce circuit area on FPGA implementation. The literature [3] indicates FPGA implementation of FIR filter using SPT coefficients, implying the FPGA applicability.

In this section, to estimate efficiency of using SPT term based on FPGA implementation, we evaluate the circuit area of multiplication using SPT term by comparing other multiplication, and implement filter with SPT coefficients on FPGA which is allocated in section Ⅲ. D.

A. The circuit area of multiplication using SPT

To evaluate practically the circuit area of multiplication using SPT on FPGA, the multiplication tool that commonly used in ALTERA company and Booth's multiplication method are compared. These results are presented in Table Ⅳ. Table Ⅳ is the example of multiplying 4 coefficient by input that implicated with two 8-bit, and two 16-bit coefficient. Also, ALTERA multiplication tool is compared as logical circuit constitution without using FPGA built-in multiplier.

TABLE IV
THE CIRCUIT AREA OF MULTIPLICATION

	Ex.1 8bit	Ex.2 8bit	Ex.3 16bit	Ex.4 16bit
	01011011 × Input	01011111 × Input	00000000 01011011 × Input	01001001 10000100 × Input
	Circuit area [LEs]			
Altera multiplication	94	94	168	168
Booth's multiplication	47	31	47	64
SPT multiplication	32	40	32	32

As a result of the Table Ⅳ, it confirmed that circuit area using SPT multiplication is increased by the number of "1" bits, compared with that ALTERA multiplication tool and Booths multiplication are increased by the coefficient's bit count, the switch of '01' , '10'. Theoretically, since the SPT multiplication can increase a bit count as many as it wishes without a increase of circuit area, accurate quantization of coefficient on filter design can be expected. Comparing with the each circuit area, the circuit area using SPT multiplication is lower than the other multiplication method on FPGA.

B. The circuit area of FIR filter with SPT term on FPGA

Next, by using result of section Ⅳ. A, we implement a filter with SPT coefficient on FPGA which is allocated in section Ⅲ. D. The result of Fig. 3's circuit area on FPGA are shown in Table Ⅴ.

As a result, a lower circuit area on FPGA is confirmed the filter with SPT coefficient than standard filter. And it is also shown that more circuit area increases, more filter characteristic converges as SPT increases. As it is trade-off between circuit area and filter characteristics, it is needed to chooses appropriate SPT number. Comparing SPT = 6 and SPT = 20, SPT = 6 with low information is a lower circuit area than SPT = 20, but it's filter response come down than SPT = 20. For this time, when SPT = 20, the circuit area is reduced more than half amount which maintains similar filter response of standard filter.

TABLE V
CIRCUIT AREA OF FIR FILTER OF FIG. 3

	Circuit area [LEs]
Standard FIR filter	400
SPT=6 FIR filter	81
SPT=14 FIR filter	135
SPT=20 FIR filter	163

V. Conclusion

This paper suggests FIR filter with SPT coefficient to apply Software Defined Radio (SDR) applications, aiming fast and lower circuit area by using a existing coefficient of digital filter. To use SPT coefficient is easy for quantization and approximation of filter coefficient, and can reduce circuit area on FPGA implementation. We transform the coefficients of the standard filter to SPT term by using a new SPT allocation algorithm. Next, to estimate circuit area using SPT term on FPGA, we compare SPT multiplications of circuit area to other multiplication on FPGA implementation and confirm the lower circuit area of SPT multiplication. In addition, based on FPGA, we implement filter allocated SPT term. As a result, trade-off between the total SPT number and circuit area is shown, and by comparing filter allocated SPT term to standard filter, the lower circuit area of filter with SPT term has also confirmed.

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