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Programmable Nano-Switch Array Using SiN/GaAs Interface Traps on a GaAs Nanowire Network for Reconfigurable BDD Logic circuits

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Abstract

Programmable nano-switch arrays on GaAs-based nanowire networks are investigated for a reconfigurable binary-decision-diagram (BDD) logic circuit. A programmable switch was simply realized by inserting a SiN_x thin layer between a metal gate and a nanowire. Fabricated switches were characterized in terms of hysteresis curve, program time dependences of off-state retention time, and on-state current. HCl treatment on SiN_x prior to metal gate formation was found to remarkably improve the switching characteristics. We experimentally demonstrated correct and stable operation of a four-input reconfigurable BDD circuit integrating the switch array with HCl treatment.

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1. Introduction

Semiconductor nanowire is a promising candidate for the transistor channel material in logic large-scale integrated circuits (LSIs) beyond 10-nm technology [1-2]. Bottom up formation technique is expected for its mass production because small fine nanowires can be produced in a simple way with low cost [2]. On the other hand, problems are in the flexibility and accuracy in position control, which are strongly necessary in the current LSI physical architecture. Thus alternative circuit architectures utilizing nanowire and related structures have been investigated [3,4]. We have proposed and developed a binary-decision-diagram (BDD)-based logic circuit, which is implemented on a regular nanowire network structure [5-9]. Furthermore, we recently proposed and demonstrated a reconfigurable BDD logic circuit utilizing a programmable switch array [10]. This circuit can change its logic function dynamically by external programming signals without changing the physical network configuration. Therefore various logic functions can be implemented on a nanowire network structure. The performance of the circuit such as reconfiguration speed and stability depends directly on the performance of the switches. The purpose of this paper is to investigate the operation of the programmable nano-switches formed on GaAs-based nanowires in detail. Their effect on the circuit operation is confirmed by fabrication and characterization of four-input reconfigurable BDD circuits.

2. Concept of reconfigurable BDD circuits

Schematic of the reconfigurable BDD logic circuit on GaAs nanowire network is shown in Fig. 1. The physical nanowire network represents a universal graph of Boolean functions using Shannon's expression [10]. Programmable nano-switch array is integrated in leaves of the graph and connected to a common terminal. Circuit reconfiguration is made by connecting or disconnecting the leaves and the terminal by

switching nanowire conductance in the switch array. In this study, the switch was realized by inserting a SiN_x thin layer between a metal gate electrode and a GaAs nanowire. In this system, electron traps are known to be formed in SiN_x/GaAs interface [11]. The conductance in the nanowire is switched on and off by charging or discharging the SiN_x/GaAs interface traps. On and off states are programmed with negative and positive gate voltages, respectively. After programming, a conduction state is preserved even when the gate voltage is turned off. This switch has a simple structure and is realized by only adding SiN_x deposition process to circuit fabrication process.

3. Experimental

Nanowires were formed by EB lithography and wet chemical etching an (100) AlGaAs/GaAs modulation doped heterostructure wafer. The wire direction was $\langle 0-11 \rangle$ and the sidewall facet was (111)B. For programmable nano-switches, a SiN_x ($x = 1.2$) insulating layer was deposited by electron cyclotron resonance chemical vapor deposition (ECR-CVD) at a substrate temperature 260 °C. SiN_x thickness was about 10 nm. For good interface formation in the device fabrication, the surface treatment is important to remove surface chemical contamination. Prior to the gate metal formation, SiN_x surface was treated by 5 % HCl solution. The device without the HCl treatment was also fabricated for comparison. A PtPd gate electrode was formed by sputtering. Four-input reconfigurable circuits were also fabricated on hexagonal nanowire networks with the same process. In the circuit fabrication, PtPd Schottky wrap gates (WPGs) for path switches were formed prior to deposition of SiN_x layer.

4. Results and discussion

Figure 2 shows hysteresis characteristics of fabricated switches with and without the HCl treatment. The wire width and the gate length were 610 nm and 480 nm,

respectively. The measurement was carried out at room temperature (RT). The initial threshold voltages, V_{th0} , for switches with and without HCl treatment were -0.6 V and -0.9 V, respectively. Fabricated switches showed clockwise hysteresis. This result confirmed that electrons traps were formed by inserting the SiN_x layer in the gate. Both on and off states of the nanowire conductance at $V_G = 0$ V were successfully realized. The amount of hysteresis depended on the surface treatment. Large hysteresis of 2 V was obtained in the switch with HCl treatment. Estimated trapped density from the hysteresis curves in the devices with and without the treatment was $2.4 \times 10^{12} \text{ cm}^{-2}$ and $1.4 \times 10^{12} \text{ cm}^{-2}$, respectively.

Figure 3(a) shows the program-time dependence of the off-state retention time, τ_R . It was defined as a time period in which V_{th} was larger than 0 V after off-state programming. Programming voltage, V_P , was 2 V. Here we focused on the off state because the nanowires always appeared the on-state in initial and the stability of the circuit operation was determined by the off state. τ_R increased rapidly when the programming time increased from 0 to 10 ns. When the programming was longer than 10 ns, it became almost constant. The increase of τ_R in the short programming time was due to RC delay by a gate resistance of 100 Ω and a parasitic cable capacitance of 100 pF. τ_R of the switch with HCl treatment was more than tenfold of that without the treatment. Considering that the present system was a short channel high-electron-mobility transistor (HEMT) with SiN_x/GaAs interface traps, τ_R is theoretically given by [12,13]

$$\tau_R = \tau_e \ln \left(-\frac{qn_T}{C_{AlGaAs}V_{th0}} \right) = \tau_e \ln \left(-\frac{\alpha V_P}{V_{th0}} \right), \quad (1)$$

where τ_e is the emission time constant of interface traps, q is the elemental charge, n_T is

the trapped electron density, n_T is empirically expressed as $\alpha C_{\text{AlGaAs}} V_p / q$, where C_{AlGaAs} is the capacitance of a AlGaAs layer. α is $V_{\text{SiN}} / (V_{\text{AlGaAs}} + V_{\text{SiN}})$ where V_{SiN} and V_{AlGaAs} are voltage drops in the SiN_x and the AlGaAs layers, respectively. Calculated off-state retention time using Eq. (1) with α of 0.8 and threshold voltages in Fig. 2 were plotted in Fig. 3(a). The experimental data agreed with the theoretical values. The large difference of the retention time is understood by the difference of emission time constant, τ_e .

τ_e increases when the trap level became deep. Trap energy from a GaAs conduction band edge, E_T , was evaluated from Arrhenius plot of τ_e . E_T in the devices with and without HCl treatment was 280 meV and 370 meV, respectively. Both energies corresponded to the reported SiN_x/GaAs interface trap levels [11]. On the other hand, it has not been clarified that the HCl treatment resulted in deeper energy traps with high density. Its possible role is to supply H⁺ ions. Abrupt slope in the transfer curve as compared to that without the treatment in Fig. 2 indicated the decrease of the continuous interface states. Assuming the diffusion of H⁺, this result could be understood by the termination of dangling bond by H⁺. In addition, H⁺ in the SiN_x is known to create discrete electron traps [14], which might be deep and high density. One possible way to confirm that H⁺ plays a dominant role is using other surface treatments including hydrogen. For example, H₂SO₄ solution or H₂ annealing should affect similarly as HCl treatment. However, further investigation is necessary to confirm that such diffusion of H⁺ occurs.

Short programming time is desirable for switching the conductance in the dynamic reconfiguration of circuits. Figure 3(b) shows the on-state current in the switch as a function of the programming time. V_p was -2 V. The current was normalized with saturated current obtained at 10 sec after the programming. Minimum on-state programming time, τ_{Ponmin} was defined as the time where the normalized current

reached unity. Evaluated τ_{Ponmin} of were 3×10^{-4} sec, almost in the same for two devices. The on-state programming took longer time than the off-state one. This is simply because the on-state is realized by detrapping of electrons and this process takes longer time than capturing due to the existence of the energy barrier of E_T . It was found that τ_{Ponmin} could be decreased by increasing V_p . Large negative programming voltage causes high field in the system and enhances the carrier emission by the field-assisted tunneling [15]. The details will be reported elsewhere.

Effects of the performance of the switches in integrated circuit level were investigated experimentally. Figure 4 shows a SEM image of a fabricated four-input reconfigurable BDD circuit on a hexagonal nanowire network. 15 path switch and 16 programmable switches were integrated in this circuit. The circuit area was $38 \times 58 \mu\text{m}^2$. All of four-input Boolean logics ($2^n = 65526$ functions, where n is the number of programmable switches) can be operated with only this circuit.

Figure 5 shows measured input-output waveforms of fabricated reconfigurable circuits integrating switch arrays without and with the HCl treatment. As an example, circuits were programmed to operate a NOR function using program voltage of ± 4 V for 1 s and ± 2 V for 10 ms without and with the HCl treatment, respectively. Input signal frequency was 100 Hz. Electrons were injected from the root and the current in the terminal was measured as output. Both fabricated circuits operated correctly at RT. In case of integrating a switch array without HCl treatment, the base line of the output gradually increased with time as shown in Fig. 5(a), even though high voltage programming was made for long time. Such unstable operation was caused by incomplete off-state in the switch array due to short retention time. On the other hand, as expected from the data in Fig. 3(a), stable operation of the switches with HCl treatment results in the stable operation of the circuit. Stable operation could maintain for 2 sec, which corresponded to the off-state retention time in Fig. 3(a). Observed

behaviors indicated that the retention time and the switching speed of the conduction state in the switch array directly influenced the stability and reconfiguration speed of the circuit. From the data in Fig. 3(b), circuit reconfiguration within 0.25 msec is possible when $V_p = \pm 2$ V and it will be further reduced by increasing V_p . If the operation frequency is increased, the programming time becomes short and conductance switching becomes insufficient. From the data in Fig. 3, the programmable switch operation degraded when $f > 3$ kHz. On the other hand, the obtained programming time is similar between devices with and without HCl treatment. Therefore it is thought that the HCl treatment does not degrade the operation as compared with that without treatment even though frequency is increased.

A possible approach to realize long stable circuit operation is interface engineering in the switch to control band bending in the SiN/GaAs interface to relax build-in field so as to suppress carrier emission from the trap at zero gate bias.

4. Conclusions

Programmable nano-switch arrays on GaAs-based nanowire networks were investigated for a reconfigurable binary-decision-diagram (BDD) logic circuit. Programmable switches were fabricated by inserting a SiN_x thin layer between a metal gate and a nanowire. The sample in which HCl treatment was made on the SiN_x prior to metal gate formation remarkably improved hysteresis curve, program time dependences of off-state retention time, and on-state current. We successfully fabricated a four-input reconfigurable BDD circuit integrating the switch array and demonstrated correct and stable operation of the circuit with HCl treatment process.

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Figure captions

Figure 1 Schematics of a reconfigurable BDD logic circuit and a programmable nano-switch array on a AlGaAs/GaAs hexagonal nanowire network.

Figure 2 Hysteresis characteristics of fabricated programmable switches.

Figure 3 Program time dependences of (a) Retention time after off-programming which $V_p = 2$ V, (b) current recovery ratio after on-programming which $V_p = -2$ V. The wire width and the gate length were 480 nm, and 600 nm, respectively.

Figure 4 SEM image of a fabricated four-input reconfigurable BDD circuit.

Figure 5 Input-output waveforms of fabricated circuits programmed to operate NOR. (a) without HCl treatment and (b) with HCl treatment.

Fig.1

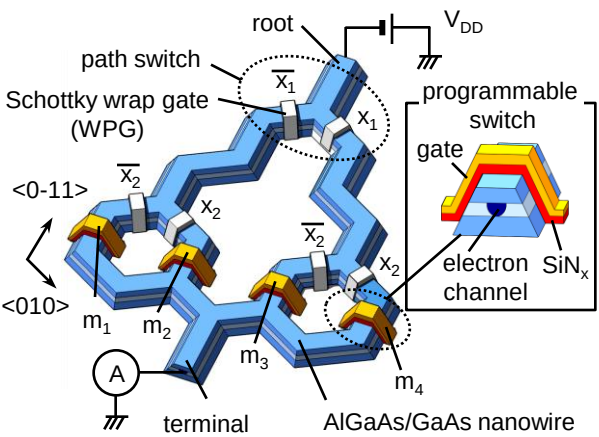


Fig.2

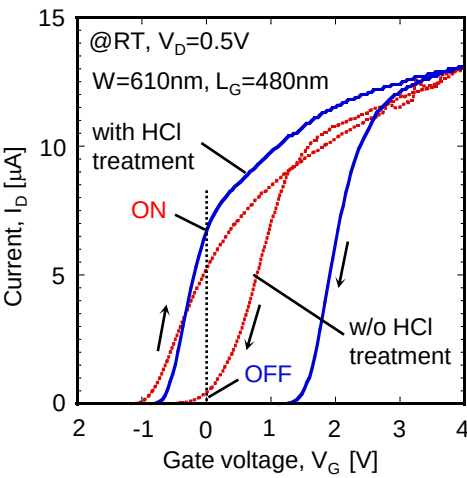


Fig.3

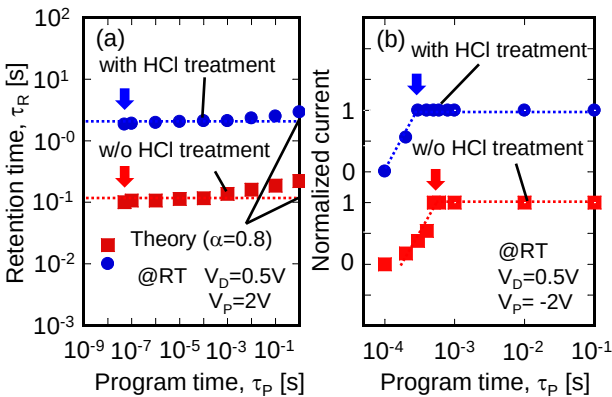


Fig.4

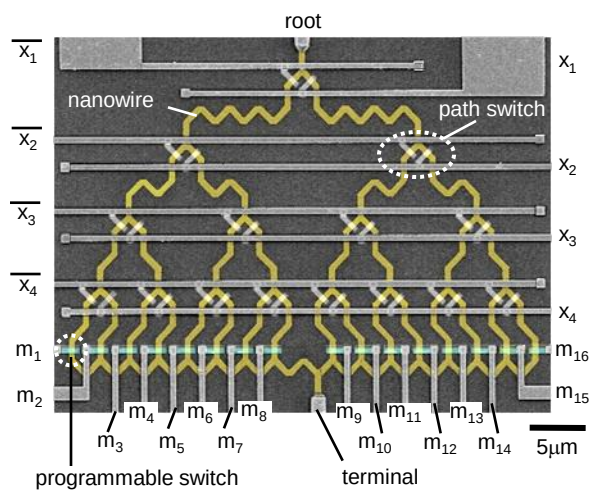


Fig.5

