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**High-k Al₂O₃ MOS Structures with Si Interface Control Layer
Formed on Air-Exposed GaAs and InGaAs Wafers**

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Abstract

This paper attempts to realize unpinned high-k insulator-semiconductor interfaces on air-exposed GaAs and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ by using the Si interface control layer (Si ICL). Al_2O_3 was deposited by *ex-situ* atomic layer deposition (ALD) as the high-k insulator. By applying an optimal chemical treatment using HF acid combined with subsequent thermal cleaning below 500°C in UHV, interface bonding configurations similar to those by *in-situ* UHV process was achieved both for GaAs and InGaAs after MBE growth of the Si ICL with no trace of residual native oxide components.

As compared with the MIS structures without Si ICL, insertion of Si ICL improved the electrical interface quality a great deal both for GaAs and InGaAs, reducing frequency dispersion of capacitance, hysteresis effects and interface state density (D_{it}). A minimum value of D_{it} of $2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ was achieved both for GaAs and InGaAs. However, the range of bias induced surface potential excursion within the band gap was different, making formation of electron layer by surface inversion possible in InGaAs, but not possible in GaAs. The difference was explained by the disorder induced gap state (DIGS) model.

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Keywords: Al_2O_3 , MIS, Si ICL, GaAs, InGaAs, hydrofluoric acid

1. Introduction

In the main stream of silicon-based electronic, the ultimate scaling limit of Si MOS transistors is approaching rapidly [1,2]. In order to extend the CMOS technology beyond this limit along the line of the so-called More Moore approach on the Si platform, intensive research efforts are currently going on to develop MOS transistors formed on high-mobility III-V channel materials. Here, the key point is realization of high performance high-k MOS gate stacks on III-V materials. Additionally, such gate stacks are also required for development of “Beyond CMOS” devices using III-V nanowire transistors.

However, surfaces of III-V materials are known to be very difficult to passivate due to strong tendency of Fermi level pinning at insulator-semiconductor (I-S) interfaces [3, 4]. For this, a new method of direct deposition of high-k insulators such as HfO_2 and Al_2O_3 on III-V semiconductors by the atomic layer deposition (ALD) has recently become a popular approach [5-9]. In contrast to previous standard deposition technologies like thermal and plasma chemical vapour deposition (CVD), it is a much gentler process to surfaces with monolayer level control and some built-in in-process effect of interface self-cleaning and thinning of native oxides [7, 8]. However, a recent detailed study on the ALD $\text{Al}_2\text{O}_3/\text{GaAs}$ interface [9] indicated existence of strong Fermi level pinning, and one is not sure whether such a direct deposition approach, although it is simple and practical, is truly viable for fabrication of high performance III-V MOS gate stacks.

In contrast to this, our method for surface passivation of III-V materials is a much more sophisticated one, inserting a Si interface control layer (Si ICL) at the I-S interface [10,11]. Here, the Si ICL is grown *in situ* by molecular beam epitaxy (MBE) on the

MBE-grown clean III-V surface. Using this method, we recently reported on successful fabrication of the HfO_2/GaAs high-k MOS structure, realizing a completely unpinned I-S interface with a minimum of interface state density (D_{it}) of $1 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ or below [12, 13]. However, the drawback of this process is that it cannot be applied to standard III-V epitaxial wafers with air-exposed surfaces, because it requires *in-situ* MBE growth of both of the III-V material and the Si ICL. This is obviously a severe constraint for device fabrication in industrial environments.

To solve this difficulty, we attempt in this paper to make the Si ICL method applicable to air-exposed GaAs and InGaAs wafers. In view of applications to *n*-channel enhancement MOSFETs by surface inversion, a Zn-doped p-type bulk GaAs wafer and an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ epitaxial wafers grown by metal-organic chemical vapour deposition (MOCVD) with Zn doping were used. As the high-k insulator, Al_2O_3 films formed by the ALD process were chosen. Prior to the MBE growth of the Si ICL, efforts were made to minimize native oxide components on the wafer surfaces by various wet surface treatments. By using HF-based surface treatment combined with a thermal cleaning, interface bonding configurations similar to those obtained by *in-situ* UHV process was realized. As compared with the $\text{Al}_2\text{O}_3/\text{GaAs}$ and $\text{Al}_2\text{O}_3/\text{InGaAs}$ MIS structures without Si ICL, insertion of the Si ICL achieved large reduction of interface state density, D_{it} , giving a minimum value of $2 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ for both GaAs and InGaAs. However, as for the range of surface potential excursion within the energy gap, the result was much more favorable in InGaAs than GaAs, and this was explained by the disorder induced gap state (DIGS) model [14].

2. Experimental

The sample fabrication sequence is shown in Fig.1. The sample piece taken from an air-exposed p-type GaAs wafer or p-type InGaAs/InP epitaxial wafer was subjected to a surface treatment. Then, it was introduced into the MBE chamber and a thermal cleaning was applied before the MBE growth of the Si ICL in order to remove residual native oxide components. Then, a Si ICL was grown at the substrate temperature of 300°C up to 6 ML refering to our recent work [13]. The source was the Si k-cell heated at 1200°C. After the growth of the Si ICL, an ultrathin SiN_x buffer layer was formed by *in-situ* partial nitridation of the Si ICL by using a plasma radical beam source. Then, the sample was annealed in UHV to remove physisorbed arsenic component. Subsequently, the sample was taken out from the MBE chamber, and transferred to the ALD chamber. Here, the SiN_x/Si structure effectively prevents subcutaneous oxidation during sample transfer in air in spite of the monolayer level thickness of the SiN_x buffer layer, as confirmed previously [12]. As the main high-k insulator, an Al₂O₃ film was deposited by the standard ALD process. Here, reactants were supplied in a pulse flow sequence of H₂O (0.015sec) - purge (5sec) - trimethylaluminium (TMA) (0.015sec) - purge (5sec), at 300°C in a N₂ flow of 20 sccm at 0.3 Torr. A typical value of relative dielectric constant of the resultant ALD Al₂O₃ film was 9-10 with a resistivity of about 10¹⁵ Ωcm.

For chemical characterization, the sample surface was studied by *in-situ* X-ray photoelectron spectroscopy (XPS) using Al Kα source (1486.6 eV) at each step of sample fabrication.

For electrical characterization, capacitance-voltage (C-V) measurements were carried out on MIS capacitors. To make GaAs and InGaAs MIS capacitors, Al field

plate and Au/Zn/Au back contact were formed by evaporation. They were annealed at 400°C in nitrogen for 3min. As reference samples, MIS structures without the Si ICL were also prepared.

3. Results and discussion

3.1 Removal of native oxide layer by an optimal chemical surface treatment

To make the Si ICL method applicable to air exposed III-V wafer, successful removal of native oxides from the surface is a key point. Figure 2(a) shows the XPS spectra obtained on an as-received GaAs wafer. The result indicates that a mixed native oxide layer consisting of Ga₂O₃ and As₂O₃ with a thickness of 1.5-2.0 nm exists on the surfaces. A similar result was obtained for InGaAs as shown elsewhere [15]. These uncontrolled native oxide layers must be removed by a suitable surface treatment prior to the Si ICL growth.

For this, we carried out a systematic study on oxide removal by wet chemical treatments. The aim was not simply to select a treatment which maximizes oxide removal after the chemical treatment, but to determine a treatment which makes the interface structure after the Si ICL growth as close as possible to that of the *in-situ* process. Investigated treatments included a solution of H₂SO₄:H₂O₂:H₂O= 3:1:1 for GaAs, a solution of H₃PO₄:H₂O₂:H₂O=1:1:38 for InGaAs, aqueous solutions of HCl, NH₄OH, HF for both, and Furuuchi SEMICOCLEAN solution for both which is a commercial alkaline based solution frequently used for removing surface native oxide layer of semiconductor substrates before epitaxial growth. After careful study of the

resultant data, we came to a conclusion that the HF solution gives the best result both for GaAs and InGaAs.

The series of XPS data taken on GaAs surface after the HF treatment are summarized in Fig.2 (b)-(d). The time length for dipping the sample into the HF solution in the dark was as short as 40 sec which was the optimum condition that we empirically found. As shown in Fig. 2 (b), the shape of Ga3d spectrum after HF treatment became almost the same as that from the MBE clean surface of GaAs, which indicated that the HF treatment removes the Ga oxide component rather efficiently, making the surface As-rich phase with As₂O₃ and elemental As. Since it is easy to remove As components in UHV environment, we believe that this is the key feature which makes the HF treatment attractive for the present purpose. However, the Ga₂O₃ component was not completely removed, because a small amount of Ga₂O₃ component was detected in the more surface-sensitive Ga2p spectra as can be seen on the right of Fig.2(b). Very similar result was obtained on the InGaAs surface.

3.2 Thermal cleaning and MBE growth of Si ICL

Figure 2 (c) shows XPS spectra of the HF-treated GaAs surface taken after a thermal cleaning at 450°C for 3min in UHV. As can be seen in Fig.2(c), As-related surface components had completely disappeared after thermal cleaning. From the viewpoint of Si ICL growth, this is very favourable, since it reduces the chance of incorporation of As into the Si ICL during its growth. In our experience, this removal of As components in a few minutes requires a temperature higher than 350°C. For example, annealing at 300°C for the period of 3 min did not remove As components completely. On the other

hand, the amount of Ga_2O_3 slightly increased, and became visible on the $\text{Ga}3d$ spectrum. This is most likely due to oxidation of GaAs caused by dissociation of volatile As_2O_3 component.

The XPS spectra taken after the MBE growth of the Si ICL at 300°C are shown in Fig. 2 (d). Here, it is clearly seen that Ga_2O_3 component disappeared again. This time, disappearance is complete in the sense that it is not visible any more in the surface sensitive $\text{Ga} 2p$ spectrum. It is highly likely that, by the presence of large amount of Si, the small amount of Ga_2O_3 was deoxidized into Ga_2O or fully deoxidized to produce SiO , and these products sublimed during the Si growth.

In addition to this, it is noted in Fig.2(d) that Ga-Si , As-Si and As-As bonding components newly appeared after the Si growth. Here, the Ga-Si component was observed only in the $\text{Ga}3d$ spectrum, and not in the $\text{Ga}3p$ spectrum. Considering the difference in the escape depth between $\text{Ga}2p$ and $\text{Ga}3d$ spectra, it indicates that the Ga-Si bonding exists at the bottom side of the Si ICL. This situation is very similar to that found in the Si ICL/ GaAs structure formed by the *in-situ* process where As atoms play a role of the surfactant forming As-As and As-Si bonds on the top of the Si ICL and leaving Ga-Si bond at the bottom [6]. Thus, we can conclude that the Si ICL was grown on the GaAs surface forming a clean Si ICL/ GaAs interface with a favourable bonding sequence.

A very similar result was also obtained on the air-exposed InGaAs surface after each step of processing, and this has been reported elsewhere in our preliminary study of formation of a $\text{HfO}_2/\text{InGaAs}$ structure [15].

Furthermore, though the data is not shown here, the elemental As component persisted after surface nitridation of the Si ICL. This is again similar to the situation observed in the SiN_x/Si ICL/GaAs structure formed by the UHV in-situ process [12]. Therefore we carried out UHV annealing after surface nitridation in order to remove the elemental As, as shown in Fig.1. We found that annealing at the temperature more than 430°C was necessary for both GaAs and InGaAs. in order to remove the physisorbed As completely from the surface.

3.3 Electrical characterization of interface using MIS capacitors.

Figure 3 (a) and (b) compare the *C-V* characteristics of the GaAs MIS diodes having ALD Al₂O₃ /GaAs and ALD Al₂O₃/Si ICL/GaAs interfaces. Here, the interface SiN_x/Si double layer is denoted as Si ICL for simplicity. The MIS structure without Si ICL shows a marked frequency dispersion, and insertion of Si ICL very much reduced frequency dispersion in the MIS structure with a smaller hysteresis. The D_{it} distributions evaluated by applying the Terman's method on the 1MHz *C-V* curves are shown in Fig.4. It is seen clearly here that the sample with Si ICL shows a large reduction of D_{it} as compared with the sample without Si ICL. A minimum value of D_{it} of $2 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ was achieved. This value is similar to that obtained on the HfO₂/ Si ICL/GaAs interface formed by the *in situ* process [12,13].

The results of *C-V* measurement on the InGaAs MIS diodes with the Al field plate are summarized in Fig. 5(a) and (b). As shown Fig. 5 (a), direct deposition of an ALD Al₂O₃ film onto the air-exposed InGaAs resulted in poor *C-V* characteristics with a large frequency dispersion under the accumulation bias, a small overall capacitance change

with bias, and distinct hysteresis effects. As shown in Fig. 5 (b), the characteristics were very much improved by inserting Si ICL. The D_{it} distributions evaluated by applying the Terman's method on the 1MHz C - V curves are summarized in Fig.6. Again, a minimum D_{it} of $2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ was achieved.

3.4 Range of surface potential excursion

For MISFET device operation, the range of bias-induced surface potential excursion is also important in addition to the minimum value of D_{it} . Although we have obtained the same minimum value of D_{it} for GaAs and InGaAs MIS diode by using the Si ICL, the range of surface potential excursion is much better in the InGaAs MIS capacitor, allowing a nearly full swing of surface potential from the neighbourhood of valence band edge to the neighbourhood of the conduction band edge within the energy gap. In contrast to this, the swing is limited approximately within lower half of the band gap in the case of GaAs even with the use of the Si ICL. Thus, the formation of electron layer by surface inversion is possible in the present $\text{Al}_2\text{O}_3/\text{Si ICL}/\text{InGaAs}$ MIS system, but not possible in the present $\text{Al}_2\text{O}_3/\text{Si ICL}/\text{GaAs}$ MIS system.

This difference can be explained by the DIGS model by Hasegawa and Ohno [14]. According to this model, disorder of interface bonds produces a U-shaped gap state continuum of lower donor states and upper acceptor states. Here, the boundary between donor and acceptor states takes place at the charge neutrality level, E_{HO} , where the state density becomes the minimum of the U-shaped distribution. The state density distribution is given empirically by the following exponential functional form.

$$D_{it}(E) = D_{it0} \exp\left(\left|E - E_{HO}\right| / E_{Oj}\right)^{nj} \quad (1)$$

where j refers to donor or acceptor state, D_{it0} is the minimum state density, and n is the empirical fitting exponent. The position of E_{HO} is determined by the band structure, and located at 0.47 eV above the conduction band for GaAs and InGaAs, obeying the so-called common anion rule [14].

In Figs.4 and 6, we see U-shaped D_{it} distributions with the minimum values taking place near 0.5 eV, roughly following the above prediction. D_{it} values also increase exponentially around the minimum point. Thus, the observed behavior is consistent with the DIGS model. The measured ranges of the bias-induced surface potential excursion are plotted in Fig.7 with respect to E_{HO} for Si ICL-controlled GaAs and InGaAs MIS systems. We note a striking similarity of the surface potential excursion range with respect to E_{HO} between the present two systems. It strongly suggests that the degree of interface order is similar between two systems due to the similarity of processing. On the other hand, the previous *in-situ* processing gave a much wider range for GaAs as also shown by a white column in Fig.7. Thus, although we could not detect a large difference between the *ex-situ* and *in-situ* methods by the XPS characterization, there must be sub-monolayer-level difference in the structure which makes the *in-situ* process better than the carefully controlled *ex-situ* process. This seems not surprising from the experience of the delicateness of the semiconductor epitaxial growth. It also indicates that, since the state density increases exponentially around E_{HO} , surface passivation of GaAs is, in general, much more difficult than that of InGaAs due to the fact that energy distance between the conduction band edge and the charge neutrality level is much larger.

4. Conclusion

In this paper, we made an effort to make our Si ICL method applicable to air-exposed GaAs and InGaAs wafers. As the high-k MIS insulator, an Al₂O₃ film by ALD was used. As for the treatment to reduce native oxides prior to MBE growth of the Si ICL, a chemical treatment using HF acid combined with subsequent thermal cleaning below 500°C in UHV was found to be optimum for both GaAs and InGaAs. Interface bonding configurations similar to those by *in-situ* UHV process was achieved after growth of the Si ICL with no trace of native oxide components.

As compared with the MIS structures without Si ICL, insertion of the Si ICL improved the electrical interface quality a great deal both for GaAs and InGaAs, reducing frequency dispersion of capacitance, hysteresis effect and D_{it} . A minimum value of D_{it} of $2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ was achieved both for GaAs and InGaAs. However, the range of bias-induced surface potential excursion within the band gap was very different, making formation of electron layer by surface inversion possible in InGaAs, but not possible in GaAs. The difference was explained by the DIGS model.

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Figure captions

Fig. 1 Sample fabrication sequence.

Fig. 2 XPS results for GaAs; (a) air-exposed surface, (b) after HF treatment, (c) after thermal cleaning at 450°C in UHV, and (d) after Si ICL growth.

Fig. 3 C - V characteristics for ALD $\text{Al}_2\text{O}_3/\text{GaAs}$ MIS structures; (a) sample without Si ICL and (b) sample with Si ICL.

Fig. 4 D_{it} distributions for GaAs MIS structures.

Fig. 5 C - V characteristics for ALD $\text{Al}_2\text{O}_3/\text{InGaAs}$ MIS structures; (a) sample without Si ICL, and (b) sample with Si ICL.

Fig. 6 D_{it} distributions for InGaAs MIS structures.

Fig.7 Ranges of bias-induced surface potential excursion for GaAs and InGaAs.

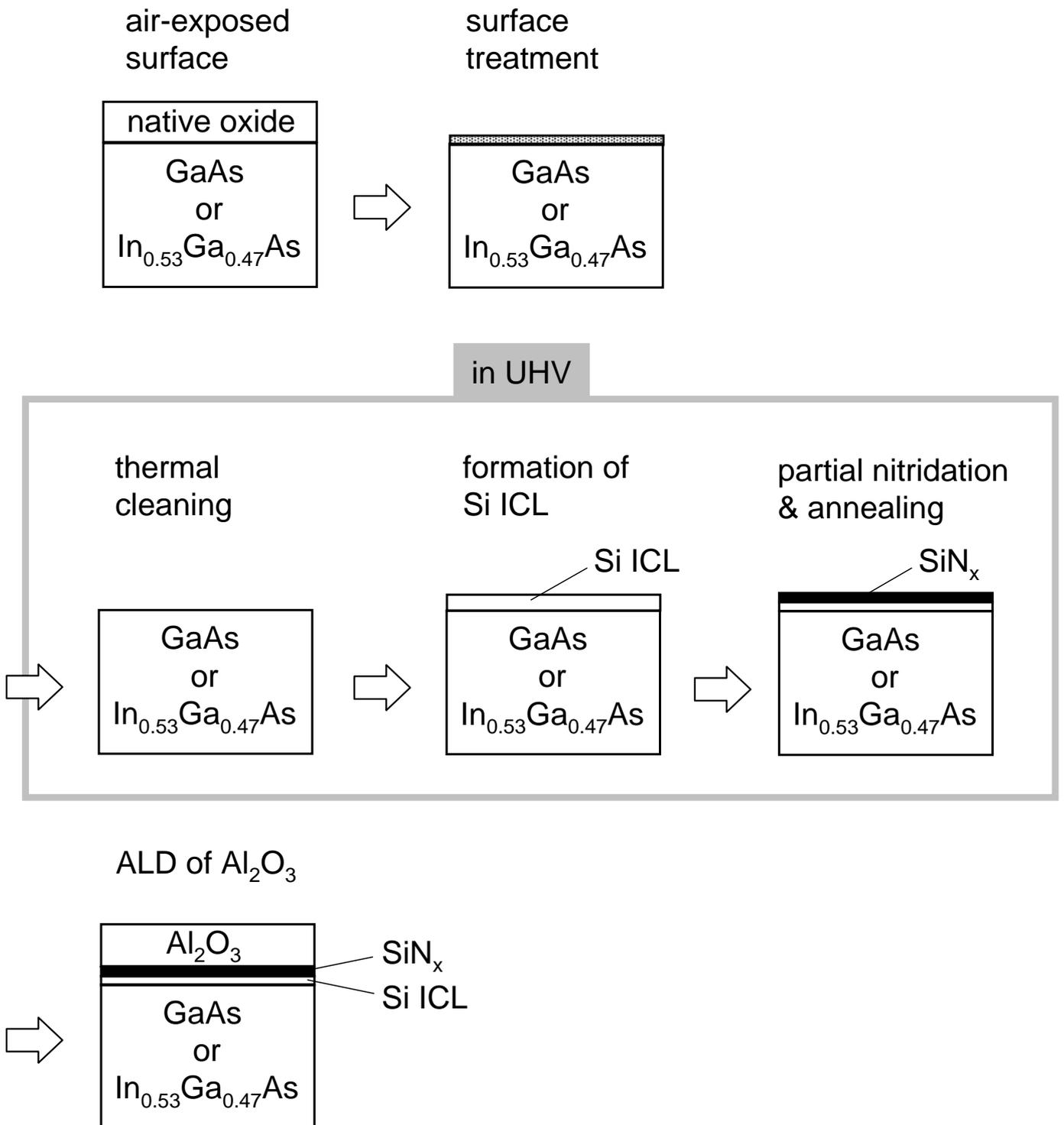
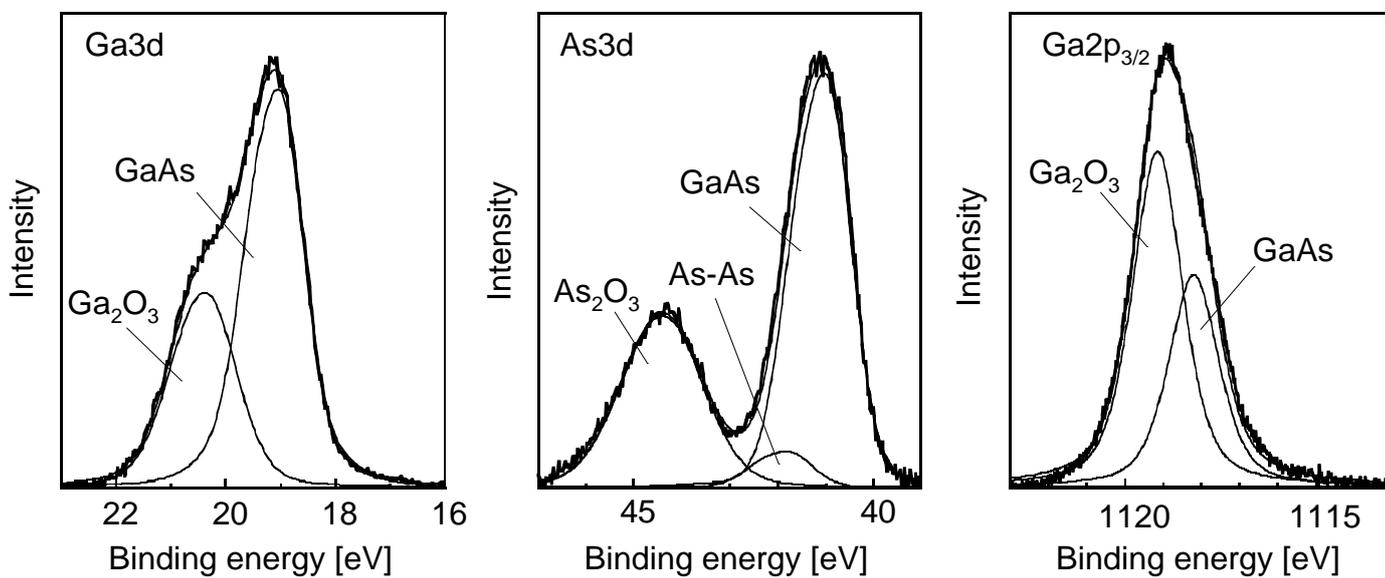
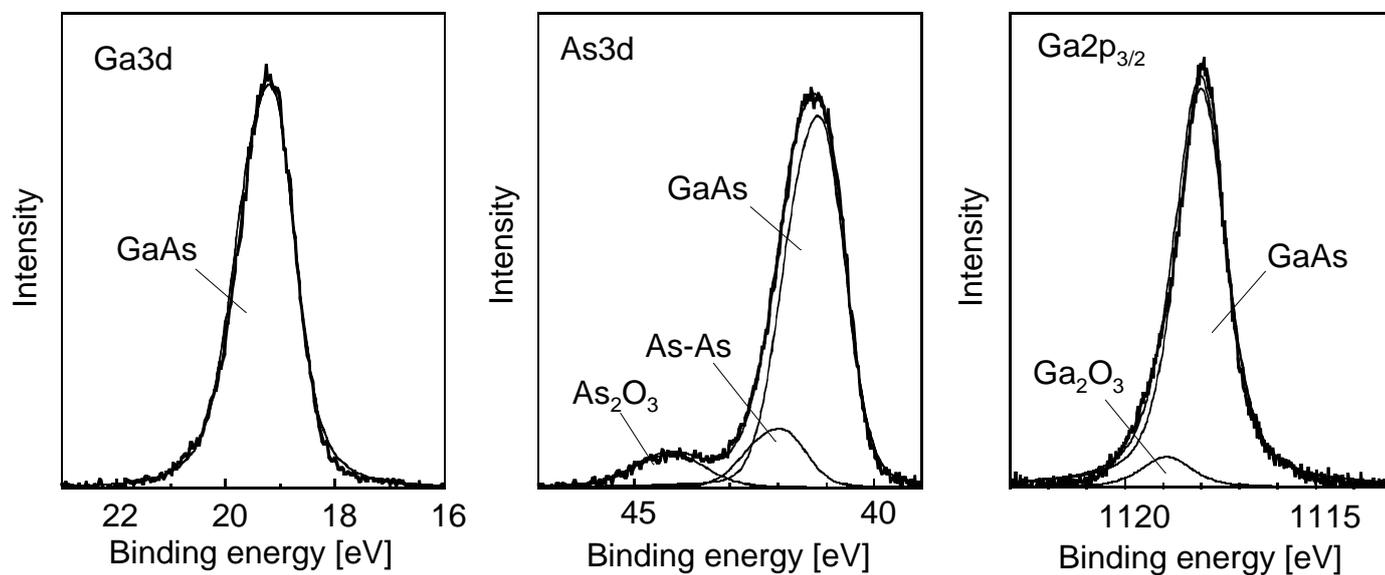


Fig. 1

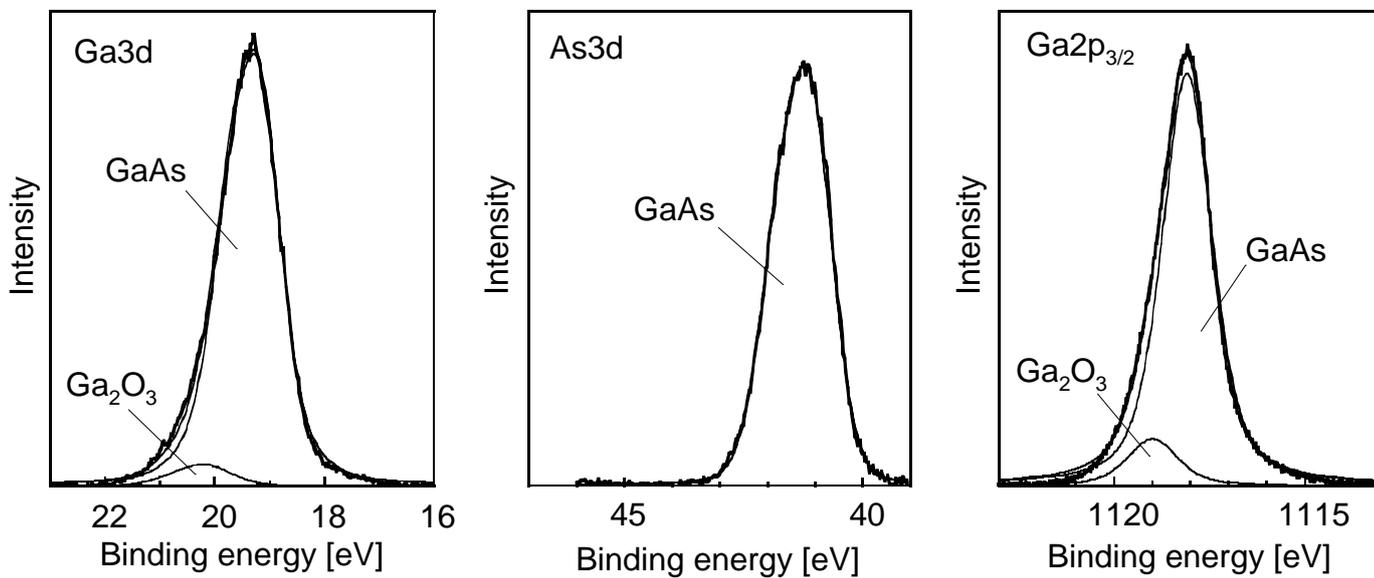


(a)

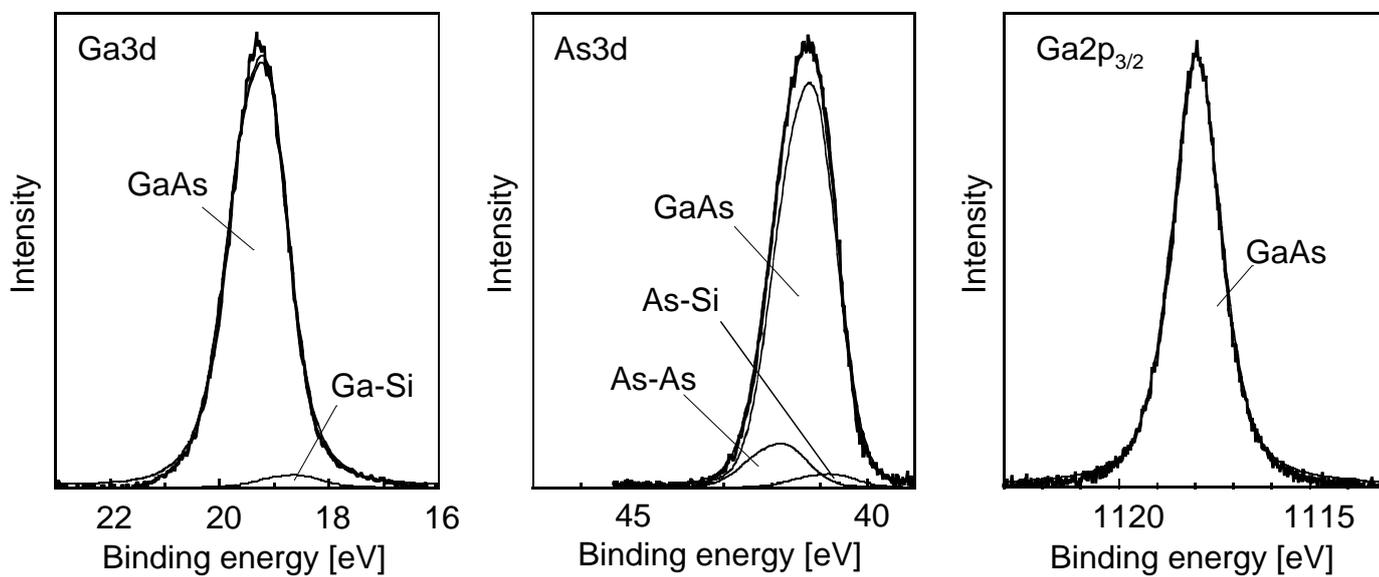


(b)

Fig. 2

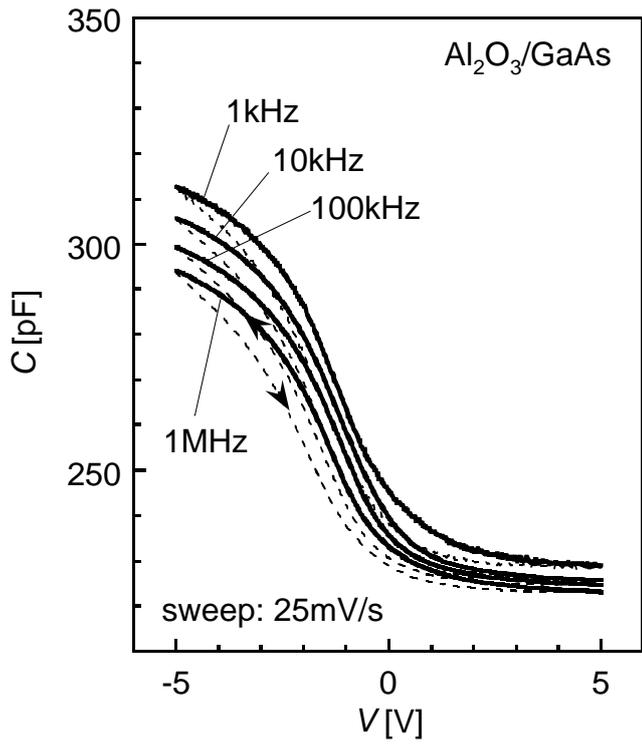


(c)

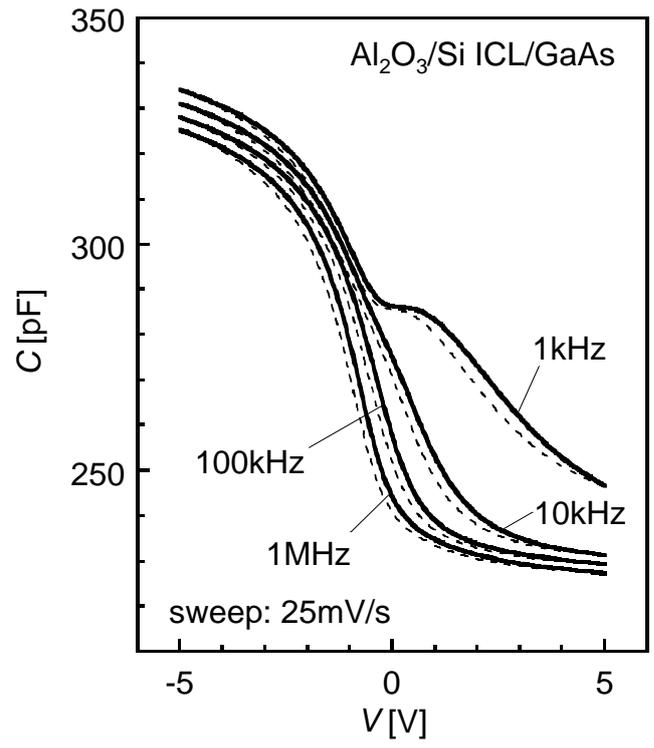


(d)

Fig. 2



(a)



(b)

Fig. 3

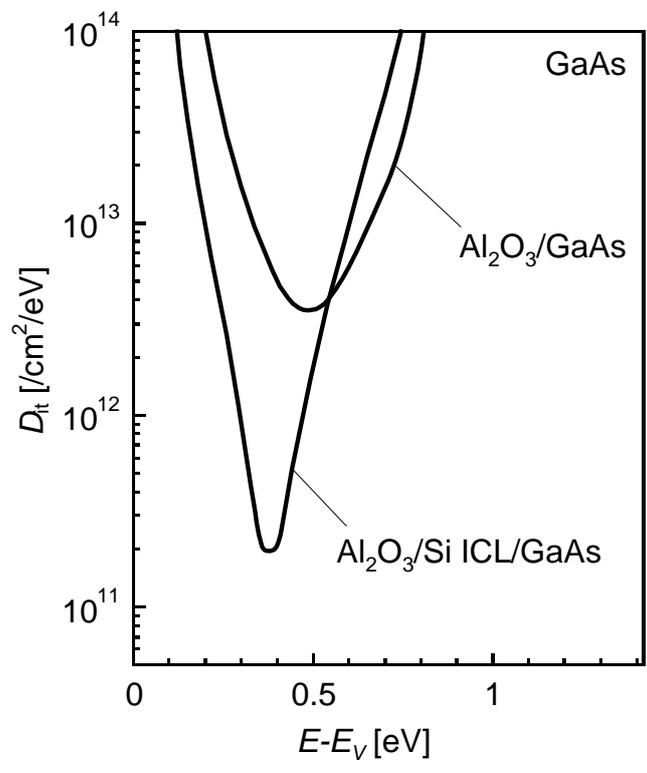
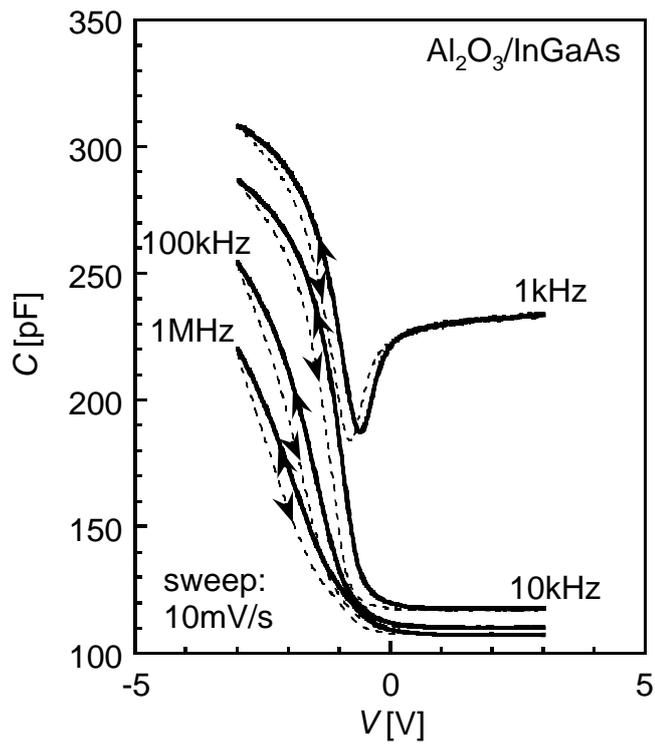
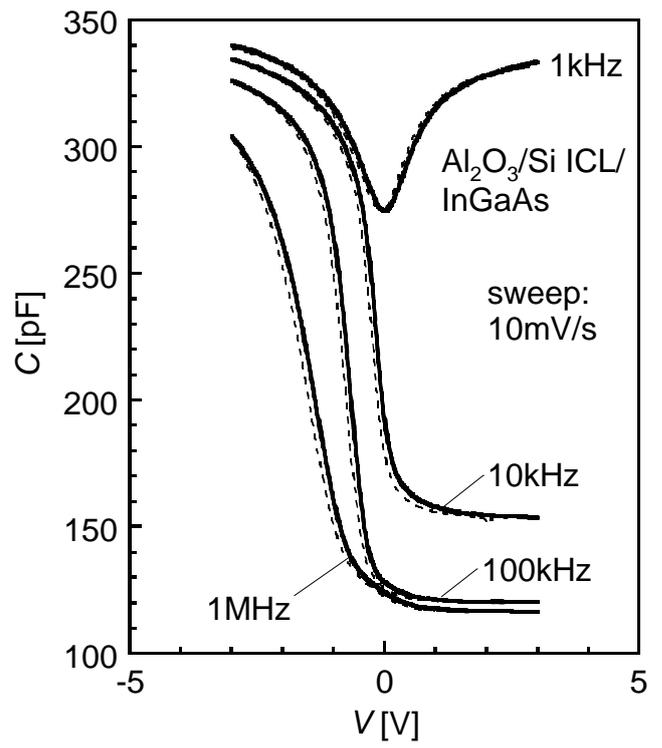


Fig. 4



(a)



(b)

Fig. 5

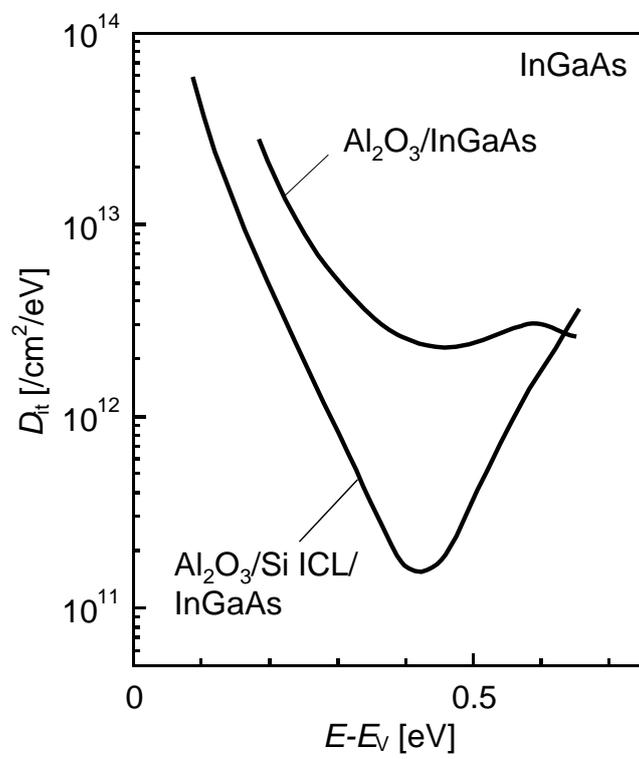


Fig. 6

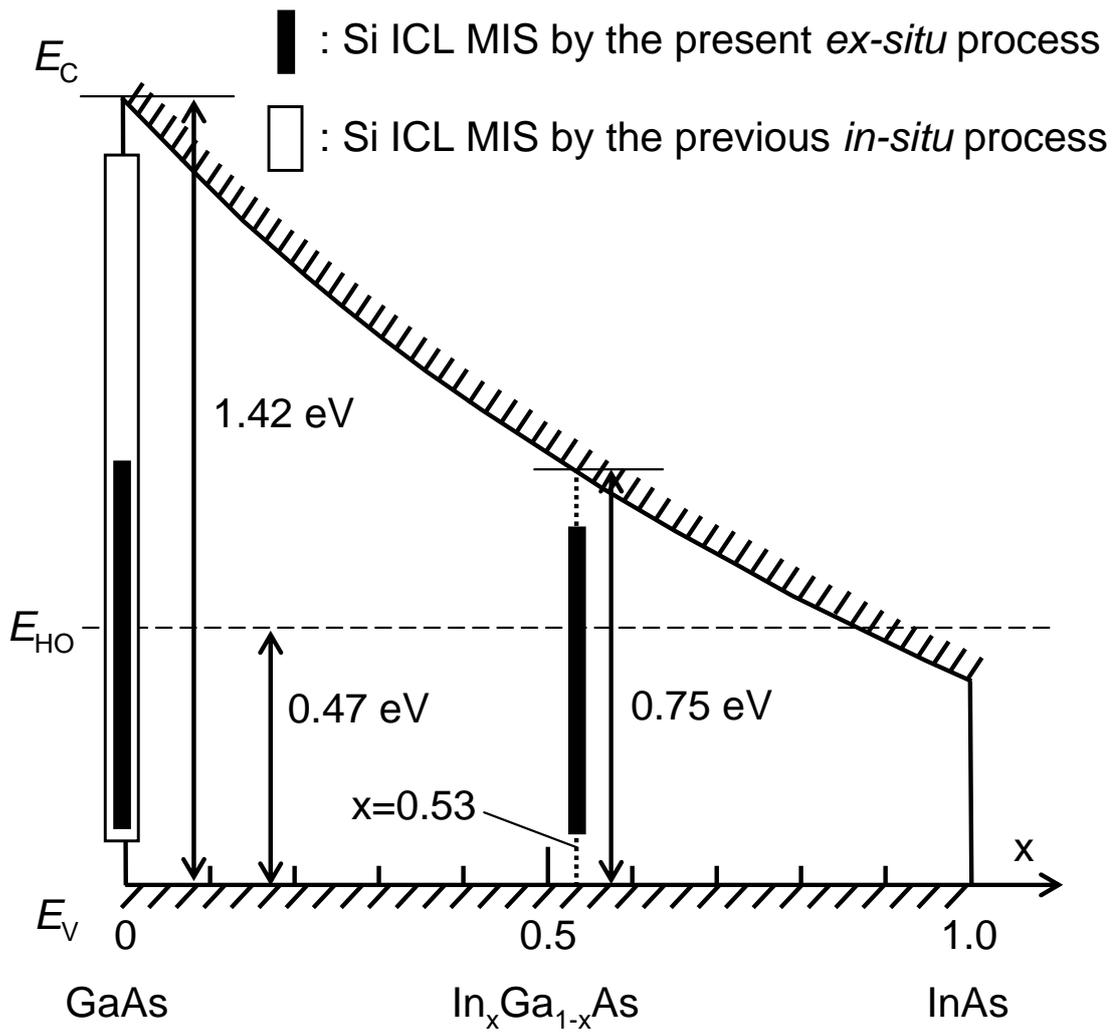


Fig. 7