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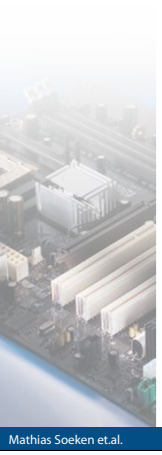
Formal Verification of UML-based Specifications

Dr. Mathias Soeken
University of Bremen

2011/1/31

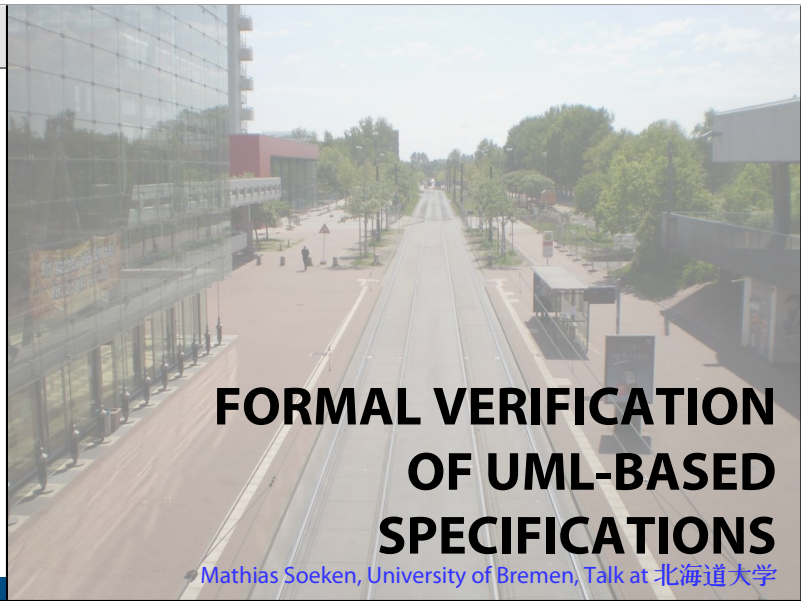
概要

In the recent years, researchers started to enrich the classical textbook specification of embedded systems by more formal descriptions such as the Unified Modeling Language (UML). This enables to lift the starting point for verifcation techniques to the specification level and leads to an improved design flow, where crucial flaws can be detected, even if no executable implementation is available. However, research on efficient solving techniques for the respective verification tasks is just at the beginning. In the talk, the improved design flow based on specifications enriched with formal descriptions is introduced. We illustrate how early design flaws become evident within this flow and briefly review algorithms aimed at detecting them. Furthermore, first experimental results are presented. Overall, the aim of the talk is to provide an introduction into this emerging area and to present first results.



Formal Verification of UML-based Specifications

Mathias Soeken, Robert Wille, and Rolf Drechsler
Institute of Computer Science, University of Bremen
Bremen, Germany
msoeken@informatik.uni-bremen.de
January 31, 2011



About

Dipl.-Inf. Mathias Soeken (msoeken@informatik.uni-bremen.de)

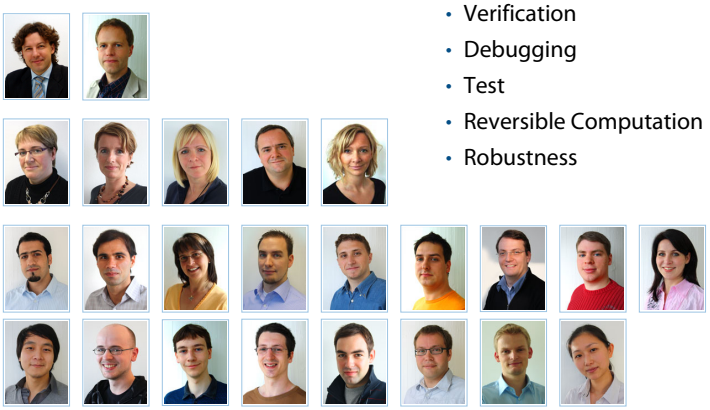
Curriculum Vitae

- 2004 - 2008: Received Diploma Degree in CS at University of Bremen
- 2008 - 2009: Internship at Mentor Graphics, Hamburg
- since 2009: PhD Student at the Computer Architecture Group of Prof. Rolf Drechsler at University of Bremen

Research Interests

- Formal Verification
  - PhD Thesis about Specification Checking
- Reversible Computation and Quantum Computation
  - Supervisor of a Graduate Students Project
  - Development of RevKit, a Toolkit for Reversible Computation WWW

Computer Architecture at University of Bremen WWW



- Verification
- Debugging
- Test
- Reversible Computation
- Robustness

Specification Verification

Specification (as Textbook)

System model (e.g. in SystemC)

Specification Verification

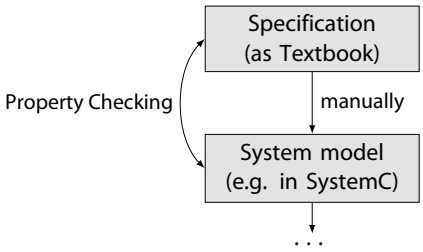
Specification (as Textbook)

manually

System model (e.g. in SystemC)

. . .

Specification Verification



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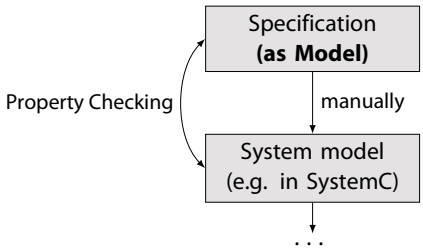

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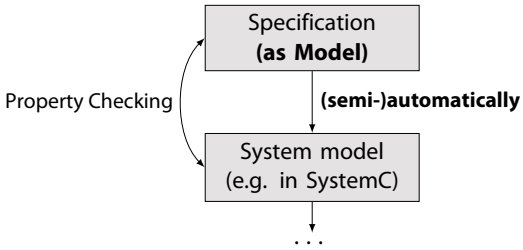

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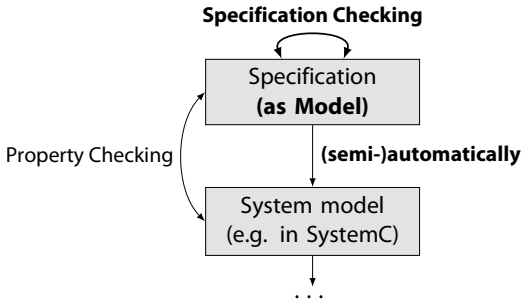

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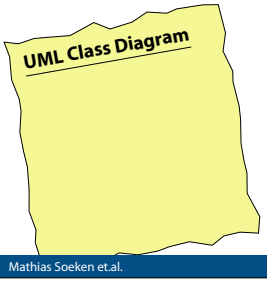

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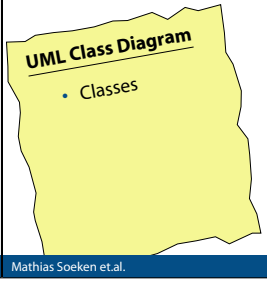
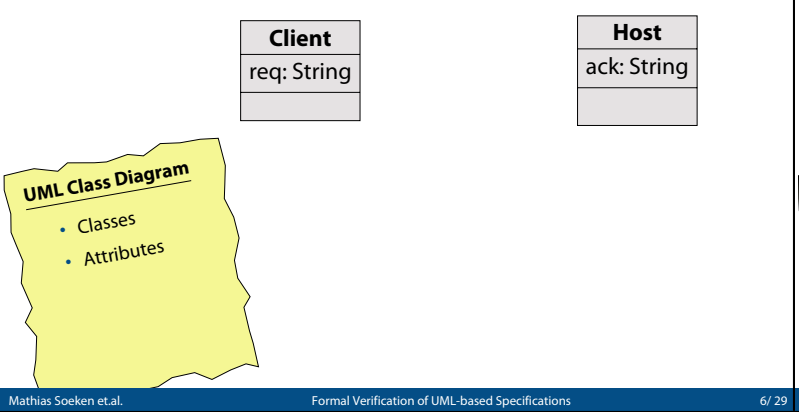
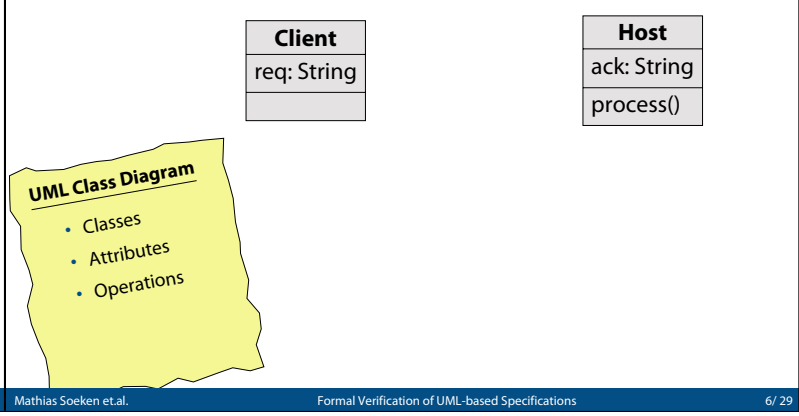



Client
req: String
Host
ack: String
UML Class Diagram
Classes
Attributes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process()
UML Class Diagram
Classes
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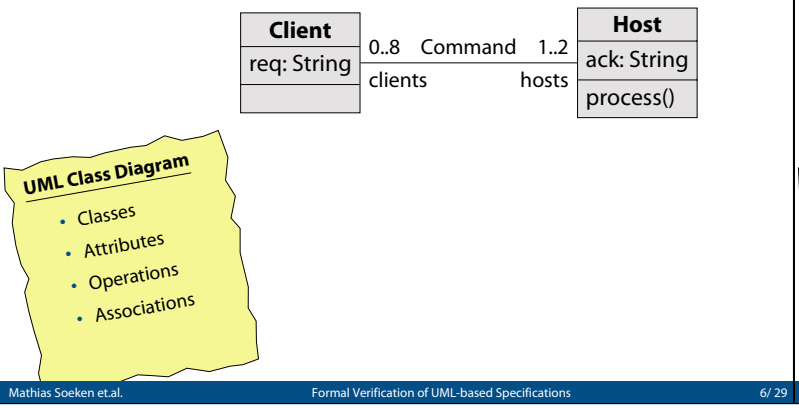
Operations


Client
req: String
0..8
Command
1..2
clients
hosts
Host
ack: String
process()
UML Class Diagram
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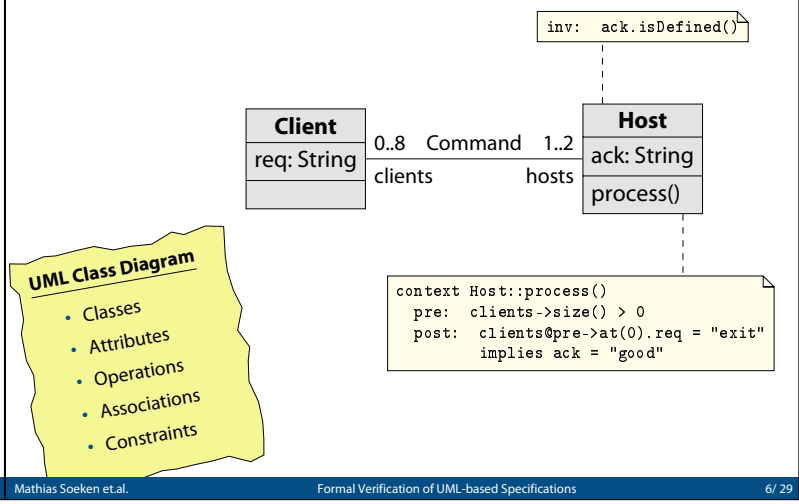
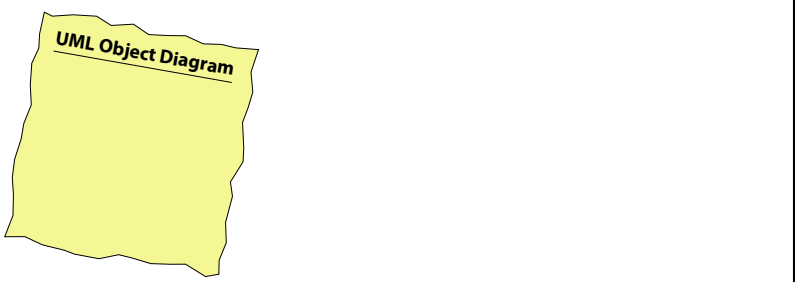
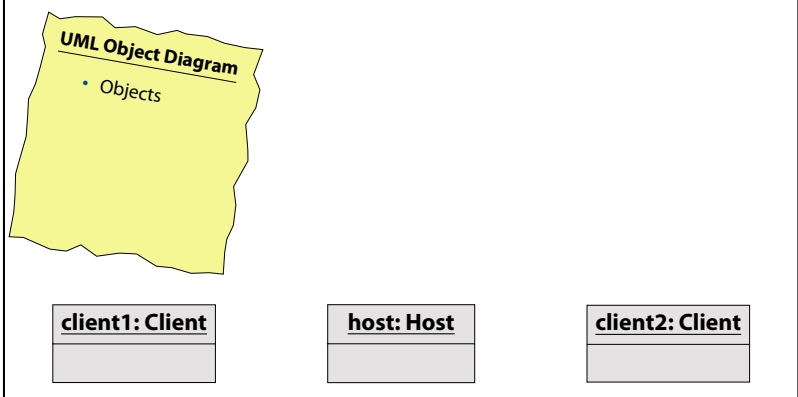
Associations


inv: ack.isDefined()
Client
req: String
0..8
Command
1..2
clients
hosts
Host
ack: String
process()
context Host::process()
pre: clients->size() > 0
post: clients@pre->at(0).req = "exit"
implies ack = "good"
UML Class Diagram
Classes
Attributes
Operations
Associations
Constraints


UML Object Diagram


UML Object Diagram
Objects
client1: Client
host: Host
client2: Client

UML Object Diagram
- Objects
- Attributes

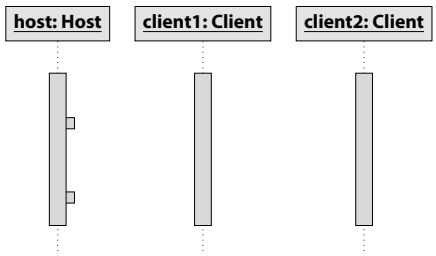
client1: Client	host: Host	client2: Client
req = "date"	ack = "good"	req = "exit"

UML Object Diagram
- Objects
- Attributes
- Links

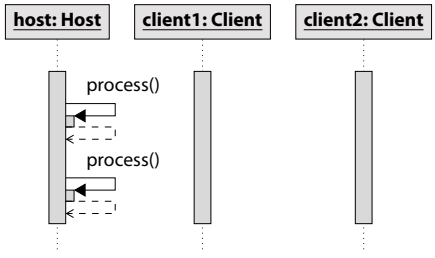
client1: Client	Command	host: Host	Command	client2: Client
req = "date"		ack = "good"		req = "exit"

UML Sequence Diagram

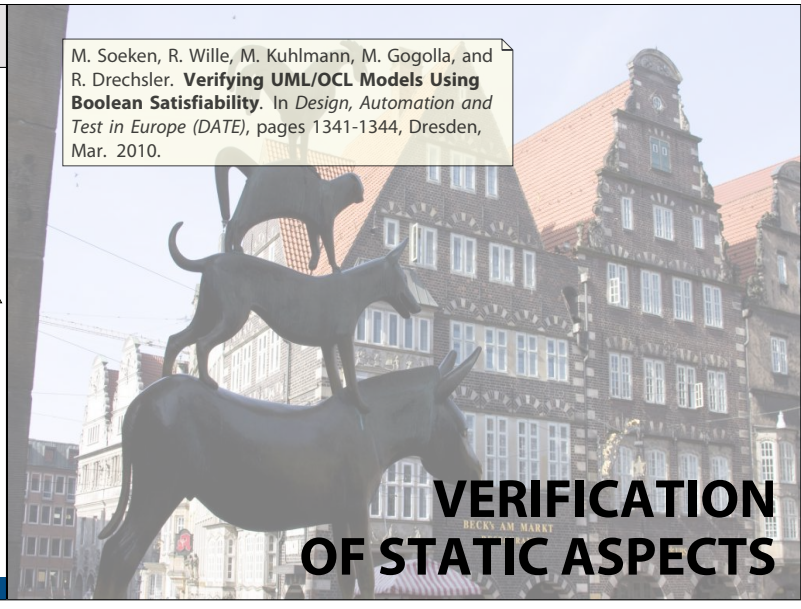
UML Sequence Diagram
- Objects



UML Sequence Diagram
- Objects
- Operation Calls

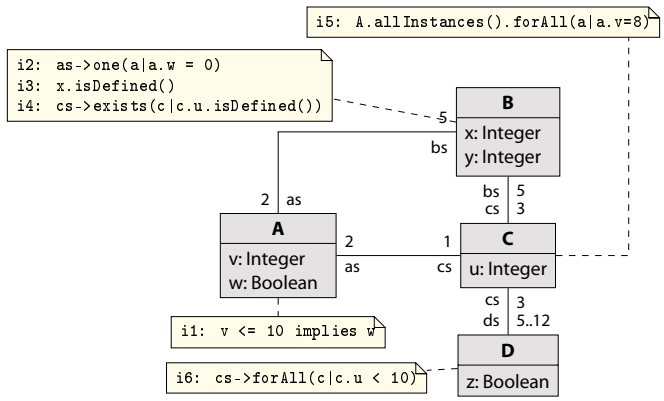


M. Soeken, R. Wille, M. Kuhlmann, M. Gogolla, and R. Drechsler. **Verifying UML/OCL Models Using Boolean Satisfiability**. In *Design, Automation and Test in Europe (DATE)*, pages 1341-1344, Dresden, Mar. 2010.



VERIFICATION OF STATIC ASPECTS

What is Inconsistency?



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What is Inconsistency?

x_C objects of **C**

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$2x_C$ objects of **A**

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x_C objects of **C**
$2x_C$ objects of **A**
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What is Inconsistency?

x_C objects of **C**
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Model is UML-inconsistent

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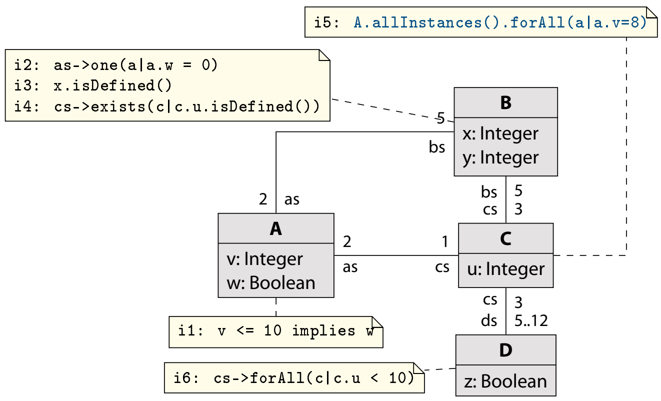
What is Inconsistency?



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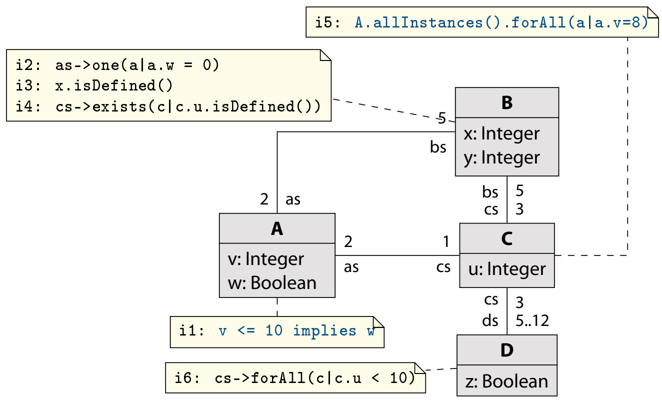

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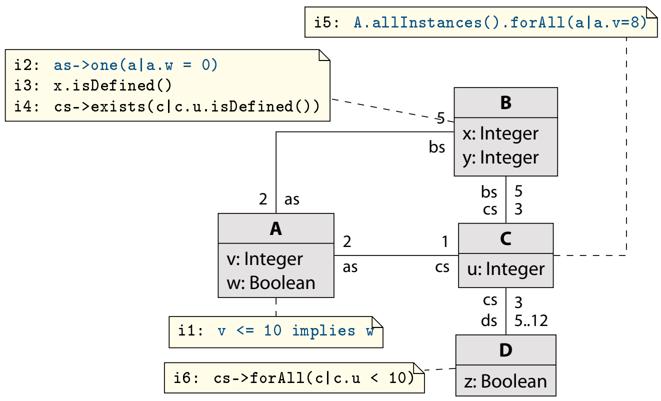
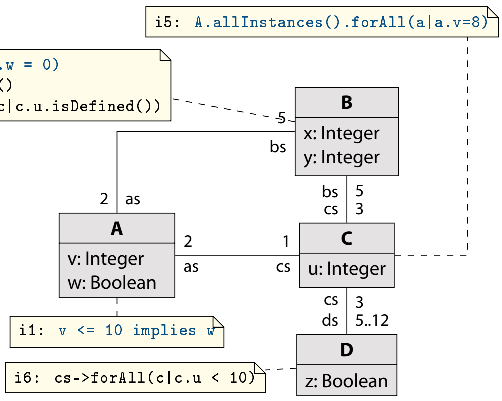
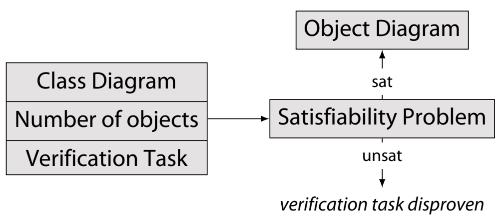


What is Inconsistency?

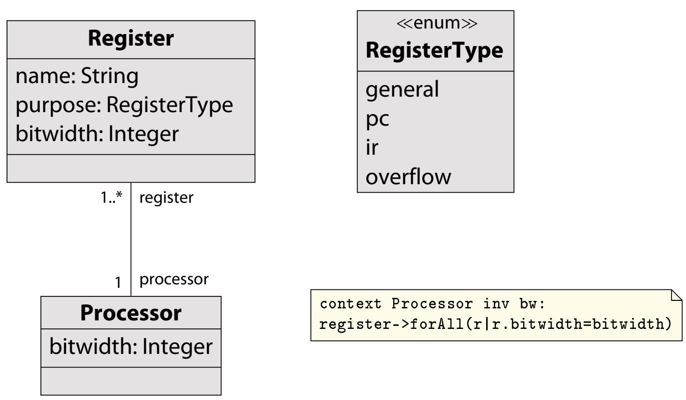
Model is OCL-inconsistent



Solving Flow

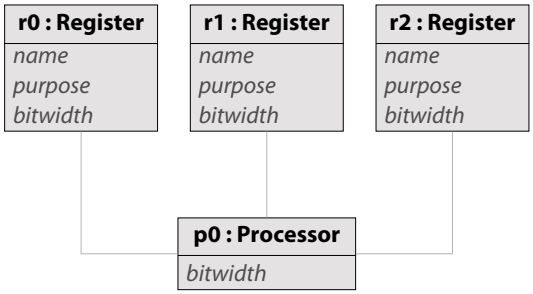


Running Example



Running Example

Is there a valid system state consisting of one processor and three registers?



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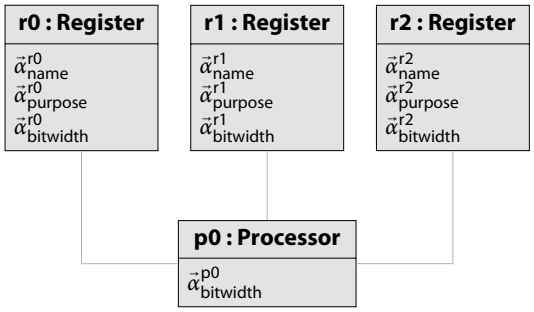

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Encoding Attributes

How many bits are needed for the bit-vectors?

$\lceil \mathrm{ld}(n+1) \rceil$ bits are needed. The additional value is for representing undefined attributes. Determination of n by type of attribute:

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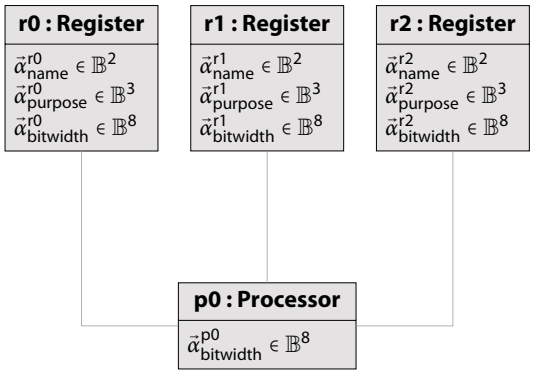

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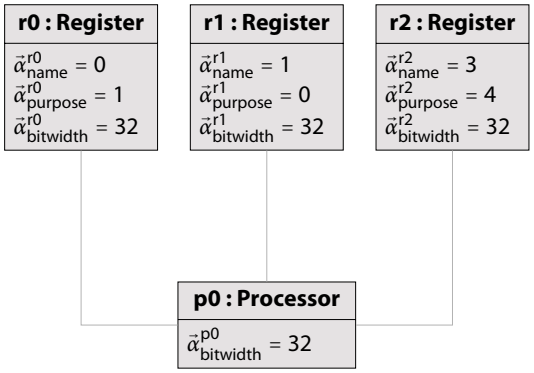

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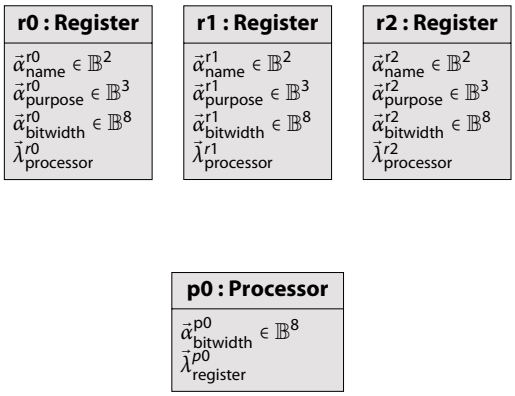

Encoding Links

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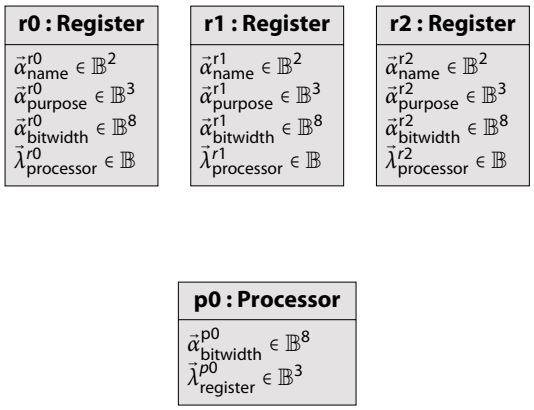

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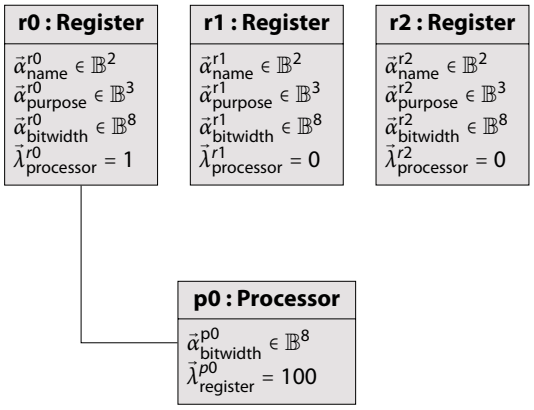

Encoding Invariants

```
context Processor inv bw:
register->forAll(r|r.bitwidth=bitwidth)
```

$$\bigwedge_{i=0}^{|\text{oid(Register)}|-1} \left[\vec{\lambda}^{p0}_{register}[i] \Rightarrow \left(\vec{\alpha}^{ri}_{bitwidth} = \vec{\alpha}^{p0}_{bitwidth}\right)\right]$$

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- Let $\mathcal{I} = \{i_1, \ldots, i_n\}$ be a set of invariants
- Let σ denote a system state, i.e. a concrete assignment of attributes and links

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$$\exists \sigma : \bigwedge_{i \in \mathcal{I}} \sigma(i)$$

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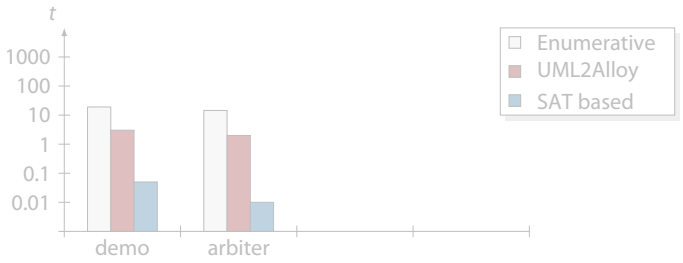
Experimental Results

- Consistency check for consistent models
- Enumerative approach is USE
- UML2Alloy converts UML models to an Alloy model which is solved by a SAT solver



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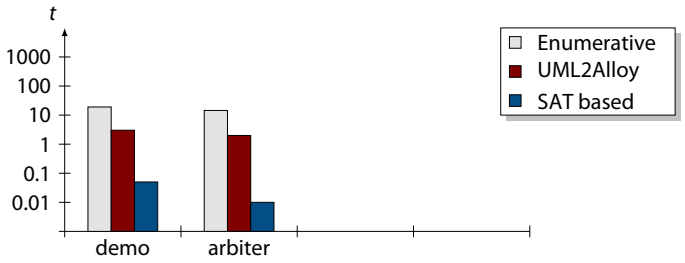

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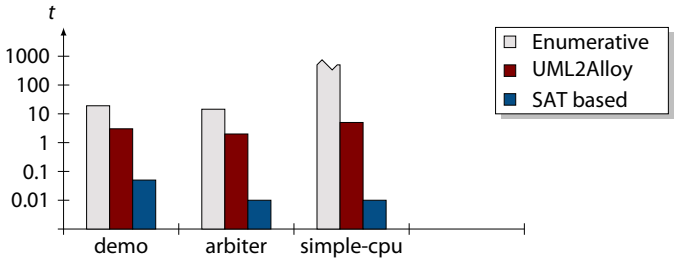

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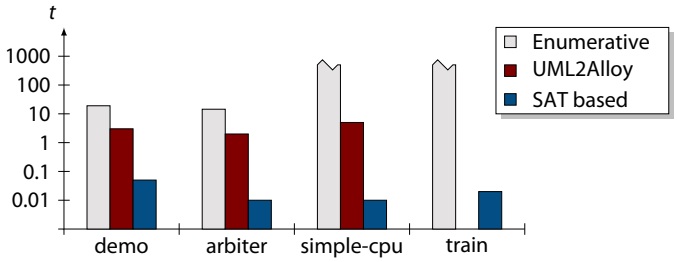

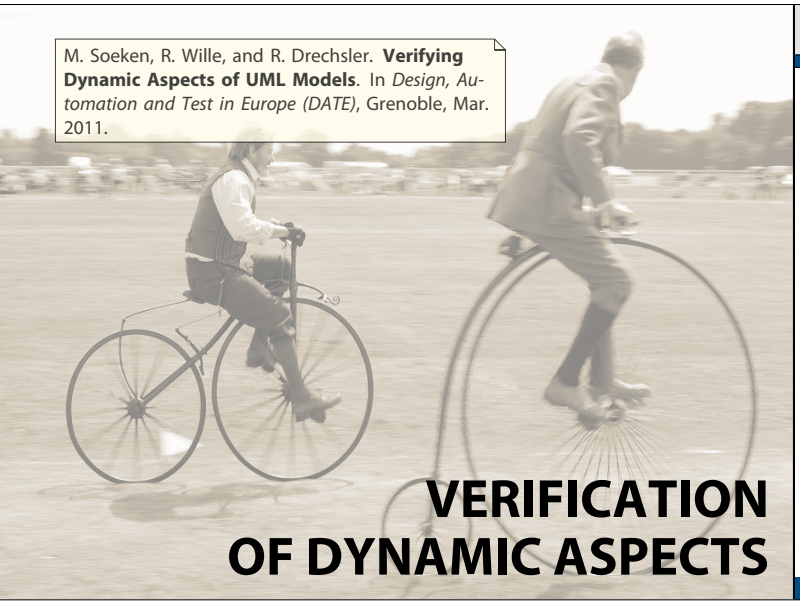

M. Soeken, R. Wille, and R. Drechsler. **Verifying Dynamic Aspects of UML Models**. In *Design, Automation and Test in Europe (DATE)*, Grenoble, Mar. 2011.

VERIFICATION OF DYNAMIC ASPECTS

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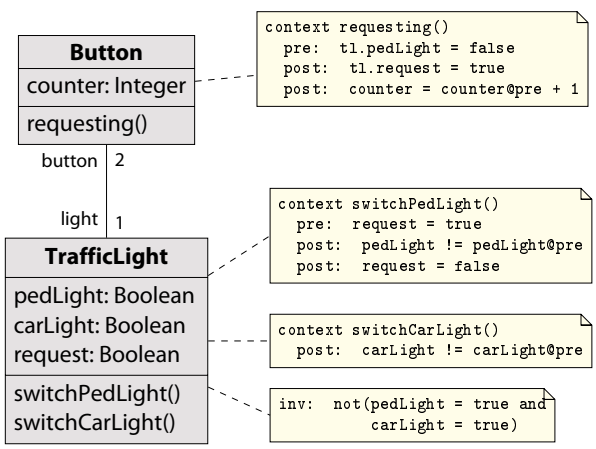
Running Example



Running Example

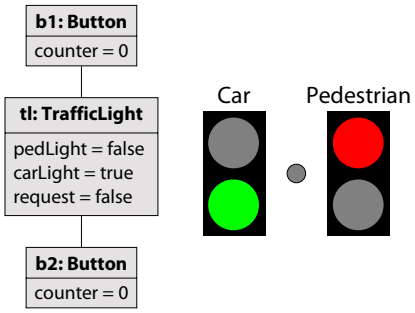
Time: 0

```
context Button::requesting()
pre:  tl.pedLight = false
post:  tl.request = true
post:  counter = counter@pre + 1

context TrafficLight::switchPedLight()
pre:  request = true
post:  pedLight != pedLight@pre
post:  request = false

context TrafficLight::switchCarLight()
post:  carLight != carLight@pre

context TrafficLight
inv:  not(pedLight = true and carLight = true)
```



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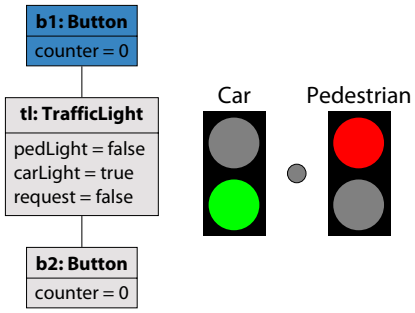

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Running Example

Time: 1

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pre: tl.pedLight = false
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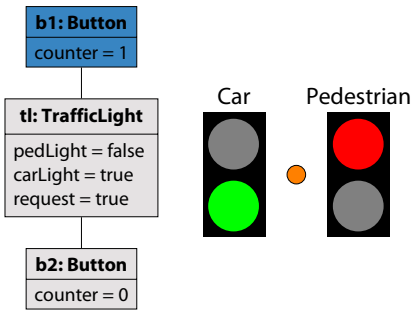

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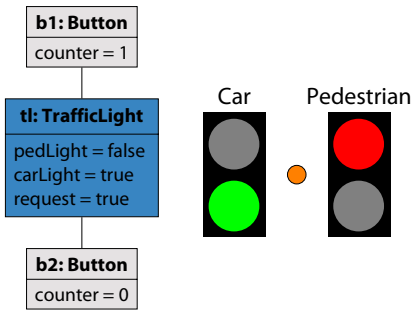

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Running Example

Time: 2

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context Button::requesting()
pre:  tl.pedLight = false
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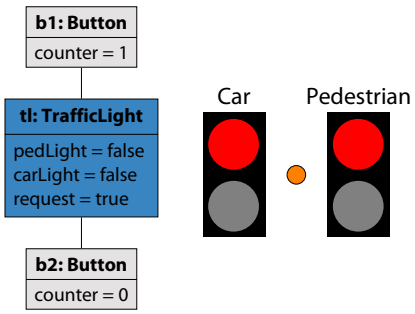

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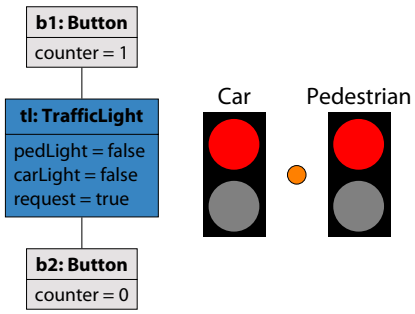

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Running Example

Time: 3

```
context Button::requesting()
pre:  tl.pedLight = false
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post:  counter = counter@pre + 1

context TrafficLight::switchPedLight()
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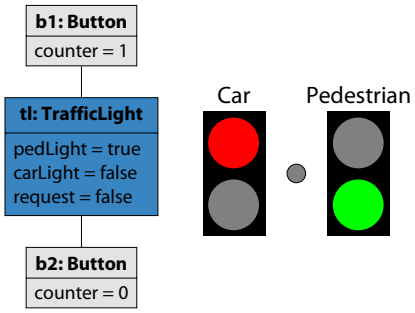

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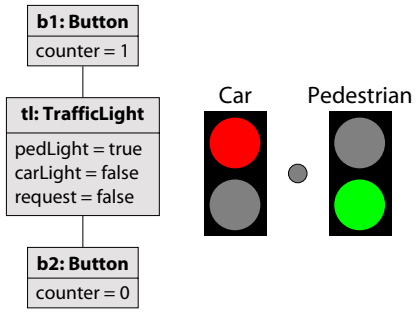

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Encoding

- Introduce time model, i.e. we consider k steps (operation calls)
- This leads to $k + 1$ system states $\sigma_0, \ldots, \sigma_k$

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$$f = \bigwedge_{t=0}^{k} \sigma_t(\mathcal{I}) \wedge \bigwedge_{t=0}^{k-1} \left(\sigma_t(\triangleleft_{op_t}) \wedge \sigma_{t+1}(\triangleright_{op_t})\right) \wedge \tau$$

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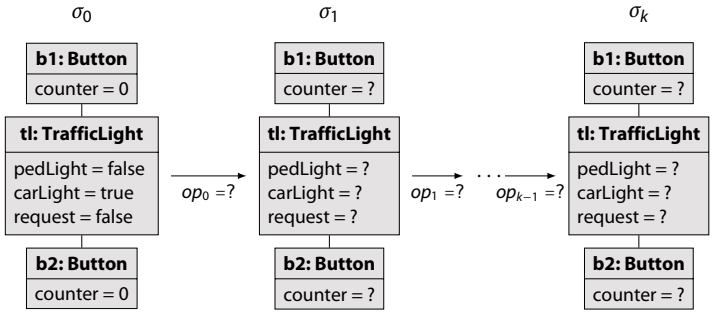
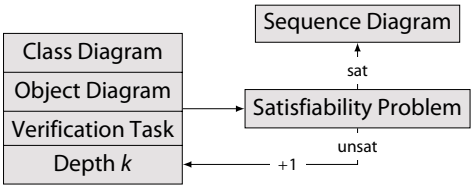
Encoding

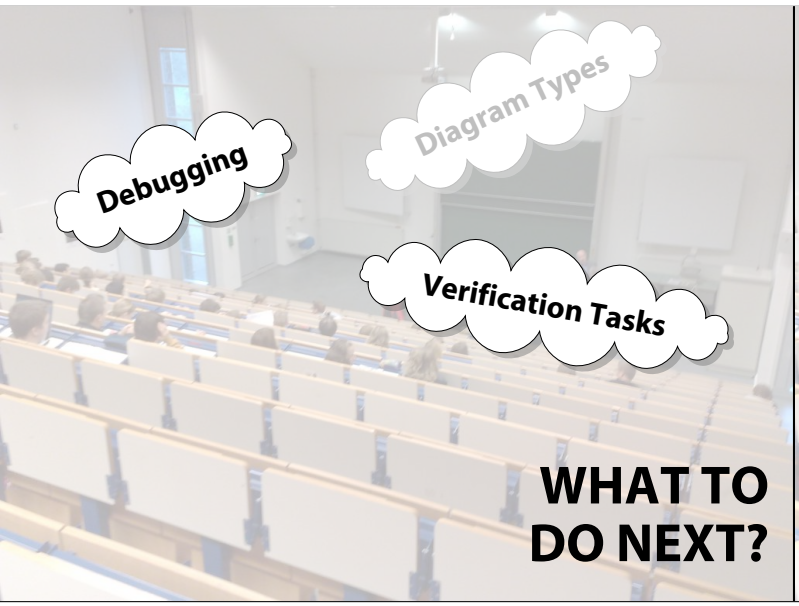


Solving Flow



Experimental Results

Name	Task	#Obj	Depth	Status	Run-time
switch	Reachability	25	23	sat	49.70
switch	Reachability	25	22	unsat	50.00
switch	Reachability	25	50	sat	621.70
switch	Reachability	9	103	sat	147.50
switch	Reachability	9	102	unsat	90.40
simple-cpu2	State Gen.	13	100	sat	1.30
simple-cpu2	State Gen.	13	100	unsat	0.40
traffic-control	Reachability	6	5	sat	0.00
traffic-control	Reachability	24	10	sat	1.60
traffic-control	State Gen.	9	30	unsat	0.10
traffic-control	State Gen.	9	100	unsat	0.40



References

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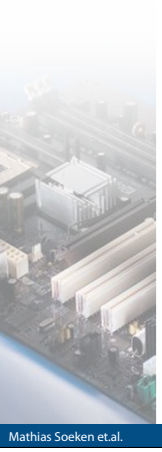
- M. Soeken, R. Wille, and R. Drechsler. **Verifying Dynamic Aspects of UML Models**. In *Design, Automation and Test in Europe (DATE)*, Grenoble, Mar. 2011. PDF



Formal Verification of UML-based Specifications

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January 31, 2011