STUDY OF ION-IMPLANTATIONS INTO $Al_xGa_{1-x}As$ AND ITS APPLICATIONS TO HETEROJUNCTION BIPOLAR TRANSISTORS

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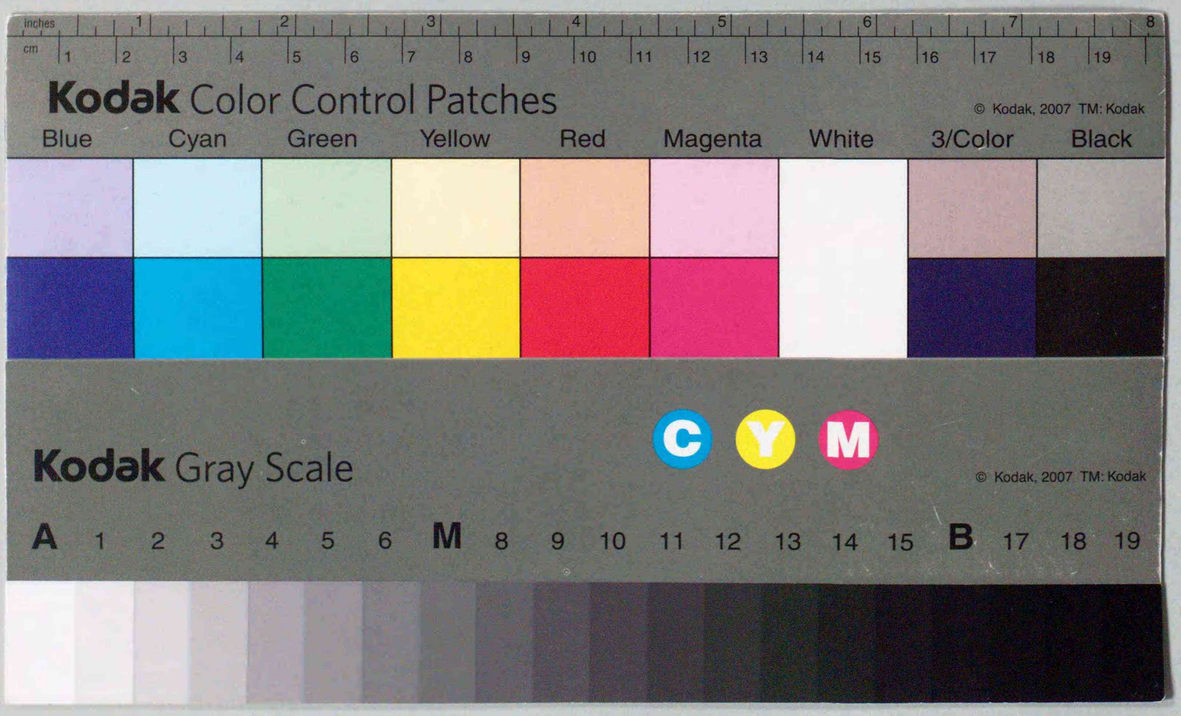

STUDY OF ION-IMPLANTATIONS INTO $Al_xGa_{1-x}As$ AND ITS APPLICATIONS TO HETEROJUNCTION BIPOLAR TRANSISTORS

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CONTENTS

Chapter 1

Introduction

1-1. Background of ion implantation

In the manufacture of Si semiconductors, ion implantation has become the most important doping technique for integrated circuits because it offers good control over impurity incorporation, reproducible results, selective area doping, and the ability to tailor the dopant concentration profile to requirements [1]. In the ion-implantation process, ionized atoms are accelerated in an electrostatic field and implanted into a solid substrate. The doping atoms introduced by ion implantation have a Gaussian range distribution around an average projected range R_P, with a standard deviation ΔR_P. The range distribution of implanted ions was first theoretically investigated by Lindhard, Scharff and Schiott (LSS) [2, 3]. The range distribution N(x) is

$$N(x) = \frac{N_S}{\sqrt{(2\pi)\triangle R_P}} \exp\left[-\frac{(x-R_P)^2}{2\triangle R_P{}^2}\right] . \quad (1\text{-}1)$$

where N_S is the implanted dose.

Ion implantation is an established step in the fabrication of many Si devices. Also, implantation is now being used in the fabrication of devices for III-V compound semiconductors such as GaAs. However, with compound semiconductors there are several obstacles to taking advantage of the doping control made possible by ion implantation that do not arise with Si. When the implanted ion dose, and thus the concentration of radiation damage, is sufficiently high, the damage clusters overlap and an amorphous region is formed. In Si, this amorphous region changes to good-quality crystal by epitaxial regrowth even after annealing at relatively low temperatures. On the other hand, in the case of GaAs, re-grown crystals of adequately good quality cannot be obtained after annealing at high temperatures because residual lattice defects cannot be canceled.

The application of ion implantation to III-V compound semiconductors can be divided into two categories: "doping" and "isolation". For example, II-group impurity atoms become acceptors by substitution for III-group lattice sites, and VI-group impurity atoms become donors by

substitution for V-group ones. Doping to layers by ion implantation has been used to fabricate active layers, such as metal semiconductor field-effect transistors (MES-FETs) fabricated by Si-ion implantation [4-6], or to form ohmic contacts, such as extrinsic p-type base layers of heterojunction bipolar transistors (HBTs) fabricated by Be-ion implantation [7]. On the other hand, ion bombardment by implantation which creates highly resistive layers, has been used to electrically isolate devices: for example, the isolation of AlGaAs/GaAs HBTs by proton or oxygen-ion (O-ion) implantation [8-10]. This electrical isolation technique is applied only to III-V compound semiconductors with wide bandgaps.

For p-type doping in GaAs, thermal diffusion with Zn in an ampoule under high arsenic pressure was used. The first implantation experiments for p-type doping were made with Zn and Cd [11-15]. Next, Be and Mg were studied as p-type doping elements [16, 17]. In particular, the formation of p-type layers in GaAs by Be-ion implantation has received considerable attention because Be is the lightest p-type dopant for GaAs [18, 19]. Consequently, the lattice disorder produced by Be-ion implantation is not very severe and can be annealed at relatively low temperatures. The electrical activation of Be implanted in GaAs is obtained with annealing temperatures as low as 500°C [18, 19]. However, annealing at 900°C is necessary to recover the crystallinity of the implanted GaAs [20, 21], resulting in the loss of Be atoms by out-diffusion at the surface and a broadening of the Be atomic distribution [22]. One solution to this problem is the use of rapid thermal annealing (RTA) methods (for example tungsten halogen lamps positioned above and underneath the wafer chamber) that have an annealing time to the order of seconds [23, 24].

As already mentioned, another application of ion implantation in III-V compound semiconductors is the production of highly resistive (isolated) layers in GaAs by radiation damage inactive-ions. Proton implantation produces radiation damage, which has a compensating effect [25, 26], however, this effect is canceled as a result of high-temperature annealing. On the other hand, O-ion implantation causes a chemical doping related deep-level, and high-temperature annealing is necessary to obtain the desired effect [27]. Thus, highly resistive layers made by O-ion implantation are thermally stable compared with those made by proton implantation.

1-2. Background of AlGaAs/GaAs heterostructure

Much interest has been focused on III-V compound semiconductor heterostructures such as AlGaAs/GaAs, InP/InGaAs, and InAlAs/InGaAs, since they have many possible applications in various types of high-speed electronic and optoelectronic devices. In particular, various investigations of the AlGaAs/GaAs heterostructure have recently advanced [28]. The AlGaAs/GaAs material system has a good lattice constant matching over all Al-As compositions. The bandgap energy E_g of the $Al_xGa_{1-x}As$ as a function of x is given by $E_g = 1.424 + 1.247x$ (eV) for $x < 0.45$ and by $E_g = 1.424 + 1.247x + 1.147(x-0.45)^2$ (eV) for higher x values. Below the critical composition $x = 0.45$, the bandgap is direct. The majority of the bandgap difference (approximately 62%) corresponds to a difference in conduction-band energy with the remainder (38%) corresponding to the valence-band energy difference. As a result, abrupt heterojunctions have significant conduction-band energy barriers.

A lot of research has made progress on the development of high-speed-device and devised circuit technologies for over-10 Gbit/s lightwave communication circuits, particularly on the decision ICs and baseband amplifiers that use Si bipolar transistors and GaAs MES-FETs. Heterostructure devices, in particular, HBTs have become candidates for higher bit-rate optical communication system. The reasons are as follows [29]: (i) Electrons travel from the emitter to the collector, perpendicular to the wafer surface. The dimensions that control transit time are established by each epitaxial grown layer thickness. (ii) It is possible to provide a high output current per unit chip area, and maintain high current density. (iii) The input voltage directly controls the density of the carriers that provide the output current, I_C, leading to output current variation of the form exp(qV/kT). The bipolar transistor's transconductance $g_m = qI_C/kT$ is the highest obtainable in any three-terminal devices. (iv) The turn-on voltage of bipolar transistors, V_{BE}, is relatively independent of device dimensions, since it corresponds to the built-in potential of a p-n junction. (v) It is possible to ensure adequate current gain with very high levels of base doping, and very low levels of emitter doping because of the large difference in bandgap between emitter and base. This leads to very low base resistance.

HBTs have a vertical epitaxial layer structure in the intrinsic transistor region, different from

Si bipolar transistors in which an emitter, a base, and a collector are laterally arranged. There are therefore various possible device structures, epitaxial layer structures, and fabrication processes for HBTs. Conventionally, AlGaAs/GaAs HBTs have an emitter-up/collector-down configuration. This is the reason that an emitter-up HBT can be fabricated only by mesa etching of emitter/base and base/collector junctions and by formation of each electrode.

HBTs can have another vertical configuration, that is, an "inverted" HBT with an emitter-down/collector-up configuration. This inverted configuration transistor rather than a conventional emitter-up HBT is especially promising as a high-speed transistor [30]. The principal advantage of the collector-up (C-up) HBT is that it permits the use of a significantly smaller collector area, leading to lower base/collector capacitance. This reduced base/collector capacitance can result in both higher operating speed of circuits and power gain. Although a C-up HBT has several advantages, extra processing steps in the fabrication of this transistor are needed to suppress the excess base leakage current that can be injected from the emitter contact layer into the extrinsic base regions. Therefore, we must make an effective "barrier" region at the extrinsic emitter/base to suppress injection currents. The advantages of the collector-up configuration have not yet been fully demonstrated and few papers have reported on high-performance transistors. This is because it is difficult to make a barrier that will completely suppress injection currents at the extrinsic emitter/base of the C-up configuration.

1-3. Objective

The objective of the present study is to produce a novel C-up AlGaAs/GaAs HBT with excellent high-frequency characteristics. For this purpose, new ideas on how to create an effective barrier region at the extrinsic GaAs/$Al_xGa_{1-x}As$ base/emitter by the refined ion implantation technique are presented. Ion implantation is the most suitable method for making a barrier region at the extrinsic emitter/base because it allows selective area doping and can tailor the doping concentration profile to requirements. One of the new attempts to create an effective barrier region selects Be-ion implantation to convert an n-type $Al_xGa_{1-x}As$ layer into a p-type one. The key steps to the creation of such a barrier are the formation of a high-quality p-n junction in the $Al_xGa_{1-x}As$ epitaxial layer and the control of the position of the p-n junction region. A high-quality p-n junction means that few

recombination components appear in the junction. The point of creating an effective barrier to suppress a troublesome injection current at the extrinsic regions is to establish whether the quality of a p-n junction is good or not. As mentioned before, there have been many papers about the properties of Be-ion-implanted GaAs, whereas there have only been a few reports on the subject of $Al_xGa_{1-x}As$ layers or $Al_xGa_{1-x}As$/GaAs heterostructures [31-35]. For this reason, detailed investigations of Be-ion-implanted $Al_xGa_{1-x}As$ layers or AlGaAs/GaAs heterostructures relative to those of Be-ion-implanted GaAs are needed that express the electrical properties as functions of the annealing temperature and Al-As composition x. In this study, the Al-As composition x is limited to between 0 and 0.3 because these x values give large conduction-band discontinuity and valence-band discontinuity between $Al_xGa_{1-x}As$ emitter and GaAs base layers to obtain a high electron injection efficiency at the emitter/base, leading to a high current gain in C-up HBTs. The objective of this study is to achieve a novel C-up configuration of HBTs, and to find a high-quality p-n junction in the $Al_xGa_{1-x}As$ layer several properties of Be-ion-implanted $Al_xGa_{1-x}As$ layers or AlGaAs/GaAs heterostructures are investigated. The motivation of this study is to improve high-frequency performance for an HBT by using a C-up configuration.

Another new attempt to create an effective barrier region in the extrinsic emitter/base regions of C-up HBTs is the formation of highly resistive (isolated) regions in the $Al_xGa_{1-x}As$ layer. Contrary to the formation of p-n junctions using a p-type dopant, ion implantations of inactive dopants are needed to form these highly resistive regions. Isolations in GaAs by inactive dopant ion implantation have been studied, but only a few papers have described the formation of a highly resistive region in $Al_xGa_{1-x}As$ or $Al_xGa_{1-x}As$/GaAs heterostructures [36, 37]. In this study, O-ion implantation is selected to create highly resistive regions as an effective barrier at the extrinsic $Al_xGa_{1-x}As$ emitter and to achieve a novel high-performance C-up HBT. The aim of using O-ion implantation is to produce a novel HBT device.

This thesis deals with two new approaches to ion implantation for achieving C-up HBTs with excellent high-frequency that can take advantage of the C-up configuration. In the first half, the main subject is the electrical properties of Be-ion-implanted $Al_xGa_{1-x}As$ or AlGaAs/GaAs heterostructures. The second half describes the properties of O-ion-implanted AlGaAs/GaAs heterostructures and the performance of C-up AlGaAs/GaAs HBTs fabricated using O-ion implantation .

1-4. Outline for the thesis

As stated above, the motivation of this study is to improve the high-frequency performance of HBTs by use of a C-up configuration. The achievement of the C-up HBT with excellent high-frequency characteristics is very important for the operation of high-frequency circuits and high bit-rate optical communication systems, such as over-40 Gbit/s. Although all chapters in this thesis include new and attractive subjects on ion-implantations or discrete device performance, the goal of this study is the fabrication of an excellent device.

In Chapter 2, basic studies in conjunction with Be-ion (Be^+) implantation into $Al_xGa_{1-x}As$ layers through SiO_2 encapsulant are described. Electrical and optical properties of the Be^+-implanted $Al_xGa_{1-x}As$ layers activated by rapid thermal annealing (RTA) are investigated as functions of the Al composition x and annealing temperatures by means of the Hall-effect, photoluminescence, and secondary ion mass spectrometry (SIMS) measurements. For the first time, the activation behavior of Be implants in the $Al_xGa_{1-x}As$ layer is shown as a function of annealing temperature. The activation fractions in the $Al_xGa_{1-x}As$ layer increase gradually with increase in annealing temperature, but these values are apparently lower than those in the GaAs. Moreover, the $Al_xGa_{1-x}As$ with larger x gives smaller activation fraction at any fixed temperature. PL intensities in the Be^+-implanted GaAs and $Al_xGa_{1-x}As$ indicate that damage recovery starts from 400°C and increases gradually with further increases in annealing temperature showing a peak at 900°C. Thus, a considerable amount of radiation damage, which causes deterioration in PL intensity, may still be present at annealing temperatures lower than 900°C.

Atomic Be depth profiles in the $Al_xGa_{1-x}As$ layers are shown before and after RTA for the first time. Be depth profiles before RTA resemble a theoretical Gaussian distribution predicted from the LSS calculations. A slight change in the Be distribution can be found in the GaAs after RTA. On the other hand, RTA causes significant Be in-diffusion in the $Al_xGa_{1-x}As$ layers, resulting in plateau-like depth profiles. Another pronounced annealing effect revealed by the SIMS analysis is the accumulation of Be at the $Al_xGa_{1-x}As/SiO_2$ encapsulant interfaces. This effect is that a large fraction of Be is piled up at the interface by out-diffusion during high-temperature RTA, and can be observed

in both GaAs and $Al_xGa_{1-x}As$ layers. However, the amount of Be atom accumulation at the $Al_{0.3}Ga_{0.7}As$ surface is larger than that of GaAs.

The lower activation fraction of Be implants in the $Al_{0.3}Ga_{0.7}As$ is found to be mainly due to loss of Be atoms from the semiconductor surface, resulting from out-diffusion and accumulation of Be at the $Al_xGa_{1-x}As/SiO_2$ encapsulant interfaces after the high temperature annealing. In ion-implanted regions, the radiation damage clusters overlap and an amorphous region is formed. When this amorphous region changes to a high quality crystal by regrowth during annealing, Be atoms are substituted for III-group sites and become "acceptor". However, in the implanted $Al_xGa_{1-x}As$, the annealing at higher temperature is needed to recover Al-As and Ga-As bonds than to recover Ga-As bond in the implanted GaAs. At low temperature annealing, Be cannot be substituted for III-group sites and because of poor crystal quality it is located at the interstitial position between sites. If high-temperature annealing is applied, a large part of the Be atoms located at the interstitial position diffuse to the semiconductor surface and accumulate at the interface without substitution of III-group sites. Since Hall-measurements are carried out after the removal of the SiO_2 encapsulant, the accumulated Be never contributes to electrical activity.

The Be redistribution and the lower activity of Be implants in the $Al_{0.3}Ga_{0.7}As$ after high-temperature RTA lead to significant problems in making high-quality p-n junctions in the $Al_{0.3}Ga_{0.7}As$ layer. Chapter 3 describes experimenting with dual implantations (co-implantations) of Be-ion plus P-ion (Be^+/P^+) and Be-ion plus As-ion (Be^+/As^+) into $Al_{0.3}Ga_{0.7}As$ layers as means to overcome these problems, and the electrical properties of the implanted layers are investigated using Hall-effect measurements. The improved electrical activity of the dual implants is observed and compared with that of the single implant. The apparent hole concentration of the Be^+/P^+ dual implants is nearly twice that of the Be^+ single implant at annealing temperatures above 650°C. The dual implantations also greatly suppresses redistribution of Be atoms, and so Gaussian-type profiles remain even after high-temperature annealing (950°C). These experimental results are explained as the stoichiometric-balance preservation. Added P or As atoms reduce the As vacant concentration in the $Al_{0.3}Ga_{0.7}As$, and at the same time increase the vacant concentration of III-group site. As a result, it is easy for Be atoms located at the interstitial position to substitute for III-group sites. The remarkable effect of dual implantations of Be^+/P^+ and Be^+/As^+ in the $Al_{0.3}Ga_{0.7}As$ layers is

demonstrated for the first time in this study.

Chapter 4 considers the next stage of a C-up HBT fabrication. One of the new methods to create an effective barrier region which suppresses excess injection current is the formation of p-n junctions in the extrinsic emitter/base. The p-n junctions are formed by Be^+-implantation. The Be^+-implantations convert an n-type $Al_xGa_{1-x}As$ layer into a p-type one. The key steps to creation of the barrier are to establish whether the quality of a p-n junction is good or not and to control the position of the p-n junction region. A high-quality p-n junction means that few recombination components appear in the junction. For this purpose, Be^+-implantation into n-type (Si-doped) $Al_xGa_{1-x}As$ ($x = 0$ and 0.3) and the subsequent RTA are carried out to characterize p-n junction quality. The p-n junction characteristics are investigated by means of I-V and C-V measurements. The forward I-V characteristics reveal that, for both the Be^+-implanted GaAs and the $Al_{0.3}Ga_{0.7}As$ diodes, the ideality factors are about $n = 1.8$ over a relatively wide current range. This n-value is obtained at annealing temperatures ranging from 600 - 850°C for the GaAs diodes and at 650 - 950°C for the $Al_{0.3}Ga_{0.7}As$ diodes. The n-value dependence on the annealing temperature of Be^+-implanted $Al_xGa_{1-x}As$ diodes is presented for the first time.

The shape of p-n junctions fabricated by Be^+-implantation ("abrupt" and "graded") are clear from C-V measurements. The C-V profiles of the Be^+-implanted GaAs diodes annealed at various temperatures indicate that the effective carrier concentration increased with increasing annealing temperatures. The C-V data also show that the Be^+-implanted GaAs diodes have graded junctions, independent of annealing temperatures. The implanted $Al_{0.3}Ga_{0.7}As$ junctions, on the other hand, have C-V characteristics which are strongly dependent on annealing temperature. These experimental data are connected to activation behaviors of Be implants in the n-type $Al_xGa_{1-x}As$ layers.

Although a lot of researches are performed in conjunction with Be^+-implantation into the $Al_xGa_{1-x}As$ layers or AlGaAs/GaAs heterostructures, the C-up AlGaAs/GaAs HBT using the Be^+-implantation results in insufficient device performance, especially for small transistors. This is mainly due to the out-diffusion of a base dopant (Be) toward the $Al_xGa_{1-x}As$ emitter and the redistribution of Be implants in the $Al_{0.3}Ga_{0.7}As$ layer after the high temperature RTA in spite of using the dual implantation technique. In addition, $Al_xGa_{1-x}As$ p-n junction quality adequate enough to suppress injection currents from the emitter contact region into the extrinsic base region at the

higher collector current densities of over around $2x10^4$ A/cm^2 cannot be obtained. Later chapters, therefore, focus on another new attempt to create an effective barrier region in the extrinsic regions of a C-up HBT, that is, the formation of highly-resistive (isolated) regions in the $Al_xGa_{1-x}As$ layer. Chapter 5 describes O-ion (O^+) implantation into $Al_xGa_{1-x}As$ layers and its application to a C-up configuration of AlGaAs/GaAs HBTs.

The electrical properties of O^+-implanted AlGaAs/GaAs heterostructures are examined. In particular, AlGaAs/GaAs diode characteristics, with correspond to the extrinsic emitter/base of the C-up HBT, are investigated as possible parameters of annealing temperatures and O^+ doses. It is clarified that only high-dose O^+ implants can create a thermally stable highly-resistive layer, which is a result of chemical-effect compensation due to the O-related deep levels in the $Al_xGa_{1-x}As$.

C-up HBTs are fabricated by combination of O^+-implantation and Zn-diffusion. As a result, owing to this novel combination, C-up HBTs can overcome difficulties in fabrication. Their DC and high-frequency characteristics are investigated as a function of the O^+ dose. It is obvious that the high-resistive barrier layer created by O^+-implantation in the extrinsic $Al_{0.3}Ga_{0.7}As$ for the C-up HBT can effectively suppress carrier injection from the emitter electrode into the extrinsic base region. This thermally stable high-resistive barrier layer provides good current gain in the C-up HBT even at high collector current densities.

Chapter 6 describes the excellent characteristics of the first small scale C-up AlGaAs/GaAs HBT with a C-doped GaAs uniform base fabricated using O^+-implantation in combination with Zn-diffusion. The high-resistive O^+-implanted AlGaAs layers provide excellent injection current blocking and current gain. For a transistor with a 2-μm x 10-μm collector, a current gain of 20 is obtained. The C-up HBT shows dependence of current gain on collector size due to a base recombination current around the collector-mesa perimeter. In a small scale transistor with a 2-μm x 2-μm collector a current gain of 15 is attained. The current gain dependence on collector size is also investigated for a C-up HBT with an $Al_xGa_{1-x}As$ graded base, and the base recombination current around the collector-mesa perimeter is shown to decrease in the case of an $Al_xGa_{1-x}As$ graded base.

A microwave transistor with a 2-μm x 10-μm collector achieves excellent high-frequency characteristics with an f_T of 68 GHz and a f_{max} of 102 GHz. A small scale C-up HBT with a 2-μm x 2-μm collector shows a higher f_{max} of 110 GHz, owing to the further reduction of C_{BC}. These high-

frequency values, in particular f_{max}s, are superior to typical values (approximately 70 GHz) of conventional emitter-up HBTs.

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Chapter 2

Be-ion implantation in $Al_xGa_{1-x}As$

2-1. Introduction

Ion-implantation plays an essential role in semiconductor device technology, so it is widely employed in the fabrication of many devices. Much interest has recently focused on $Al_xGa_{1-x}As$/GaAs heterostructure systems, because they may have great application to many types of high-speed electronic devices. Many experiments on the ion-implanted GaAs have been carried out, and as a result, a better understanding has been obtained in relation to implantation doping technology [1]. On the other hand, there have been only a few reports on the subject of $Al_xGa_{1-x}As$ or $Al_xGa_{1-x}As$/GaAs heterostructures [2-7].

An n-type layer formation in an $Al_xGa_{1-x}As$/GaAs heterostructure by using Si-ion implantation and subsequent conventional furnace annealing (CFA) has been reported by Nishi et al. [2]. Differences in the electrical activation behavior are found between the GaAs and $Al_xGa_{1-x}As$. In particular, the activation of the Si implants takes place after annealing at temperatures as low as 625°C in the GaAs, while the $Al_xGa_{1-x}As$ temperatures higher than 700°C are needed. Some data are also available on the CFA behavior of p-type implants, Be and Mg, in the $Al_xGa_{1-x}As$ [3-6]. These data show that the implants in the $Al_xGa_{1-x}As$ are activated by higher annealing temperature than those in GaAs. Comas and Bedair [7] have also reported on the p-n junction characteristics in the $Al_{0.3}Ga_{0.7}As$ fabricated by Be^+-implantation and the subsequent CFA .

A number of recent reports have demonstrated the effectiveness of rapid thermal annealing (RTA) in achieving electrically high activity with minimal redistributions of the implanted species in GaAs [8-11]. Furthermore, selected examples of practical RTA applications can be found in semiconductor devices, such as $Al_xGa_{1-x}As$/GaAs HBTs [12, 13]. In these devices, the extrinsic emitter/base regions are defined by Be^+- and O^+-implantations. These implantations and the subsequent RTA lead to a reduction in the parasitic current and capacitance in the extrinsic emitter/base region. Despite the importance demonstrated by these device applications, however, no detailed RTA study of the implants in the $Al_xGa_{1-x}As$ has been carried out up to date.

In this chapter, the electrical and optical activation characteristics of Be implants in the $Al_xGa_{1-x}As$ following RTA are described using Hall-effect and photoluminescence (PL) measurements. Of particular interest is the activation fraction dependence of Be implants in the $Al_xGa_{1-x}As$ on the annealing temperature and the Al composition x. The annealing temperatures range between 400 and 1000°C and the Al composition x ranges from 0 to 0.3. The profiles of Be atomic and hole concentrations are also determined by secondary ion mass spectrometry (SIMS) and differential Hall-effect measurements, respectively.

2-2. Experimental

A series of undoped $Al_xGa_{1-x}As$ (x=0, 0.05, 0.1, 0.2, 0.3) epitaxial layers are grown on semi-insulating Cr-doped (100) GaAs substrates by molecular-beam epitaxy (MBE). The thickness of the MBE grown layers is typically 1.5 μm. Prior to ion implantation, the samples are encapsulated with SiO_2 (about 0.25 μm thick) deposited by plasma-CVD. The implantation is carried out through the SiO_2 encapsulant with a dose of $2x10^{14}$ cm^{-2} at an energy of 100 keV at room temperature in random axis orientation to avoid ion channeling.

The implanted samples are annealed in a HEATPULSE 210T halogen lamp annealer with flowing N_2 gas. An isochronal anneal of 4 s duration is performed. The annealing temperatures are monitored by a chromel-alumel thermocouple attached to a Si wafer on which the sample is placed. At the same time, for comparison CFAs are also performed at various temperatures for 10 min in flowing N_2 gas.

The sheet concentration and Hall mobility of holes are measured at room temperature by the conventional van der Pauw technique. The ohmic contacts are formed by sintering In/Zn on the samples with a hot plate at 200°C. Electrically active carrier profiles are obtained by performing differential Hall-effect measurements in conjunction with chemical etching using $H_2SO_4 : H_2O_2 : H_2O$ solution for successive layer removal. Using the values obtained by Hall-effect measurements before and after etching of the i-th layer, the mean values (n_{eff}, μ_{eff}) for the doping as well as the mobility of this layer are obtained by the following equations:

$$\mu_{eff,\,i} = \frac{R_{H,\,s,\,i}\,\sigma^2_{s,\,i} - R_{H,\,s,\,i+1}\,\sigma^2_{s,\,i+1}}{\sigma_{s,\,i} - \sigma_{s,\,i+1}} \quad . \qquad (2\text{-}1)$$

$$n_{eff,\,i} = \frac{\sigma_{s,\,i} - \sigma_{s,\,i+1}}{q\,(x_{i+1} - x_i)\,\mu_{eff,\,i}} \quad . \qquad (2\text{-}2)$$

$R_{H,\,s}$: the sheet Hall coefficient, σ_s: the reciprocal of the sheet resistivity r_s, and $x_{i+1} - x_i$: the thickness of the etched-off layer.

The Be atomic profiles in the $Al_xGa_{1-x}As$ are measured by a secondary ion mass spectrometer using oxygen as the primary sputtering ion beam at an energy of 10.5 keV. In this case, the depth scales are established by measuring the sputtered crater depths.

Since PL is sensitive to defects, it can be used to evaluate the optical qualities of the ion-implanted layers. An Ar laser line (514.5 nm) is used as an excitation light source, and the PL spectrum is measured at room temperature by a conventional method.

2-3. Results

2-3-1. Annealing-induced change in the electrical properties of unimplanted $Al_xGa_{1-x}As$

Before discussing the electrical activation behavior of the Be implants, it should be noted that annealing-induced change in the electrical properties is observed in the MBE-grown $Al_xGa_{1-x}As$. The undoped, high-resistive $Al_xGa_{1-x}As$ changes into low-resistive, p-type material after annealing. The annealing-induced hole concentrations determined from the Hall-effect measurements versus the Al composition x for the $Al_xGa_{1-x}As$ after RTA at 900°C are shown in Fig. 2-1. This phenomenon occurs only in the Al containing MBE-grown layers but not in the GaAs. The hole concentration, which is on the order of 10^{17} cm^{-3}, distributes uniformly throughout the $Al_xGa_{1-x}As$ epitaxial layer. The samples annealed at low temperatures (<750°C), however, do not indicate a significant number of holes in the epitaxial layers. As a result of this phenomenon, plateaus-like hole concentration profiles are found in the deep portion [see Fig. 2-8 (b)].

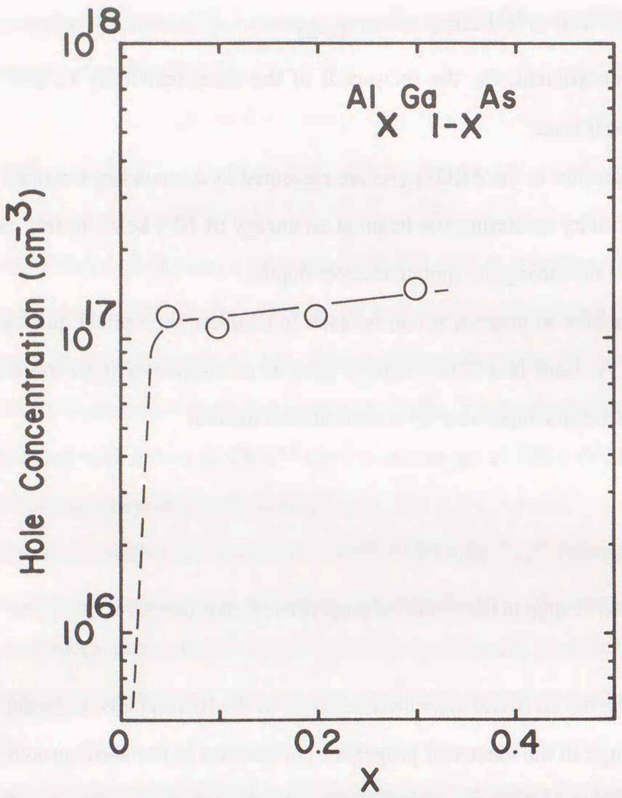

Fig. 2-1. Annealing-induced hole concentration as a function of Al composition x for $Al_xGa_{1-x}As$ after RTA at 900°C.

S. Adachi [14] has reported the observation of thermal conversion of the $Al_xGa_{1-x}As$ grown by MBE from undoped, high-resistive $Al_xGa_{1-x}As$ to low-resistivity, p-type material after annealing beyond the growth temperature (650°C). Electrical measurements indicate that a substantial concentration of residual C acceptors causes the thermal conversion of the $Al_xGa_{1-x}As$ layers. The reason why the thermal conversion occurs only in the Al containing MBE-grown layers but not in the GaAs may be related to a kind of combination between residual C acceptors and Al atoms.

2-3-2. Electrical activation behavior

The annealing behavior of apparent activation fractions of Be^+ implants in the $Al_xGa_{1-x}As$ obtained from Hall-effect measurements is shown in Fig. 2-2. In this study, apparent "activation fraction" is defined as the sheet hole concentration obtained by Hall-measurements divided by Be^+-dose. It should be noted that Be^+-implantation is carried out through the SiO_2 encapsulant. Because of losing the implants in the SiO_2 encapsulant, the experimental activation fraction do not approach 100 % even if all of the Be implants in the $Al_xGa_{1-x}As$ are activated. The annealing-induced holes also influence the actual activation fraction of the Be implants in the $Al_xGa_{1-x}As$ as mentioned in the section 2-3-1. A correction for these holes is made when determining the Be actual activation fractions.

There is a considerable difference between the GaAs and $Al_xGa_{1-x}As$ concerning the annealing behavior of the activation fraction. For the GaAs, the electrical activation occurs from 400°C and saturates at about 450°C. On the other hand, the activation fractions in the $Al_xGa_{1-x}As$ are lower than those in the GaAs. These values increase gradually with increase in the annealing temperature and exhibit the maximum value at temperatures near 900°C. Figure 2-2 also shows that at any fixed temperature the electrical activation fractions in the $Al_xGa_{1-x}As$ decrease with increasing x.

The measured hole mobility versus annealing temperature for the Be^+-implanted $Al_xGa_{1-x}As$ is shown in Fig. 2-3. As can be seen from the figure, there is a decrease in the hole mobility with an increase in x. This dependence of the hole mobility on x agrees with that obtained in the Ge- and Mg-doped $Al_xGa_{1-x}As$ [15-17]. The effective hole mass is known to be strongly connected with the hole

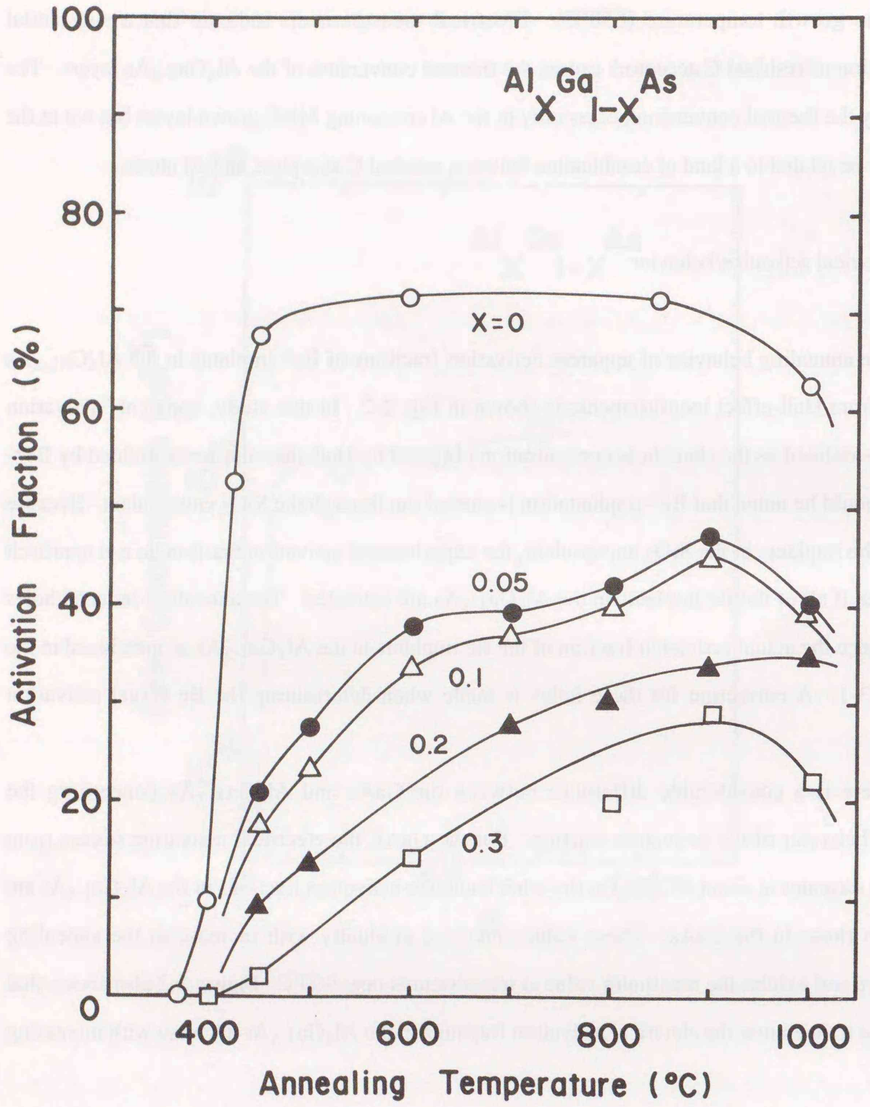

Fig. 2-2. Activation fractions in Be^{+}-implanted $Al_xGa_{1-x}As$ as a function of isochronal annealing temperature.

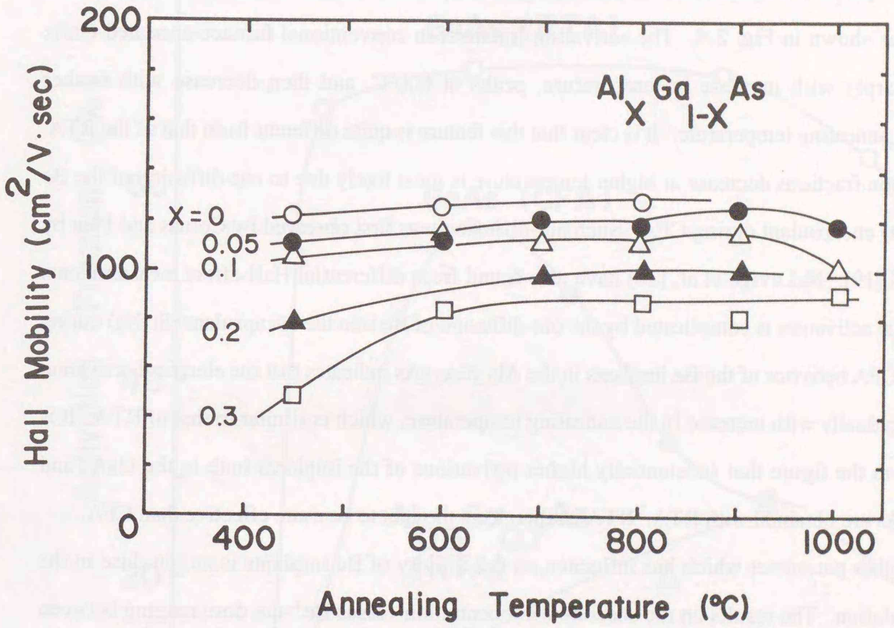

Fig. 2-3. Hall mobilities in Be^{+}-implanted $Al_xGa_{1-x}As$ as a function of isochronal anneal temperature.

mobility, and heavier masses generally give lower mobilities. The valence-band masses in the $Al_xGa_{1-x}As$ increase gradually with an increase in x [18]. Lower hole mobility values can thus be expected in the $Al_xGa_{1-x}As$ with larger x values, as evidently observed in this study. Moreover, the present data indicates that the mobilities are not low even after lower-temperature annealing, and this is especially true for samples with smaller x values.

A comparison of the electrical activation fractions between RTA and CFA is also carried out in this study, as shown in Fig. 2-4. The activation fractions in conventional furnace-annealed GaAs increase sharply with increase in temperature, peaks at 600°C, and then decrease with further increases in annealing temperature. It is clear that this feature is quite different from that of the RTA. The activation fractions decrease at higher temperature is most likely due to out-diffusion of the Be into the SiO_2 encapsulant during CFA. Such out-diffusion was first observed by Comas and Pleu by using SIMS [19]. NcLevige et al. [20] have also found from differential Hall-effect measurements that electrical activation is complicated by the out-diffusion of Be into the encapsulant (Si_3N_4) during CFA. The CFA behavior of the Be implants in the $Al_{0.3}Ga_{0.7}As$ indicates that the electrical activation increases gradually with increase in the annealing temperature, which is similar to that of RTA. It is obvious from the figure that substantially higher activations of the implants both in the GaAs and $Al_{0.3}Ga_{0.7}As$ are obtained with RTA. RTA is, therefore, thought to be more effective than CFA.

Another parameter which has influence on the activity of Be implants is an ion-dose in the Be^+-implantation. The results on the sheet hole concentration versus Be^+-ion dose ranging between $5x10^{13}$ and $2x10^{14}$ cm^{-2} in the $Al_xGa_{1-x}As$ are shown in Fig. 2-5. All of the samples are implanted through the SiO_2 encapsulants with 100 keV, and then annealed at 900°C for 4 s by the RTA. The electrical activations are found to be lower for samples with larger x values. Moreover, the activation fractions do not significantly saturate in the GaAs, but a weak saturation can be found in the $Al_xGa_{1-x}As$ at doses higher than about $1x10^{14}$ cm^{-2}. The corresponding sheet hole mobilities of the GaAs and $Al_xGa_{1-x}As$ decrease with increasing ion dose (e. g., for the GaAs from 160 cm^2/Vs for an ion dose of $5x10^{13}$ cm^{-2} to 110 cm^2/Vs for a dose of $2x10^{14}$ cm^{-2}). A similar dependence of the hole mobility on the ion-dose has also been found in the Be^+- and Zn^+-implanted GaAs [21-23].

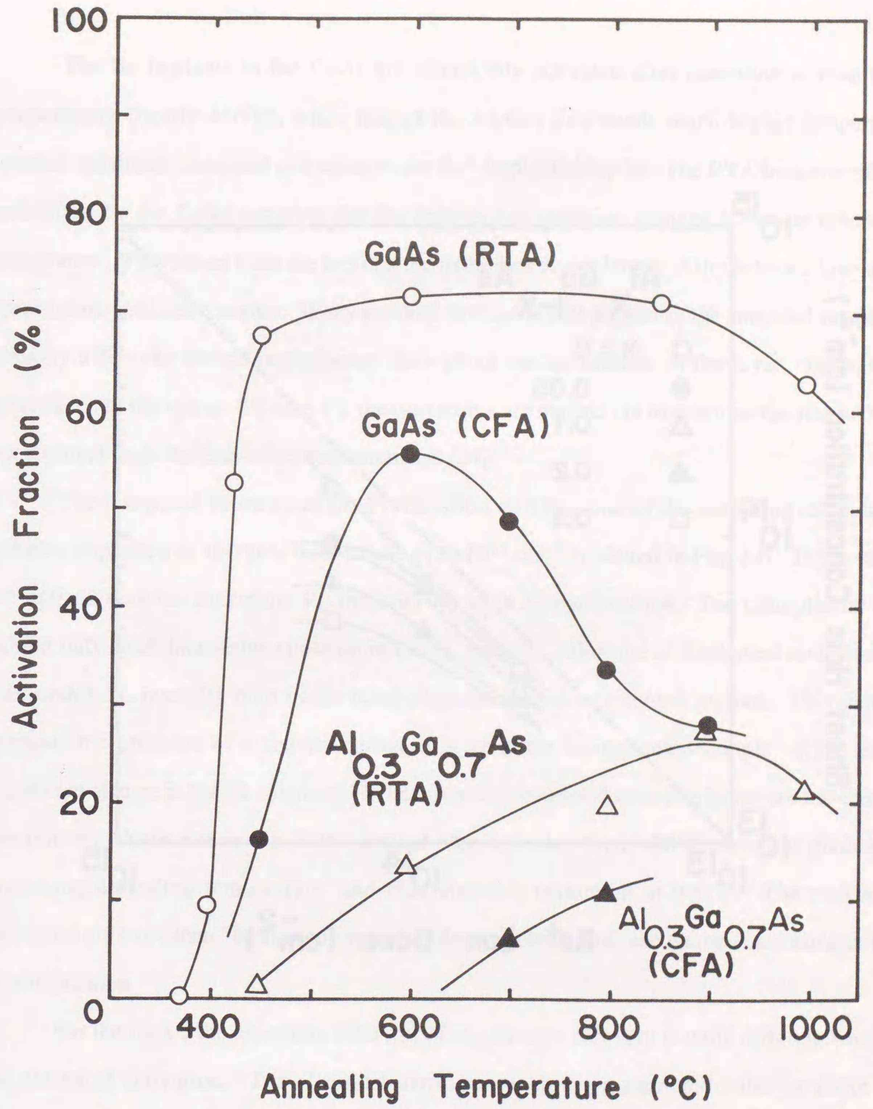

Fig. 2-4. Comparison of activation fractions in Be^+-implanted $Al_xGa_{1-x}As$ between RTA (4 s) and CFA (10 min).

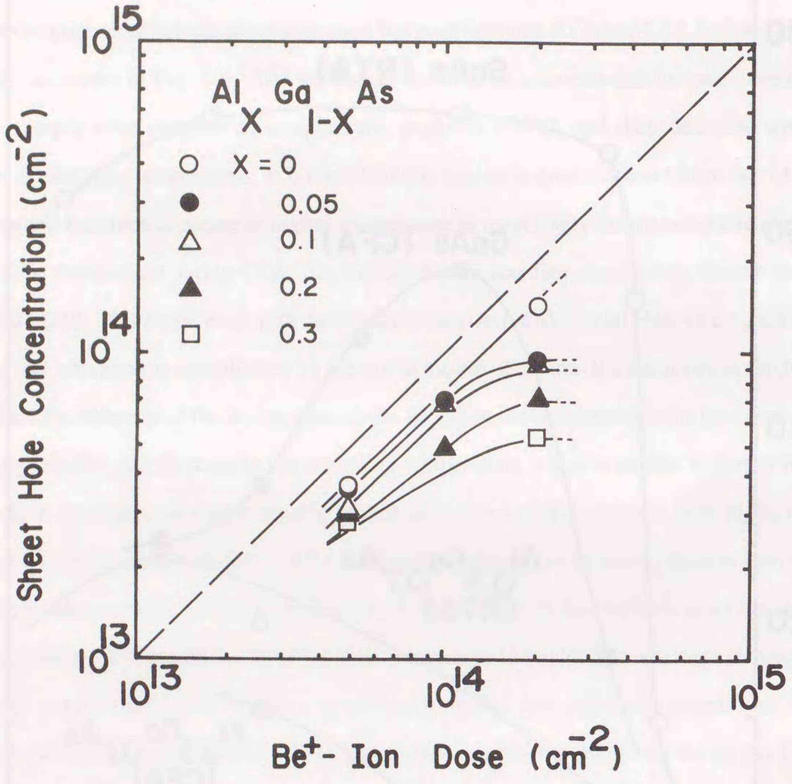

Fig. 2-5. Sheet hole concentration as a function of Be^+-ion dose in $Al_xGa_{1-x}As$ after RTA at 900°C.

2-3-3. Residual damage in the Be-ion-implanted $Al_xGa_{1-x}As$

The Be implants in the GaAs are electrically activated after annealing at relatively low temperatures (nearly 450°C), while that of the $Al_xGa_{1-x}As$ needs much higher temperatures to produce maximum electrical activation in the Be^+-implanted layers. The RTA behavior of the hole mobilities for the GaAs suggests that the recovery of radiation damage occurs at relatively low temperature. This comes from the fact that the mobilities do not largely differ between low- and high-temperature annealed samples. If any residual damage is still present in the annealed sample, it will strongly affect the device performance throughout carrier lifetime in the layer. Because of the importance of the carrier lifetime, PL measurements are carried out to examine the residual damage not apparent from the Hall-effect measurements [24].

The integrated intensity of the PL emission as a function of the annealing temperature for samples implanted at 100 keV with a dose of $2x10^{14}$ cm^{-2} is plotted in Fig. 2-6. These values are normalized with the maximum PL intensity for each Al composition. The unimplanted samples exhibit only weak band-edge emission in the PL spectra. All of the as-implanted samples show no measurable PL intensity both in the band-edge and longer-wavelength regions. This fact clearly suggests the presence of a heavily damaged layer in the as-implanted sample. RTA leads to a significant change in the PL intensity. In addition, defect-related emission bands are not observed in this process. As is seen in Fig. 6, the damage recovery starts from 400°C, increases gradually with increasing annealing temperature, and then shows a maximum at 900°C. The maximum PL intensities are more than 20 times stronger than those obtained from the unimplanted samples for each Al composition.

For the GaAs, the annealing behavior of the damage recovery is quite different from that of the electrical activation. The electrical activation achieves a saturated value at about 450°C. However, radiation damage which deteriorate the PL intensity is present even when the sample is annealed at 450°C or higher temperatures. A similar tendency can also be recognized for the $Al_xGa_{1-x}As$, although it is not so conspicuous compared with the GaAs. Based on the above experimental results, an annealing temperature of about 900°C is necessary both for maximum electrical activation and damage recovery in the GaAs and $Al_xGa_{1-x}As$.

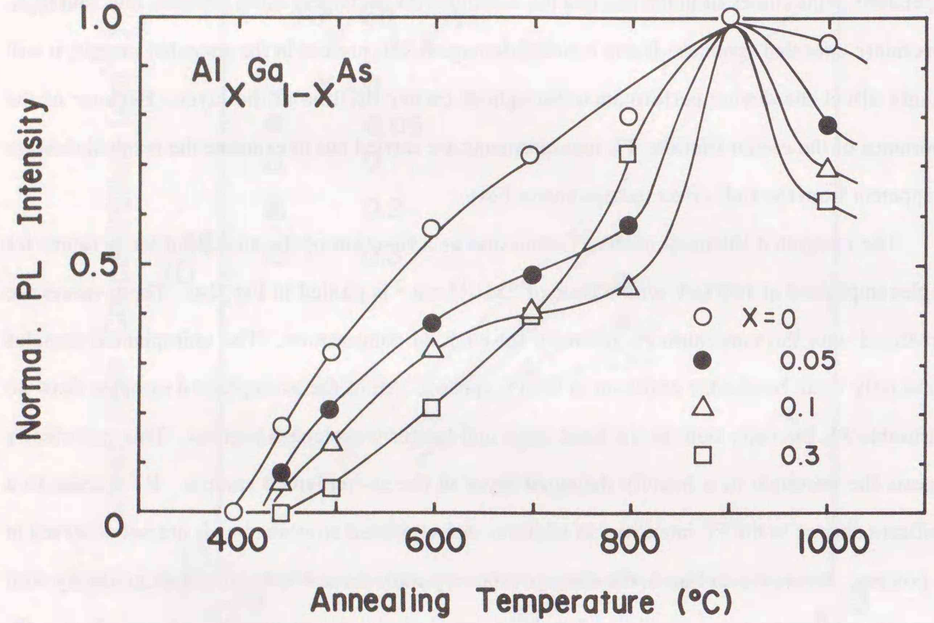

Fig. 2-6. Normalized PL intensity as a function of annealing temperature for Be^+-implanted $Al_xGa_{1-x}As$.

2-3-4. Atomic SIMS profiles

Be-atomic depth profiles are investigated using SIMS analysis. The data are taken continually removing the $SiO_2/Al_xGa_{1-x}As$ layers by sputtering with O^+-primary-ion bombardment. The intensity of the Be^+ secondary ions is not corrected for changes in the SIMS sensitivity in the SiO_2 and $Al_xGa_{1-x}As$

The SIMS Be profile in the GaAs both before and after RTA (800°C) are shown in Fig. 2-7 (a). The profile of the as-implanted sample, peaking at about 0.18 μm from the SiO_2/GaAs interface, resembles the theoretical curve (Gaussian distribution) which is obtained from LSS range statistic. A slight redistribution of the Be is found to occur after RTA, where a Gaussianlike profile moves into the bulk with a slightly changes sharp. A profile comparison between unannealed and annealed samples also shows that Be accumulation occurs at the SiO_2/GaAs interface by RTA.

A distinct anomaly is observed in the $Al_{0.3}Ga_{0.7}As$ on the SIMS profiles of Be after RTA, as shown in Fig. 2-7 (b). In the figure, the profile before and after an annealing at 600 and 800°C are compared. The as-implanted profile is near Gaussian, which is the same as that of the GaAs. There is a significant diffusion of Be toward the bulk side during RTA and, as a result, the samples show broad plateaus move deeply into the bulk as the annealing temperature increases. The accumulation of Be at the interface can also be clearly found even at low-temperature annealing (600°C).

Many data exist on Zn-diffusion into the $Al_xGa_{1-x}As$ as a function of the Al composition x [25]. These data show that the diffusion coefficient of Zn in the $Al_xGa_{1-x}As$ increases with increasing x. Comas and Bedair [6] have found that the Be implants in the $Al_xGa_{1-x}As$ show significant redistribution and anomalous diffusion effects upon annealing at 800°C. The present results also show noticeable diffusion of the Be implants in the $Al_{0.3}Ga_{0.7}As$ but not so in the GaAs. These results indicate that a diffusion coefficient of Be in the $Al_{0.3}Ga_{0.7}As$ is larger than that in the GaAs.

One of the most pronounced annealing effects found in this study is the accumulation of Be at the SiO_2/GaAs or $SiO_2/Al_{0.3}Ga_{0.7}As$ interface (i. e., large Be implants are piled up at the interface during RTA). Because of higher energy particle irradiation, ion implantation usually generates many

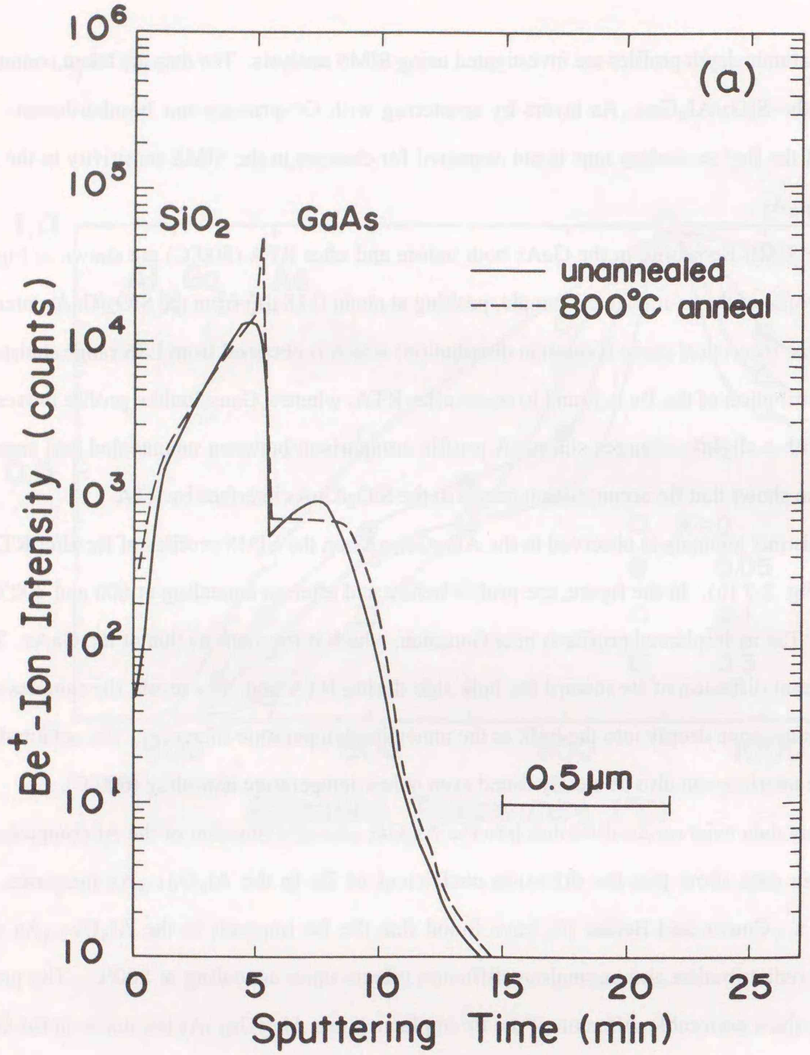

Fig. 2-7. (a) SIMS $^{9}Be^{+}$ profile in the SiO_2 encapsulant and GaAs before and after RTA.

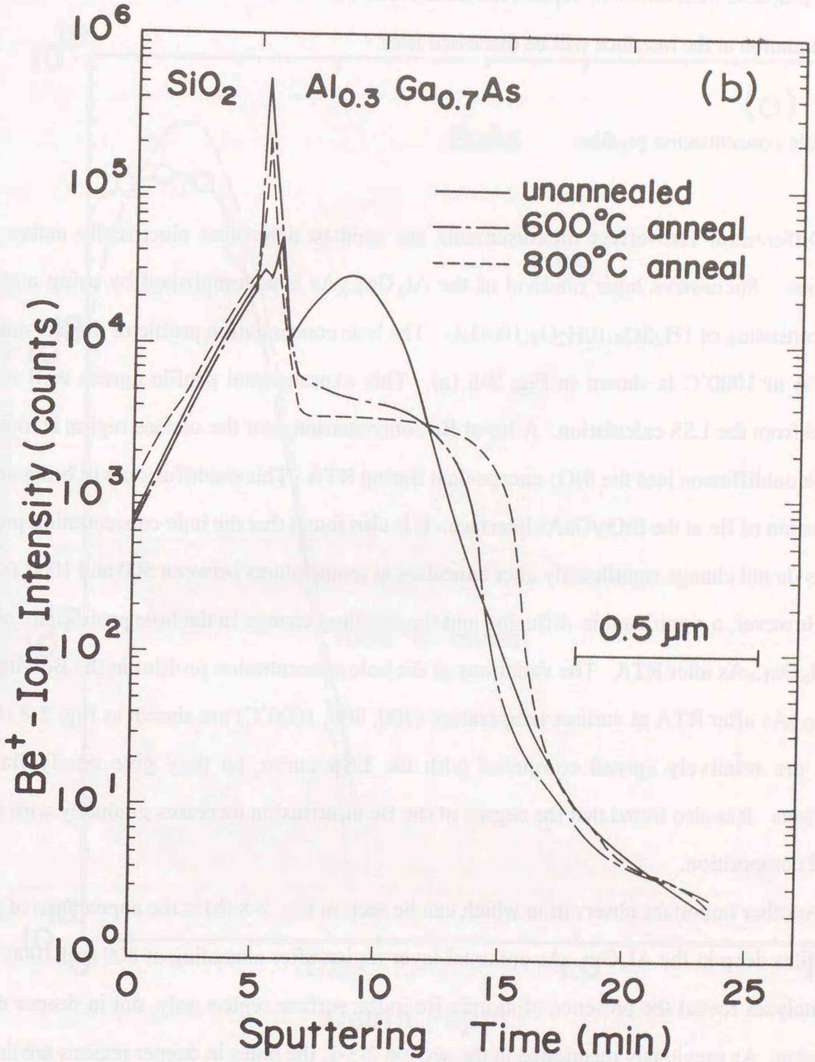

Fig. 2-7. (b) SIMS $^{9}Be^{+}$ profiles in the SiO_2 encapsulant and $Al_{0.3}Ga_{0.7}As$ before and after RTA.

lattice defects or causes the surface to be amorphized. An enhanced diffusion and subsequent redistribution of the Be implants may occur in a heavily damaged layer during annealing [26]. This is the most probable mechanism to explain the Be accumulation at the interface. The mechanism of the Be accumulation at the interface will be discussed later.

2-3-5. Hole concentration profiles

Differential Hall-effect measurements are used to determine electrically active carrier distribution. Successive layer removal of the $Al_xGa_{1-x}As$ is accomplished by using a chemical etchant consisting of $1H_2SO_4$:$10H_2O_2$:$100H_2O$. The hole concentration profile of the Be^+-implanted after RTA at 1000°C is shown in Fig. 2-8 (a). This experimental profile agrees well with that predicted from the LSS calculation. A lot of Be concentration near the surface region is most likely due to Be outdiffusion into the SiO_2 encapsulant during RTA. This outdiffusion will bring about the accumulation of Be at the SiO_2/GaAs interface. It is also found that the hole concentration profiles in the GaAs do not change significantly after annealing at temperatures between 500 and 1000°C.

However, a significant in-diffusion and the resulting change in the hole profiles are observed in the $Al_xGa_{1-x}As$ after RTA. The variations of the hole concentration profiles in the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ after RTA at various temperature (700, 800, 1000°C) are shown in Fig. 2-8 (b). The profiles are relatively spread compared with the LSS curve, so they give nearly flat depth distributions. It is also found that the degree of the Be in-diffusion increases gradually with increase in the Al composition.

Another important observation which can be seen in Fig. 2-8 (b) is the appearance of plateau-like profiles deep in the $Al_xGa_{1-x}As$ epitaxial layer region after annealing at 800 and 1000°C. The SIMS analyses reveal the presence of atomic Be in the surface region only, not in deeper epitaxial layer region. As previously mentioned in the section 2-3-1, the holes in deeper regions are due to the annealing-induced ones which may be attributed to unidentified p-type residual impurities or complexes consisting of these impurities and lattice native defects.

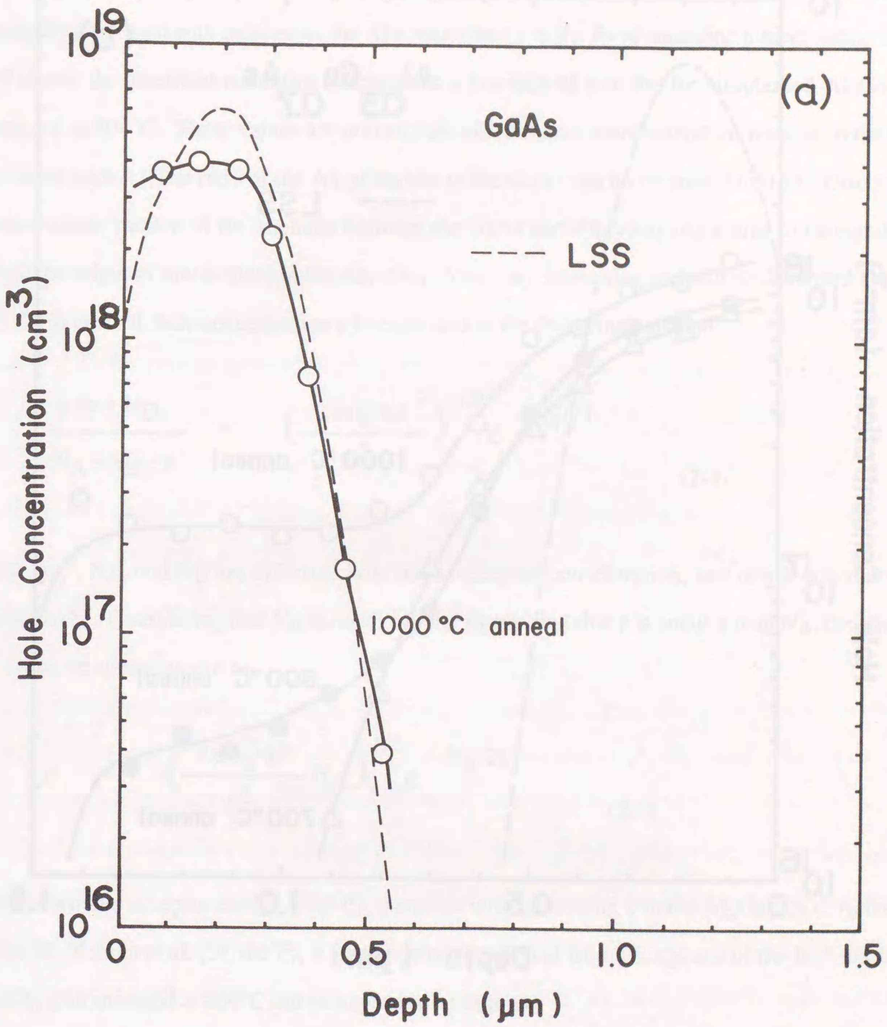

Fig. 2-8. (a) Hole concentration profile in Be^+-implanted GaAs after RTA at 1000°C.

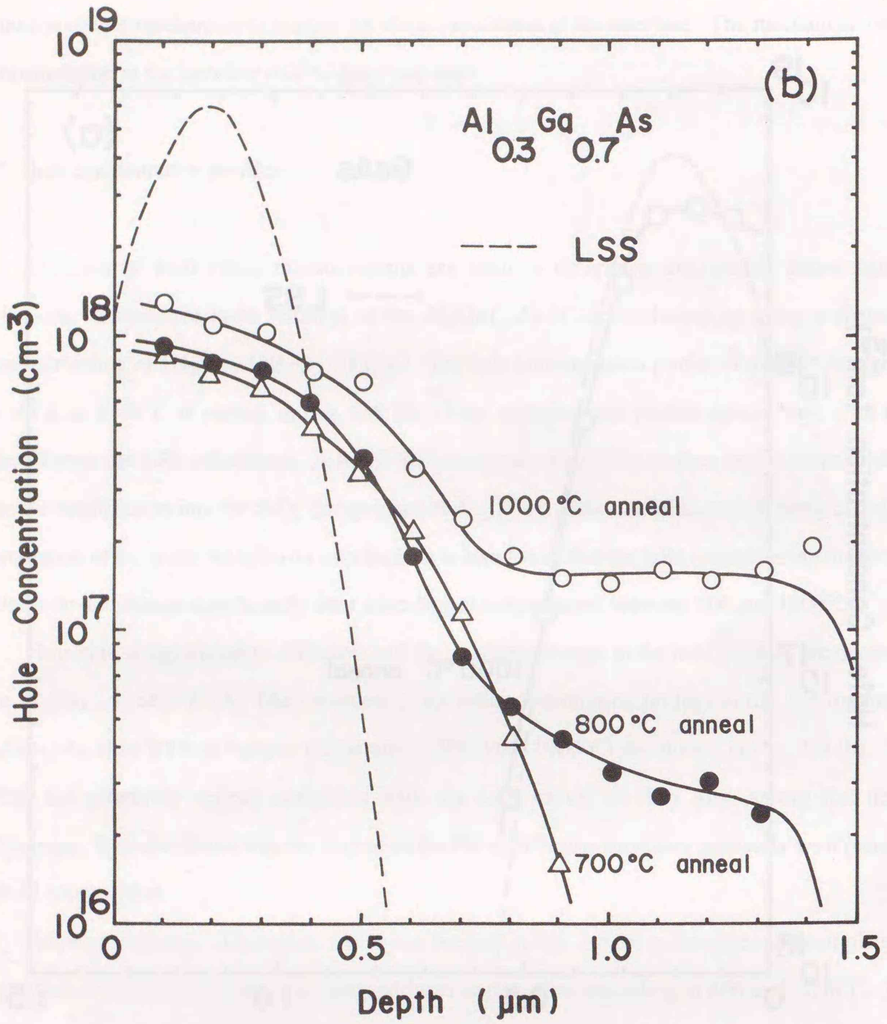

Fig. 2-8. (b) Hole concentration profile in Be^+-implanted $Al_{0.3}Ga_{0.7}As$ after RTA at 700, 800, and 1000°C.

2-4. Discussions on the low Be activity in $Al_xGa_{1-x}As$

Hall-effect measurements show that the electrical activation of Be implants in the $Al_xGa_{1-x}As$ gradually decreased with increase in the Al composition x at the fixed annealing temperatures. Figure 2-9 shows the electrical activation fractions as a function of x in the Be^+-implanted $Al_xGa_{1-x}As$ annealed at 800°C. These values are normalized with the maximum activation fraction in the GaAs (x=0) for each x. The ratio of the $Al_{0.3}Ga_{0.7}As$ to the GaAs can be estimated to 0.28. Discrepancy in activation fraction of Be implants between the GaAs and $Al_{0.3}Ga_{0.7}As$ seems to be significant. Thus, the origin of low activity in the $Al_{0.3}Ga_{0.7}As$ is very interesting and will be discussed.

In general, hole concentration p is expressed as the following equation:

$$\frac{p\,(p + N_D)}{N_A - N_D - p} = \left(\frac{2\pi m_h^* kT}{h^2}\right)^{3/2} e^{-E_A/kT} \quad . \qquad (2\text{-}3)$$

Here, m_h^*, N_A, and N_D are effective hole mass, acceptor concentration, and donor concentration, respectively. Considering that N_D is much smaller than p, and that p is smaller than N_A, the equation (2-3) can be approximated as

$$p = \left(\frac{2\pi m_h^* kT}{h^2} N_A\right)^{1/2} e^{-E_A/2kT} \quad . \qquad (2\text{-}4)$$

It is known that acceptor energy level E_A increases with increasing x in the $Al_xGa_{1-x}As$. According to the M. Yokota et al. [3], the E_A is empirically determined from PL spectra of the Be^+-implanted $Al_xGa_{1-x}As$ annealed at 800°C can be expressed as follows:

$$E_A\,(x)\,(meV) = 36.7\,x + 20.0. \qquad (2\text{-}5)$$

The ratio of p at various Al compositions to that at x=0 can be estimated using the Equation (2-4) and (2-5), assuming that m_h^* and N_A of the $Al_xGa_{1-x}As$ are not considerably different from those of the GaAs. Calculated ratios of p from x=0 to x=0.3 are also plotted in Fig. 2-9. It is found that the

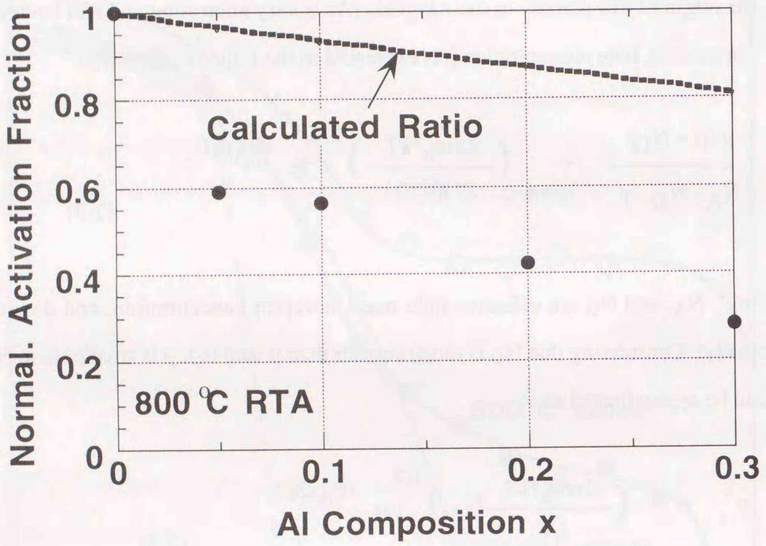

Fig. 2-9. Electrical activation fractions as a function of Al composition x in the Be^+-implanted $Al_xGa_{1-x}As$ annealed at 800°C. The calculated ratio is also plotted in the figure.

calculated ratio of p at x=0.3 to x=0 is 0.8. Thus, the lower activity of Be implants in the $Al_{0.3}Ga_{0.7}As$ cannot be explained by acceptor energy level E_A alone which increases linearly with increasing x.

The assumption that N_A of the GaAs is identified with that of the $Al_xGa_{1-x}As$ may be responsible for this large discrepancy between the experiment and the calculations. As mentioned before, the SIMS depth profile of the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ after high temperature annealing shows significant out-diffusion of Be implants at the interface between the SiO_2 encapsulant and $Al_{0.3}Ga_{0.7}As$. Because of this out-diffusion of Be implants, the integrated amount of Be atoms decreases compared with that of the GaAs. Therefore, the lower activity of Be implants in the $Al_{0.3}Ga_{0.7}As$ is mainly ascribed to the significant out-diffusion of Be after high temperature annealing. CFA behavior of the Be implants in the $Al_{0.3}Ga_{0.7}As$ has shown lower activity compared with RTA. This is because out-diffusion of Be implants by using CFA becomes more enhanced.

The mechanism of the significant out-diffusion of Be implants after high temperature annealing will be discussed. In ion-implanted regions, the radiation damage clusters overlap and an amorphous region is formed. When this amorphous region changes to a high quality crystal by regrowth during annealing, Be atoms are substituted for III-group sites and become "acceptor". However, K. Kakimoto and T. Katoda [27] have reported that by using Raman spectroscopy measurements there is quite a difference in annealing temperature for crystal recovery between the Si-ion-implanted GaAs and $Al_{0.3}Ga_{0.7}As$. The recovery temperature of Al-As and Ga-As bonds in the implanted $Al_{0.3}Ga_{0.7}As$ is higher than that of the Ga-As bond in the implanted GaAs. Thus, it is speculated that the annealing at higher temperature is needed to recover Al-As and Ga-As bonds in the Be^+-implanted $Al_xGa_{1-x}As$ than the Ga-As bond in the Be^+-implanted GaAs. At low temperature annealing, Be cannot be substituted for III-group sites and because of poor crystal quality it is located at the interstitial position between sites. If high-temperature annealing is applied, a large part of the Be atoms located at the interstitial position diffuse to the semiconductor surface and accumulate at the interface without substitution of III-group sites. Since Hall-measurements in order to estimate the electrical activity are carried out after the removal of the SiO_2 encapsulant, the accumulated Be never contributes to the electrical activity.

2-5. Conclusions

In this chapter, RTA behavior of the Be^+-implanted $Al_xGa_{1-x}As$ ($0 \le x \le 0.3$) is investigated by means of Hall-effect, PL, and SIMS measurements. The following conclusions can be drawn from these experiments.

(i) The electrical activation of Be implants in the GaAs occurs at annealing temperatures from 400°C and saturates at about 450°C. The activation fractions in the $Al_xGa_{1-x}As$ increase gradually with increase in the annealing temperature, but these values are apparently lower than those in the GaAs. Moreover, the $Al_xGa_{1-x}As$ with larger x gives smaller activation fraction at any fixed temperature.

(ii) PL intensities in the Be^+-implanted GaAs and $Al_xGa_{1-x}As$ indicate that the damage recovery starts from 400°C and increase gradually with further increase in the annealing temperature showing a peak at 900°C. Thus, a considerable amount of radiation damage, which acts to deteriorate the PL intensity, may still be present at annealing temperatures lower than 900°C.

(iii) RTA of Be implants is shown to produce higher electrical activity than CFA. This is true in both GaAs and $Al_xGa_{1-x}As$.

(iv) Atomic Be depth profiles in the $Al_xGa_{1-x}As$ before RTA resemble a theoretical Gaussian distribution predicted from the LSS calculations. A slight change in the Be distribution can be found in the GaAs after RTA. On the other hand, RTA brings about significant Be in-diffusion in the $Al_xGa_{1-x}As$ resulting in plateau-like depth profiles. Another pronounced annealing effect observed from the SIMS analysis is the accumulation of Be at the $Al_xGa_{1-x}As/SiO_2$ encapsulant interfaces. This effect is that a large fraction of Be is piled up at the interface by out-diffusion during RTA, and can be observed both in the GaAs and $Al_xGa_{1-x}As$.

(v) The lower activation fraction of Be implants in the $Al_{0.3}Ga_{0.7}As$ is found to be mainly due to loss of Be atoms from the semiconductor surface, resulting from out-diffusion and accumulation of Be at the $Al_xGa_{1-x}As/SiO_2$ encapsulant interfaces after the high temperature annealing. In the implanted $Al_xGa_{1-x}As$, the annealing at higher temperature is needed to recover Al-As and Ga-As bonds than to recover Ga-As bond in the GaAs. At low temperature annealing, Be cannot be substituted for III-group sites and because of poor crystal quality it is located at the interstitial position between sites. If high-temperature annealing is applied, a large part of the Be atoms located at the interstitial position diffuse to the semiconductor surface and accumulate at the interface without substitution of III-group sites. Since Hall-measurements are carried out after the removal of the SiO_2 encapsulant, the accumulated Be never contributes to the electrical activity.

(vi) The electrical activation profiles of the Be implants in the GaAs and $Al_xGa_{1-x}As$ are found to coincide well with the SIMS Be profiles. Annealing-induced change in the electrical properties is also found in undoped molecular beam epitaxial $Al_xGa_{1-x}As$. This change leads to the conversion of unimplanted, high-resistive $Al_xGa_{1-x}As$ layers into low-resistive, p-type layers.

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Chapter 3

Dual implantation in $Al_xGa_{1-x}As$

3-1. Introduction

In Chapter 2, electrical properties of the Be^+-implanted GaAs and $Al_xGa_{1-x}As$ after RTA have been described. It is found that the electrical activation fraction of Be implants in the $Al_xGa_{1-x}As$ is significantly lower than that in the GaAs [1]. In addition, remarkable redistribution of the Be atoms is observed in the $Al_xGa_{1-x}As$ after RTA. Low electrical activity and redistribution of Be implants are disadvantageous for the fabrication of various devices using the Be^+-implantation.

The use of dual implantation of dopant ions and complementary species has been first proposed by Heckingbottom and Ambridge [2]. For example, dual ions of Be and As is abbreviated as "Be^+/As^+". This dual implantation is beneficial in that stoichiometric-balance preservation in dual implants helps to assure activation and suppress redistribution of the dopant ions. A pronounced effect has been reported on a number of dual-implant combinations in the GaAs, such as Mg^+/As^+ [3, 4], Zn^+/As^+ [5], Zn^+/Se^+ [6], C^+/O^+ [7], C^+/Ga^+ [8], Ge^+/Ga^+ [9], Ge^+/As^+ [10], Se^+/Ga^+ [11, 12], and Si^+/P^+ [13]. It is reported that for the $Al_xGa_{1-x}As$ the dual-implantation effect has also been assured regarding combination of Mg^+/P^+ [14]. The Mg^+/P^+ dual-implantation in the $Al_xGa_{1-x}As$ improved activity of Mg^+ and suppress its redistribution.

The purpose of this chapter is to enhance electrical activity of Be implants and to suppress its redistribution after high-temperature annealings in the $Al_xGa_{1-x}As$ using Be^+/P^+ or Be^+/As^+ dual implantation. Hole concentration and mobility dependence on annealing temperature are measured at temperatures up to 950°C. Differential Hall-effect measurements are also used to determine electrically active carrier profiles in the implanted samples.

3-2. Experimental

The undoped $Al_{0.3}Ga_{0.7}As$ epitaxial layers are grown on semi-insulating Cr-doped (100) GaAs substrates by MBE. Be^+ ions were implanted with a dose of $1x10^{14}$ cm^{-2} at 50 keV. P^+ or

As^+ ions are then implanted with a dose of $1x10^{14}$ cm^{-2} at 150 keV (P^+) and 195 keV (As^+). The P^+ ion energy (150 keV) is chosen so that a projected range (R_p) of Be^+ ions coincides with that of P^+ ions. The As^+ ion energy (195 keV) selected in this study is an upper limit of the ion implantation machine used. In the case of Be^+/As^+ implants, Be^+-ion implantation is performed through SiO_2 films (0.08 μm thick) deposited by plasma-enhanced chemical vapor deposition. The SiO_2 films are then removed by HF etchant, and As^+ ions are implanted at 195 keV into the samples. This procedure assured that R_p of Be^+ coincides with that of As^+. All ion implantations are carried out at room temperature in a random axis orientation to avoid ion channeling.

The implanted samples are annealed in a Heatpulse 210T halogen lamp annealer with flowing N_2 gas for 4 s as mentioned in Chapter 2. No dielectric encapsulant is employed because thermal stress at the interface will have deleterious effects on the annealed sample.

Electrical measurements are carried out using van der Pauw technique. Hole concentration profiles are obtained by differential Hall-effect measurements in conjunction with chemical etching using H_2SO_4:H_2O_2:H_2O etchant for successive layer removal.

3-3. Results and discussions

3-3-1. Behavior of Be activation fractions

Figure 3-1 shows the annealing temperature dependence of sheet hole concentration and Hall mobility for the Be^+/P^+-implanted $Al_{0.3}Ga_{0.7}As$ layers. The results of Be^+-implanted ones are also shown in the figure. For the Be^+ and Be^+/P^+ implants, no electrical activation occurred at annealing temperatures below 550°C. Above this temperature sheet hole concentrations increase gradually with increases in annealing temperatures in both implants. Activation efficiency for samples annealed at 950°C are 33 % (Be^+) and 76 % (Be^+/P^+). The dual implant thus results in significant improvement in the electrical activity compared with the implant of Be^+ only.

As illustrated in Fig. 3-1, Hall-mobility data show no significant annealing temperature dependence for both single and dual implants. Mobilities for dual-implanted samples are slightly lower than those for the single-implanted samples. A similar tendency is also found in the Zn^+/As^+-

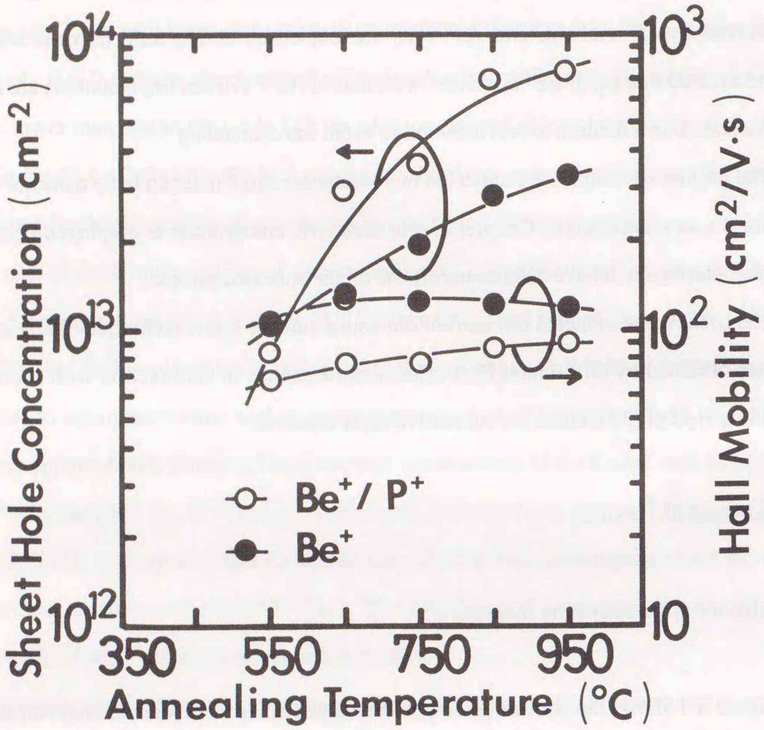

Fig. 3-1. Sheet hole concentration and Hall mobility in the Be^+- and Be^+/P^+-implanted $Al_{0.3}Ga_{0.7}As$ as a function of annealing temperatures.

or Mg^+/As^+-implanted GaAs [3-5]. The low mobilities for the dual implant suggest that the radiation damage may still be present in the implanted layers.

The annealing temperature dependence of sheet hole concentration and Hall mobility for Be^+ and Be^+/As^+ dual implants in the $Al_{0.3}Ga_{0.7}As$ is shown in Fig. 3-2. As in the case of the Be^+/P^+ implant, no electrical activation occurs at annealing temperatures below 550°C. Above this temperature the sheet hole concentrations also gradually increase with increases in the annealing temperatures. Activation efficiencies obtained for samples annealed at 950°C are 39 % (Be^+) and 61 % (Be^+/As^+) [15]. It is also found that the activation efficiency of the Be^+/As^+ implant becomes higher than that of the Be^+ implant at annealing temperatures above 750°C. On the other hand, the efficiency of the Be^+/P^+ implant exceeds that of the single implant at temperatures above 550°C. Heavier ions ($^{75}As^+$) usually produce a greater degree of radiation damage than lighter ions ($^{31}P^+$). Thus lower activation efficiencies for the Be^+/As^+ dual implant at lower annealing temperatures can be ascribed to residual radiation damage.

3-3-2. Depth profiles in $Al_{0.3}Ga_{0.7}As$

Figure 3-3 shows hole concentration profiles for the Be^+ and Be^+/P^+ implants in the $Al_{0.3}Ga_{0.7}As$ annealed at 950°C. There is significant diffusion of Be atoms in the single-implanted sample toward the bulk side (in-diffusion) during RTA. There is also significant loss of the Be^+ implant in the $Al_{0.3}Ga_{0.7}As$ (out-diffusion). This is easily understood from a comparison of the total (integrated) Be concentrations between unannealed and annealed samples. As a result, the sample shows a broad plateau in the hole concentration profile. The profile of the Be^+/P^+ implant, on the other hand, resembles the theoretical curve (Gaussian distribution) obtained from the energy range statistics proposed by LSS [16]; the experimental profile gives R_p of 0.18 μm, in agreement with that predicted from the LSS calculation.

Hole concentration profiles for the Be^+ and Be^+/As^+ implants in the $Al_{0.3}Ga_{0.7}As$ annealed at 950°C are shown in Fig. 3-4. As seen in the figure, the single-implanted sample shows a broad plateau, suggesting in-diffusion and out-diffusion of Be atoms in this sample. Also, as in the case of the Be^+/P^+ implant, a Gaussian-type profile is obtained in the Be^+/As^+ dual-implanted sample. The

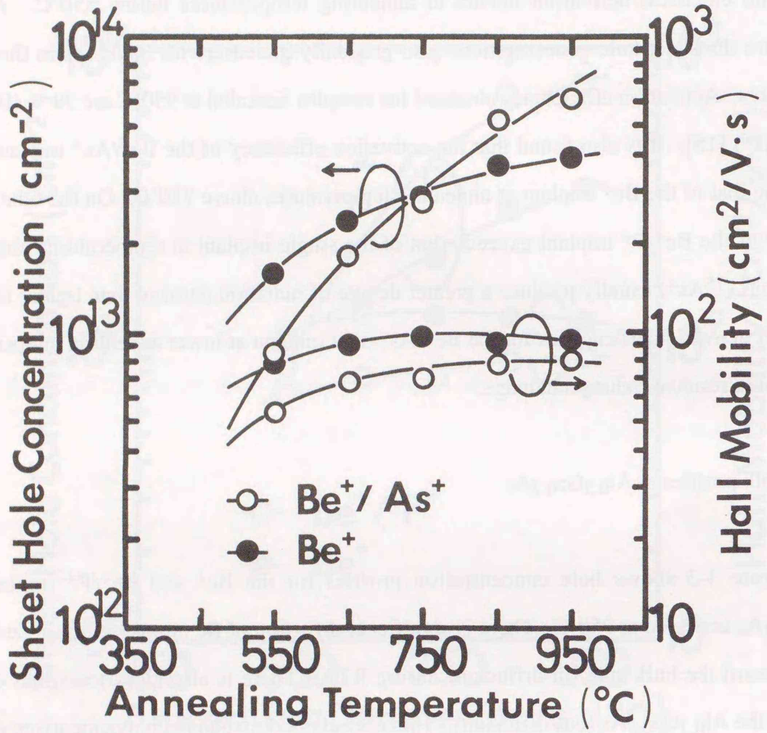

Fig. 3-2. Sheet hole concentration and Hall mobility in the Be^+- and Be^+/As^+-implanted $Al_{0.3}Ga_{0.7}As$ as a function of annealing temperatures.

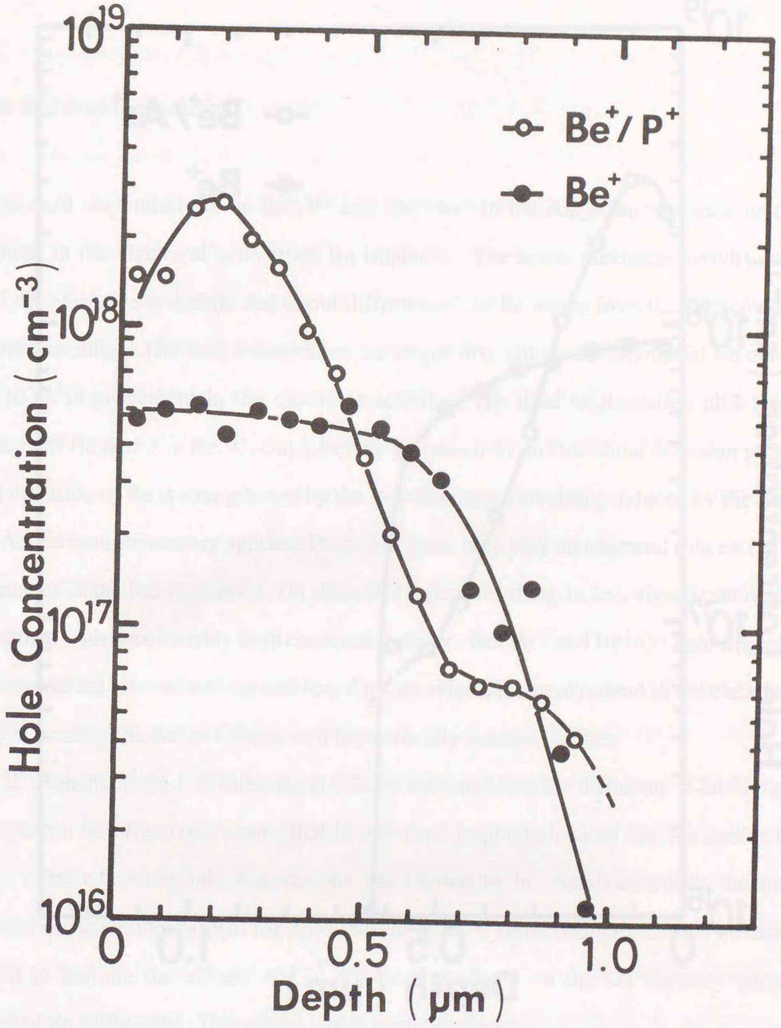

Fig. 3-3. Hole concentration profiles of the Be^+ and Be^+/P^+ dual implamts in $Al_{0.3}Ga_{0.7}As$ after annealing at 950°C.

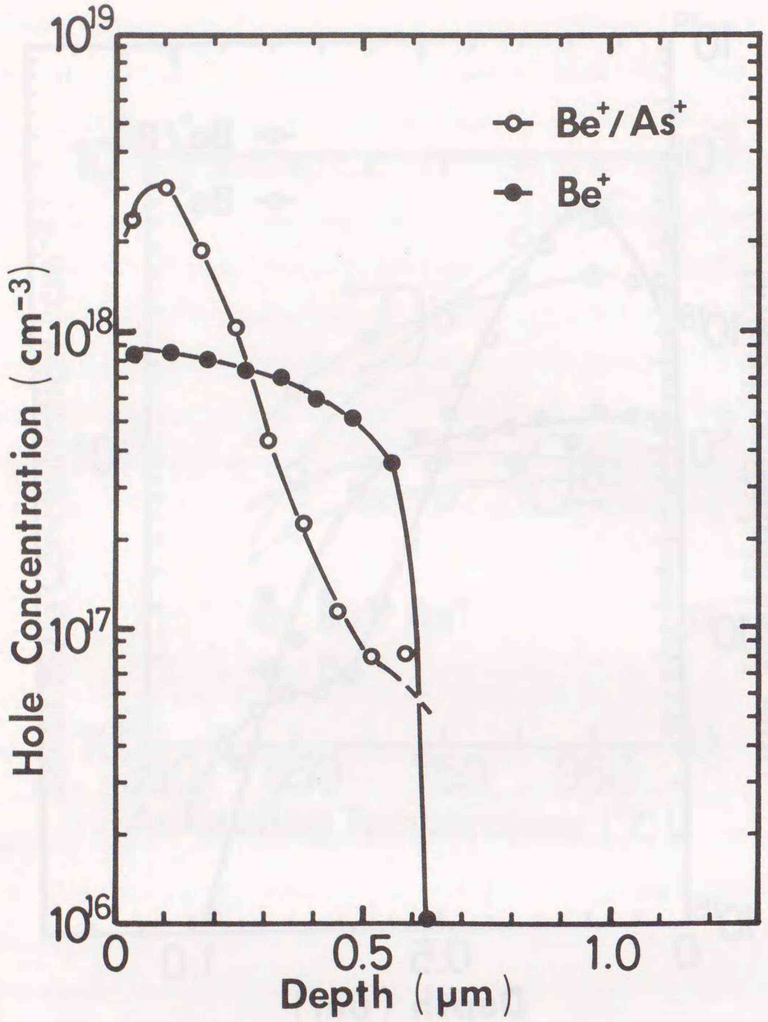

Fig. 3-4. Hole concentration profiles of the Be^+ and Be^+/As^+ dual implants in $Al_{0.3}Ga_{0.7}As$ after annealing at 950°C.

R_p value, approximately 0.1 μm, obtained in this case is lower than that of the Be^+/P^+ dual implant (nearly 0.18 μm). This is because the Be^+ ions are implanted through SiO_2 films only in the case of Be^+/As^+.

3-3-3. Effect of dual-implantation

The dual implantations of Be^+/P^+ and Be^+/As^+ in the $Al_{0.3}Ga_{0.7}As$ lead to significant improvement in the electrical activity of Be implants. The lower electrical activity in the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ is mainly due to out-diffusion of the Be atoms from the surface during high-temperature annealing. The dual implantation technique may reduce the amount of Be out-diffusion, resulting in an improvement in the electrical activity. The dual implantation also leads to less redistribution of Be atoms in the $Al_xGa_{1-x}As$ may be caused by an interstitial diffusion process. This interstitial diffusion of Be is strengthened by the stoichiometric imbalance induced by the implantation process. Added complementary species, P^+ or As^+ ions, may play an essential role on the reduction of As vacancies in the ion-implanted $Al_{0.3}Ga_{0.7}As$ layers, resulting in less-significant redistribution of the Be atoms with considerably high electrical activity. Be^+/Ar^+ and Be^+/O^+ dual implantations in the $Al_{0.3}Ga_{0.7}As$ are also carried out and found no considerable improvement in the electrical activity [17]. This is because the Ar^+ or O^+ is a stoichiometrically inactive species.

E. B. Stoneham and J. F. Gibbons [18] have indicated that the diffusion of Zn implants in the $GaAs_{0.6}P_{0.4}$ can be effectively controlled by the dual implantations of Ga, As and/or P prior to annealing. The experimental observations are shown to be consistent with the interstitial-substitutional diffusion mechanism for Zn-diffusion in III-V semiconductors. This diffusion model is modified to include the effects of Ga, As, or P implants on the Ga vacancy concentration dependence of Zn diffusivity. This model yields a relationship

$$D_{Zn} \approx f(C_{Zn}) / C_V.$$

where D_{Zn} is the diffusion coefficient of the Zn, C_V is the Ga vacancy concentration, and f is a function roughly proportional to the square of the Zn concentration C_{Zn}. When $[V_{Ga}]$ and $[V_{As, P}]$ are the equilibrium concentrations of Ga vacancies and column-V vacancies, respectively, the following relationship should hold good with the equilibrium condition,

$[V_{Ga}]\ [V_{As,\,P}] = \text{const.}$

An excess of Ga vacancies should result from an excess of As or P in the material, and vice versa, since the concentration of lattice sites remains the same for column-III atoms as for column-V atoms. Thus, it is expected to find in most III-V compounds and their alloys that implantation of column-V elements with Zn should inhibit Zn diffusion, while implantation of column-III elements with Zn should tend to enhance the diffusion.

The effect of dual implantation of Be^+/P^+ or Be^+/As^+ in the $Al_{0.3}Ga_{0.7}As$ is explained on the basis of this interstitial-substitutional diffusion model. The diffusion behavior of Be implants in the $Al_xGa_{1-x}As$ is identical to that of Zn implants in the $GaAs_{0.6}P_{0.4}$. The diffusion coefficient of the Be is proportional to a reciprocal of the concentration of column-III (Ga or Al) vacancies. The implantations of P or As with Be into the $Al_xGa_{1-x}As$ can suppress significant Be diffusion during annealing because P or As implants enhance the concentration of column-III (Ga or Al) vacancies resulting from reduction of column-V vacancies.

3-4. Conclusions

Dual implantation of Be^+/P^+ or Be^+/As^+ into the $Al_{0.3}Ga_{0.7}As$ are carried out, and electrical properties of the implanted layers are investigated by Hall-effect measurements. Improved electrical activity is observed for the dual implants compared with the Be implant. In particular, in the case of the Be^+/P^+ dual implants, apparent hole concentration becomes nearly twice as high as that of the Be^+ implant at annealing temperatures above 650°C. The dual implantations also greatly suppresses redistribution of Be atoms, and so Gaussian-type profiles remain even after high-temperature annealing (950°C). The effect of dual implantation of Be^+/P^+ or Be^+/As^+ in the $Al_{0.3}Ga_{0.7}As$ is explained on the basis of the interstitial-substitutional diffusion model. The reduction of As vacancies introduced by P^+- or As^+-implantations suppressed diffusion of Be implants in the $Al_xGa_{1-x}As$. In particular, suppression of the Be out-diffusion in the semiconductor surface improved electrical activity.

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Chapter 4

Electrical properties of Be-ion-implanted $Al_xGa_{1-x}As$ p-n junctions

4-1. Introduction

Chapter 4 considers the next stage of a C-up HBT fabrication. One of the new methods to create an effective barrier region at the extrinsic emitter/base which suppresses excess injection current is the formation of p-n junctions by Be^+-implantation into the n-type $Al_xGa_{1-x}As$ layer. The key steps to creation of the barrier are to establish whether the quality of a p-n junction is good or not and to control the position of the p-n junction region. In this chapter, for this purpose, the electrical properties of $Al_xGa_{1-x}As$ p-n junctions fabricated by Be^+-implantations are described. A few reports have been presented describing the properties of ion-implanted GaAs p-n junctions [1-4]. The junctions are fabricated by Be^+- or C^+-implantation into the n-type GaAs. The forward current-voltage (I-V) characteristics show ideality factors of 1.6 - 2.0, indicating that the current is controlled mainly by generation and recombination (g-r) in the depletion region. They are still far from being the ideality junction characteristic (n=1), but they allow the fabrication of adequate p-n junctions to be applied to some devices.

Only one report has been presented so far about properties of implanted $Al_xGa_{1-x}As$ p-n junctions [5]. The p-n junctions are fabricated by Be^+-implantation into the n-type $Al_{0.3}Ga_{0.7}As$, and showed an ideality factor of about 2. Graded or abrupt junction behavior is found to be implant dose dependent. Be concentration profiles taken by SIMS indicate that the graded junctions observed for higher dose ($>1\times10^{14}$ cm^{-2}) implants are due to in-depth diffusion of Be atoms.

In the Chapter 2, the RTA behaviors of electrical activation fraction of Be implants in undoped $Al_xGa_{1-x}As$ (x=0 - 0.3) were investigated. The activation fraction in GaAs comes to approximately 100% even at low annealing temperatures (450°C) with no significant diffusion of Be implants. On the other hand, the maximum activation fraction (40 %) in the $Al_{0.3}Ga_{0.7}As$ occur at higher annealing temperatures near 900°C. An anomalous diffusion of Be implants is observed at higher annealing temperatures for samples with larger Al compositions. Also, the optical activation behavior of Be

implants is strongly influenced by the radiation damage produced during implantation. This damage may bring about an increase in the g-r current in the junction. However, it is possible to remove the damage by high-temperature annealing. PL intensity measurements, in fact, reveal that the amount of radiation damage in the Be^+-implanted $Al_xGa_{1-x}As$ decrease significantly with an increase in the annealing temperature. It can thus be expected from these facts that the quality of the $Al_xGa_{1-x}As$ p-n junctions fabricated by Be^+-implantation will strongly depend on annealing temperatures.

In this chapter, the characteristics of p-n junctions fabricated by Be^+-implantation into the n-type $Al_xGa_{1-x}As$ grown by MBE are investigated by means of I-V and capacitance-voltage (C-V) measurements. Of particular interest are the annealing temperature dependence of the ideality factor and the C-V characteristics for the Be^+-implanted GaAs and $Al_{0.3}Ga_{0.7}As$ p-n junctions. For comparison, the characteristics of MBE-grown junctions (hereafter referred to as grown-in junction) are also examined.

4-2. Experimental

$Al_xGa_{1-x}As$ MBE wafers with two different Al compositions x (x=0 and 0.3) are used. These wafers are grown on n-type GaAs substrates (Si-doped $n=3\times10^{18}$ cm^{-3}). The MBE wafers consist of three epitaxial layers: an n-type $Al_xGa_{1-x}As$ (Si-doped $n=6\times10^{17}$ cm^{-3} for x=0 and 3×10^{17} cm^{-3} for x=0.3), a p-type $Al_xGa_{1-x}As$ (Be-doped, 5×10^{18} cm^{-3}), and a p-type GaAs cap layer are introduced for obtaining low ohmic contact resistivity. Be^+-implantation is carried out with a dose of 2×10^{14} cm^{-2} at an energy of 100 keV at room temperature in a random axis orientation to avoid ion channeling.

Schematic representation of the Be^+-implanted distribution superimposed on the background impurity levels of the MBE wafers is shown in Fig. 4-1. In the figure, the arrows P1 and P2 represent the positions of the p-n junction to be fabricated by MBE growth (grown-in junction) and subsequently by Be^+-implantation, respectively. The implanted samples are then annealed using a Heatpulse 210T halogen lamp annealer with flowing N_2 gas as mentioned in Chapter 2. An isochronal RTA of 4 s duration is performed in the temperature range between 400 and 950°C without any dielectric encapsulants.

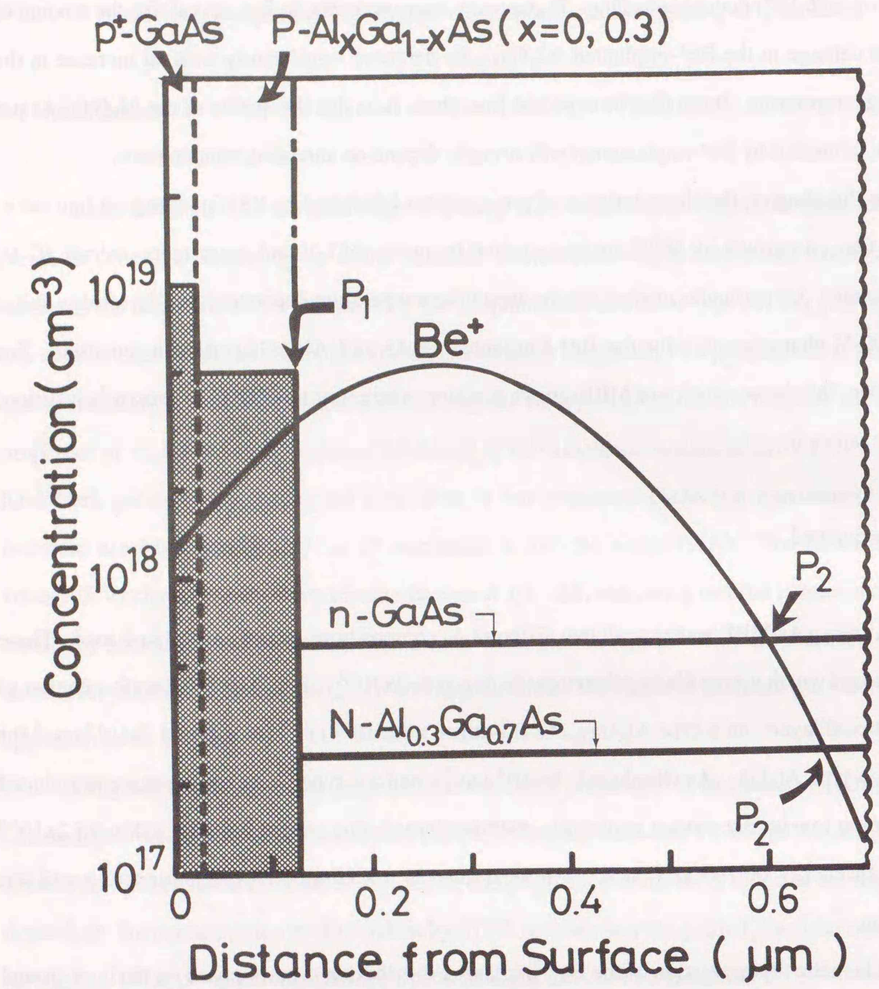


Fig. 4-1. Schematic representation of Be^+ ion-implanted LSS distribution superimposed on the background impurity levels of the MBE wafer. P_1 and P_2 represent the positions of the grown-in junction and the implanted p-n junction, respectively.

The fabricated diodes are illustrated in Fig. 4-2. After implantation and subsequent RTA, an individual 80-μm diameter diode is made by lift-off and mesa-etching techniques [6]. The ohmic metals used are Ti/Pt/Au for the p-type (top surface) and AuGe/Ni/Ti/Au for the n-type (rear surface) electrodes. They are alloyed at 350°C for 30 s.

4-3. Results and discussions

4-3-1. Forward I-V characteristics

For the p^+-n one-sided step junction, a forward biased current J_F is expressed as follows:

$$J_F = q\sqrt{\frac{D_P}{\tau_p}}\,\frac{n_i^2}{N_D}\exp\left(\frac{qV}{kT}\right) + \frac{qW}{2}\sigma v_{th} N_t n_i \exp\left(\frac{qV}{2kT}\right) \qquad (4\text{-}1)$$

where D_P is the diffusion coefficient of the minority carriers, τ_p is the lifetime of the minority carriers, n_i is the intrinsic carrier density, N_D is the donor density, W is the total depletion layer width, σ is the capture cross-section of the carriers, v_{th} is the thermal velocity of the carriers and N_t is the trap center density. Generally, J_F is experimentally expressed as follows: $J_F \propto I_0 \exp(qV/nkT)$, where the ideality factor is n=1 for a diffusion current and n=2 for a g-r current.

Figure 4-3 shows the forward I-V characteristics of the Be^+-implanted $Al_xGa_{1-x}As$ (x=0 and 0.3) diodes after RTA at 850°C. It is clear from the figure that the characteristic curve of the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ diode is shifted toward the higher voltage side (~0.4 V) compared with the curve of the GaAs diode. This voltage difference corresponds to the difference in built-in voltage between them.

For both the GaAs and the $Al_{0.3}Ga_{0.7}As$ p-n junction, the g-r current is dominant in the current region below 0.1 mA, showing an ideality factor of about n=1.8. Helix et al. [1] have reported that the forward I-V characteristic showing an ideality factor of n=1.6 in the GaAs p-n junction fabricated by Be^+-implantation after conventional furnace annealing (900°C, 30 min). Comas and Bedair [5] have also reported that the ideality factor of n=2.0 in the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ p-n junction after conventional furnace annealing (800°C, 1 h).

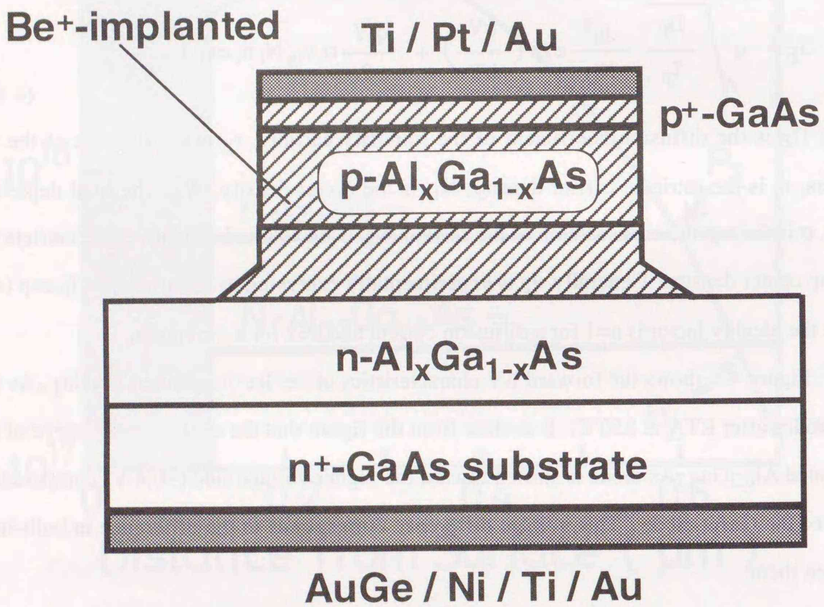


Fig. 4-2. Schematic cross-sectional view of the fabricated AlGaAs/GaAs diode.

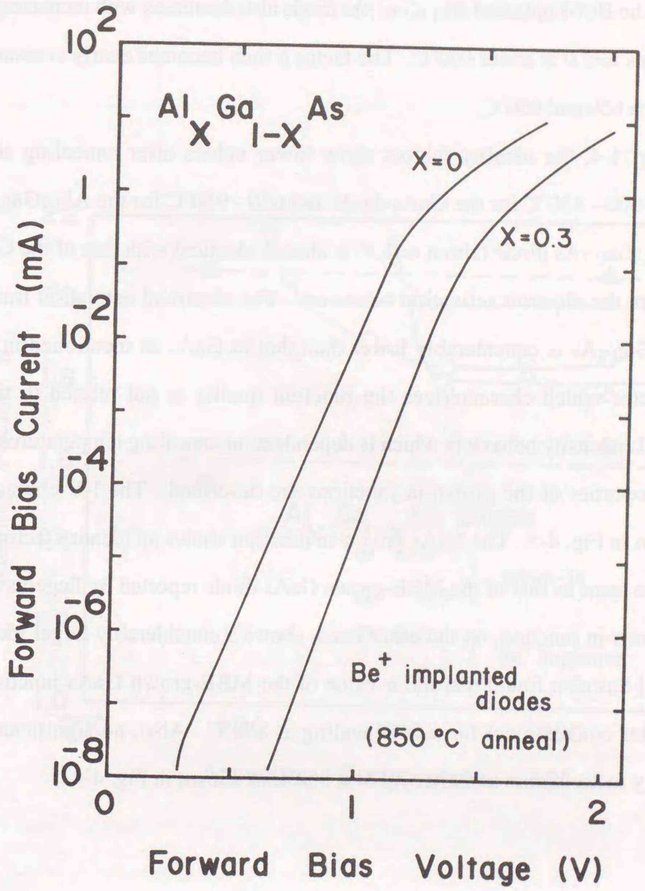


Fig. 4-3. Forward I-V characteristics of the Be+-implanted p-n junctions.

Figure 4-4 shows the annealing temperature dependence of the ideality factors for implanted p-n junctions and grown-in junctions. The ideality factor n for the implanted GaAs diode decreases with increasing annealing temperature and reaches n=2.0 at about 450°C. Then, n is nearly constant (n=1.82) up to 850°C, and further increase in temperature results in an increase in the ideality factor. The ideality factor for the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ diode also decreases with increasing annealing temperature and reaches n=2.0 at about 600°C. The factor n then becomes nearly constant (n=1.80) at temperatures between 650 and 950°C.

As seen in Fig. 4-4, the ideality factors show lower values after annealing at restricted temperature ranges of 600 - 850°C for the GaAs diode and 650 - 950°C for the $Al_{0.3}Ga_{0.7}As$ diode. The factor for the $Al_{0.3}Ga_{0.7}As$ diode (about n=1.8) is almost identical with that of the GaAs diode. This result differs from the electron activation behaviors. The electrical activation fraction of Be implants in the $Al_{0.3}Ga_{0.7}As$ is considerably lower than that in GaAs as mentioned in Chapter 2. Thus, the ideality factor which characterizes the junction quality is not related to the electron activation, but to the PL intensity behaviors which is dependent on annealing temperatures.

Next, some properties of the grown-in junctions are described. The I-V characteristics of these diodes are shown in Fig. 4-5. The GaAs grown-in junction shows an ideality factor of n=1.54. This value is nearly the same as that of the MBE-grown GaAs diode reported by Ilegems (n=1.7) [7]. The $Al_{0.3}Ga_{0.7}As$ grown-in junction, on the other hand, shows a considerably larger ideality factor (n=2.08). Ilegems [7] has also found that the n-value of the MBE-grown GaAs junction does not change before and after conventional furnace annealing at 850°C. Also, no significant change is observed in the ideality factor before and after RTA at 850°C as shown in Fig. 4-4.

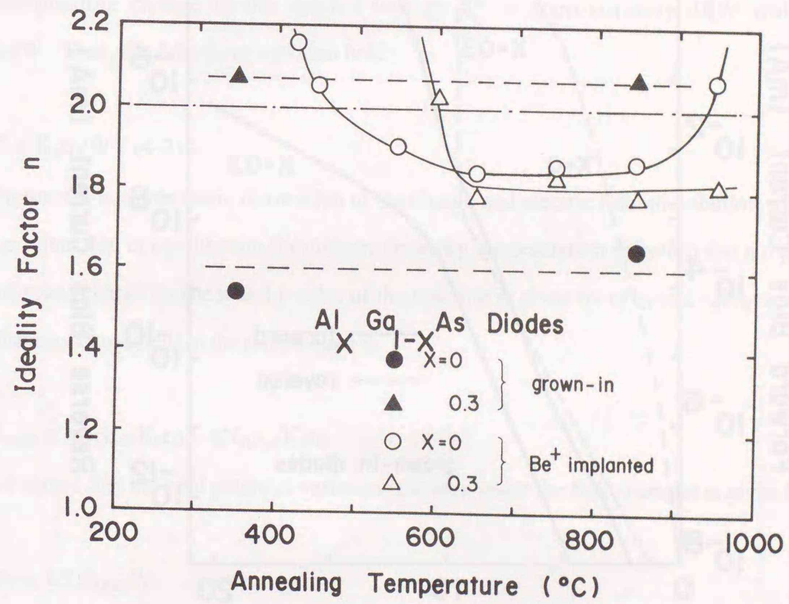


Fig. 4-4. Ideality factor n versus annealing temperature for the Be^+-implanted and the grown-in $Al_XGa_{1-X}As$ diodes.

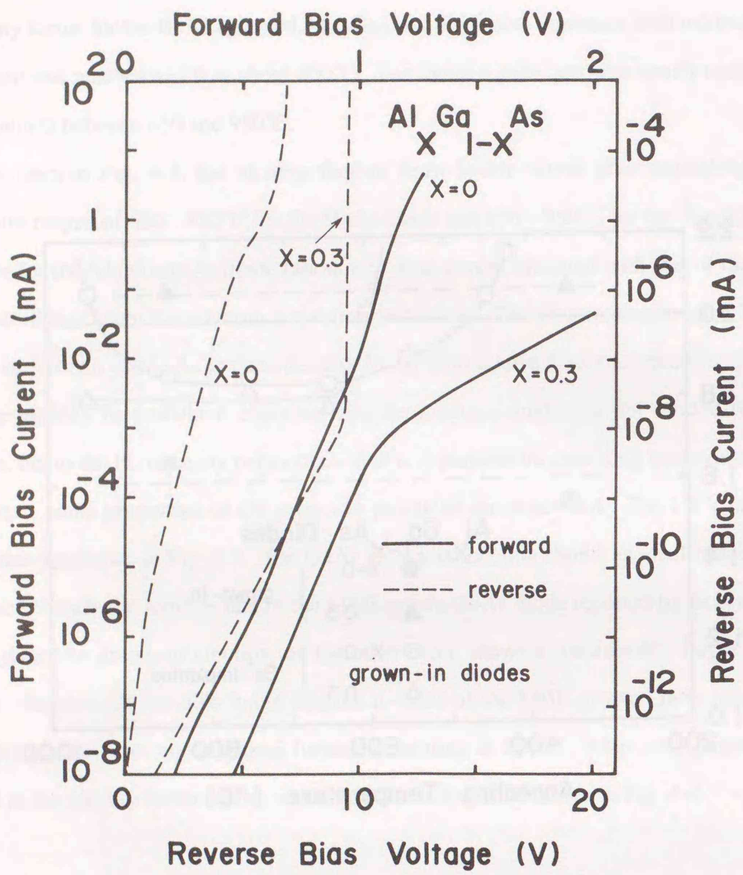


Fig. 4-5. Forward and reverse I-V characteristics of the $Al_xGa_{1-x}As$ grown-in diodes.

4-3-2. C-V characteristics

4-3-2-1. Theoretical approach

Capacitance per unit area is defined as $C \equiv dQ / dV$, where dQ is an incremental increase in charge per unit area upon an incremental change dV in applied voltage. The increase in depletion layer width and the corresponding increase in charge bring about an increase in the electric field by an amount $dE = dQ/K_s\varepsilon_0$, where K_s is the dielectric constant, and ε_0 is the permittivity of free space. The corresponding change in the applied voltage dV is approximately dEW which equals $(dQ/K_s\varepsilon_0)W$. Thus, the following equation holds

$$C = K_s\varepsilon_0/W. \quad (4\text{-}2)$$

Figure 4-6 is a schematic illustration of the charge and electric field distribution within a step (abrupt) p-n junction in equilibrium for uniform impurity concentration in both p and n regions. The density of space charge on the n and p sides of the junction is given by qN_D and $-qN_A$, respectively. The maximum electric field in the p-n junction is

$$E_{max} = qN_Dx_n/K_s\varepsilon_0 = qN_Ax_p/K_s\varepsilon_0. \quad (4\text{-}3)$$

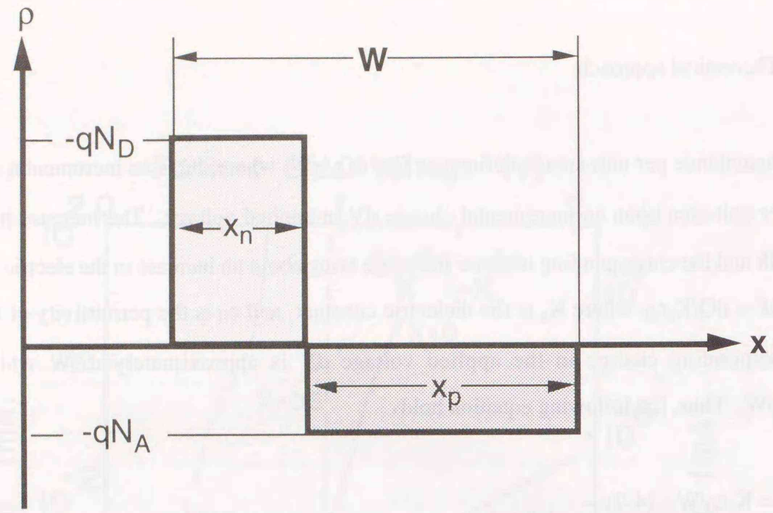
Figure 4-6 shows that the total potential variation (the area under the field triangle) is given by

$$\Phi_T = 1/2\ E_{max}W. \quad (4\text{-}4)$$

The total depletion region width W of a step p-n junction can be obtained as a function of the total electrostatic potential variation from one side of the junction to the other Φ_T,

$$W = \sqrt{\frac{2K_s\varepsilon_0}{q}\ \frac{N_A + N_D}{N_A\ N_D}\ \Phi_T} \quad (4\text{-}5)$$

When the concentration of the impurity on one side of the junction is much larger than that on the other side of the junction, for example, $N_A \gg N_D$, this results in the simpler form,



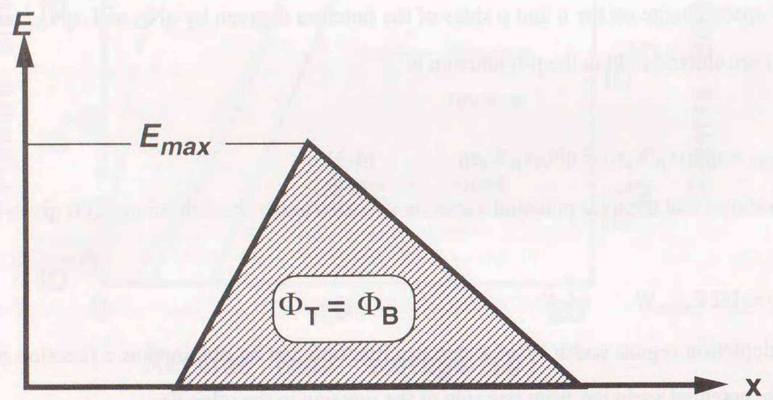


Fig. 4-6. Schematic illustration of the charge and electrical field distribution within a step (abrupt) p-n junction in equilibrium.

$$W = \sqrt{\frac{2K_s\varepsilon_0}{qN_D}\,\Phi_T} \qquad (4\text{-}6)$$

If positive voltage V_R is applied to the n-region with respect to the p-region, the total electrostatic potential across the junction Φ_T will increase by that amount $\Phi_T=\Phi_B+V_R$, where Φ_B is the built-in voltage. From Equations (4-2) and (4-6),

$$C = \sqrt{\frac{qK_s\varepsilon_0N_D}{2\,(V_R+\Phi_B)}} \qquad (4\text{-}7)$$

which can be rearranged to yield

$$\frac{1}{C^2} = \frac{2}{qK_s\varepsilon_0N_D}\,(V_R+\Phi_B) \qquad (4\text{-}8)$$

It is evident that by plotting C^{-2} versus V_R, a straight line should result if the actual impurity distribution can be approximated by the one-side step-junction model.

Another simple approximation, that is, "the linearly graded p-n junction" is described as shown in Fig. 4-7. The total depletion region width W is given by

$$W = \left[\frac{12K_s\varepsilon_0\Phi_T}{qa}\right]^{1/3} \qquad (4\text{-}9)$$

where "a" is gradient of impurity concentration at the junction. Similarly to the step p-n junction case, a straight line should result by plotting C^{-3} versus V_R for linearly graded junctions.

The charge on the heavily doped side of the depletion region will change by dQ as the applied reverse voltage is changed by dV, where dQ = qN(W)dW. The change in an applied voltage is

$$dV = dE\,W = \frac{qN(W)d(W^2)}{2K_s\varepsilon_0} \qquad (4\text{-}10)$$

Thus, an expression for the impurity concentration at the edge of the space-charge region is

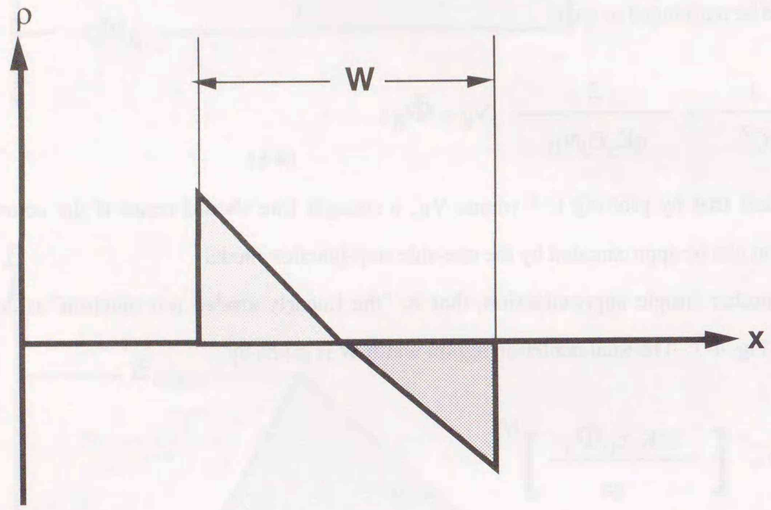


Fig. 4-7. Schematic illustration of the charge distribution within a linearly graded p-n junction in equilibrium.

$$N(W) = \frac{2}{qK_s\varepsilon_0} \frac{1}{d(1/C^2)/dV} \quad . \qquad (4\text{-}11)$$

4-3-2-2. Be-ion-implanted and grown-in $Al_xGa_{1-x}As$ p-n junctions

Figure 4-8 shows the plots of C^{-2} and C^{-3} versus the reverse bias voltage V_R for the grown-in and the Be^+-implanted GaAs p-n junctions annealed at 850°C, respectively. For the Be^+-implanted junction, a linear relationship is found for the C^{-3} plot, indicating that the p-n junction is linearly graded. In the case of the grown-in junction, on the other hand, C^{-2} is found to vary linearly with V_R, indicating that the p-n junction is abrupt. The C-V data for the Be^+-implanted GaAs junction after annealing at various temperatures also provide a linear relationship for C^{-3} vs. V_R rather than a plot of C^{-2} vs. V_R which represents a graded junction.

The C-V profile which indicates effective carrier concentration N_{eff} versus depletion width for diodes annealed at various temperatures are shown in Figs. 4-9 (a) for GaAs and (b) for the $Al_{0.3}Ga_{0.7}As$. Effective carrier concentration N_{eff} which corresponds to N(W) is measured using Equation (4-11). The profiles of the grown-in junctions are also plotted in the figures. For the Be^+-implanted GaAs diodes, N_{eff} increases with increasing annealing temperature. From the result for activation of Be implants, no difference in the C-V profiles can be expected after annealing at temperatures above 450°C. However, these results indicate that N_{eff} strongly depends on annealing temperature, and only the C-V profile for the diode after annealing at 850°C agrees with the calculated profile assuming an LSS profile and complete activation of Be implants. This fact suggests that the activation behavior of Be implants in the Si-doped GaAs may differ from the case of undoped GaAs. The GaAs grown-in junctions, on the other hand, show plateau in the profiles, and no significant change in N_{eff} can be found before and after RTA at 850°C.

Figure 4-10 shows the sheet carrier concentration and the Hall mobility for the Be^+-implanted n-type GaAs (Si-doped, $n=1\times10^{18}$ cm^{-3}, thickness is 1.0 μm) as a function of the annealing temperatures. Be^+ is implanted with a dose of 4×10^{14} cm^{-2} at 100 KeV. It is found from the figure that the Be^+-implanted n-type (Si-doped) GaAs still keeps n-type conduction below 750°C, on the contrary, it changes to p-type conduction over 750°C. As shown in Chapter 2, Be implants in the

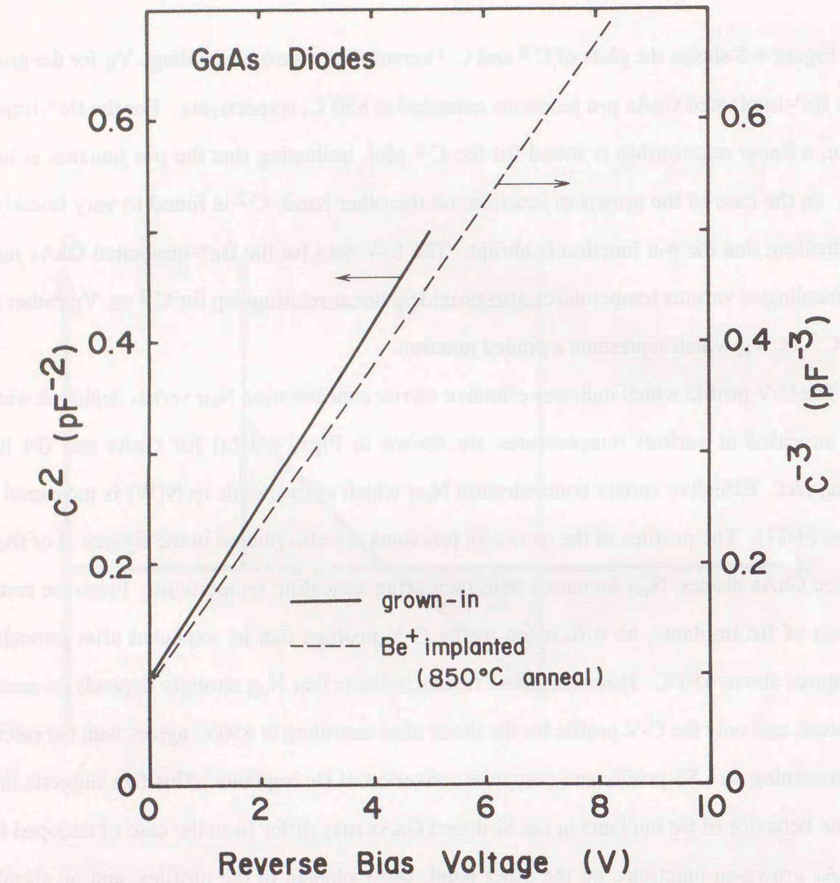


Fig. 4-8. C^{-2} and C^{-3} versus reverse bias voltage for the grown-in and the Be^+-implanted GaAs diodes, respectively.

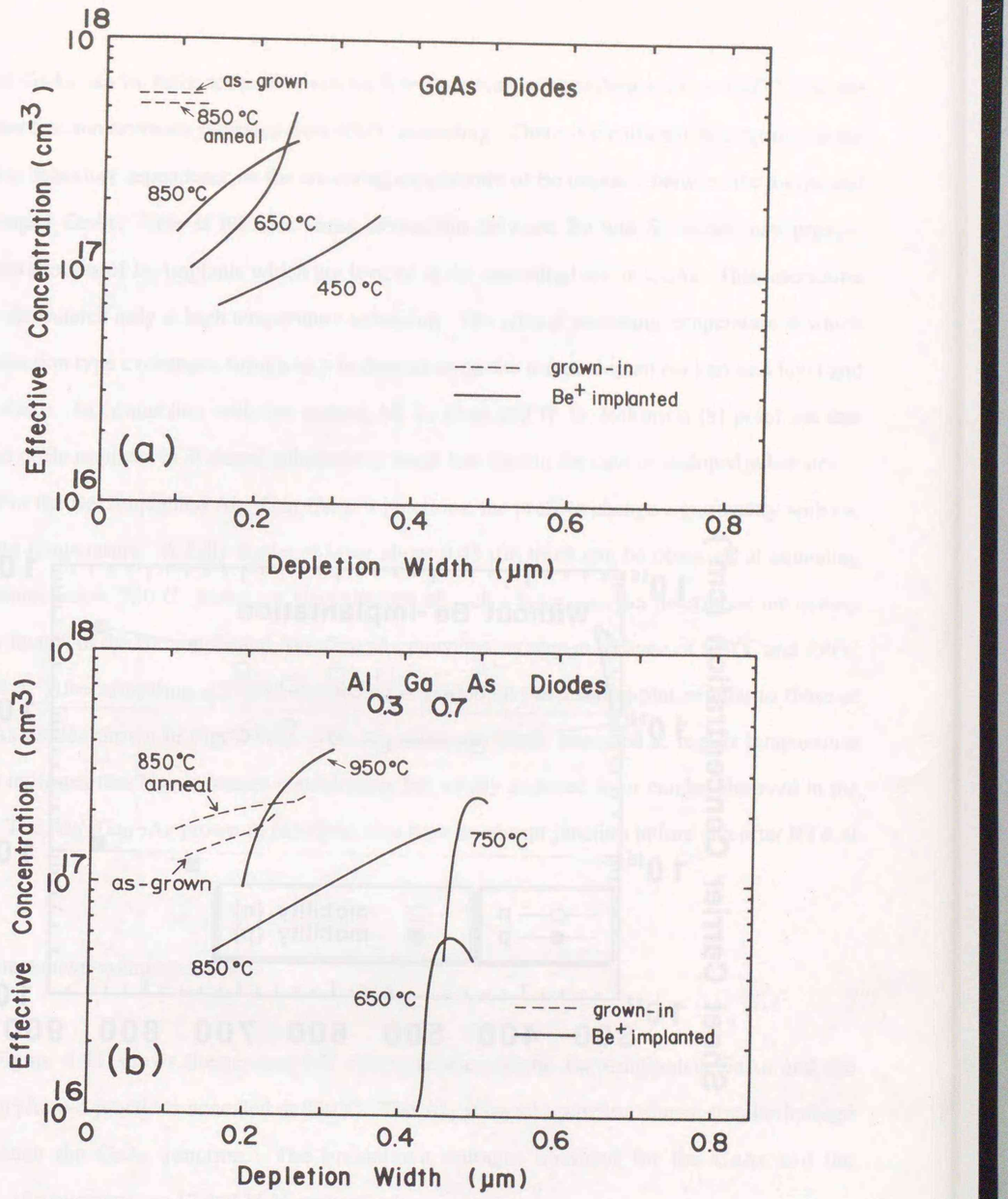


Fig. 4-9. (a) C-V profiles of the GaAs p-n junctions after annealing at various temperatures. (b) C-V profiles of the $Al_{0.3}Ga_{0.7}As$ p-n junctions after annealing at various temperatures.

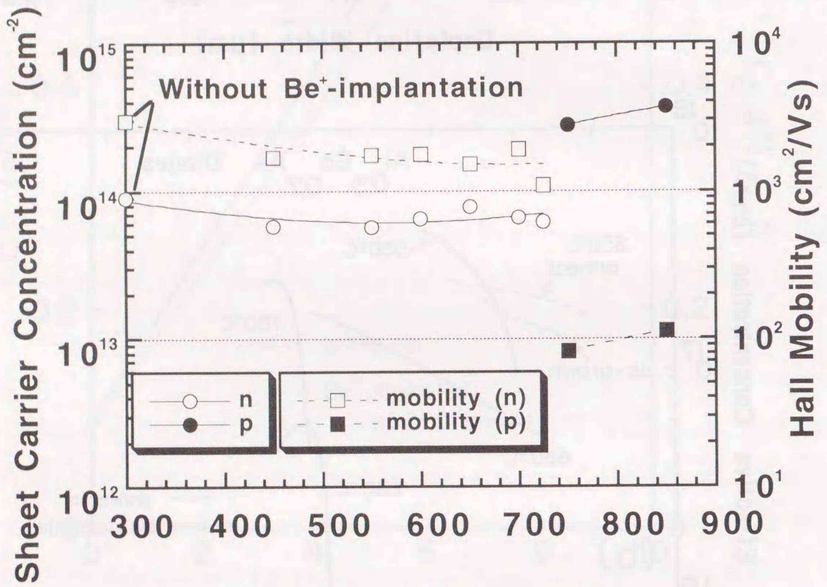


Fig. 4-10. Sheet carrier concentration and Hall mobility for the Be^+-implanted n-doped GaAs as a function of annealing temperatures.

undoped GaAs can be fully activated even for low-temperature annealing such as 450°C, and the activation fraction becomes saturated over 450°C annealing. There is significant discrepancy in the activation behaviors dependence on the annealing temperature of Be implants between the n-type and the undoped GaAs. This is because some interaction between Be and Si atoms may prevent activation process of Be implants which are located at the interstitial site in GaAs. This interaction may be dissociated only at high temperature annealing. The critical annealing temperature at which the conduction type exchanges from n to p is dependent on the n-type dopant background level and the Be doses. In connection with this matter, M. D. Deal and H. G. Robinson [8] point out that diffusion of Be implants in Si-doped substrates is much less than in the case of undoped substrates.

For the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ p-n junctions, the profiles change significantly with the annealing temperature. A fully depleted layer about 0.45 μm thick can be observed at annealing temperatures below 750°C. However, the existence of such a layer does not deteriorate the quality (ideality factor) of the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ junctions, as seen in the case of 650°C and 750°C in Fig. 4-4. After annealing at 850°C, the profile is graded on the semilog-plot, similar to those of the GaAs diodes shown in Fig. 4-9(a). The $Al_{0.3}Ga_{0.7}As$ diode annealed at higher temperature (950°C) indicates that N_{eff} increases considerably but a fully depleted layer can be observed in the profile. The $Al_{0.3}Ga_{0.7}As$ grown-in junctions also have an abrupt junction before and after RTA at 850°C.

4-3-3. Breakdown voltage behavior

Figure 4-11 shows the reverse I-V characteristics of the Be^+-implanted GaAs and the $Al_{0.3}Ga_{0.7}As$ p-n junctions annealed at 850°C. The $Al_{0.3}Ga_{0.7}As$ junction shows smaller leakage current than the GaAs junction. The breakdown voltages obtained for the GaAs and the $Al_{0.3}Ga_{0.7}As$ junctions are 10 and 16 V, respectively.

The annealing temperature dependence of the breakdown voltages is also investigated for the Be^+-implanted diodes. The results are shown in Fig. 4-12. For the GaAs diodes, the breakdown voltage is nearly constant at annealing temperatures up to 850°C and gradually decreases above this

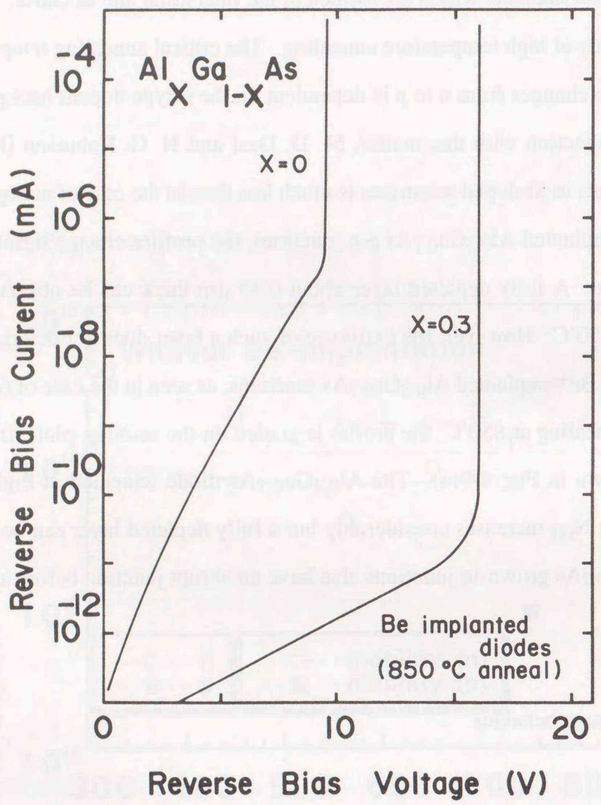


Fig. 4-11. The reverse I-V characteristics of the Be+-implanted p-n junctions.

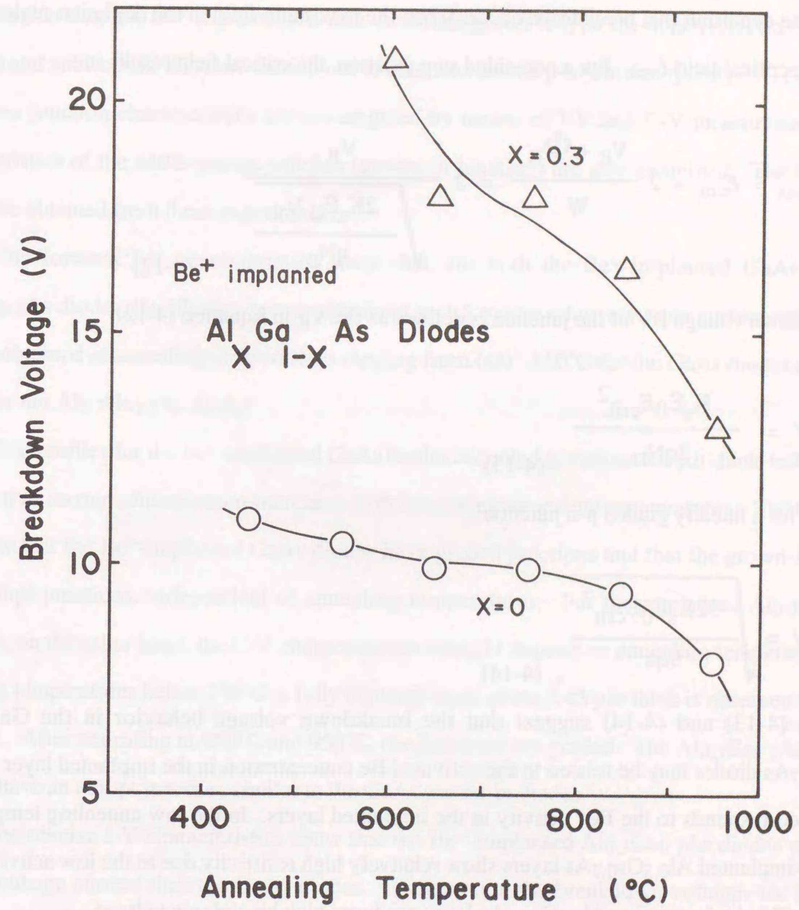


Fig. 4-12. The breakdown voltage versus the annealing temperatures for the Be+-implanted $Al_xGa_{1-x}As$ diodes.

temperature. The breakdown voltage for the $Al_{0.3}Ga_{0.7}As$ diodes, on the other hand, strongly depends on annealing temperatures.

According to the avalanche breakdown process, the breakdown voltage of p-n junctions is based on the condition that breakdown occurs when the maximum field in the depletion region E_{max} reaches the critical field E_{crit}. For a one-sided step junction, the critical field results in

$$E_{max} = E_{crit} = 2\frac{V_R + \Phi_B}{W} = 2\frac{V_R}{\sqrt{\frac{2K_S\varepsilon_0 V_R}{qN_D}}} \quad . \quad (4\text{-}12)$$

The breakdown voltage BV of the junction is defined as the V_R in Equation (4-12)

$$BV = \frac{K_S\varepsilon_0 E_{crit}^2}{2qN_D} \quad . \quad (4\text{-}13)$$

Similarly, for a linearly graded p-n junction

$$BV = \sqrt{\frac{32K_S\varepsilon_0 E_{crit}^3}{9qa}} \quad . \quad (4\text{-}14)$$

Formulas (4-13) and (4-14) suggest that the breakdown voltage behavior in the GaAs and $Al_{0.3}Ga_{0.7}As$ diodes may be related to the activated Be concentration in the implanted layer. In this case, N_D corresponds to the Be^+ activity in the implanted layers. In the low annealing temperature case, Be^+-implanted $Al_{0.3}Ga_{0.7}As$ layers show relatively high resistivity due to the low activity of Be implants. This high-resistive $Al_{0.3}Ga_{0.7}As$ layer produces high breakdown voltage.

As seen in Fig. 4-5, the $Al_{0.3}Ga_{0.7}As$ grown-in diodes show an abrupt breakdown, while the GaAs diodes show a relatively soft breakdown. It is also found that the breakdown voltages of the grown-in junctions do not change before and after RTA at 850°C. Moreover, the breakdown voltage of the grown-in junction is found to be lower than that of the Be^+-implanted junction. This corresponds to the fact that the effective acceptor concentration in the p-type layer of the grown-in junction is higher than that of the Be^+-implanted junction as shown in Fig. 4-1. These data are the first experimental results for the Be^+-implanted $Al_xGa_{1-x}As$ diodes.

4-4. Conclusions

In this chapter, Be^+-implantation into the MBE-grown n-type (Si-doped) $Al_xGa_{1-x}As$ (x=0 and 0.3) and subsequent RTA are carried out to characterize the p-n junction quality. RTA behavior of the p-n junction characteristics are investigated by means of I-V and C-V measurements. The characteristics of the MBE-grown junction (grown-in junction) are also examined. The following results are obtained from these experiments.

The forward I-V characteristics show that, for both the Be^+-implanted GaAs and the $Al_{0.3}Ga_{0.7}As$ diodes, the ideality factors are about n=1.8 over a relatively wide current range. This value is obtained at annealing temperatures ranging from 600 - 850°C for the GaAs diodes and 650 - 950°C for the $Al_{0.3}Ga_{0.7}As$ diodes.

C-V profiles for the Be^+-implanted GaAs diodes annealed at various temperatures indicate that the effective carrier concentration increases with increasing annealing temperatures. The C-V data also show that the Be^+-implanted GaAs diodes have graded junctions and that the grown-in diodes have abrupt junctions, independent of annealing temperatures. For the implanted $Al_{0.3}Ga_{0.7}As$ junctions, on the other hand, the C-V characteristics strongly depend on annealing temperatures. At annealing temperatures below 750°C, a fully depleted layer about 0.45 μm thick is observed in the C-V profile. After annealing at 850°C and 950°C, the junctions are graded. The $Al_{0.3}Ga_{0.7}As$ grown-in diode have an abrupt junction, similar to the GaAs grown-in diodes.

The reverse I-V characteristics show that the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ diodes exhibited smaller leakage current than the GaAs diodes. Furthermore, the breakdown voltages for the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ diodes strongly depend on annealing temperature, in contrast to the GaAs ones. These breakdown behavior of the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ diode has close relation with the acceptor concentration in the p-type $Al_{0.3}Ga_{0.7}As$ layer.

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Chapter 5

Oxygen-ion implantation for applications to heterojunction bipolar transistors

5-1. Introduction

5-1-1. Application of ion implantations to heterojunction bipolar transistors

Chapters 2 and 3 mainly discuss the electrical properties of the Be^+-implanted $Al_xGa_{1-x}As$ layers activated by RTA. In particular, it is shown that the activation efficiency of Be implants in the $Al_{0.3}Ga_{0.7}As$ layer is significantly lower than that in the GaAs and that a remarkable redistribution of the Be atom occur in the $Al_{0.3}Ga_{0.7}As$ after high-temperature annealing [1]. However, it is pointed out that these disadvantages can be overcome through a dual implantation of dopant ions and complementary species (i. e., Be^+/P^+ or Be^+/As^+) [2]. In the case of especially Be^+/P^+ dual implants, apparent hole concentration is shown to become nearly twice that of Be implant. In addition, the dual implantations can suppress redistribution of Be atoms.

Chapter 4 discuss the quality of p-n junctions in the GaAs and $Al_{0.3}Ga_{0.7}As$ fabricated by Be^+-implantation. Anneals at 600 - 850°C for the GaAs diodes and 650 - 900°C for the $Al_{0.3}Ga_{0.7}As$ ones are shown to lead to the lowest ideality factor values (about n=1.8). This indicates that the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ diodes are almost identical in quality to the GaAs diodes after 650°C annealing [3].

In this chapter, applications of ion-implantations to active devices using AlGaAs/GaAs heterostructures are described. As mentioned in Chapter 1, HBT is known to be a high-speed device that well utilizes the features of heterostructures [4]. For the past ten years, HBTs have been used to build devices with excellent high-frequency performance [5-11]. Although the advantages of HBTs were first recognized by Shockley in 1948, they could not be produced until the early 1970s when MBE became advanced enough to provide good control of layer thickness and composition. The typical III-V compound HBT has a vertical structure in the intrinsic transistor area because each layer for the emitter, base and collector is epitaxially grown in turn by MBE or metalorganic chemical vapor deposition (MOCVD) on the semi-insulated substrate. A cross-sectional view of the structure of a

typical AlGaAs/GaAs HBT is schematically illustrated in Fig. 5-1. This HBT has the emitter-up (E-up) configuration where the emitter layer is the top layer.

The advantage of using AlGaAs/GaAs heterojunctions instead of GaAs homojunctions in the emitter/base is higher injection efficiency [12, 13]. A representative band diagram for an n-p-n HBT with a wide-bandgap emitter and an abrupt emitter/base junction is illustrated in Fig. 5-2. The bandgap of the emitter is larger than that of the base material and the conduction- and valence-band offsets reduce the injection of the base majority carriers (holes) into the emitter. The current gain h_{FE} is given by

$$h_{FE} = \frac{n_E v_e N_{CB} N_{VB}}{p_B v_h N_{CE} N_{VE}} \exp [\triangle Eg / kT] \qquad (5\text{-}1)$$

where n_E is the electron concentration of emitter, v_e is electron velocity, N_{CB} and N_{CE} are the densities of states in the conduction band for the base and emitter, p_B is the base hole concentration, v_h is the hole velocity, and N_{VB} and N_{VE} are the densities of states in the valence band for the base and emitter. ΔE_g is the difference in the bandgap between emitter and base. When ΔE_g is greater than 250 meV (10kT), h_{FE} can be improved on the order of 10^4 over the homojunction case.

The base layer can be more heavily doped than the emitter while keeping high current gain. Compared with conventional homojunction bipolar transistors, HBTs have a very low base resistance, leading to superior high-speed circuit performance.

5-1-2. Advantage of the collector-up heterojunction bipolar transistor

In general, p-type dopant ions are implanted into the extrinsic base layer of AlGaAs/GaAs HBTs to reduce the base resistance [14]. For this purpose, Be^+-implantation has been widely used because Be^+ is the lightest dopant. However, recent progress in epitaxial growth technologies has made it possible to attain doping level over the middle of $1x10^{19}$ cm^{-3} for p-type dopants such as C in the GaAs or $Al_xGa_{1-x}As$ base layer [15, 16]. In addition, recently it has been shown that Zn-diffusion by the open-tube method is effective to enhance hole concentration in the extrinsic GaAs

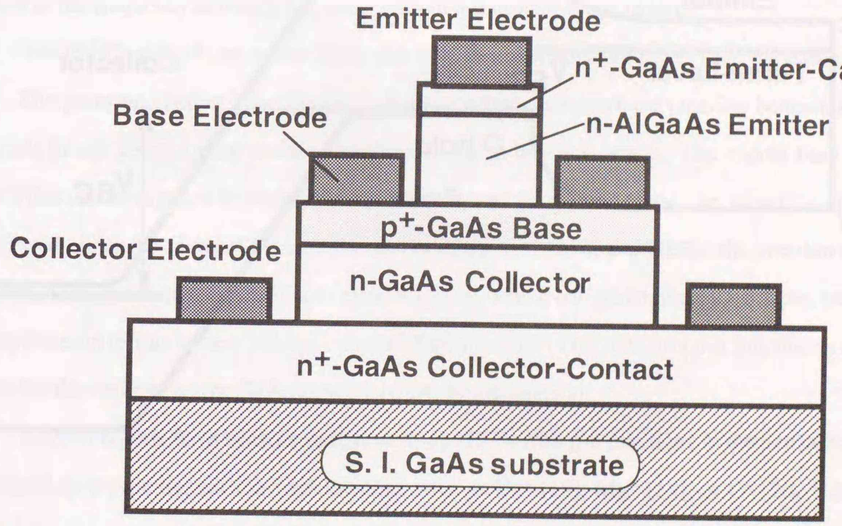


Fig.5-1. The schematic structure of a typical AlGaAs/GaAs HBT.

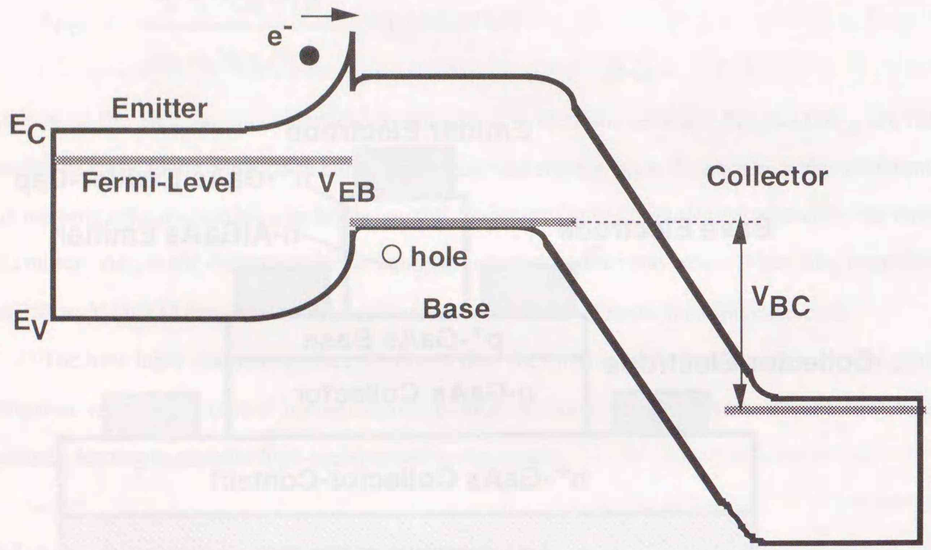


Fig. 5-2. A representative band diagram for an n-p-n HBT with a wide-bandgap emitter and an abrupt emitter/base junction.

base layer [17]. So, the Be^+-implantation in the extrinsic base layer and the subsequent high-temperature annealing are not needed to reduce base resistance.

As mentioned in Chapter 1, the new application of Be^+-implantations is the fabrication of C-up configuration in HBTs. Ion-implantations are useful for the creation of a barrier region that can suppress the excess current injection at the extrinsic emitter/base region for C-up HBTs [18]. The structure of the C-up AlGaAs/GaAs HBT is schematically illustrated in Fig. 5-3. With the C-up, or "inverted" HBT structure, there is no need for the extrinsic base/collector junction area beneath the base electrode. To draw upon the inherent abilities of HBTs, a C-up configuration is very attractive because its base/collector capacitance C_{BC} is lower than that of an E-up configuration where the parasitic capacitance beneath the base electrode is relatively large [13]. This characteristic of the C-up HBT is advantageous in increasing power gain and the maximum oscillation frequency f_{max}. f_{max} is defined as the frequency at which the power gain of a transistor drops to unity.

For the C-up HBT, an emitter/base junction area is absolutely larger than the base/collector area. The parasitic current injection through the extrinsic emitter/base junction beneath the base electrode brings about a drop in the current gain even at low bias levels. The excess base leakage current that can be injected from the emitter electrode into the extrinsic base one, therefore, should be suppressed under the forward bias condition. In AlGaAs/GaAs n-p-n HBTs, the creation of a p-n junction in the extrinsic n-type AlGaAs emitter region, which has wider energy bandgap, enables to the suppression of this excess leakage current. The potential of the AlGaAs p-n junction provides a barrier for the intrinsic p-type GaAs/n-type AlGaAs heterojunction.

Several reports have been presented on C-up HBTs with p-n junctions in the extrinsic emitter fabricated by p-type dopant ion-implantations such as Be^+ [18], Mg^+ [19], or C^+ [20, 21]. High-frequency characteristics of a cutoff frequency f_T of 18 GHz and f_{max} of 15 GHz for the Mg^+/P^+ dual-implanted C-up HBT [19] and f_T of 23 GHz and f_{max} of 54 GHz for a C^+/F^+ dual-implanted one [20] have been reported. However, in C-up HBTs with p-n junctions in the extrinsic emitter fabricated by ion-implantations, the current gain rapidly drops when collector current density (J_C) is beyond around $1x10^4$ A/cm^2 [20]. This is because the excess leakage current begins to flow into the extrinsic emitter p-n junctions under the high forward-bias condition that should give high J_C. The schematic band-diagram of a p-n junction fabricated by ion-implantation in the extrinsic $Al_xGa_{1-x}As$

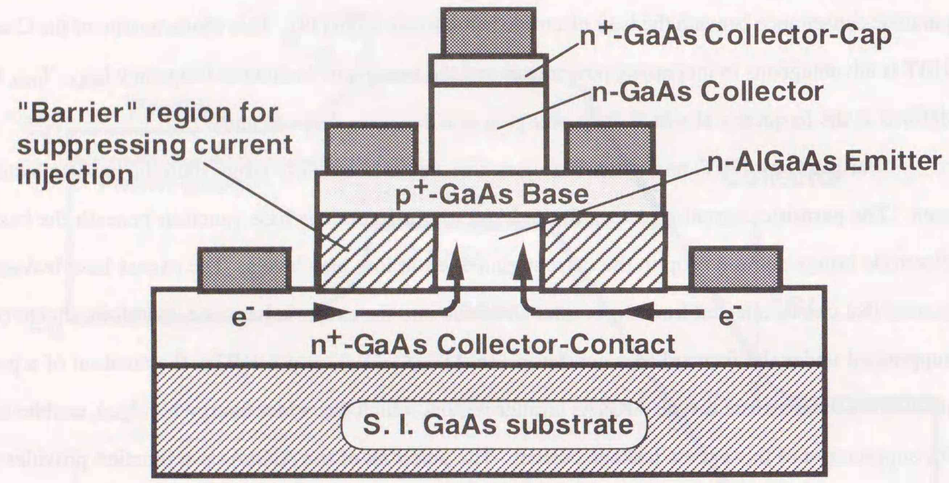


Fig. 5-3. The schematic structure of the collector-up AlGaAs/GaAs HBT.

emitter layer is shown in the Fig. 5-4. It can be seen that recombination current components are dominant in the Be^+-implanted $Al_xGa_{1-x}As$ p-n junctions, compared with the grown-in junction made by epitaxial growth, as mentioned in Chapter 4. Therefore, the formation of a p-n junction in the extrinsic emitter fabricated by ion-implantation is not sufficient to suppress the excess current from being injected from the emitter electrode into the extrinsic base one.

5-1-3. Oxygen-ion implantation for creating a high-resistive barrier layer

Another new method of suppressing injection current is the formation of a high-resistive layer in the extrinsic $Al_xGa_{1-x}As$ emitter layer. The schematic band-diagram of a high-resistive $Al_xGa_{1-x}As$ layer in the extrinsic emitter is shown in the Fig. 5-5. This high-resistive layer forms a "barrier" that suppresses carrier injections even under high the forward-bias condition. The barrier effect for the sufficient high-resistivity in the AlGaAs layer should be much better than the p-n junction barrier.

A high-resistive AlGaAs layer can be easily created by inactive ion-implantations of H^+, B^+, or Ar^+ [22]. The radiation damage induced during these ion-implantations can convert n-type AlGaAs layers into highly resistive ones. Yet, at the same time, these inactive species deteriorate device performance. Moreover, these implantations are carried out through the extrinsic GaAs base layer, so the resistivity of the GaAs base layer also increases due to the radiation damage [23].

Any p-type dopant incorporation into the inactive ion-implanted extrinsic GaAs layer will enhance hole concentration. For this purpose, Zn-diffusion is used to reduce the base resistance which is increased by ion-implantations of inactive atoms. Zn-diffusion is extremely effective for achieving doping in higher concentrations on the GaAs surface compared with other p-type dopants [17]. However, Zn-diffusion is accompanied by high-temperature processing, that recovers the high-resistive AlGaAs regions by the ion-implantation damage to an n-type conductivity.

Only O^+-implantation can overcome this problem. The O^+-implanted high-resistive AlGaAs layers are more thermally stable due to the creation of oxygen-related deep levels [24]. The use of O^+-implantation produces a high-resistive barrier in the extrinsic AlGaAs layer that suppresses current injection even for the high-temperature processing during Zn-diffusion.

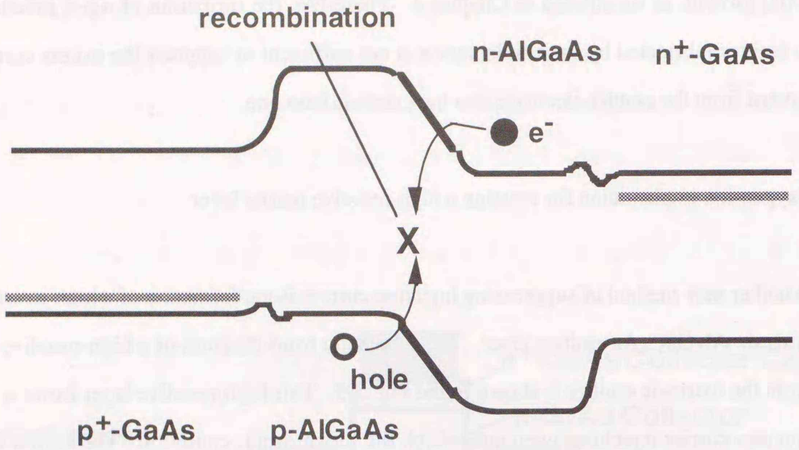


Fig. 5-4. The schematic band-diagram for a p-n junction fabricated by ion implantation in the extrinsic $Al_xGa_{1-x}As$ emitter layer.

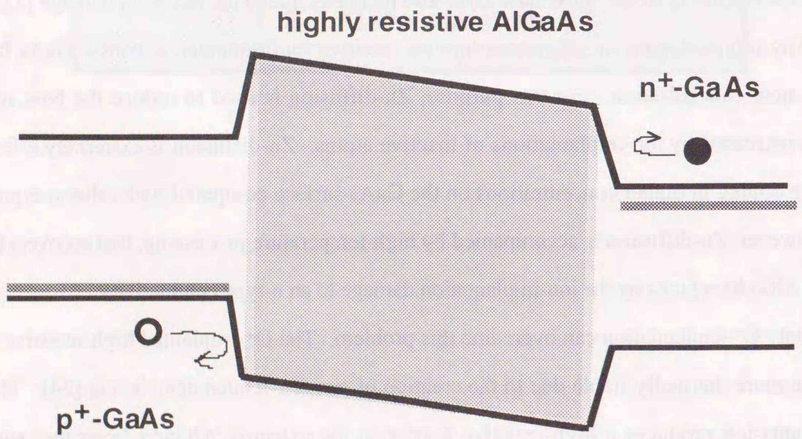


Fig. 5-5. The schematic band-diagram for a high-resistive $Al_xGa_{1-x}As$ layer in the extrinsic

In this chapter, aiming at the application of the C-up HBT fabrication, the electrical properties of O^+-implanted AlGaAs/GaAs heterostructures are described in terms of the creation of high-resistive layers. Diode characteristics, corresponding to the extrinsic emitter/base of C-up HBTs dependence on the annealing temperature and the O^+-doses are examined. Next, the fabrication of C-up HBTs by the O^+-implantation is described. DC and RF characteristics of the C-up HBTs are then investigated as a function of O^+-doses. The optimum O^+-implantation conditions are discussed in relation to device performance.

5-2. Characteristics of oxygen-ion-implanted AlGaAs/GaAs diodes

5-2-1. Diodes fabrication process

Figure 5-6 is a schematic cross-sectional view of the structure of a AlGaAs/GaAs diodes. The epitaxial layers of the diodes are grown on semi-insulating GaAs substrate by MOCVD. The diode consists of four layers: a 50-nm-thick p-type C-doped GaAs layer ($p=3.8\times10^{19}$ cm^{-3}), an 150-nm-thick n-type Si-doped $Al_{0.3}Ga_{0.7}As$ layer ($n=3\times10^{17}$ cm^{-3}), an 150-nm-thick n-type Si-doped $Al_{0.3}Ga_{0.7}As$ layer ($n=3\times10^{18}$ cm^{-3}), and a 700-nm-thick n-type Si-doped GaAs layer ($n=2\times10^{18}$ cm^{-3}).

O^+ is implanted to two doses (3×10^{13} and 3×10^{14} cm^{-2}) at an acceleration energy of 100 keV. After RTAs ranging between 600°C and 900°C, Zn-diffusion is carried out at 550°C for 1 min using the open-tube method in an atmosphere of N_2. The p-n junction area is 20-μm square.

5-2-2. Oxygen-ion-implanted diodes characteristics

Figure 5-7 shows the forward current-density versus voltage (J-V) characteristics for diodes by the low-O^+ dose (3×10^{13} cm^{-2}) as a parameter of the annealing temperature. The J-V characteristics for the high-O^+ dose (3×10^{14} cm^{-2}) are shown in Fig. 5-8. The 550°C anneal in the figures is only the Zn-diffusion temperature without RTAs.

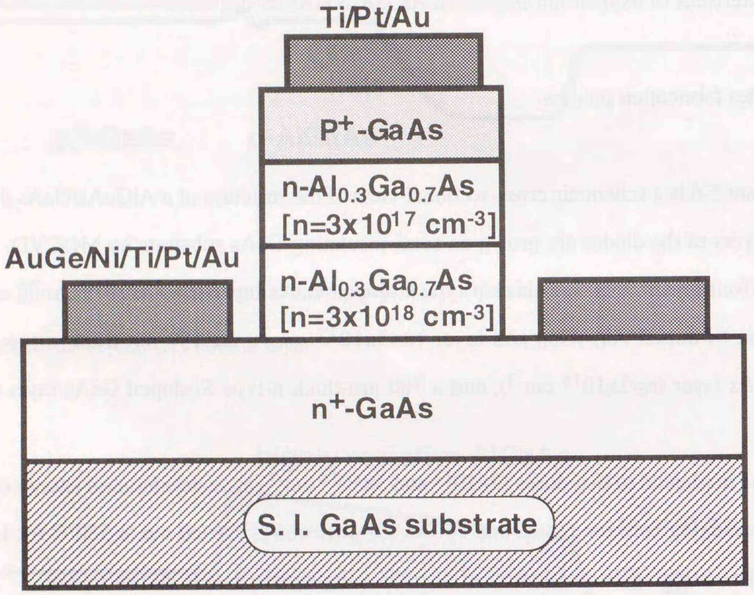


Fig. 5-6. The schematic structure of the AlGaAs/GaAs diode.

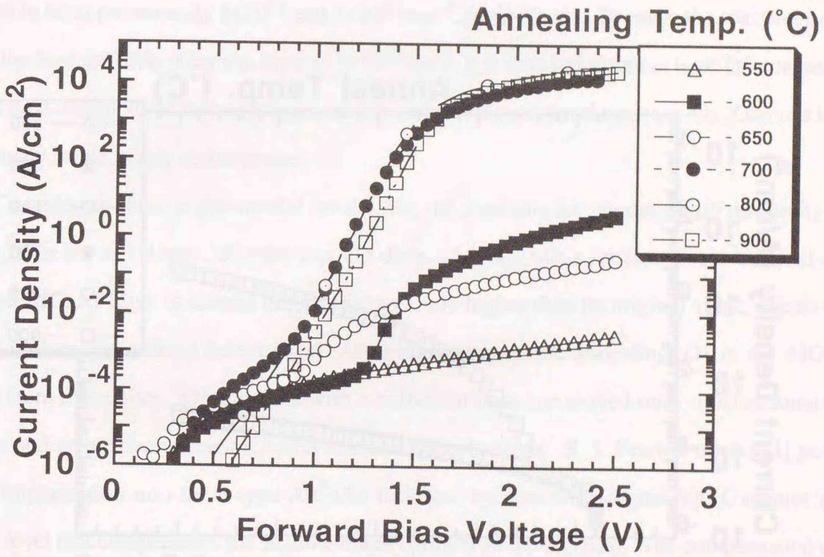


Fig. 5-7. The forward J-V characteristics for diodes with low-O^+-dose implantation ($3x10^{13}$ cm^{-2}) as a parameter of annealing temperature.

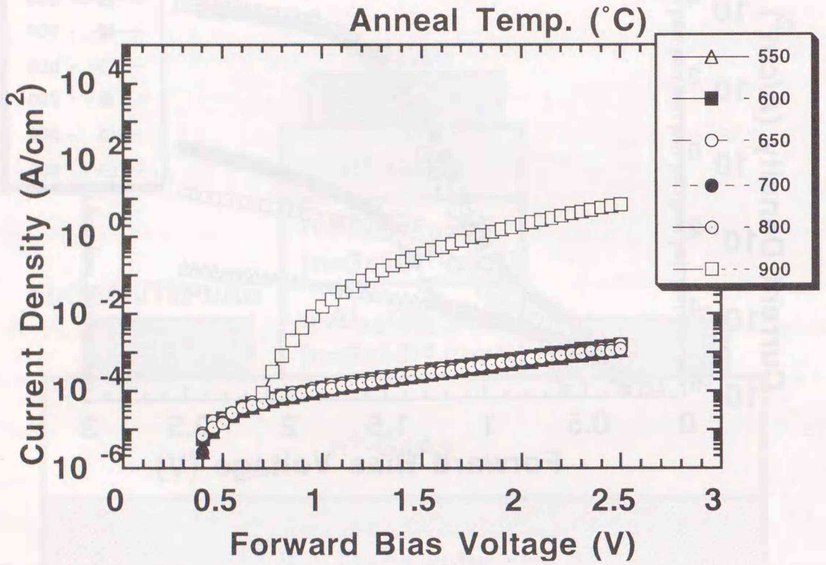


Fig. 5-8. The forward J-V characteristics for high O^+-dose implantation ($3x10^{14}$ cm^{-2}).

For the low ion doses, J-V characteristics show the high-resistivity up to 650°C, and they change to the p-n junction ones, resulting from the recovery of the high-resistivity due to the radiation damage, beyond 700°C. On the other hand, for the high ion doses, J-V characteristics keep the high-resistive one even at high temperature annealing. There is a slight recovery of the high-resistivity only above 900°C.

The peak concentration of the O^+-implantation profile for the low- and high-O^+-dose is estimated to be approximately $1x10^{18}$ and $1x10^{19}$ cm^{-3}, respectively. Because the maximum doping level of the Si-doped $Al_{0.3}Ga_{0.7}As$ layer is $3x10^{18}$ cm^{-3}, it is concluded that at least O^+-concentration excess n-type doping level in the background can completely convert the n-type $Al_{0.3}Ga_{0.7}As$ layer to the thermally stable highly-resistive one.

Considering these experimental results, the mechanisms for creating high resistivity in the AlGaAs layer are as follows. For the low O^+-dose, with any other species, a resistivity of the as-implanted AlGaAs layer is several orders of magnitude higher than its original value, due to carrier trapping at damage-induced defect sites. After high-temperature annealing, O^+ in the AlGaAs is released from those sites. O^+ implants with a sufficient dose are moved onto substitutional lattice positions and create deep acceptor levels that can trap electrons. S. J. Pearton et al. [24] point out that O^+-implantation into the n-type AlGaAs followed by annealing above 600°C creates a deep acceptor level that compensates the shallow donors present in the material. The compensation caused by ion-induced damage is stable only to 600°C, whereas the chemically induced compensation in O^+-implanted AlGaAs is stable above 950°C.

5-2-3. Nitrogen-ion-implanted diodes characteristics

It is found that high O^+ implants can create the thermally stable high-resistive layer of the $Al_{0.3}Ga_{0.7}As$ after high-temperature annealing. One question that should be addressed is: Is this true for other species ? For the comparison, N^+ is implanted into the same heterostructure to investigate the diode characteristics as a function of the annealing temperature. N^+ is selected because the mass of nitrogen (14) is very close to that of oxygen (16). The radiation damage from N^+-implantation is

on the same level as that from O^+-implantation. The comparison of the diode characteristics between N^+- and O^+-implantation also makes it possible to check compensation mechanisms.

The N^+ acceleration energy (90 keV) is chosen so that the R_p of O^+ ions coincides with that of N^+ ions. The N^+-implantation is carried out with $3x10^{14}$ cm^{-2}. Figure 5-9 shows the forward J-V characteristics of the N^+-implanted diodes annealed at 550 and 800°C. The J of the diode annealed at 550°C is two orders of magnitude higher than the O^+-implanted one, and, in contrast to the case with O^+-implantation, its high-resistivity recovers at 800°C. This tendency is obviously different from the O^+-implanted diode characteristics with the same dose. Thus, the main origin of the thermally stable high-resistivity with O^+-implantation is not radiation damage during implantation with high ion-doses, but rather a chemical effect, that is, O-related deep levels in the $Al_{0.3}Ga_{0.7}As$. These results strongly suggest that only O^+-implantation can provide the high-resistive barrier layer in the $Al_{0.3}Ga_{0.7}As$ whose characteristics are unchanged even with high-temperature processing such as Zn-diffusion.

5-3. Characteristics of the oxygen-ion-implanted collector-up HBTs

5-3-1. Device fabrication process

The C-up HBT wafers used are grown by MBE on semi-insulating GaAs. The layer structures are shown in Table 5-1. The HBT wafer has a C-doped $Al_xGa_{1-x}As$ graded base with a doping level of $2.5x10^{18}$ cm^{-3} and a thick $Al_{0.3}Ga_{0.7}As$ emitter layer (400 nm).

The fabrication process flow of a C-up HBT in a schematic cross-sectional view is shown in Fig. 5-10. First, reactive-ion etching is carried out using Cl_2/Ar mixed gas-plasma excited in an electron-cyclotron-resonance reactor to define the collector-mesas. The etching depth is controlled to leave an approximately 50-nm GaAs collector layer on the base layer. Here, plasma-enhanced CVD silicon-dioxide is used as an etching mask.

Then, after 0.2-μm thick silicon-nitride sidewalls are formed around the collector-mesa, O^+ is implanted along 7° off from the <100> axis at an ion acceleration energy of 100 keV. After the O^+-implantations, Zn-diffusion into the extrinsic base region is carried out at 550°C. The Zn-diffusion

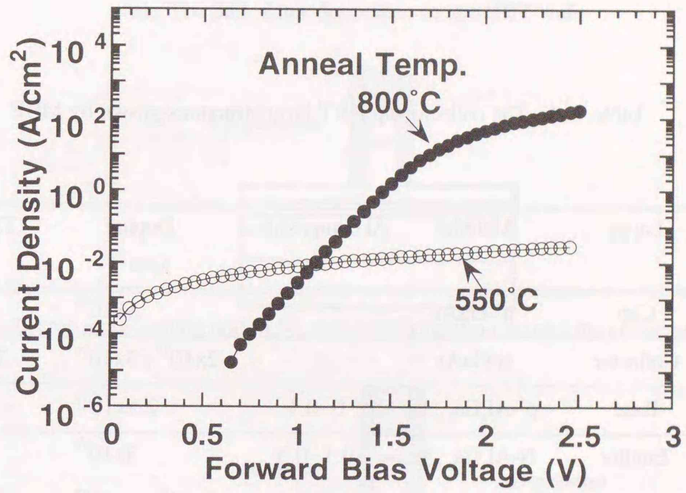
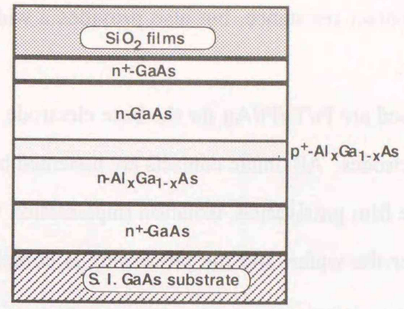


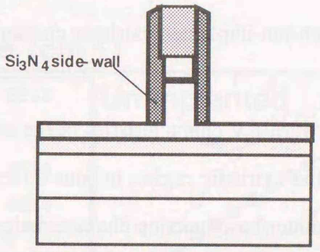
Fig. 5-9. The forward J-V characteristics of the N^+-implanted diodes annealed at 550 and 800℃.

Table. 5-1. The collector-up HBT layer structures grown by MBE.

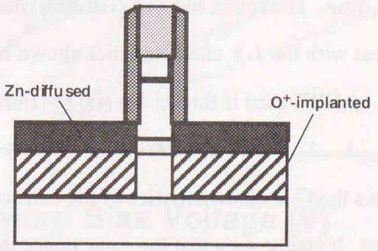
Layer	Material	Al composition x	Doping (cm^{-3})	Thickness (nm)
Cap	n^+-GaAs		$5x10^{18}$	100
Collector	n-GaAs		$2x10^{17}$ / $5x10^{16}$	200 / 300
Base	p^+-$Al_xGa_{1-x}As$	0 -0.1	$2.5x10^{18}$	80
Emitter	N-$Al_xGa_{1-x}As$	0.1 -0.3	$3x10^{17}$	30
	N-$Al_xGa_{1-x}As$	0.3	$3x10^{17}$ / $2x10^{18}$	170 / 170
	N-$Al_xGa_{1-x}As$	0.3 - 0	$2x10^{18}$	30
Emitter-Contact	n^+-GaAs		$5x10^{18}$	700



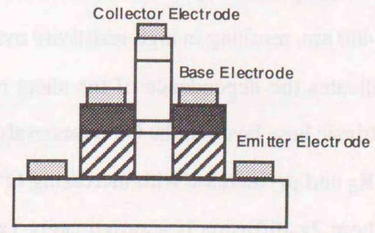
(a). The SiO_2 films deposition on the HBT wafer .



(b). The collector-mesa etching and Si_3N_4 side-wall formation around the collector-mesa region.



(c). The O^+ implantation into the extrinsic base/emitter region and Zn-diffusion into the extrinsic base layer.



(d). The non-selfaligned base, collector and emitter electrode formation after the base/emitter mesa etching.

Fig. 5-10. The fabrication process flow of a C-up HBT.

not only lowers the base contact resistance, but also provides a wide margin for the reactive-ion etching of the collector layer.

The ohmic metals used are Pt/Ti/Pt/Au for the base electrode and AuGe/Ni/Ti/Pt/Au for the emitter and the collector electrodes. All ohmic contacts are patterned by conventional non-selfaligned processing. Silicon-dioxide film passivation, isolation implantation with protons, and contact hole formation are performed for the wafer, and the processing is completed with Ti/Au interconnect metallization.

5-3-2. Characteristics of the oxygen-ion-implanted extrinsic emitter/base junctions

Figure 5-11 shows the forward J-V characteristics of the extrinsic emitter/base region in a C-up HBT. O^+ is implanted into the extrinsic region at four doses: $5x10^{13}$, $1.5x10^{14}$, $3x10^{14}$, and $4x10^{14}$ cm^{-2}. The unimplanted emitter/base junction characteristics are also plotted in the figure. It is obvious that the p-n junction characteristic of the O^+-implanted diode changes to the high-resistive one with increasing O^+-dose. However, the J-V characteristics of O^+-implantation of $3x10^{14}$ cm^{-2} are not in good agreement with the J-V characteristics shown in Fig. 5-7. This is because the emitter layer thickness of the C-up HBT used is thicker by 100 nm than the n-type AlGaAs layer of the diode structure in section 5-2.

Figure 5-12 shows the C-V characteristics of the extrinsic emitter/base diodes with a junction area of 300 μm x 300 μm. It can be seen that the capacitance decreases and the thickness of depletion layer becomes wider with increasing O^+-dose. This tendency agrees with the J-V characteristics shown in Fig. 5-11. The depletion layer thickness of the O^+-implanted diode with a dose of $1.5x10^{14}$ cm^{-2} reaches 400 nm, resulting in high-resistivity over the entire emitter layer.

Figure 5-13 indicates the dependence of the sheet resistance R_S and the specific contact resistivity ρ_C of the extrinsic base layer on the O^+-doses evaluated using the transmission line model (TLM) method. Both R_S and ρ_C increase with increasing O^+-dose, but the R_S of the O^+-implanted p-type GaAs layer without Zn-diffusion is approximately $1x10^5$ Ω/square. Zn-diffusion after O^+-implantation is, thus, obviously very effective in lowering the extrinsic base resistivity. The depth

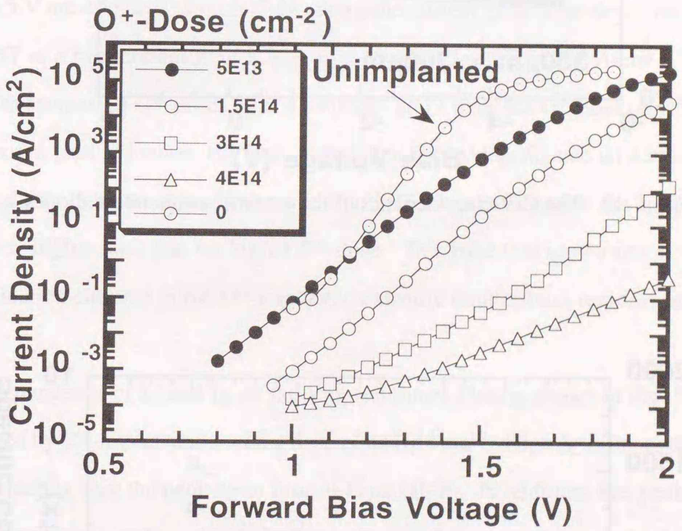


Fig. 5-11. The forward J-V characteristics of the extrinsic emitter/base region in the C-up HBT.

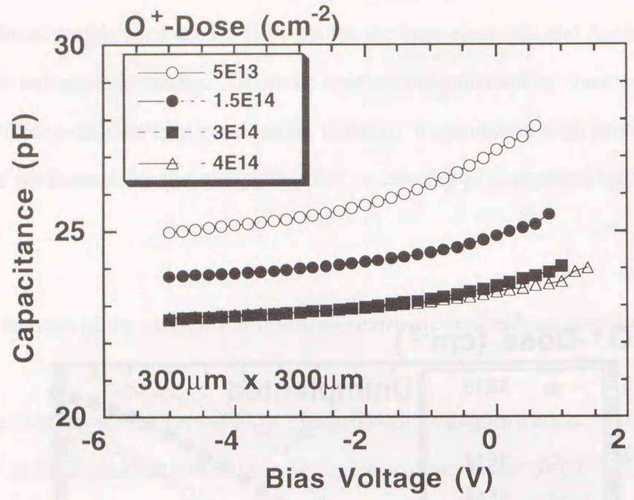


Fig. 5-12. The C-V characteristics of the extrinsic emitter/base diodes.

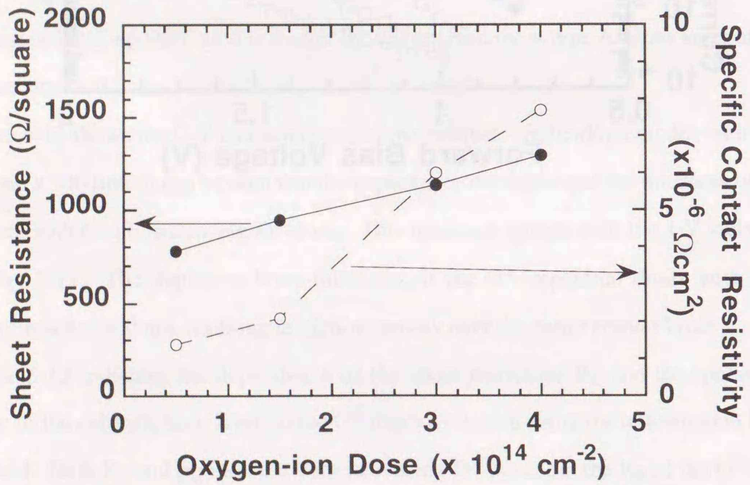


Fig. 5-13. The dependence of the sheet resistance and the specific contact resistivity of the extrinsic base layer on O^+ doses.

from the surface that Zn diffused into GaAs layers is estimated to be about 100 nm, so the diffused Zn dose not reach the AlGaAs emitter layer.

5-3-3. DC characteristics for the collector-up HBTs

The curve-tracer photograph in Fig. 5-14 shows the common-emitter collector I_C-V_{CE} characteristics of the C-up HBT with a 2-μm x 10-μm collector dimension fabricated by O^+-implantation with a dose of $3x10^{14}$ cm^{-2}. A maximum current gain of 12 and a breakdown voltage BV_{CEO} of 8.5 V are obtained. Figure 5-15 shows the current gain dependence on the O^+-doses for the C-up HBT at a bias condition of a V_{CE} of 1 V and a J_C of $2.5x10^4$ A/cm^2. The current gain increases with increasing O^+-doses, and it saturates at 12 over the O^+-dose of $1.5x10^{14}$ cm^{-2}. To check the current gain reduction, the base current density J_B dependence on a base-emitter voltage V_{BE} is plotted as a function of the O^+ dose in Fig. 5-16. It is evident that the J_B for the O^+-dose of $5x10^{13}$ cm^{-2} is higher than that for higher O^+-dose. This base leakage current seems to be due to base recombination currents in the O^+-implanted extrinsic emitter/base regions, as discussed in the session 5-2.

The dependence of J_C and J_B on the V_{BE} (Gummel-Plot) is shown in Fig. 5-17 for the C-up HBT fabricated by O^+-implantation with a dose of $4x10^{14}$ cm^{-2}. High J_C of more than $1x10^5$ A/cm^2 is attained, which is near the peak J_C of typical E-up HBTs. In addition, this peak J_C is five times higher than that of previous C-up HBTs [20, 21] fabricated using p-n junction formed in the extrinsic $Al_{0.3}Ga_{0.7}As$ emitter layer by ion implantations of p-type dopants. These results reveal that the high-resistive barrier layer created by O^+-implantation in the extrinsic $Al_{0.3}Ga_{0.7}As$ for the C-up HBT can effectively suppress the injection current from the emitter electrode into the extrinsic base region. That is to say, high-performance C-up HBTs can be obtained through the combination of the high-ion-dose O^+-implantation and Zn-diffusion into the extrinsic base region.

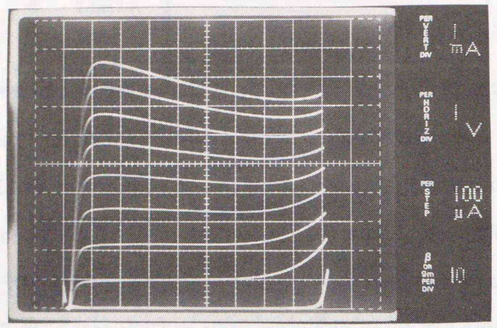


Fig. 5-14. The common-emitter collector I_C-V_{CE} characteristics of the C-up HBT with a 2-µm x 10-µm collector.

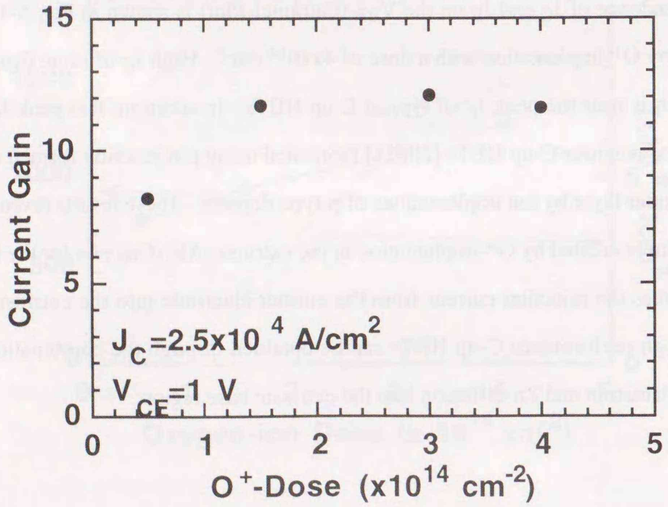


Fig. 5-15. The current gain dependence on O^+ doses for the C-up HBT.

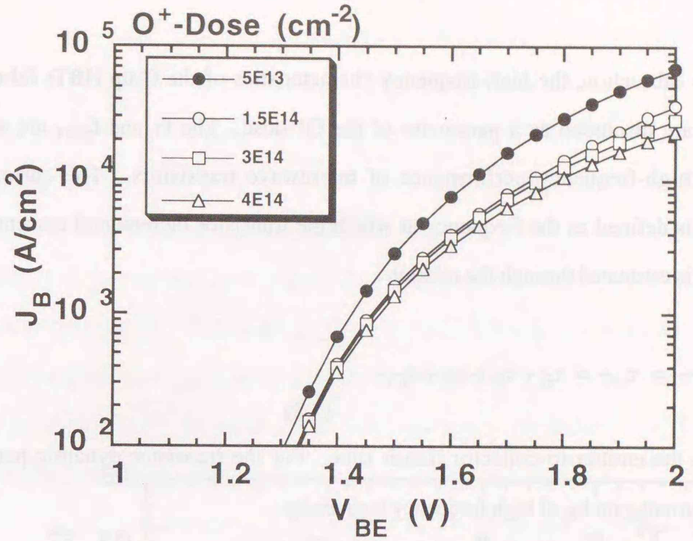


Fig. 5-16. J_B dependences on a base-emitter voltage V_{BE} plotted as a function of O^+ dose.

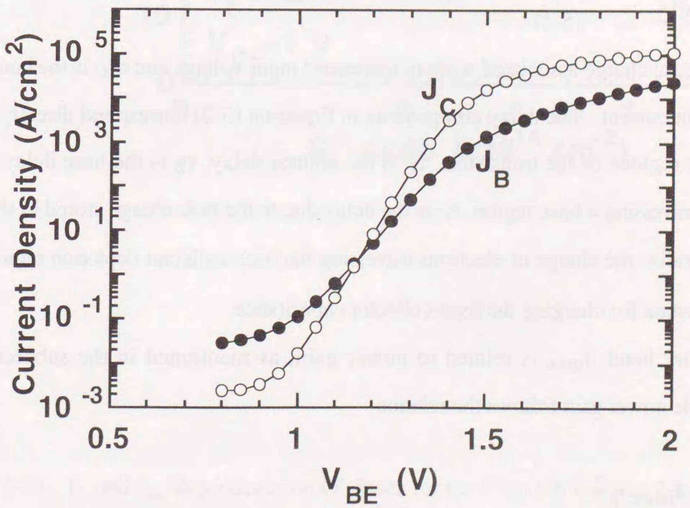


Fig. 5-17. The dependence of J_C and J_B on V_{BE}.

5-3-4. RF characteristics for the collector-up HBTs

In this subsection, the high-frequency characteristics of the C-up HBTs fabricated by O^+-implantation are discussed as a parameter of the O^+-dose. The f_T and f_{max} are widely used to evaluate the high-frequency performance of microwave transistors. The current-gain cutoff frequency f_T is defined as the frequency at which the transistor incremental current gain drops to unity. The f_T is estimated through the relation

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_B + \tau_C + \tau_{CC} \qquad (5\text{-}2)$$

where τ_{EC} is the emitter-to-collector transit time. For the transistor dynamic performance, the incremental current gain h_{fe} at high frequency is given by

$$h_{fe} = \left| \frac{dI_C}{dI_B} \right| = \left| \frac{dI_C}{dQ_B} \frac{1}{j\omega} \right| = \frac{f_T}{f} \qquad (5\text{-}3)$$

Then,

$$\tau_{EC} = \frac{dQ_B}{dI_C} . \qquad (5\text{-}4)$$

where dQ_B is the base charge associated with an increment input voltage and dI_C is the corresponding increment in output current. The delay components in Equation (5-2) correspond directly to charges stored in different regions of the transistor. τ_E is the emitter delay, τ_B is the base delay associated with the electron traversing a base region, τ_C is the delay due to the hole charge stored in the base that is required to neutralize the charge of electrons traversing the base-collector depletion region, and τ_{CC} is the RC time constant for charging the base-collector capacitance.

On the other hand, f_{max} is related to power gain, as mentioned in the subsection 5-3-1. Maximum available power gain follows the relation

$$G_p = \left[\frac{f_{max}}{f} \right]^2 . \qquad (5\text{-}5)$$

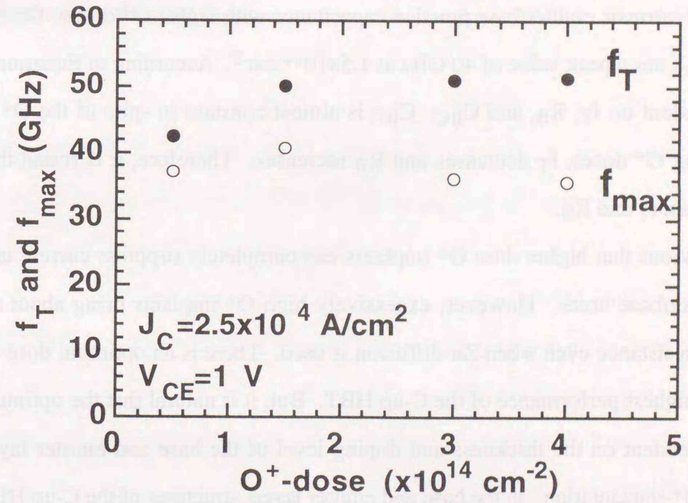


Fig. 5-18. f_T and f_{max} dependence on O^+ doses for the C-up HBT with a 2-μm x 10-μm collector.

For bipolar transistors a convenient approximate expression for f_{max} is

$$f_{max} = \left[\frac{f_T}{8\pi R_B C_{BC}}\right]^{1/2} \qquad (5\text{-}6)$$

where R_B is the parasitic base resistance.

In this study, f_T and f_{max} are characterized by extrapolation of current gain $|h_{21}|^2$ and Mason's unilateral gain using S-parameters measured on a wafer from 0.5 to 50 GHz. Figure 5-18 exhibits f_T and f_{max} dependence on the O^+ dose for the C-up HBT with the 2-μm x 10-μm collector dimension. f_T increases with increasing the O^+ dose, and it reaches to a constant value of 50 GHz over $1.5\text{x}10^{14}$ cm^{-2}. This is due to the emitter charging time reduction. This time reduction is attributed to a decrease in the extrinsic emitter/base junction capacitance with higher O^+ doses. On the other hand, the plotted f_{max}s has a peak value of 40 GHz at $1.5\text{x}10^{14}$ cm^{-2}. According to Equation (5-6), f_{max} is strongly dependent on f_T, R_B, and C_{BC}. C_{BC} is almost constant in spite of the O^+ dose change. With increasing O^+ doses, f_T decreases and R_B increases. Therefore, it is found that f_{max} is the trade-off between f_T and R_B.

It is obvious that higher dose O^+ implants can completely suppress current injection in the extrinsic emitter/base areas. However, excessively high O^+ implants bring about an increase in extrinsic base resistance even when Zn-diffusion is used. There is an optimum dose of O^+ implant that gives the highest performance of the C-up HBT. But, it is natural that the optimum dose of O^+ implant is dependent on the thickness and doping level of the base and emitter layers which are implanted by O^+-implantation. In the base and emitter layers structures of the C-up HBT used in this experiment, the O^+ dose of $1.5\text{x}10^{14}$ cm^{-2} is found to be optimum for high-frequency characteristics (f_T and f_{max}).

5-4. Conclusions

In this chapter, the electrical properties of O^+-implanted AlGaAs/GaAs heterostructures are investigated for the purpose of application to the C-up HBT. AlGaAs/GaAs diode characteristics, corresponding to the extrinsic emitter/base of the C-up HBT, are fabricated and examined by means

of I-V and C-V measurements as parameters of the annealing temperature and the O^+ dose. It is clarified that only high-dose O^+ implants can create a thermally stable highly-resistive layer, which is a result of chemical-effect compensation due to the O-related deep levels in the AlGaAs.

For the fabrication of C-up HBTs, non-self-aligned process is used. The extrinsic emitter/base region of the C-up HBT is fabricated by combination of O^+-implantation and Zn-diffusion. DC and RF characteristics of the C-up HBT are also investigated as a function of the O^+ dose. It is obvious that the high-resistive barrier layer created by O^+-implantation in the extrinsic $Al_{0.3}Ga_{0.7}As$ for the C-up HBT can effectively suppress injection current from the emitter electrode into the extrinsic base region. This thermally stable high-resistive barrier layer provides good current gain in the C-up HBT. In addition, it is found that there is an optimum dose of O^+-implant that provides the highest values of f_T and f_{max}.

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Chapter 6

High-performance small scale collector-up AlGaAs/GaAs heterojunction bipolar transistors

6-1. Introduction

In Chapter 5, it is clearly shown that the O^+-implantation is effective in giving the n-type $Al_xGa_{1-x}As$ layer thermally stable high-resistivity, resulting from the compensation effect for n-type conductivity due to the O-related deep level. The O^+-implantation into the $Al_xGa_{1-x}As$ layer leads to its successful application to the AlGaAs/GaAs C-up HBTs [1 -3].

This chapter describes high-performance small-scale AlGaAs/GaAs C-up HBT's with a heavily C-doped base layer fabricated using combination of O^+-implantation and Zn-diffusion. The use of a C-doped base is especially effective for small-scale C-up HBTs, compared with conventional base dopants such as Be and Zn, because it suppresses the undesirable turn-on voltage shift between emitter and base. This shift is induced by base dopant diffusion in the intrinsic area around the collector-mesa perimeter during the high-temperature Zn-diffusion process after implantation.

Recently, interest has also been focused on scaling down the lateral dimensions of HBTs to improve high-frequency characteristics and to reduce power dissipation in integrated circuits. Although small scale E-up HBTs have been successfully fabricated using a variety of self-aligned structures [4, 5], their high-frequency characteristics, f_T and f_{max}, have not been adequately obtained. The reason for this is that the reduction of C_{BC} relative to the emitter dimensions is essentially limited by the E-up configuration. In contrast, C_{BC} for the C-up configuration is approximately in proportion to its collector dimensions since the parasitic C_{BC} corresponding to the extrinsic base area can be neglected [6]. Therefore, the C-up configuration is very attractive when both ultra-high-speed and low-power dissipation are needed in digital integrated-circuit applications [7].

The advantage of the C-up HBT over the E-up HBT is simply estimated using a self-aligned square HBT structure whose emitter (for E-up) or collector (for C-up) is surrounded by an extrinsic

base region as shown in Fig. 6-1. As described in Chapter 5, f_{max} is an important parameter to evaluate the high-frequency characteristics of high-speed transistors. As shown in Equation (5-6), f_{max} is related to f_T, R_B and C_{BC}, and only C_{BC} is strongly dependent on the configuration of HBT. When one emitter or collector length (width) is W μm and an extrinsic base length (width) is 1 μm, C_{BC} is expressed as

$$C_{BC}\,(\text{E-up}) = (W+2)^2 \times c_{BCi} + 4(W+2) \times c_{BCL}. \quad (6\text{-}1)$$

$$C_{BC}\,(\text{C-up}) = W^2 \times c_{BCi} + 4W \times c_{BCL}. \quad (6\text{-}2)$$

where c_{BCi} is the intrinsic capacitance per unit area and c_{BCL} is the periphery capacitance component per unit length. R_B is approximated

$$R_B \cong (R_S \times \rho_C)^{1/2} / 4W. \quad (6\text{-}3)$$

According to Equation (5-6), intrinsic f_{max}s for an E-up-HBT and a C-up HBT are approximately calculated as a function of W. The results are shown in Fig. 6-1 using typical parameters of f_T=80 GHz, c_{BCi}=0.4 fF/μm^2, c_{BCL}=0.1 fF/μm, R_S=500 Ω/square and ρ_C=1x10^{-6} Ωcm^2. It is clearly found that the intrinsic f_{max}s for the C-up HBT are increasing significantly with the reduction in W. In particular, the f_{max} can exceed 200 GHz under a 2-μm collector dimension. On the other hand, an increment of the intrinsic f_{max}s for the E-up HBT with the reduction in W is very small because the parasitic C_{BC} cannot be reduced even in emitter dimensions reduction.

For E-up HBTs, one serious problem in laterally scaling down HBTs is the current gain reduction caused by surface recombination in the extrinsic base region [8]. It is also possible that a similar problem occurs in the C-up HBTs. Despite the importance of current gain in scaling down transistors, detailed studies of the C-up HBTs have not been done. In this chapter, current gain dependence on collector dimensions is investigated for C-up HBTs, and it is found that the base recombination current around the collector-mesa perimeter is responsible for a current gain reduction.

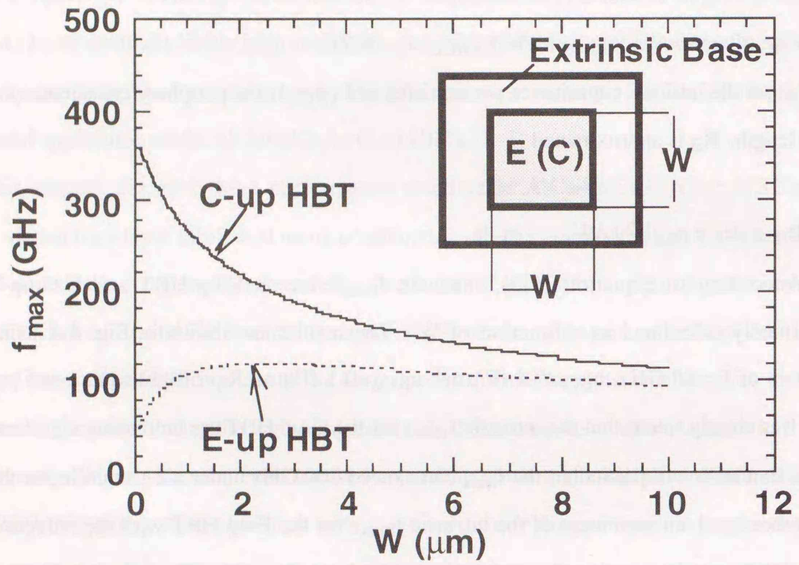

Fig. 6-1. Comparison of f_{max} between self-aligned collector-up and emitter-up HBTs as a function of an emitter or collector length W.

6-2. Device fabrication process

The layer structure of the C-up HBT grown by low-pressure MOCVD is outlined in Table 6-1. For comparison of current gain dependence on collector size, another C-up structure with an $Al_xGa_{1-x}As$ (x=0.1~0) graded base grown by MBE is used. This wafer is identified to the HBT wafer used in Chapter 5. Both HBT structures are grown using C as the base dopant, but the doping level of the graded base layer ($2.5x10^{18}$ cm^{-3}) is about one order of magnitude lower than that of the uniform one. The $Al_xGa_{1-x}As$ graded base layer thickness is 80 nm. An emitter grading is introduced on both sides of the $Al_{0.3}Ga_{0.7}As$ emitter layer. Devices are fabricated using a process similar to that described in Chapter 5. All ohmic electrodes are patterned by non-self-aligned processing.

6-3. DC characteristics

6-3-1. Characteristics of oxygen-ion-implanted AlGaAs/GaAs emitter/base junctions

Figure 6-2 shows typical common-emitter I-V characteristics for the C-up HBT with a 2-μm x 10-μm collector. The maximum current gain is 20 at a collector current density J_C of $3x10^4$ A/cm^2. Gummel-plots, that is, J_C and J_B as a function of V_{BE} are shown in Fig. 6-3 for the same device. A conspicuous decrease in current gain is not observed, even at a J_C greater than $1x10^5$ A/cm^2. This indicates as mentioned in Chapter 5 that the injection current through the extrinsic emitter/base junction is kept negligibly low, even at a high V_{BE}. The characteristics of the extrinsic emitter/base diodes can give more direct information.

Figure 6-4 shows I-V curves for 6-μm x 6-μm diodes corresponding to the O^+-implanted extrinsic and intrinsic (unimplanted) AlGaAs/GaAs emitter/base junctions. A schematic cross-sectional view of the diodes is also shown in the figure. The I-V relationship of the O^+-implanted diode indicates the presence of the high-resistive barrier layer in the heterojunction. At a bias voltage of 1.5 V, for example, the forward current is on the order of $1x10^{-4}$ A/cm^2, resulting in a current density more than eight orders of magnitude lower than the intrinsic emitter/base junction. The

Table. 6-1. The C-up epitaxial layer structures grown by MOCVD.

Layer	Material	Al composition x	Doping (cm^{-3})	Thickness (nm)
Cap	n^+-GaAs		$5x10^{18}$	150
Collector	un-GaAs		undoped	250
Base	p^+-GaAs		$2x10^{19}$	50
Emitter	n-$Al_xGa_{1-x}As$	0 -0.3	$3x10^{17}$	20
	n-$Al_xGa_{1-x}As$	0.3	$3x10^{17}$	150
	n-$Al_xGa_{1-x}As$	0.3 - 0	$3x10^{17}$ - $2x10^{18}$	30
Emitter-Contact	n^+-GaAs		$5x10^{18}$	700

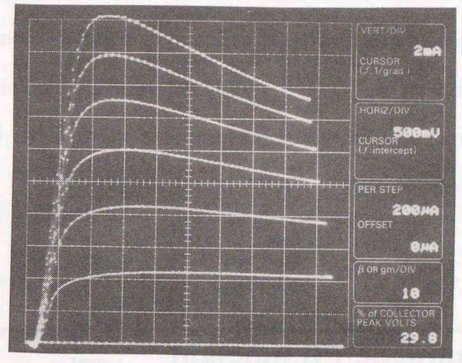

Fig. 6-2. The common-emitter I-V characteristics for a C-up HBT with a 2 μm x 10 μm collector.

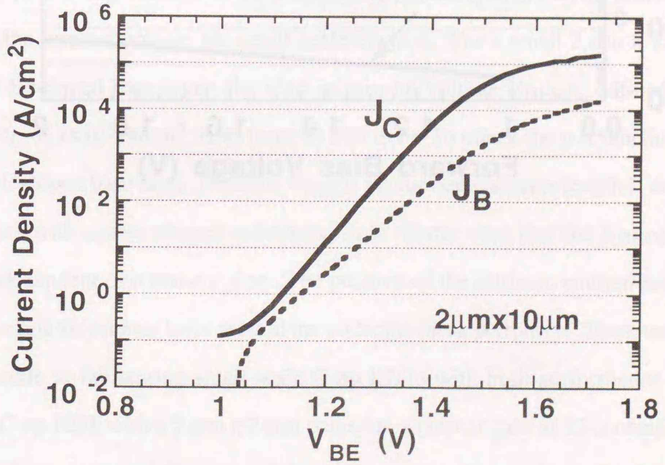

Fig. 6-3. The Gummel-plots for a C-up HBT with a 2-μm x 10-μm collector.

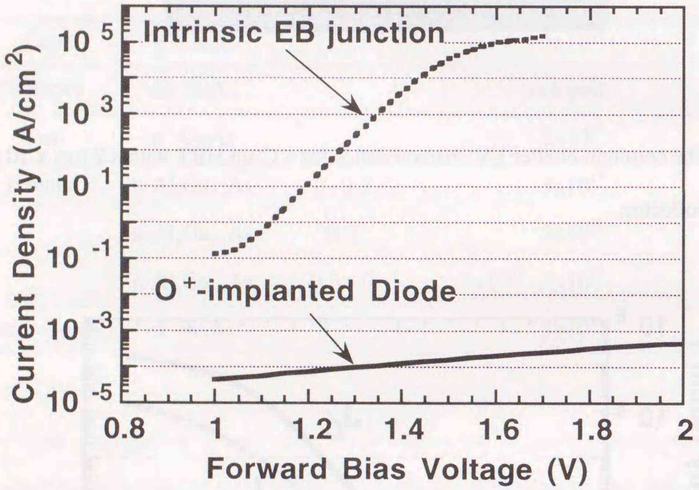

Fig. 6-4. The I-V characteristics of diodes corresponding to the extrinsic AlGaAs/GaAs emitter/base junctions and the intrinsic emitter/base junctions.

barrier layer was also characterized by C-V measurements. Figure 6-5 shows the behavior of diode capacitance versus bias voltage for O^+-implanted and unimplanted emitter/base junctions with 300-μm x 300-μm dimensions. The capacitance of the O^+-implanted diode is found to be much lower than that of the unimplanted diode, and almost independent of the bias voltage. The capacitance for the extrinsic O^+-implanted emitter/base junction is estimated to be approximately two orders lower than that of the intrinsic one at a bias voltage of 1.5 V. These results confirm that the undesirable parasitic effects associated with the external emitter/base junction are well suppressed by the O^+-implantation.

6-3-2. Current gain dependence on collector dimensions

Prior to discussions about current gain dependence on collector dimensions, we should take notice of current gain reductions due to the turn-on voltage shift induced by base dopant diffusion in the intrinsic area. In the case of C-up HBTs with a Be-doped base layer fabricated by ion-implantation into the extrinsic emitter/base junction, the position of the intrinsic p-n junction shifted toward the emitter layer around the collector-mesa periphery during implantation and high-temperature processing because of the undesirable diffusion of Be. This shift causes a prominent increase in the turn-on voltage for small scale devices. For a small 2-μm x 2-μm collector C-up HBTs with Be-doped base layer, the shift in turn-on voltage V_{BEON}, defined as the V_{BE} which produces a J_C of $1x10^3$ A/cm^2, is as large as 250 mV. To check the p-n junction shift for the C-up HBTs with C-doped base layer, plots for V_{BEON} versus one collector length L are shown in Fig. 6-6 for transistors with square-shaped collectors. It is clearly seen that the V_{BEON} values are almost constant, independent of transistor size. The position of the intrinsic emitter/base p-n junction dose not move toward the emitter layer around the collector-mesa periphery. Thus, use of a C-doped base is indispensable to fabricating small-scale C-up HBTs with high performance. In fact, even in a small-scale C-up HBT with a 2-μm x 2-μm collector, a current gain of 15 is obtained.

In order to examine current gain dependence on collector size in the fabricated C-up HBTs with C-doped base layer and to specify the origin of the excess base current, the base current I_B is divided into two components, as is done for E-up HBTs; that is,

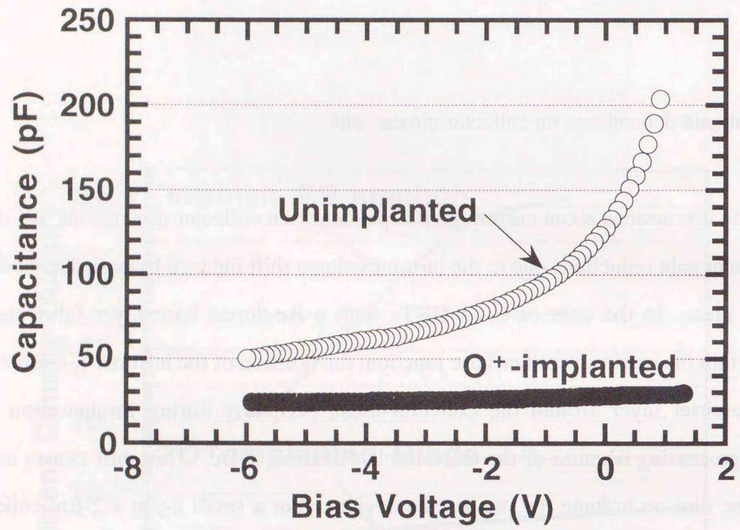

Fig. 6-5. The behaviors of capacitance versus bias voltage for 300-μm x 300-μm O^+-implanted emitter/base junctions and unimplanted ones.

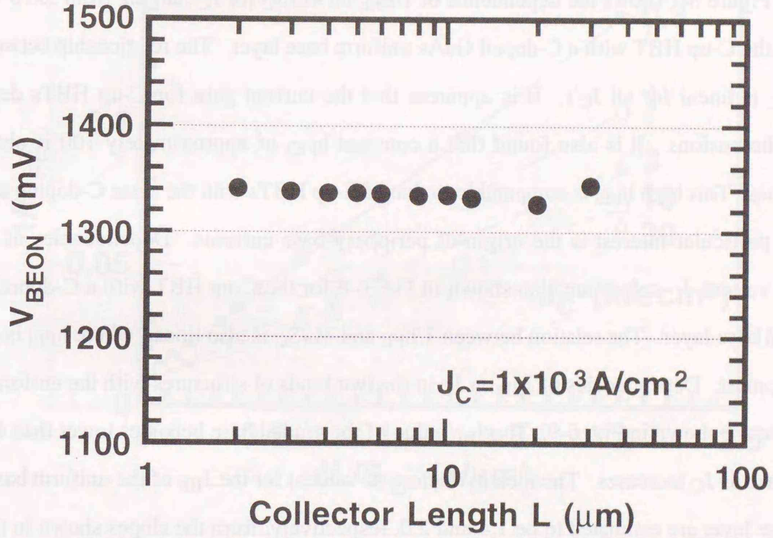

Fig. 6-6. Turn-on voltage, V_{BEON} (emitter/base voltage at J_C of $1x10^3$ A/cm^2) versus one collector length L for square C-up HBTs.

$$I_B = J_{Bi} \times S_C + J_{BP} \times 4L. \quad (6\text{-}4)$$

where J_{Bi} is the intrinsic base current density, S_C (= L x L) is the collector-mesa area, and J_{BP} is the periphery base current around the collector-mesa per unit length. Using Equation (6-4), the reciprocal of h_{FE} is written as

$$1/h_{FE} = 1/h_{FEi} + (J_{BP}/J_C) \times (4L/S_C). \quad (6\text{-}5)$$

where h_{FEi} is the intrinsic current gain. When J_C is constant, the excess base current is proportional to $4L/S_C$. Figure 6-7 shows the dependence of $1/h_{FE}$ on $4L/S_C$ for J_C ranging from 3×10^2 to 3×10^4 A/cm^2 for the C-up HBT with a C-doped GaAs uniform base layer. The relationship between $1/h_{FE}$ and $4L/S_C$ is linear for all J_C's. It is apparent that the current gain for C-up HBTs depends on collector dimensions. It is also found that a constant h_{FEi} of approximately 100 is obtained by extrapolation. This high h_{FEi} is comparable to that of E-up HBTs with the same C-doping level.

Of particular interest is the origin of periphery base currents. Dependencies of $1/h_{FE}$ on $4L/S_C$ for various J_C values are also shown in Fig. 6-8 for the C-up HBT with a C-doped $Al_xGa_{1-x}As$ graded base layer. The relation between $1/h_{FE}$ and $4L/S_C$ is also linear, where h_{FEi} is estimated to be 14 at most. Dependencies of J_{BP} on J_C in the two kinds of structures with the uniform and the graded base are shown in Fig. 6-9. The J_{BP} value of the graded base becomes lower than that of the uniform base as J_C increases. The ideality factors (n-values) for the J_{BP} of the uniform base and the graded base layer are estimated to be 1.4 and 2.0, respectively, from the slopes shown in the figure, where n-values for J_C obtained from the Gummel-plots are 1.1 for both structures. The n-value of 2.0 in the graded base C-up HBT indicates that the periphery base current is dominated by a generation-recombination current at the edge of O^+-implanted emitter areas.

On the other hand, the n-value of 1.4 in the uniform base C-up HBT implies that J_{BP} is dominated by other recombination current components which show an n-value near unity besides a recombination current at the edge of O^+-implanted emitter areas. The recombination current with the O^+-implantation is almost the same level as the case of the C-up HBT with an $Al_xGa_{1-x}As$ graded base layer. Thus, the increment of J_{BP} in the uniform base compared with the graded base is responsible for other current components. Other sources for J_{BP} can be recombination carriers generated in the interface between the neutral base and extrinsic one, and/or in the surface extrinsic

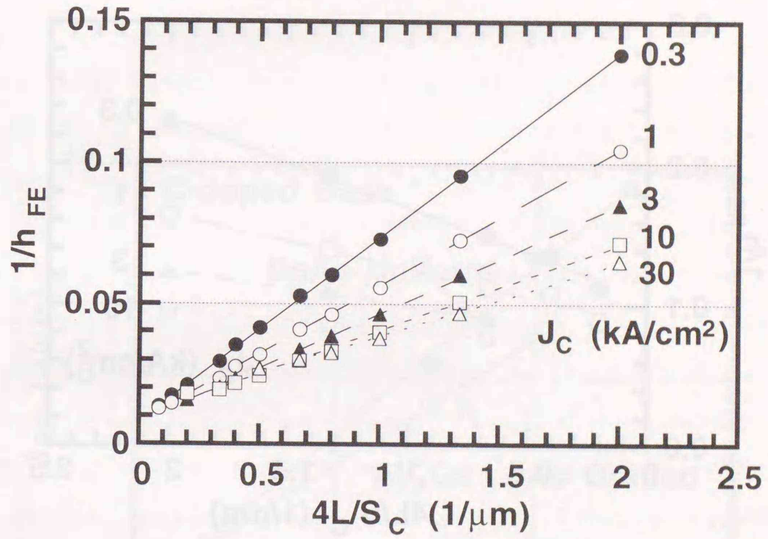

Fig. 6-7. The reciprocal of h_{FE} versus $4L/S_C$, the ratio of the total periphery 4L to collector-mesa area S_C, as a function of J_C for square C-up HBTs with a unifrom GaAs base.

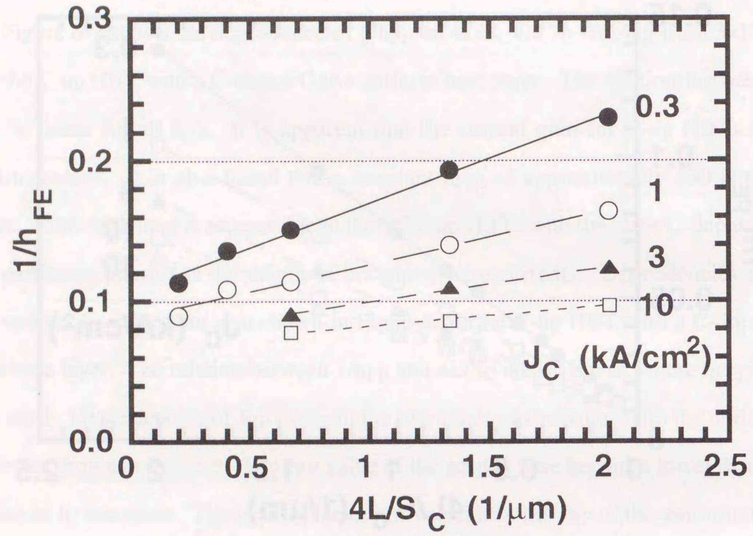

Fig. 6-8. The reciprocal of h_{FE} versus $4L/S_C$, the ratio of the total periphery 4L to collector-mesa area S_C, as a function of J_C for square C-up HBTs with a graded $Al_xGa_{1-x}As$ base.

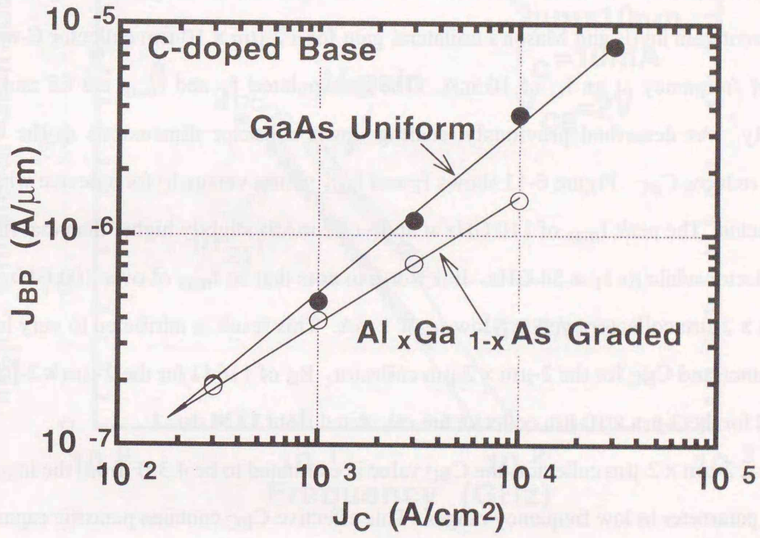

Fig. 6-9. Comparison for periphery base current unit length J_{BP} dependence on J_C for C-up HBTs with a uniform GaAs and graded $Al_xGa_{1-x}As$ base layers.

base area. The use of the graded base can reduce these significant recombination currents due to carriers moving across the neutral base region because carriers accelerated by the quasi-electric field in the graded base layer are more efficiently collected without lateral diffusion in the base. Therefore, a C-up HBT with a high-quality C-doped $Al_xGa_{1-x}As$ graded base layer will enable further improvement of h_{FE} in small scale C-up HBTs.

6-4. RF characteristics

Fabricated microwave C-up HBTs with a uniform base layer are characterized by S-parameters measured on a wafer from 0.5 to 50 GHz, as shown in Chapter 5. Figure 6-10 shows typical current gain $|h_{21}|^2$ and Mason's unilateral gain for a 2-μm x 10-μm collector C-up HBT as a function of frequency at an I_C of 10 mA. The extrapolated f_T and f_{max} are 68 and 102 GHz, respectively. As described previously, scaling down collector dimensions in the C-up HBT efficiently reduces C_{BC}. Figure 6-11 shows f_T and f_{max} values versus I_C for a device with a 2-μm x 2-μm collector. The peak f_{max} of 110 GHz at an I_C of 2 mA is slightly higher than that for a 2-μm x 10-μm collector while its f_T is 54 GHz. It is worth to note that an f_{max} of over 100 GHz is obtained for a 2-μm x 2-μm collector even at a low I_C of 1 mA. This result is attributed to very low product base resistance and C_{BC} for the 2-μm x 2-μm collector. R_B of 116 Ω for the 2-μm x 2-μm collector and 38.6 Ω for the 2-μm x 10-μm collector are calculated from TLM data.

For a 2-μm x 2-μm collector, the C_{BC} value is estimated to be 4.3 fF from the imaginary part of the Y_{12} parameter in low frequency ranges. This effective C_{BC} contains parasitic capacitance and is divided into three components as

$$C_{BC} = C_{BCP} + c_{BCi} \times S_C + c_{BCL} \times L_T. \qquad (6\text{-}3)$$

where C_{BCP} is the parasitic capacitance between wirings and L_T (μm) is the total periphery length around the collector-mesa area. C-V measurements for large base/collector junctions (100 μm x 100 μm) revealed a c_{BCi} of 0.42 fF/μm^2. Using this c_{BCi} value, C_{BCP} and c_{BCL} are obtained by plotting "$C_{BC} - c_{BCi} \times S_C$" versus L_T for various microwave transistors with different collector sizes as shown in Fig. 6-12. As a result, C_{BC} is expressed as "2.2 + 0.42 x S_C + 0.06 x L_T (fF)" for the

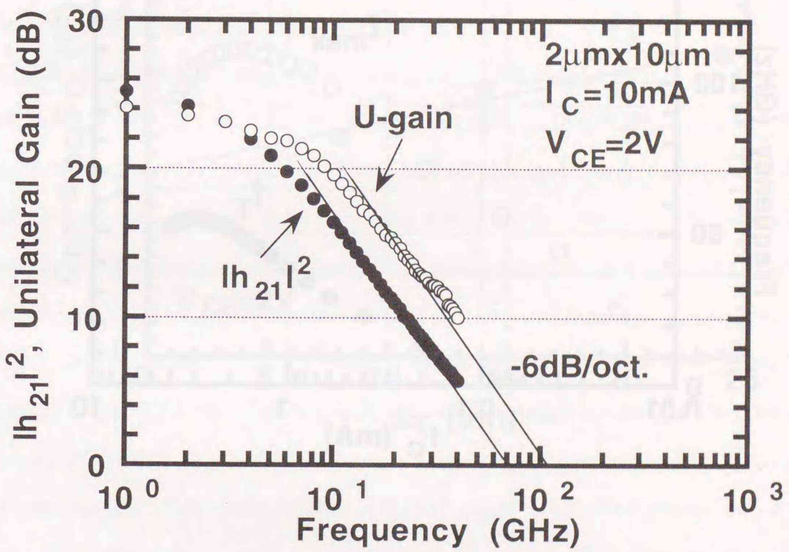

Fig. 6-10. The current gain $|h_{21}|^2$ and unilateral gain as a function of frequency for a microwave transistor with a 2-μm x 10-μm collector.

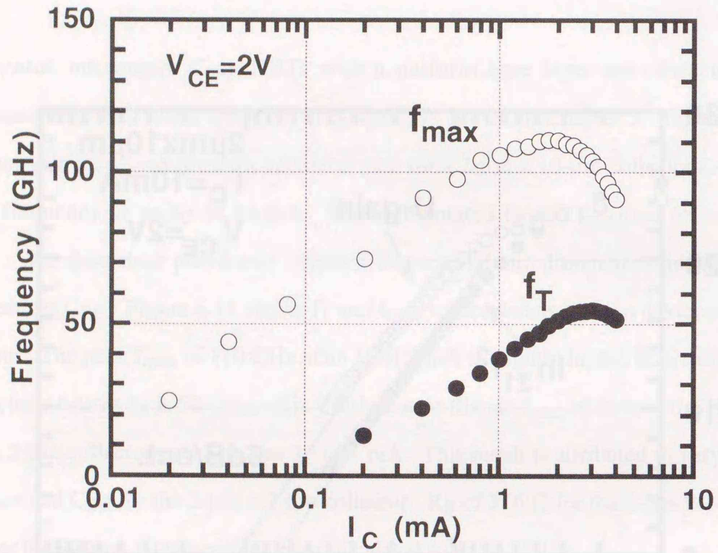

Fig. 6-11. f_T and f_{max} as a function of I_C for C-up HBTs with a 2-μm x 2-μm collector.

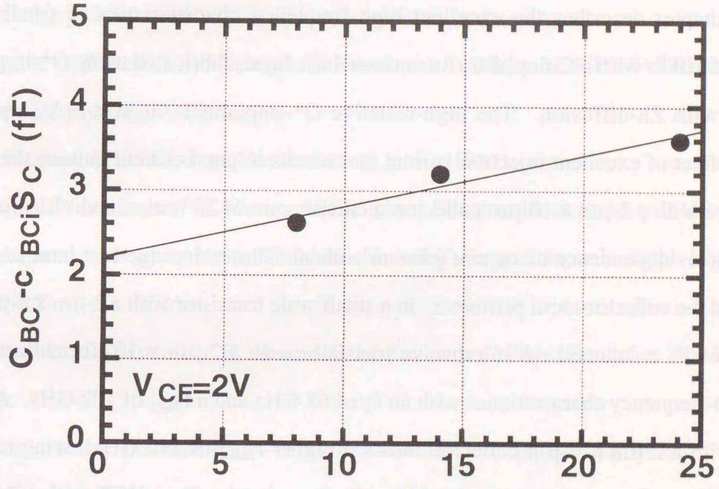

Fig. 6-12. "C_{BC} - c_{BCi} x S_C", vs. L_T for microwave transistors with different sized collectors (2 μm x 2 μm, 2 μm x 5 μm, 2 μm x 10 μm)

present C-up HBT with a 0.25 μm-thick undoped GaAs collector. Therefore, the actual C_{BC} corresponding to "C_{BC} - C_{BCP}" for a C-up HBT with a 2-μm x 2-μm collector is estimated to be as low as 2.2 fF. This value is extremely low compared to E-up HBTs with the same transistor dimension.

6-5. Conclusions

This chapter describes the excellent high-frequency characteristics of small scale C-up AlGaAs/GaAs HBTs with a C-doped GaAs uniform base layer, fabricated using O^+-implantation in combination with Zn-diffusion. The high-resistive O^+-implanted $Al_{0.3}Ga_{0.7}As$ layer provides suppression effect of excellent injection current and results in good current gain of the C-up HBT. For a transistor with a 2-μm x 10-μm collector, a current gain of 20 is obtained. It is found that the C-up HBT shows dependence of current gain on collector dimension due to a base recombination current around the collector-mesa perimeter. In a small scale transistor with a 2-μm x 2-μm collector, current gain of 15 is attained. A microwave transistor with a 2-μm x 10-μm collector achieves excellent high-frequency characteristics with an f_T of 68 GHz and a f_{max} of 102 GHz. A small scale C-up HBT with a 2-μm x 2-μm collector shows a higher f_{max} of 110 GHz owing to the further reduction of C_{BC}. It is also demonstrated that the f_{max} for the C-up HBT with a 2-μm x 2-μm collector is over 100 GHz even at a low I_C of 1 mA. The current gain dependence on collector dimension is also investigated for a C-up HBT with the $Al_xGa_{1-x}As$ graded base layer, and the base recombination current around the collector-mesa perimeter is shown to decrease in the case of the $Al_xGa_{1-x}As$ graded base layer.

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Chapter 7

Summary of this study

The first half of this chapter deals with the electrical properties of the Be-ion-implanted $Al_xGa_{1-x}As$ or AlGaAs/GaAs heterostructures. The rapid thermal annealing (RTA) behavior of the Be^+-implanted $Al_xGa_{1-x}As$ ($0 \le x \le 0.3$) is studied by measuring the Hall-effect, by measuring photoluminescence (PL) intensity, and by secondary ion mass spectrometry (SIMS). The dual ion combinations of Be^+/P^+ and Be^+/As^+ are implanted into the $Al_{0.3}Ga_{0.7}As$ to improve the electrical activity of the Be^+-implants. Then, Be^+ is implanted into the MBE-grown n-type $Al_xGa_{1-x}As$ (x=0, 0.3) and subsequent RTA is carried out to evaluate p-n junction quality. The RTA behavior of the p-n junction is investigated by measuring current-voltage (I-V) and capacitance-voltage (C-V), compared with that of the MBE-grown junction (grown-in junction).

The second half of the chapter deals with O^+-implantation into AlGaAs/GaAs heterostructures and its application to the C-up HBT. O^+-implantations are used to form high-resistive barrier regions in the extrinsic $Al_xGa_{1-x}As$ emitter layers to suppress an excess injection current between the emitter contact region and the extrinsic base layer. Lastly, the excellent high frequency characteristics of small scale C-up AlGaAs/GaAs HBTs with a C-doped GaAs uniform base layer, fabricated by using O^+-implantation in combination with Zn-diffusion, are demonstrated. The following results are obtained from experiments:

I. Be-ion-implantation into $Al_xGa_{1-x}As$

(a) The electrical activity of Be implants in the GaAs occurs at annealing temperatures starting from 400°C and saturates at approximately 450°C. On the other hand, the activity of Be in the $Al_xGa_{1-x}As$ increases gradually with increases in the annealing temperature, but these values are apparently lower than those in the GaAs. Moreover, larger Al composition x give smaller activation fractions at any fixed temperature. It is obvious that the lower activity of Be implants in the $Al_xGa_{1-x}As$ is mainly ascribed to the significant out-diffusion of Be after high temperature annealing.

(b) RTA of Be implants produces higher electrical activity than conventional furnace annealing. This is true for both GaAs and $Al_xGa_{1-x}As$.

(c) The PL intensities in the Be^+-implanted GaAs and $Al_xGa_{1-x}As$ indicate that optical activity starts from 400°C and increases gradually with further increases in the annealing temperature, showing a peak at 900°C. Thus, a considerable amount of radiation damage, which deteriorates the PL intensity, may still be presented at annealing temperatures lower than 900°C.

(d) The atomic Be depth profiles in the $Al_xGa_{1-x}As$ before RTA correspond to theoretical Gaussian distribution predicted from the LSS calculations. A slight change in the Be distribution can be found in the GaAs after RTA. On the other hand, RTA brings about significant Be in-diffusion in the $Al_xGa_{1-x}As$, resulting in plateau-like depth profiles. Another pronounced annealing effect inferred from the SIMS analysis is the accumulation of Be at the $Al_xGa_{1-x}As/SiO_2$ encapsulant interfaces. This leads to a large fraction of Be piling up at the interface by out-diffusion during RTA and can be observed both in GaAs and $Al_xGa_{1-x}As$.

(e) The electrical activity profiles of Be implants in the GaAs and $Al_xGa_{1-x}As$ are found to coincide well with the SIMS Be profiles. Annealing-induced changes in the electrical properties are also found in the undoped $Al_xGa_{1-x}As$ wafers grown by MBE. These changes lead to the conversion of unimplanted, high-receptive $Al_xGa_{1-x}As$ layers into low-resistivity, p-type layers.

II. Dual implantations into $Al_xGa_{1-x}As$

(a) Dual implantation techniques are used to enhance the electrical activity of Be implants in the $Al_xGa_{1-x}As$ layers. The dual implantation of Be^+/P^+ or Be^+/As^+ in the $Al_{0.3}Ga_{0.7}As$ significantly enhances the electrical activity of Be implants.

(b) The lower electrical activity in the Be^+-implanted $Al_{0.3}Ga_{0.7}As$ layer is mainly due to the out-diffusion of the Be atoms from the semiconductor surface during annealing. The technique also leads to a less significant redistribution of the Be atoms in the $Al_xGa_{1-x}As$, possibly because of an interstitial diffusion process that is strengthened by the stoichiometric imbalance created by the implantation process. Added complementary species, P^+ or As^+ ions (group III elements), play an

essential role in the reduction of As vacancies in the ion-implanted $Al_{0.3}Ga_{0.7}As$ layers, resulting in a less significant redistribution of the Be atoms with considerably high electrical activity.

III. Electrical properties of Be^+-implanted $Al_xGa_{1-x}As$ p-n junctions

(a) The forward I-V characteristics show that for both the Be^+-implanted GaAs and the $Al_{0.3}Ga_{0.7}As$ diodes, the ideality factors are about 1.8 over a relatively wide current range. This value is obtained at annealing temperatures ranging from 600 - 850°C for the GaAs diodes and 650 - 950°C for the $Al_{0.3}Ga_{0.7}As$ diodes.

(b) The reverse I-V characteristics show that the implanted $Al_{0.3}Ga_{0.7}As$ diodes exhibit a smaller leakage current than the GaAs ones. The breakdown voltages for the implanted $Al_{0.3}Ga_{0.7}As$ diodes, unlike the GaAs ones, strongly depended on annealing temperature.

(c) The C-V profiles for the Be^+-implanted GaAs diodes annealed at various temperatures indicate that the effective carrier concentration increases as the annealing temperature increases. The C-V data also shows that the Be^+-implanted GaAs diodes have graded junctions and that the grown-in junctions have abrupt ones, independent of annealing temperature. For the implanted $Al_{0.3}Ga_{0.7}As$ junctions, however, the C-V characteristics strongly depend on annealing temperature. At a temperature below 750°C, a fully depleted layer with a thickness of about 0.45 μm is observed in the C-V profile. After annealing at 850°C and 950°C, the shape of junctions is graded. The $Al_{0.3}Ga_{0.7}As$ grown-in diodes have an abrupt junction, similar to the GaAs grown-in ones.

IV. Oxygen-ion-implantation for application to heterojunction bipolar transistors

(a) The $Al_{0.3}Ga_{0.7}As$/GaAs diode characteristics, corresponding to the extrinsic emitter/base junction of the C-up HBT are examined by means of I-V and C-V measurements with different annealing temperatures and different O^+ doses. These measurements show that only high-dose O^+ implants can create a thermally stable high-resistive layer, which is a result of chemical-effect compensation due to the O-related deep levels in the AlGaAs.

(b) C-up HBTs are fabricated by a combination of O^+-implantation and Zn-diffusion. Their current gain and high-frequency characteristics are also investigated as a function of the O^+ dose. It is clear that the high-resistive barrier layer created by O^+-implantation in the extrinsic $Al_{0.3}Ga_{0.7}As$ for the C-up HBT can effectively suppress excess injection current from the emitter contact region into the extrinsic base region. This thermally stable high-resistive barrier layer provide good current gain at a high collector current density in the C-up HBT.

V. High-performance small scale collector-up AlGaAs/GaAs HBTs

(a) The high-performance of small scale C-up AlGaAs/GaAs HBTs with a C-doped GaAs uniform base layer fabricated using O^+-implantation in combination with Zn-diffusion is demonstrated. For a transistor with a 2-μm x 10-μm collector, a current gain of 20 is obtained. It is found that the current gain of the C-up HBT with a GaAs uniform base layer depends on the collector dimension because of a base recombination current around the collector-mesa perimeter. In a small scale transistor with a 2-μm x 2-μm collector a current gain of 15 is attained.

(b) A microwave transistor with a 2-μm x 10-μm collector achieves excellent high-frequency characteristics with an f_T of 68 GHz and an f_{max} of 102 GHz. A smaller C-up HBT with a 2-μm x 2-μm collector shows a higher f_{max} of 110 GHz owing to the further reduction of C_{BC}.

(c) The dependence of the current gain on collector dimension is also investigated for the C-up HBT with an $Al_xGa_{1-x}As$ graded base layer. The base recombination current around the collector-mesa perimeter decreases in the case of an $Al_xGa_{1-x}As$ graded base but not in the case of a GaAs uniform base layer.

Acknowledgment

The author would like to express his sincere gratitude to Professor Junichiro Nakahara of Hokkaido University for his encouragement, guidance and suggestion on the present work, and also to Professors Takashi Sanbongi, Hiroshi Wada, and Ikuo Suemune of Hokkaido University for their helpful suggestions. He would like to express his sincere appreciation to Professor Kunio Hikichi of Hokkaido University, who recommended the thesis topic.

The author would like to acknowledge the continuing guidance and encouragement of Dr. Tadao Ishibashi throughout this study. The author also wishes to express his grateful thanks to Drs. Tatsuo Izawa, Kazuo Hirata, Yoshihiro Imamura, and Yasunobu Ishii for their kind encouragement and guidance. The author would like to thank Dr. Yutaka Matsuoka for HBT fabrication and measurement, Dr. Sadao Adachi for his kind guidance and valuable discussions in relation to ion-implantation and annealing, and Dr. Hiroshi Ito for the growth of diode and HBT wafers. He would also like to thank Drs. Hajime Yamazaki and Takashi Honda for ion-implantation, and Dr. Yoshikazu Honma for SIMS analysis. The author is deeply indebted to Drs. Kouichi Nagata and Osaake Nakashima for fabrication processes, and thanks are due to his many colleagues, in particular the members of the HBT research groups at NTT LSI Laboratories.

Appendix

InP/InGaAs collector-up heterojunction bipolar transistors fabricated using Fe-ion implantation

A-1. Introduction

HBTs configured using $In_{0.53}Ga_{0.47}As$ (with energy gap 0.75 eV) as the base and InP (whose bandgap is 1.34 eV) or InAlAs as the wide-gap emitter have a number of attractive features. In particular, high electron mobility in InGaAs, 1.6 times higher than GaAs and 9 times higher than Si. The extent of transient electron velocity overshoot is also greater in InGaAs, InP than in GaAs. As a result, higher f_T values can be obtained with InGaAs HBTs than with GaAs based devices. In addition, the bandgap of InGaAs is smaller than that of GaAs or Si. The resulting turn-on V_{BE} of HBTs is correspondingly smaller, and as a result, the power-supply voltage and power dissipation can be lower. This improves the power-delay product in logic circuits.

This appendix describes the first InP/InGaAs C-up HBTs with epitaxial regrown base and collector layers onto emitter layer. Fe-ion (Fe^+)-implantation is used to define the intrinsic emitter/base junctions and a self-aligned fabrication processing for small-scale C-up HBTs.

Although there are several reports on AlGaAs/GaAs and InAlAs/InGaAs C-up HBTs [1-5], there are few on InP/InGaAs C-up HBTs. The most important process step in the fabrication of C-up HBTs is the formation of a barrier at the extrinsic emitter/base regions to suppress an excess injection current under forward bias voltage. In AlGaAs/GaAs and InAlAs/InGaAs heterostructures, high-resistive layers formed by O^+- or H^+-implantations in AlGaAs or InAlAs have been used as the barrier layers. In the InP/InGaAs heterostructure, however, it is difficult to form such a barrier layer by conventional ion-implantation-bombardment. Fe^+-implantation is therefore used to convert an n-type InP layer in the extrinsic emitter into a highly resistive one. This layer is made stabler by the subsequent high temperature regrowth process, which results in the creation of deep acceptors in the InP layer [6].

A-2. Diode characteristics of Fe-ion-implanted InGaAs/InP p-n junctions

It has been reported that the defects created in InP tend to pin the Fermi level in the upper half of the bandgap and that it is therefore difficult to obtain the highly resistive of n-type material by ion-bombardment. On the other hand, it is well known that many Fe atoms occupying group-III lattice sites act as compensating deep acceptors [7, 8]. Thus, the highly resistive InP layer can be formed by Fe^+-implantation and subsequent high-temperature annealing, attributed to the creation of deep acceptors in InP layer.

The p^+-InGaAs/N-InP/n^+-InGaAs diode structure is fabricated to examine a high-resistive barrier layers introduced by Fe^+-implantation in InP. This diode corresponds to the extrinsic emitter/base heterostructure in C-up HBTs. Although a number of reports on the electrical properties of Fe^+-implanted InP layers have been presented, there have been few reports on the characteristic of Fe^+-implanted InP/InGaAs heterostructure diode. Table A-I shows the diode layer structures grown by low-pressure metalorganic vapor phase epitaxy (MOVPE).

Figure A-1 (a) illustrates cross-sectional schematic views of the fabricated diodes. Fe^+ is first implanted through the N-InP using a photoresist as a mask. Then, the upper p^+-InGaAs layer is regrown at 650°C onto the entire InP layer. The Pt/Ti/Pt/Au ohmic metal is then formed on the p^+-InGaAs layer and is sintered at 300°C. The p^+-InGaAs and the implanted InP layer are then removed by wet-etching using the Pt/Ti/Pt/Au as a mask, and the Ti/Pt/Au ohmic metal is evaporated on the unimplanted n^+-InGaAs layer.

For comparison, diodes made by conventional inactive-ion species (H^+, Ar^+, and O^+) implantations are also tested, but the implantation of these ions through the p^+-InGaAs and N-InP layers different from that of Fe^+. In these diodes, the p^+-InGaAs layer is not regrown on any implanted layers. The subsequent processes are the same as those used to fabricate the Fe^+-implanted diodes.

The implantation conditions are outlined in Table A-II. Each implantation energy is chosen to give approximately the same projected range distribution, at least so as to reach the whole InP layer. Ion doses are optimized to obtain the highest resistivity value in the range between 1×10^{13} and 5×10^{14} cm^{-2}.

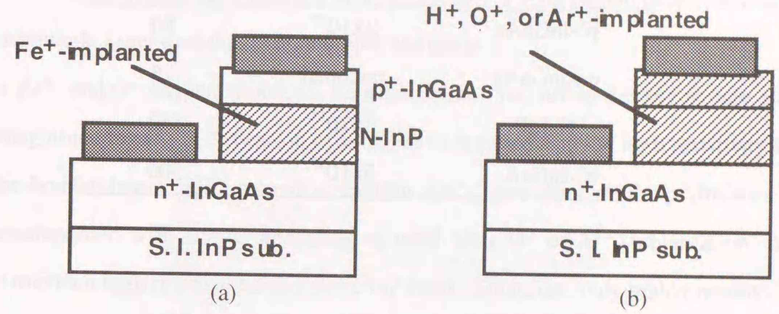

Fig. A-1. Cross-sectional schematic views of Fe^+-implanted and H^+, O^+, or Ar^+-implanted diodes.

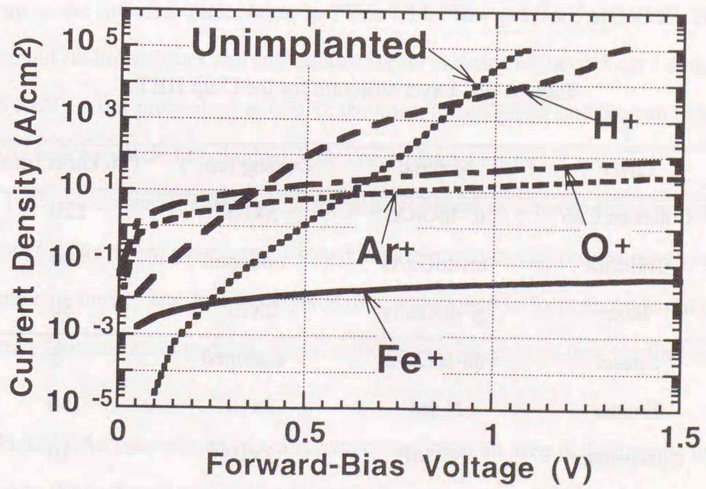

Fig. A-2. I-V characteristics of unimplanted and H^+-, Ar^+-, O^+-, and Fe^+-implanted InP/InGaAs diodes.

Table A-I. Epitaxial diode structure.

Material	Doping (cm^{-3})	Thickness (nm)
p^+-InGaAs	$2x10^{19}$	80
un-InGaAs	undoped	5
N-InP	$3x10^{17}$	150
n^+-InGaAs	$5x10^{18}$	500

Table A-II. Implant species, energy, and dose.

Species	Energy (keV)	Dose (10^{14} cm^{-2})
$^{56}Fe^+$	75	3
$^{1}H^+$	40	5
$^{40}Ar^+$	200	2
$^{16}O^+$	110	0.1

Table A-III. Layer structure for the C-up HBT.

Layer	Material	Doping (cm^{-3})	Thickness (nm)
Collector Cap	n^+-InGaAs	$3x10^{19}$	120
Collector	un-InGaAs	undoped	400
Base	p^+-InGaAs	$2x10^{19}$	80
Spacer	un-InGaAs	undoped	5
Emitter	N-InP	$3x10^{17}$	50
Sub Emitter	N^+-InP	$2x10^{19}$	10
	n^+-InGaAs	$5x10^{18}$	400
Buffer	un-InP	undoped	100

Figure A-2 shows the I-V characteristics of unimplanted (intrinsic) and implanted diodes for which the p^+-InGaAs/N-InP junction was 2 μm x 10 μm. The Fe^+-implantation has the highest resistivity in the InP layer, and at a forward-bias voltage of 0.9 V its current density is more than six orders of magnitude lower than that of an unimplanted diode.

For Ar^+- and O^+-implantations, on the other hand, this current density is only about three orders of magnitude lower. S. J. Pearton et al. [6] have reported that the high resistivity in the InP layer by ion-bombardment easily recover even after 400°C annealing. If the p^+-InGaAs regrowth process accompanied with 650°C annealing is used after O^+ or Ar^+-implantation, it may be impossible to obtain high-resistive barrier in the InP layer. Therefore, only highly resistive InP layer formed by Fe^+-implantation and subsequent regrowth process can provide the barrier to suppress undesirable excess current from an n^+-InGaAs layer to a p^+-InGaAs one.

A-3. Fabrications of C-up HBT using Fe-ion-implantation and regrowth

The C-up HBT layer structures are listed in Table A-III. Figure A-3 shows the schematic cross-sectional view of the self-aligned InP/InGaAs C-up HBT. The C-up HBT layer structures are first grown up to the InGaAs spacer layer in Table III by low-pressure MOVPE. Fe^+ is implanted into the patterned InGaAs spacer and InP emitter layers at doses of $3x10^{14}$ cm^{-2} and an acceleration energy of 75 KeV. After preheating at 650°C, the base, the collector and the cap layers are regrown on the all areas which include Fe^+-implanted and unimplanted layers.

The Ti/Pt/Au collector electrode is formed and used as a mask when reactive-ion etching performed with Cl_2/Ar mixed gas-plasma excited in an electron-cyclotron-resonance reactor is used to define the collector-mesa. The InGaAs layer is also wet-etched to form an undercut area around the collector-mesa. The total etching depth measured with a stylus-contact-type profiler is approximately 520 nm.

The Pt/Ti/Pt/Au base ohmic metal is evaporated onto an area including the entire collector-mesa. Owing to the undercut region, the base ohmic contact is self-aligned to the collector with a base-metal overlaid structure [9]. B/E mesa-etching is then performed using a wet-etching system selective for InGaAs and InP layers, and the Ti/Pt/Au emitter electrode is formed. Deep isolation

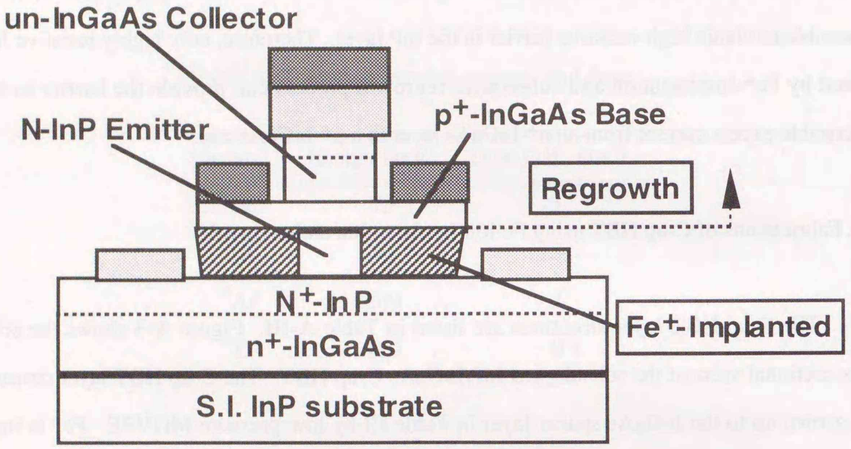

Fig. A-3. The C-up HBT fabricated by self-aligned processing.

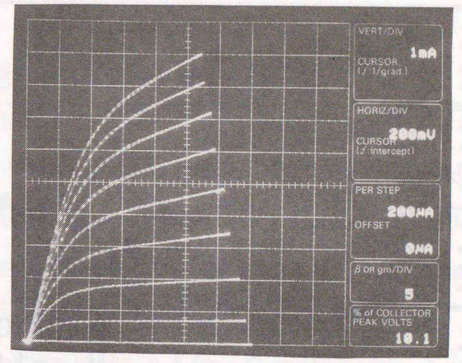

Fig. A-4. Common-emitter I-V characteristics for an InP/InGaAs C-up HBT with a 2-μm x 5-μm collector.

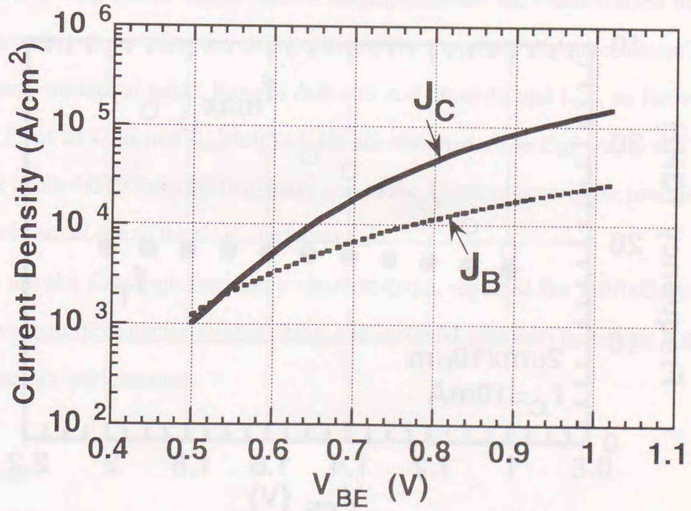

Fig. A-5. Gummel-plots for a C-up HBT with a 2-μm x 2-μm collector.

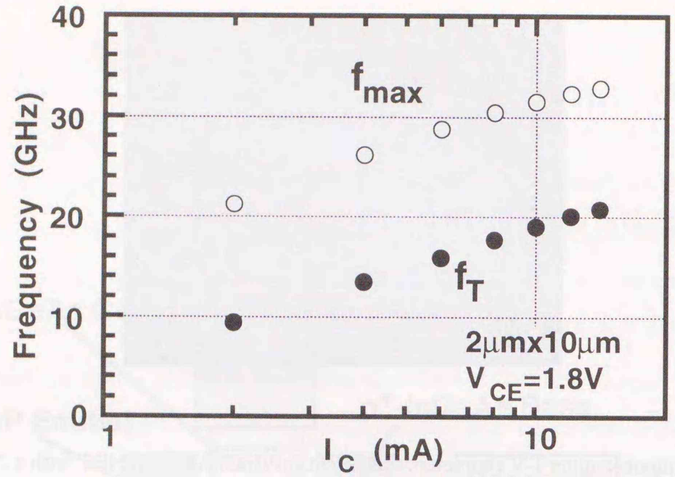

Fig. A-6. f_T and f_{max} as a function of I_C for a C-up HBT with a 2-μm x 10-μm collector.

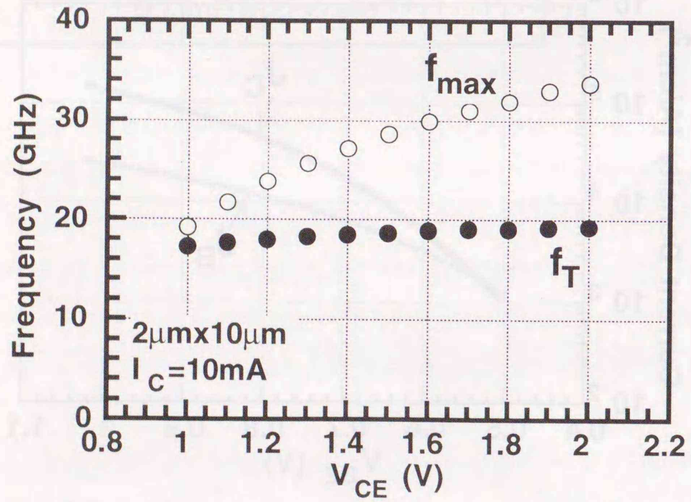

Fig. A-7. f_T and f_{max} as a function of V_{CE} for a C-up HBT with a 2-μm x 10-μm collector.

mesa-etching and polyimide film passivation are performed for the wafer, and the processing is completed with Ti/Pt/Au interconnect metallization.

A-4. DC and RF characteristics of C-up HBTs

Figure A-4 shows typical common-emitter I-V characteristics for InP/InGaAs C-up HBTs with a 2-μm x 5-μm collector. The maximum current gain is 8 at a collector current density J_C of about $4.5 \times 10^4 A/cm^2$. Figure also exhibits small offset voltage due to the C-up HBT feature which the area of the E/B junction equals to that of the B/C one.

Gummel-plots are shown in Fig. A-5 for a C-up HBT with a 2-μm x 2-μm collector. This transistor exhibits a high J_C, more than $1 \times 10^5 A/cm^2$, without decrease in current gain. In addition, a high J_C is attained even in transistors with an E/B junction smaller than 1 μm x 1 μm. These results confirm that the undesirable excess base current associated with the extrinsic emitter/base junction is sufficiently suppressed by the combination of the Fe^+-implantation and the subsequent high-temperature annealing (regrowth).

Microwave C-up HBTs with a 2-μm x 10-μm collector are characterized by S-parameters measured on a wafer. f_T and f_{max} are estimated from the frequency dependencies of typical current gain and Mason's unilateral gain. Figures A-6 and A-7 show f_T and f_{max} as functions of I_C and V_{CE}. A peak f_T of 21 GHz and f_{max} of 33 GHz are obtained. The C_{BC} value at a V_{CE} of 1 V is estimated to be about 4.0 fF from the imaginary part of the Y_{12} parameter in the low-frequency range. This value is very small due to the C-up configuration.

Theses are the first high-frequency characteristics reported for InP/InGaAs C-up HBTs. Further improvement of collector-mesa etching and epitaxial regrowth technique will lead to even better high-frequency performance.

A-5. Conclusions

Small self-aligned InP/InGaAs C-up HBTs with epitaxial base and collector layers regrown onto the emitter layer are fabricated. Fe^+-implantation is used for forming a high-resistive barrier to

suppress undesirable excess injection current from an n^+-InGaAs emitter contact layer to a p^+-InGaAs base one in the extrinsic region. This high resistivity of the Fe^+-implanted InP layer allows J_C to be greater than $1x10^5$ A/cm^2 even for small-scale C-up HBTs. For a microwave transistor with a 2-μm x 10-μm collector, f_T is 21 GHz and f_{max} is 33 GHz.

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