A Subthreshold MOS Neuron Circuit Based on the Volterra System

Tetsuya Asai, Yusuke Kanazawa, and Yoshihito Amemiya

***Abstract*—We present an analog neuron circuit consisting of a small number of metal-oxide semiconductor (MOS) devices operating in their subthreshold region. The dynamics of the circuit were designed to be equivalent to the well-known Volterra system to facilitate developing the circuit for a particular application. We show that a simple nonlinear transformation of system variables in the Volterra system enables designing a neuron-like oscillator, which can produce sequences in time of identically shaped pulses (spikes) by using current-mode subthreshold MOS circuits. We present experimental results of the fabricated neuron circuits as well as an application in an inhibitory neural network, where the neurons compete with each other in the frequency and time domains.**

***Index Terms*—CMOS analog integrated circuits, integrate-and-fire neurons, neural competition, Volterra equation.**

I. Introduction

STIFF responses of spiking neurons prevent us from simulating large-scale spiking neural networks on conventional digital systems (computers) because the time-step values in the simulation have to be chosen to be much smaller than the spike widths. Analog very large-scale integration (VLSI) implementations of the networks enable studying the dynamic properties in real time, independent of system size, which implies that the neural VLSI is a possible tool for developing an artificial neural system that is superior to our central nervous system.

A number of spiking neurons on VLSIs have already been developed including silicon neurons that emulate cortical pyramidal neurons [1], FitzHugh-Nagumo neurons with negative resistive circuits [2], and artificial neuron circuits based on byproducts of conventional digital circuits [3]–[5]. Since recent functional models of spiking neural networks tend to use integrated-and-fire neurons (IFNs) rather than Hodgkin-Huxley-type neurons [6], neuromorphic engineers have developed hardware neural systems with several types of IFN circuits to investigate the effect of spike timing and synchrony on the network's computational properties. They include competitive neural circuits with IFNs for processing sensory signals [7], hardware depressing synapses [8], and learning circuits with spike-driven synaptic plasticity [9], [10].

The IFN models are useful for both simulating spiking neural networks on digital computers and designing them on VLSIs; however, their theoretical analyses, e.g., the stability analysis of the neuron's dynamics, are not easy due to the IFNs reset (discontinuous) operations in time after the firing. In this paper, we propose an IFN circuit based on the Volterra system [11] whose dynamics are continuous in time. Using the Volterra system in the neuron circuit has two merits: 1) the underlying mechanism for the Volterra system is both qualitatively and quantitatively known [12], which facilitates designing a neural circuit suitable for a particular application and 2) by introducing a simple nonlinear transformation of system variables, the Volterra system can be represented by the linear combination of exponential functions, which is very useful for designing the dynamics in current-mode subthreshold MOS circuits [13].

This paper is organized as follows. In Section II, we first introduce a traditional IFN model and then propose a MOS IFN circuit whose dynamics are designed to be equivalent to that of the Volterra system. In Section III, we show experimental results of the fabricated IFN circuits. Section IV shows an application of the IFNs in an inhibitory neural network whose neurons compete with each other in the frequency and time domains. Section V is the summary.

II. IFN Circuit Based on the Volterra System

The IFN is defined as follows: 1) the neuron produces a pulsive output, which is called a *spike*, when the membrane potential exceeds a certain threshold value and 2) after the spike is produced, the membrane potential is reset to its resting potential [14]. Typical dynamics of the two-step IFN model are given by

$$\tau_{\mathrm{e}}\frac{dE}{dt} = -E + I_{\mathrm{in}}^{(e)} \tag{1}$$

$$\tau_{\mathrm{i}}\frac{dI}{dt} = -I + I_{\mathrm{in}}^{(i)} \tag{2}$$

$$\tau_{\mathrm{m}}\frac{dU}{dt} = -(U - V_{\mathrm{rest}}) + E - I \tag{3}$$

where U, E, I, and V_{rest} represent the membrane potential, the excitatory postsynaptic potential (EPSP), the inhibitory postsynaptic potential (IPSP), and the resting potential, respectively, and $\tau_{\mathrm{e,i,m}}$ stands for the time constants. The neuron accepts excitatory $I_{\mathrm{in}}^{(e)}$ and inhibitory input currents $I_{\mathrm{in}}^{(i)}$ through the excitatory and inhibitory synapses. An excitatory input increases the membrane potential, whereas an inhibitory input decreases it. When membrane potential U exceeds a given threshold value, a spike is produced. Then, the membrane potential is reset to the resting potential. Note that this reset operation is not included in (1) to (3).

We propose using the Volterra system to mimic the integrate-and-reset operations in the IFN model. The Volterra

Manuscript received September 15, 2002.

The authors are with the Department of Electrical Engineering, Hokkaido University, Sapporo 060-8628, Japan. This work was supported by the New Energy and Industrial Technology Development Organization (NEDO) of Japan under a Grant entitled "Analog Reaction-Diffusion Chip: The Development of Functional LSIs Recovering Fingerprint Images" in 2000.

Digital Object Identifier 10.1109/TNN.2003.816357

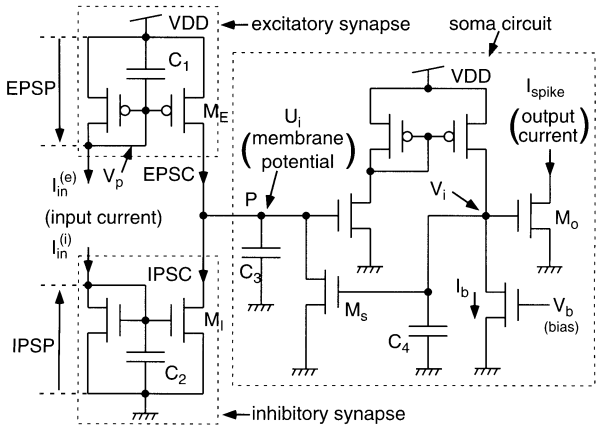

Fig. 1. IFN circuit composed of a soma inhibitory-, and excitatory-synapse circuits.

system was originally introduced to explain the oscillatory levels of certain fish catches in the Adriatic, and is given by

$$\dot{z}_1 = z_1(a - z_2) \tag{4}$$

$$\dot{z}_2 = z_2(z_1 - 1) \tag{5}$$

where z_1 represents the prey population, z_2 the predator population, and a the positive constant [12]. The system exhibits initial-value-dependent oscillatory behaviors, and its trajectory can analytically be obtained as

$$z_1 + z_2 - \ln z_1 - a \ln z_2 = c \tag{6}$$

where c represents a positive constant. We assume that prey population z_1 represents the membrane potential of an IFN, and that the predator population z_2 is used to reset the membrane potential.

By introducing a new variable $y_i = \ln z_i$, we obtain

$$\dot{y}_1 = a - \exp(y_2) \tag{7}$$

$$\dot{y}_2 = \exp(y_1) - 1 \tag{8}$$

from (4) and (5), respectively. We show that this system can easily be implemented on analog VLSIs by using current-mode subthreshold MOS circuits [13]. Fig. 1 shows our IFN circuit constructed of analog CMOS circuits. The circuit implements a soma circuit based on the Volterra system as well as the excitatory and inhibitory synapses of the neuron model. For the time being, we consider the operation of the soma circuit.

The EPSC increases the membrane potential U_i, while the IPSC decreases it. An increase in the membrane potential in the soma circuit induces an increase in potential V_i. Thus, when the membrane potential exceeds a certain threshold voltage, the input node P of the membrane is suddenly shunted by transistor $\mathrm{M_s}$. The shunted current increases exponentially with increasing membrane potential. The sudden current increase represents spike generation. The output current I_{spike} is obtained by transistor $\mathrm{M_o}$.

In the subthreshold region of operation without body effect, the drain-source current of the saturated MOS transistor is given by

$$I_{\mathrm{ds}} = I_0 \exp(\kappa V_{\mathrm{gs}}/V_T) \tag{9}$$

where I_{ds} represents the drain-source current, V_{gs} the gate-source voltage ($\geq 4V_T$ for saturation), I_0 the MOS fabrication parameter, κ the effectiveness of the gate potential, and $V_T \equiv kT/q \approx 26$ mV at room temperature (k is Boltzmann's constant, T the temperature, and q the electron charge) [15]. Typical parameters for minimum-size devices fabricated in a standard analog 1.5-μm n-well process are $I_0 = 0.5 \times 10^{-15}$ A and $\kappa = 0.6$. The dynamics of the membrane potential in terms of the EPSC and IPSC are, thus, given by

$$C_3 \frac{dU_i}{dt} = -g\,U_i + (\mathrm{EPSC} - \mathrm{IPSC}) - I_0 \exp(\kappa V_i/V_T) \tag{10}$$

where C_3 represents the membrane capacitance of the soma and g the leak conductance between the membrane and the ground. Equation (10) is equivalent to (3) when $V_{\mathrm{rest}} = 0$ and the last term at the right of (10) is zero. This term represents the current of transistor $\mathrm{M_s}$, and this transistor acts as the shunting inhibitor. The degree of inhibition is determined by the value of V_i. The dynamics of V_i are

$$C_4 \frac{dV_i}{dt} = I_0 \exp(\kappa U_i/V_T) - I_b \tag{11}$$

where C_4 represents the capacitance. When U_i increases, V_i increases as well. The V_i increase generates pulsive output currents (spikes) in transistors $\mathrm{M_s}$ and $\mathrm{M_o}$. The increase in the drain-source currents of transistor $\mathrm{M_s}$ induces a subsequent shunting inhibition, which means that membrane potential U_i is reset to zero after the spike is produced. Notice that (10) and (11) are equivalent to (7) and (8), respectively, when the leak conductance is zero. The soma circuit is thus an electronic analog of the Volterra system.

The EPSC and IPSC in the neuron circuit, which correspond to the current of transistors $\mathrm{M_E}$ and $\mathrm{M_I}$, respectively, are represented by

$$\mathrm{EPSC} = I_0 \exp(\kappa \mathrm{EPSP}/V_T) \tag{12}$$

$$\mathrm{IPSC} = I_0 \exp(\kappa \mathrm{IPSP}/V_T) \tag{13}$$

from (9). Then, the dynamics of the excitatory and inhibitory synapse circuit obey

$$C_1 \frac{d\mathrm{EPSP}}{dt} = -I_0 \exp(\kappa \mathrm{EPSP}/V_T) + I_{\mathrm{in}}^{(e)} \tag{14}$$

$$C_2 \frac{d\mathrm{IPSP}}{dt} = -I_0 \exp(\kappa \mathrm{IPSP}/V_T) + I_{\mathrm{in}}^{(i)} \tag{15}$$

where $I_{\mathrm{in}}^{(e)}$ (or $I_{\mathrm{in}}^{(i)}$) represents the excitatory (or inhibitory) input current and C_1 (or C_2) the capacitance between the excitatory (or inhibitory) synapse and the soma. Equations (14) and (15) are qualitatively equivalent to (1) and (2), respectively, since the exponential functions in the former two are monotonically increasing functions.

III. Experimental Results

We fabricated a prototype IFN chip using a 1.5-μm CMOS process (MOSIS, vendor: AMIS). Fig. 2 shows a micrograph of the IFN circuit. The capacitors $\mathrm{C_1}, \mathrm{C_2}, \mathrm{C_3}$, and $\mathrm{C_4}$ were designed with a large capacitance due to the limited time resolution of our measuring systems. The capacitors took up a total area of 120 μm $\times$ 200 μm.

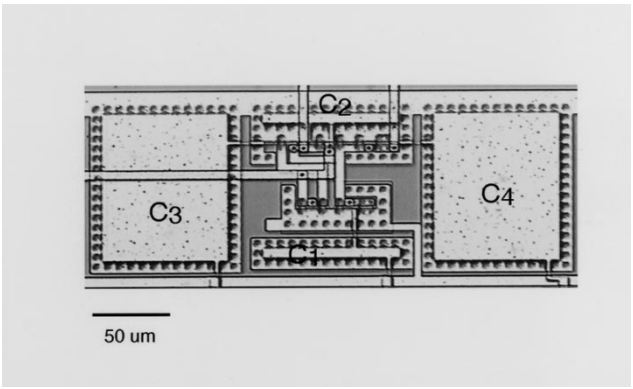

Fig. 2. Chip micrograph of fabricated IFN circuit.

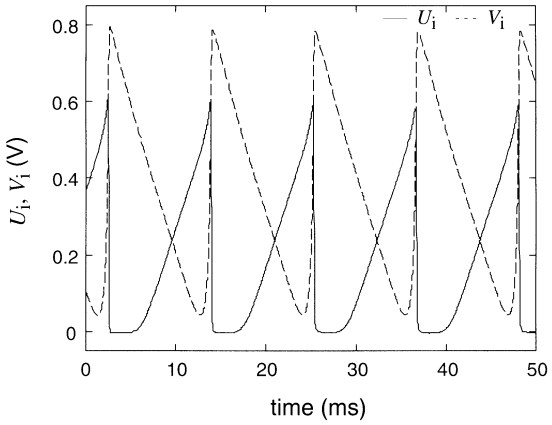

Fig. 3. Experimental results of IFN circuit for stationary inputs.

First, we confirmed the oscillatory behavior of the IFN circuit to stationary inputs. The input current (EPSC-IPSC) and the bias current I_b were set at 1 nA. The supply voltage was set at 5 V. Fig. 3 shows the experimental results. When the value of U_i exceeded the threshold voltage ($\approx$0.5 V), V_i suddenly increased. Consequently, U_i was reset to zero when $V_i \geq 0.6$ V. Fig. 4 shows closed (U_i, V_i) phase plane trajectories. The solid and dashed curves represent nullclines of the circuit. A fixed point, which is given by a cross point of the nullclines, was obtained as $(U_i, V_i) = (0.48\ \mathrm{V}, 0.49\ \mathrm{V})$.

Fig. 5 shows the results of the IFN circuit for spike inputs. The supply voltage was set at 5 V, and the bias current I_b was set at 100 nA. In the experiment, periodic current pulses were applied to the excitatory and inhibitory synapse circuits. When an input pulse was applied to the inhibitory synapse circuit, the membrane potential U_i decreased due to the increase in the IPSP. Similarly, the membrane potential increased due to the input pulse applied to the excitatory synapse circuit. When the IPSP fell below a certain threshold voltage, a spike was generated due to the reduced shunting inhibition by the IPSC. The spike current I_{spike} ($\approx$100 nA) was five orders of magnitude larger than the resting current ($\approx$1 pA), and these two could, thus, be very easily distinguished from each other.

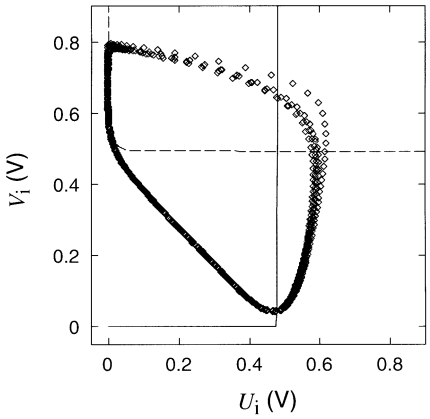

Fig. 4. Closed (U_i, V_i) phase plane trajectories of the IFN circuit.

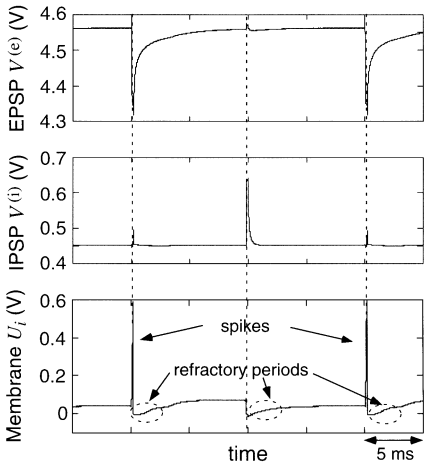

Fig. 5. Experimental results of IFN circuit for spike inputs.

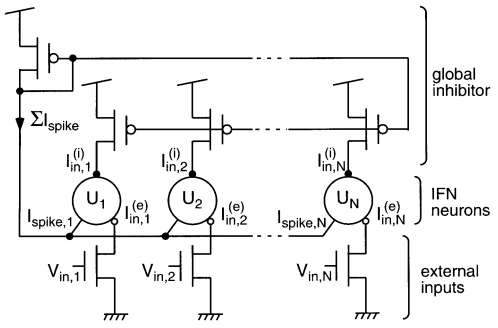

Fig. 6. Inhibitory neural circuits using IFNs.

IV. Applications: Frequency- and Temporal-Domain Neural Competition

We constructed an inhibitory neural network in which the IFN circuits are coupled to each other through all-to-all inhibitory connections of equal strength [16]. This coupling reduces the complexity of the connection of N neurons to $O(N)$. Fig. 6 shows the reduced network consisting of N IFN circuits and a global inhibitor, which is constructed of $(N+1)$ pMOS transistors. Each IFN circuit accepts an intrinsic external input V_{in}. The nMOS transistors connected to the IFN circuits produce an excitatory input current $I_{\mathrm{in}}^{(e)}$. The global inhibitor receives the sum

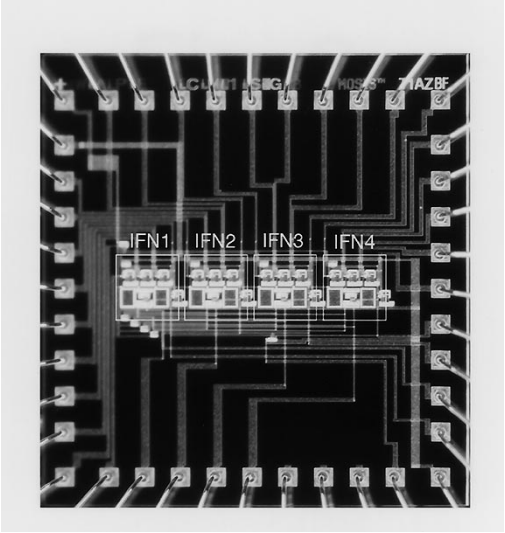

Fig. 7. Chip micrograph of fabricated four-IFN network.

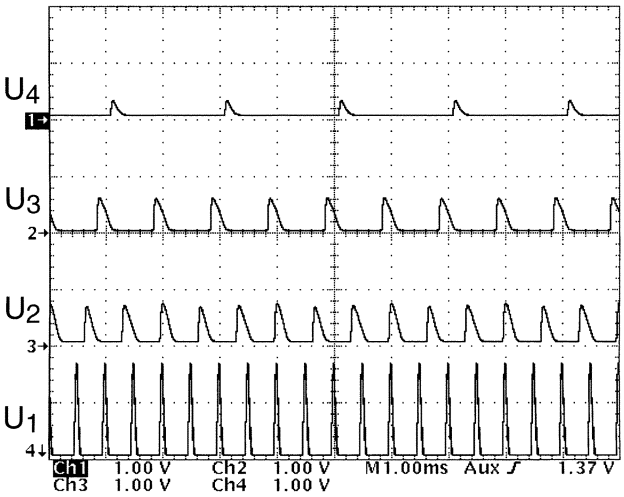

Fig. 8. Experimental results for four-IFN network. (Firing-rate encoding).

of the IFN outputs ($\sum_i^N I_{\mathrm{spike},i}$). This total current is copied in each IFN circuit to produce the inhibitory input current $I_{\mathrm{in}}^{(i)}$.

Fig. 7 is a photograph of the chip that contains four IFN circuits and one global inhibitor circuit. The results for a four-neuron network are shown in Figs. 8 and 9. In these experiments, external input values were encoded as either a firing rate or spike timing. Encoding the external input as a firing rate means that the strength of the external input is equivalent to the frequency of the train of identically shaped voltage pulses V_{in}. Encoding the external input as spike-timing code means that the strength is equivalent to the timing of spike generation relative to the timing of its external periodic input.

The results for the firing-rate encoded input are shown in Fig. 8. The amplitudes of the input current pulses $|I_{\mathrm{in}}^{(e)}|$ were fixed at 100 nA. The frequencies of four periodic pulses $I_{\mathrm{in},1}^{(e)}; I_{\mathrm{in},2}^{(e)}; I_{\mathrm{in},3}^{(e)}$; and $I_{\mathrm{in},4}^{(e)}$ were set at 200 kHz, 150 kHz, 100 kHz, and 50 kHz, respectively. Because IFN circuits inhibit each other through the global inhibitor, IFNs receiving high-frequency input remained active, while those receiving low-frequency inputs became inactive.

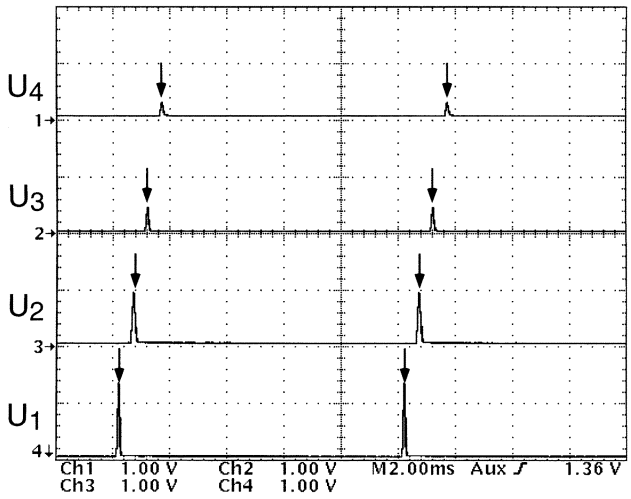

Fig. 9. Experimental results for four-IFN network. (Spike-timing encoding).

When inputs encoded as spike timings were applied to the same network, it showed quite a different qualitative behavior, as shown in Fig. 9. Here, the external input values are transformed into the initial delay times of the periodic input pulses. In Fig. 9, the arrows show the timing at which each IFN received the input pulse. This demonstrates that competition occurred in terms of the times at which the input pulse reached the individual IFNs. This phenomena ("first come, first served" or "early arrival matters") simply originates from the refractory period of the IFN circuits and the lateral inhibition. It should be noted that frequency-domain competition was achieved by introducing analog inputs that carried encoding in the form of the firing-rate frequency, while competition in the time domain was achieved by having inputs that carried encoding in the form of the spike timing.

V. Summary

We proposed and fabricated a simple IFN circuit based on the Volterra system and an inhibitory neural network consisting of a few of these circuits. The IFN circuit was designed to produce sequences of spikes in time according to the strengths of the signals on its inhibitory and excitatory inputs. Experimental results showed that the IFN circuit was equivalent to the Volterra system and that it had the same qualitative properties as the two-step IFN model. As an example, a inhibitory neural network was fabricated to demonstrate the network's competitive behavior in the frequency and time domains.

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