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Single-electron AND/NAND logic circuits based on a self-organized dot network

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We experimentally demonstrated single-electron operations of an AND/NAND logic circuit based on a self-organized GaAs quantum-dot (QD) network fabricated by applying a selective-area metalorganic vapor-phase epitaxy technique. Single-electron logic operations using four cooperating single-electron tunneling (SET) transistors has been tested. This logic circuit has an architecture based on a binary decision diagram (BDD) using a Coulomb blockade (CB) in GaAs QDs, which is a representation of digital logic functions using directed graphs. BDD node devices consisting of two SET transistors achieved a two-way path switching operation in single-electron mode due to the CB effects which appeared complementarily in the two SET transistors at 1.9 K. We also demonstrated an AND/NAND operation in a logic circuit by integrating two BDD nodes. © 2003 American Institute of Physics. [DOI: 10.1063/1.1614845]

Single-electron logic circuits have received substantial attention because they have a low power consumption and a high-density integration, which enables adding a new function to present devices.^{1,2} This is because single-electron tunneling (SET) transistors can control the exact number of electrons in a nanoscale island via Coulomb blockade (CB) effects. To date, SET circuits using complementary-metal-oxide-semiconductor (CMOS)-type logic architectures have been developed.^{3–6} However, the practical problems of high-density integration, such as small gain and the unilateral nature of the devices, impede replacing CMOS logic circuits of current large-scale integrated circuits (LSIs) in conventional architecture. Thus, an architecture based on binary decision diagram (BDD) is proposed for SE-logic system applications to overcome these shortcomings.^{7,8} In this architecture, the key device as a unit element of the circuit is called a BDD node device, which works as a path switch of SE transport between two branches using CB,⁹ and the function of any complicated logic can be realized by the combination of the node devices.

Because the BDD logic architecture is based on the graphical representation of the logic, it is feasible if the network-like structure of SET transistors arrays is realized.¹⁰ In this letter, we report on the fabrication and experimental operation of SET logic circuits based on network of GaAs quantum dot (QD) and quantum wires (QWRs). Arrays of SET transistors utilizing a QD are fabricated by using selective-area metalorganic vapor-phase epitaxy (SA-MOVPE) on partially masked GaAs substrates.^{3,11,12} Based on these nanostructures, SE BDD logic circuits are constructed by integrating four SET transistors.

Figure 1(a) shows an array of SET transistors grown by SA-MOVPE. The unit cell of the array is the region enclosed by the white box and is schematically shown in Fig. 1(b). It consists of four SET transistor structures. As we reported in

previous papers,^{12,13} each SET transistor structure, consisting of a QD, QWRs, and tunneling barriers, indicated by the white circle in the figure, can be fabricated by SA-MOVPE growth on partially masked GaAs (001) substrates with a zigzag-shaped mask opening. Their network-like arrays are realized by an appropriate repetition and connections of the single structures. The whole structure as well as a single SET transistor structure are formed by utilizing the nature of SA-MOVPE, in which nanostructures surrounded by crystallographic facets can be formed self-organizingly simply by a design of the mask patterning.¹² Cathodoluminescence study for this network reveals the formation of highly uniform arrays of QDs and QWRs.

This kind of network-like array of SET transistors is compatible with a BDD architecture for the logic circuit application. A BDD is a way of representing digital logic functions by using a directed graph, rather than a Boolean expression.^{7,8} Figure 2(a) shows a schematic representation of a BDD node. The output of the logic is determined by a messenger that enters from a root and exits from one of the two terminals (“1” or “0”); the terminals is selected by the logic input X_i , to the node. This architecture can realize any

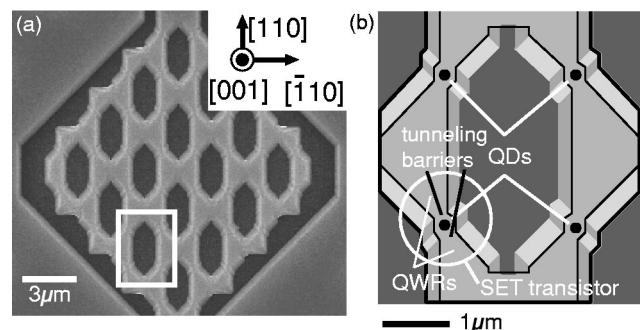


FIG. 1. (a) Scanning electron microscope image of an array of SET transistor structures fabricated by SA-MOVPE. (b) Schematic illustration of the unit cell of the array, which is enclosed by a white box of Fig. (a). The unit cell consists of four SET transistors, and each SET transistor consists of a QD, QWRs, and tunneling barriers.

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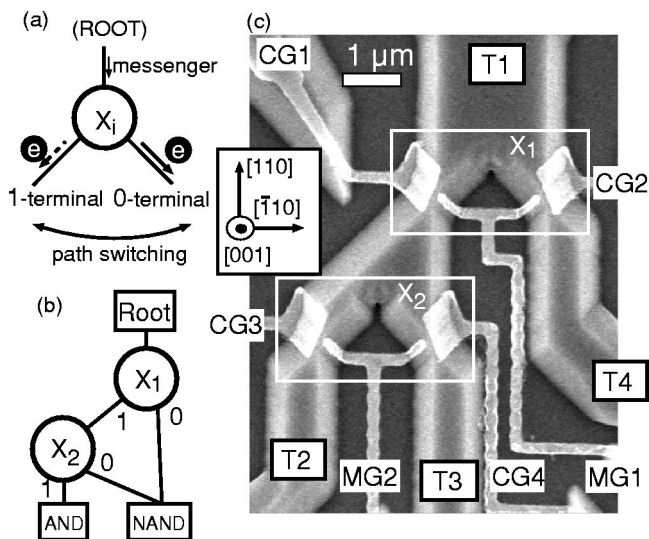


FIG. 2. (a) Symbol of a BDD node and the implementation of the node device using SET transistors. (b) Graphic representation of AND/NAND circuit based on the BDD architecture. X_1 and X_2 enclosed by a circle represent the BDD nodes. (c) SEM image of the fabricated BDD AND/NAND circuit.

kind of logic function by combining BDD nodes appropriately.¹⁰ An example of AND/NAND logic function of the BDD is illustrated in Fig. 2(b). In this case, one can easily imagine that a path between the ROOT and the AND terminal, which a messenger takes, is opened when input (X_1, X_2) is (1,1); otherwise, the messenger takes the path from the ROOT to the NAND terminal. In our implementation, we used a single electron as a messenger and two SET transistors sharing an input gate (MG1) as the logic input of the BDD node. The node device function is achieved when the transistor in the left branch is in on-status and that in the right one is in off-status for an input “1,” and when their on- and off-status are flipped for an input “0.” We note that it is possible to determine the logic function by tracing the path upward as well as downward, since there is only one path from ROOT to either of the logic terminals. In all the experiments that follow, we define the current as positive if it is from ROOT to terminals; thus the electrons go upward.

Figure 2(c) shows a scanning electron microscope (SEM) image of a single-electron BDD AND/NAND logic circuit based on the dot-wire coupled structure array shown in Fig. 1(a). The circuit consists of four dual-gated SET transistors.^{13,14} SE transport in SET transistors is controlled by two main gates (MG1, MG2) and four control gates (CG1, CG2, CG3, CG4). Among them, MG1 and MG2, which are the common gates for two transistors, correspond to the logic input for the BDD node X_1 and X_2 , respectively. T1, T2, and the sum of T3 and T4 ($T_3 + T_4$) correspond to the ROOT, AND, and NAND terminals, respectively. The nanoscale dots and large terminals for wiring are formed simultaneously due to the mask design, showing a compatibility between the BDD logic and network-like array of SET transistors and effectiveness of SA-MOVPE for its realization.

Figure 3(a) shows the current versus the main-gate voltage characteristics of two SET transistors located in each branch of the first node device (X_1) corresponding to Fig. 2(c). In this measurement, T3 is set to open and T1 is biased

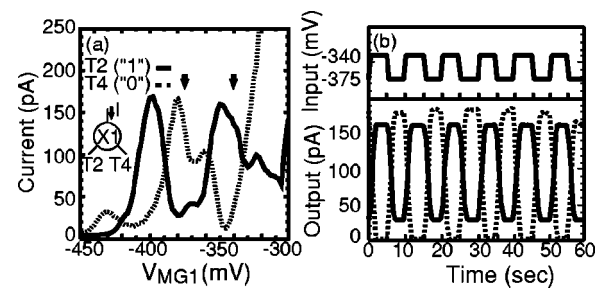


FIG. 3. (a) Coulomb oscillations (COs) of SET transistors in T2 and T4 terminals in the first BDD node (X_1), as a function of main gate (MG1) measured at 1.9 K. Here, CG1 was set to -600 mV and CG2 was set to -750 mV, which are optimized to switch the transport path between the two branches appropriately. T1 was biased at $V_{T1} = 0.1$ mV and the current was measured at terminals T2 and T4. For $V_{MG1} \sim -340$ mV, CO showed a peak for the left branch and a valley for the right. The peak–valley relations were exchanged at $V_{MG1} \sim -375$ mV. (b) Two-way switching operation when a square wave is applied to MG1 as an input signal. The current output was only observed at T2 and T4 when V_{MG1} was -340 mV (“1” input) and -375 mV (“0” input), respectively, correspond to the arrows in (a).

at $V_{T1} = 0.1$ mV, and the I_{T2} and I_{T4} currents that pass through terminals T2 and T4 are measured. The temperature was 1.9 K. Oscillations of the current, I_{T2} and I_{T4} , were observed when the main-gate voltage V_{MG1} is increased from -300 to -450 mV. These were confirmed to be Coulomb oscillations (COs) by measuring Coulomb diamonds, characteristics of differential conductance, dI_{T4}/dV_{T1} (dI_{T2}/dV_{T1}) versus bias, V_{T1} , the gate input, and V_{MG1} . A typical Coulomb gap (V_{gap}) was approximately 3 mV, and the total capacitance C_{Σ} and electronic diameter L of the QD are estimated to be 53 aF and 115 nm, respectively, using the equations $V_{gap} = e/C_{\Sigma}$ and $C_{\Sigma} = 4\epsilon L$, where ϵ is dielectric constant. These results are similar to those of the previous samples with the same structure.¹⁴ In dual-gated SET transistors, the position of these peaks and valleys can be controlled by adjusting the voltage of control gate CG1 (CG2).^{13,14} In the present condition for CG1 and CG2, the peak and valley of the two COs in the two SET transistors appeared complementarily at V_{MG1} of approximately -340 and -375 mV. Thus, a SE path from T1 (ROOT) can be set to T2 (logic “1”) for $V_{MG1} = -340$ mV, and T4 (logic “0”) for $V_{MG1} = -375$ mV. Figure 3(b) shows a two-way path switch operation when a square wave voltage was applied to the input MG1. The square wave is tuned so that it generates and switches the voltage -340 mV (logic “1”) and -375 mV (logic “0”). These results clearly demonstrate the switching of a SE transport path between T2 and T4 by MG1 using CB. The operation of a second BDD node (X_2) was also confirmed when MG2 is used as a logic input. Although the results are not shown here, we would like to emphasize that the V_{MG2} to obtain a “1” (T2) and a “0” (T3) logic output was the same as that of the first node device. Furthermore, the current level of two BDD node devices was quite similar. These results clearly show that four SET transistors fabricated by using SA-MOVPE achieved the same performance, which is important to realize integrated circuits.

We investigated the operation of a BDD AND/NAND logic circuit consisting of two SE BDD nodes. Experimental AND and NAND operations are shown in Fig. 4. Here the V_{MG1} (V_{MG2}) = -340 mV and -375 mV correspond to the

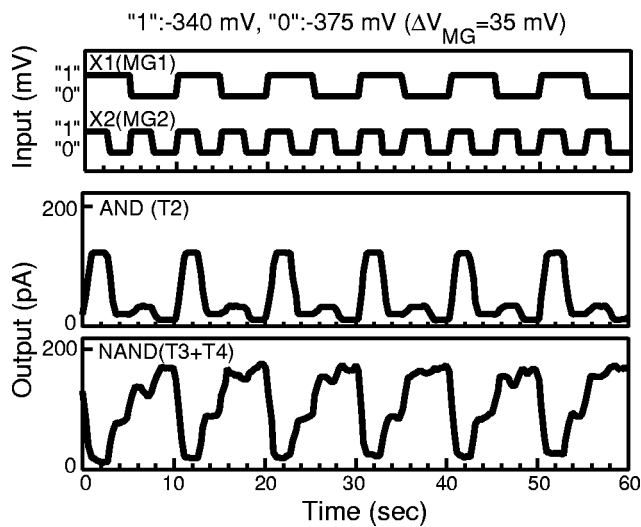


FIG. 4. Experimental operations of the BDD AND/NAND circuit at 1.9 K.

logic input “1” and “0,” respectively. The input for the two nodes of the device was applied by square waves. All logic-input combinations were applied to MG1 and MG2. The current output was obtained in the AND terminal (T2) only in the case of $(X_1, X_2) = (1, 1)$, and the NAND terminal (T3 + T4) had a current output for other logic inputs. The result clearly demonstrates that the AND/NAND operation of the SE BDD logic circuit. Operation of integrated circuits relies on even performance of individual devices; thus, the present SA-MOPVE technology is thought to be effective in realizing quantum integrated circuits that are very sensitive to the size and shape of the nanostructures.

Finally, we briefly discuss the advantage of SET devices for logic circuits. As often reported, the advantage of SET devices for logic circuits is that they consume little power. The minimum energy E_{sw} which path switching requires is the charging energy E_c ,¹⁵ which is provided by charging and discharging one electron from one transistor to another. In reality, due to the finite gain in SET transistors, it is replaced

by an energy to charge the gate capacitance, $C_{MG}\Delta V_{MG}^2$. In the present case, E_{sw} was estimated to be 2.8×10^{-21} J. This value is very small as compared to present CMOS devices ($\sim 1.7 \times 10^{-16}$ J).¹⁶ Further reduction of the dot size would enable increasing SET-transistor gain and approximating E_{sw} close to E_c , which would result in operations much closer to the quantum limit as well as at higher temperatures.

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