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GaAs dot-wire coupled structures grown by selective area metalorganic vapor phase epitaxy and their application to single electron devices

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We describe a method for fabricating GaAs dot arrays and dot-wire coupled structures having periodic nanofacets which uses selective area metalorganic vapor phase epitaxy. First, a thin GaAs buffer layer and an AlGaAs layer are grown on a masked substrate having wirelike openings with periodic width modulation. The width of AlGaAs wirelike structure is naturally squeezed by the periodic combination of nanofacets, and its top (001) surface is partially isolated by a self-limited region. Next, an AlGaAs/GaAs quantum well structure is fabricated on the substrate to form dots on the narrower top terraces, wires on the wider terraces, and ridge wires in the self-limited region. Cathodoluminescence images clearly showed dot arrays and dot-wire coupled structures were formed using this method. A single electron transistor with the same structure was also fabricated, and clear Coulomb blockade oscillation was observed. We also describe single electron tunneling devices with these dot arrays and dot-wire coupled structures. © 2001 American Institute of Physics. [DOI: 10.1063/1.1389482]

I. INTRODUCTION

Recent advances in crystal growth and device fabrication techniques have made it possible to fabricate quantum functional devices with semiconductor quantum structures such as quantum dots (QDs). In particular, single electron transistors (SETs) and circuits integrating them have received substantial attention because of their potential low power consumption and high density integration.¹ For their fabrication, it is vitally important to develop technologies for forming nanometer scale QDs and quantum wires, which are coupled together through tunneling barriers, and are precisely controlled in their size and position. Furthermore, process-induced damage and contamination must also be prevented in the fabrication of large scale SET circuits. Self-organized fabrication using selective area growth is one of the most promising ways to meet these requirements.^{2,3}

Our group has successfully fabricated SET devices and integrated circuits by using selective area metalorganic vapor phase epitaxy (SA-MOVPE).⁴⁻⁶ In those structures, however, the dots and wires are mainly obtained by the depletion layer from the sidewall Schottky gate. This makes it difficult to form tunnel barriers sufficiently high for high temperature operation.

In this article, we describe a method for fabricating GaAs quantum dot array and dot-wire coupled structures having periodic nanofacets that uses SA-MOVPE and their application to single electron devices. After a brief summary of our experimental procedure in Sec. II, we describe in Sec. III SA-MOVPE growth on a masked substrate with periodic modulated opening areas. We obtained structures having a periodic combination of nanofacets and a dot array. Dot-wire coupled structures were formed as a result of the proper de-

sign of the mask patterns. Spatially resolved cathodoluminescence (CL) images demonstrated the formation of dot array and dot-wire coupled structures with strong lateral confinement and high potential barriers. In Sec. IV, we discuss the electron transport properties of single electron transistors having the dot-wire coupled structures. We observed clear Coulomb blockade oscillation and a Coulomb diamond at low temperatures, indicating that dots and tunneling barriers were successfully fabricated. In Sec. V, we describe a design for various single electron devices having strong confinement. We conclude with a brief summary in Sec. VI.

II. EXPERIMENTAL PROCEDURE

Figures 1(a) and 2(a) show schematic illustrations of the pattern of the masked substrates used for the selective area growth. We formed 40-nm-thick SiON by plasma deposition on GaAs (001) substrates. Wire-like opening patterns with periodic zigzag edge were formed using electron beam lithography and wet chemical etching. Orientation of two edge were in the [110] and [100] directions. By varying their lengths appropriately, we defined wire-like opened areas with periodic width modulation.

A low-pressure, horizontal reactor MOVPE system was used for the growth, and TMGa, TMAI, and AsH₃ were used as source materials. The typical growth rate was 0.79 $\mu\text{m/h}$ for the GaAs and 1.26 $\mu\text{m/h}$ for the Al_{0.3}Ga_{0.7}As. The V/III ratios were set to 34 and 146, respectively. The growth temperature was set to 700 °C for all layers. The samples were characterized by scanning electron microscopy (SEM) and CL measurement at 6.8 K. The sample structure for the CL measurement was as follows: a 10 nm GaAs buffer layer, a 700 nm Al_{0.3}Ga_{0.7}As lower barrier layer, a 2.4 nm GaAs quantum well layer, a 250 nm Al_{0.3}Ga_{0.7}As upper barrier layer, and a GaAs capping layer.

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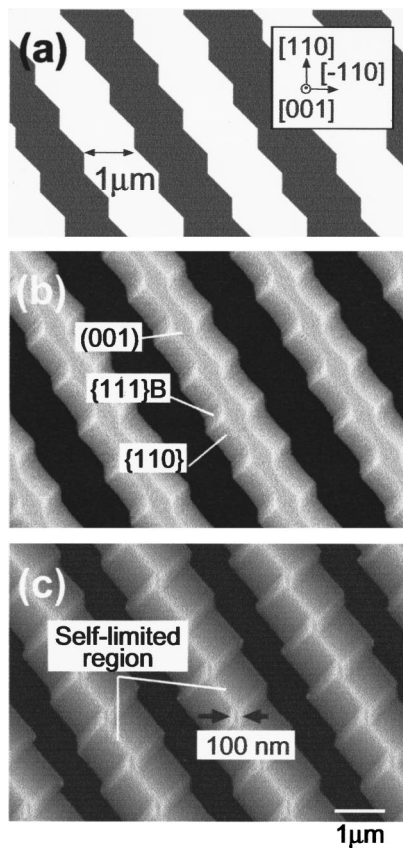


FIG. 1. (a) Schematic illustration of masked substrate corresponding to dot array. SEM images of selectively grown AlGaAs structure on the substrate for growth thicknesses of (b) 400 and (c) 700 nm. In (b), a combination of the $\{111\}B$ and $\{110\}$ nanofacets was formed as sidewalls and modulated the (001) top region. In (c), self-limited regions and isolated (001) top terraces periodically appeared.

For the study of their transport properties, we grew selectively doped double heterostructures with the following layer sequence: a 300 nm buffer layer, a 50 nm $Al_{0.3}Ga_{0.7}As$ layer, a 15 nm GaAs quantum well layer, a 40 nm n -doped $Al_{0.3}Ga_{0.7}As$ layer, and a 10 nm GaAs capping layer. Typical values of the electron mobility and sheet carrier concentration of two dimensional electron gas (2DEG) formed on a reference planar substrate were $72\,000\text{ cm}^2/Vs$ and $6.3 \times 10^{11}\text{ cm}^{-2}$ at 77 K, respectively. After the growth, Ge/Au/Ni (50/80/25 nm) ohmic contacts were formed on the grown sample as the source and drain electrodes using the lift-off method. Next, a $1\ \mu\text{m}$ length Schottky gate was formed by Al on the prominent part [see Fig. 8(b)] using the lift-off method to control the 2DEG channel width and to form a QD. The transport properties were measured at 1.7 K.

III. FORMATION OF DOT ARRAYS AND DOT-WIRE COUPLED STRUCTURES

A. Selective area growth

Figures 1(b) and 1(c) show SEM images taken after the growth of thin GaAs buffer and AlGaAs layers on the masked substrate. The growth thicknesses of AlGaAs are 400 and 700 nm on planar (unmasked) substrates like those in Figs. 1(b) and 1(c), respectively. The layers on the masked

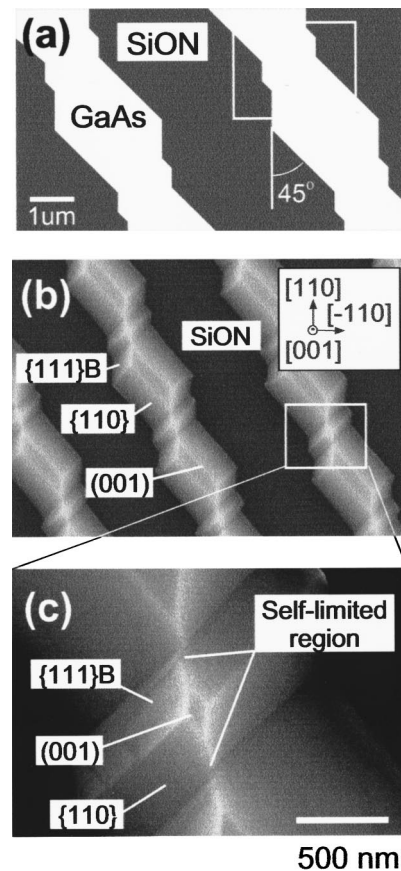


FIG. 2. (a) Schematic illustration of masked substrate corresponding to dot-wire coupled array. (b) SEM image of selectively grown AlGaAs structure on the substrate. A wider and narrower (001) top region was periodically formed due to the mask pattern. (c) Enlarged SEM image of rectangular region in (b).

substrates were slightly thicker than those on planar substrates due to both vapor phase and surface diffusion to the lateral direction, as discussed later.

For the 400 nm thickness sample [Fig. 1(b)], the structure was composed of three facets: (001) on the top surfaces, and $\{110\}$ and $\{111\}B$ at the sidewalls. The formation of the sidewall facets depended on the direction of the edge of the mask pattern. For the $[110]$ direction, $\{111\}B$ nanofacet sidewalls were formed, whereas $\{110\}$ nanofacet sidewalls were formed for the $[100]$ direction. The width of the top (001) terrace was modulated by these sidewalls.

For the 700 nm thickness sample [Fig. 1(c)], the (001) terrace was partially pinched off at the narrowest point, and ridge structures formed. These ridge structure seemed to have formed before the 700 nm growth, while their width was maintained after the pinch-off due to the self-limiting effect in SA-MOVPE.^{7,8} As a result, narrow diamond-shaped (001) terraces were periodically formed after the growth, and they became isolated by the pinched-off regions. From the SEM image in Fig. 1(c), we estimated the width of these diamond-shaped terraces to be 100 nm. This structure can be used as a base for a dot array as described later.

Next, we grew 700-nm-thick AlGaAs on the mask pattern illustrated in Fig. 2(a). The results shown in Figs. 2(b) and 2(c) were similar to those shown in Fig. 1(c). $\{111\}B$ and

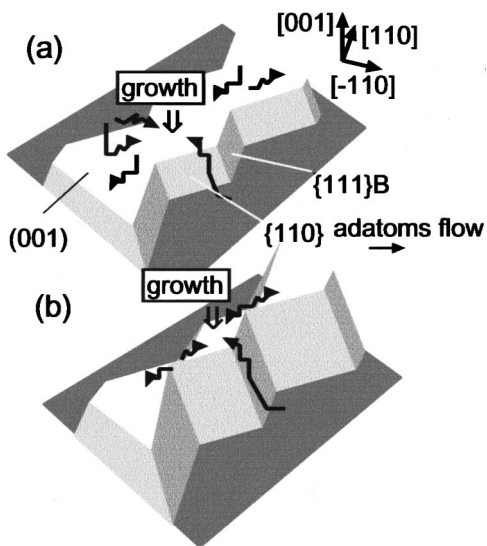


FIG. 3. Formation model for dot-wire coupled structures in selective area MOVPE. (a) corresponds to the growth before the pinch-off of the top width, and (b) corresponds to after the appearance of the pinched-off region. The direction of the flow of adatoms is indicated by the arrows.

{110} nanofacets were formed at the sidewalls depending on the direction of the mask edge. Furthermore, two types of (001) terraces were formed alternately, and they were isolated by self-limited ridge region. This is suitable pattern to form dot-wire coupled structure, that is, quantum dots formed on smaller (001) terrace region and quantum wire can be formed on (001) elongated large terrace region.

B. Growth model

The formation process of these structures is modeled as follows. Initially, AlGaAs was grown selectively on the (001) surface of the opened area. Both {111}B and {110} nanofacet sidewalls appeared during growth, as schematically shown in Fig. 3(a). This was because the growth rates on the {111}B and {110} facet sidewalls were much slower than that on the top (001) terrace. As a result, the width of the terrace was naturally squeezed by the evolution of both the {111}B and {110} facet sidewalls. As growth proceeded, the top terrace region became narrower, and finally, was pinched-off partially at the narrowest point in the wire region. As a result, ridge shaped structures were formed. At the same time, narrow diamond-shaped (001) terraces were formed at the wider regions in between the ridge regions.

In SA-MOVPE, Ga and Al atoms diffuse from the masked regions and sidewall facets to the (001) top terraces. The growth rate of the opened area is thus higher than that of the planar substrate. It depends critically on the ratio of the effective growth area to the masked area and thus depends on the mask pattern and growth time.^{9,10} In particular, the growth rate and height of the structures increases nonlinearly with time. However, growth saturates when the top terrace becomes narrower than the critical width. This is due to the balance between the detachment of atoms from the rounded top and the adsorption of atoms supplied by vapor phase or surface diffusion. As a result, the ridge shape is maintained at the pinched-off region for subsequent growth, which we re-

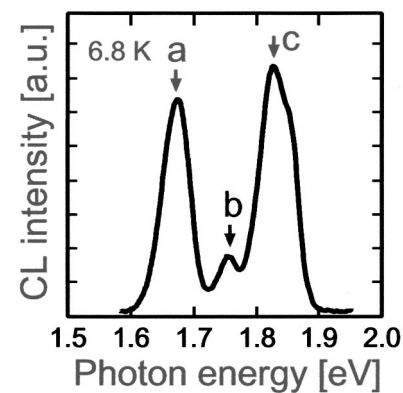


FIG. 4. Cathodoluminescence spectrum of the dot array structures.

fer to as the self-limited growth mode.^{7,8} Because the growth rate is extremely slow in the self-limited region, the concentration gradient of adatoms (Ga/Al) between the top terrace and the self-limited region becomes important, and atoms on the surface migrate from the self-limited region to the remaining top terrace,¹¹ as shown in Fig. 3(b). Thus, the growth rate on top terrace is further enhanced, and the growth rate becomes different between the terrace and self-limited region. As a result, the diamond-shaped (001) terraces become smaller as growth proceeds. This also indicates that the height is different between the top terrace and self-limited region.

C. CL characterization

To confirm our growth model, we grew an AlGaAs/GaAs/AlGaAs quantum well structure to form a GaAs dot array on the masked substrate illustrated in Fig. 1(a) and measured the spectrally and spatially resolved CL at 6.8 K. The thicknesses of the bottom AlGaAs layer and GaAs well on the planar substrate were set to 700 nm [see Fig. 1(c)] and 2.2 nm, respectively. Figure 4 shows the CL spectrum of the structure. Three peaks, located at (a) 1.67, (b) 1.76, and (c) 1.83 eV are clearly resolved in the spectra.

Figure 5 shows the spatially resolved CL images corresponding to these peaks. From the comparison with SEM images of CL image [Fig. 5(a)], the luminescence peak (a) at 1.67 eV corresponds to the emission from the GaAs dots formed on the isolated diamond shaped region. A weak luminescence image from the CL peak (b) in Fig. 5(b) is the complementary emission from GaAs dots in Fig. 5(a), which suggests the emission from GaAs layers grown on the ridge wire region. From these results, we conclude that GaAs grew mainly on the narrow diamond-shaped (001) terraces, as expected, and that GaAs dot arrays were successfully formed on the masked substrates. The thicknesses of the GaAs on the dot and in the ridge wire region were estimated from the peak energies and were 2.9 and 1.4 nm, respectively. The luminescence peak at 1.83 eV was probably from the AlGaAs buffer layers.

We also grew the same structure on the masked substrate illustrated in Fig. 2(a) and measured the CL. The CL spectra also had three peaks, at (a) 1.66, (b) 1.75, and (c) 1.84 eV, as shown in Fig. 6. The luminescence image in Fig. 7(a) shows

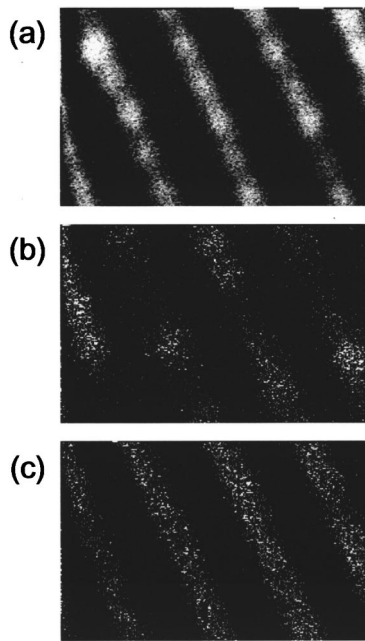


FIG. 5. Cathodoluminescence images of the dot array structures corresponding to energies indicated by arrows (a), (b), and (c) in Fig. 4.

that the luminescence peak at 1.66 eV corresponds to the wire parts in the wide (001) region. The image in Fig. 7(b) suggests that the 1.75 eV peak was from dots in the narrow (001) region. Note that these two emission images are complementary. The thicknesses of the GaAs on the wide and narrow (001) terraces were estimated to be 3.4 and 1.6 nm based on the CL peak energies, similar to the relationship between Figs. 4 and 5(c). The peak at 1.84 eV was probably from AlGaAs. The modulation of the channel width laterally confined the electrons in the dot region, which was connected to the wider channel region through the constricted region. From these results, we conclude that GaAs dot-wire coupled structures were formed and that it is possible to fabricate single dot devices like a SET.

IV. SINGLE ELECTRON TRANSISTORS USING DOT-WIRE COUPLED STRUCTURES

A. Proposed structure and design principle

A potential application of dot-wire coupled structure is a single electron transistor. We grew the AlGaAs/GaAs selec-

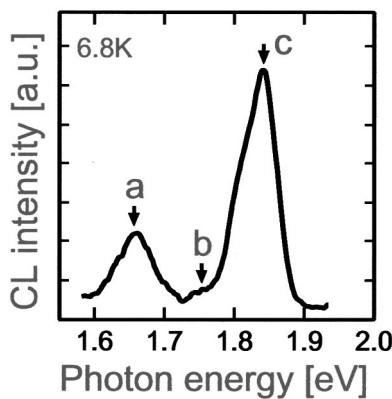


FIG. 6. Cathodoluminescence spectrum of dot-wire coupled structures.

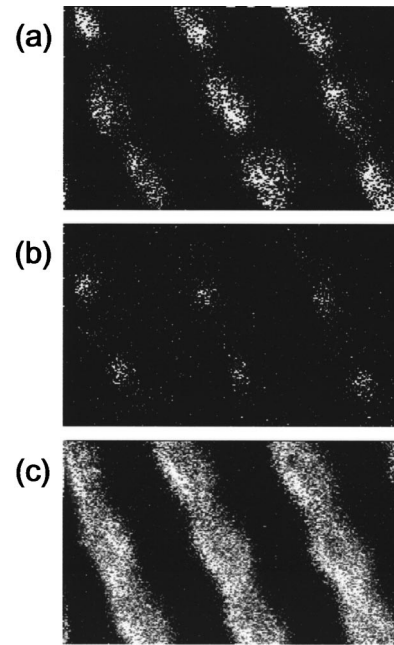


FIG. 7. Cathodoluminescence images of dot-wire coupled structures corresponding to energies indicated by arrows (a), (b), and (c) in Fig. 6.

tively doped double heterostructure shown in Fig. 8(a) on a masked substrate designed based on the dot-wire coupled array illustrated in Fig. 2(a). To fabricate a SET, we simply pick a part of the pattern [like that enclosed by the box in Fig. 2(a)] and use both ends (wire regions) as the source and drain electrodes. An Al Schottky gate electrode is formed on dot part as shown in Fig. 8(b). Narrow parts at both sides of the dot region are expected to work as tunnel barriers under the negative bias voltage on Al gate. As a result, a quantum dot is formed in this region. We estimated the geometrical

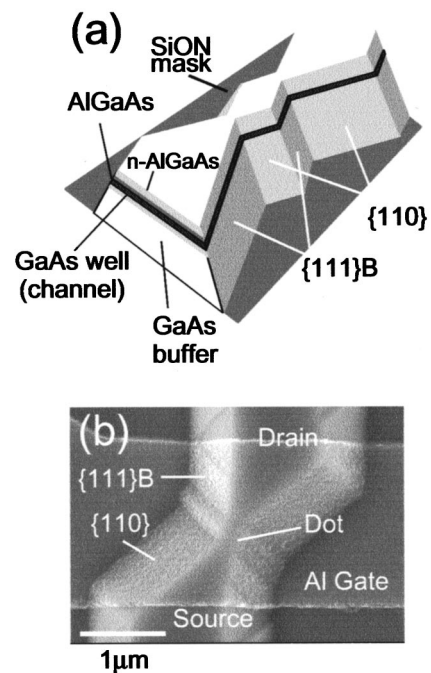


FIG. 8. (a) Schematic illustration of growth structure for single electron transistor. (b) SEM image of the device.

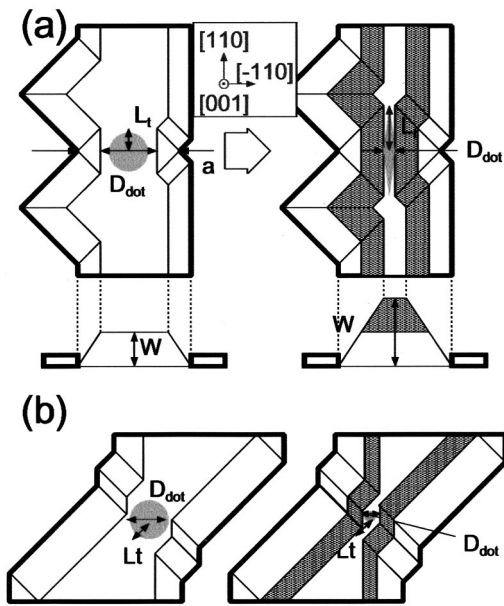


FIG. 9. Schematics of (a) previous and (b) present single electron transistors fabricated by selective area MOVPE.

diameter of the dot part to be about 150 nm. Note that the self-limited ridge regions are not formed in the present structure and GaAs channel layer is grown before the pinch-off. Further improvement in lateral confinement is likely with the use of a self-limited region, as discussed in the next section.

Our group reported SET devices and integrated circuits fabricated using SA-MOVPE.⁴⁻⁶ Our present structures have advantages for the formation of smaller size dot compared with our previous. This is schematically shown in Fig. 9.

With the previous structure in Fig. 9(a), the geometrical dot size (D_{dot}) after growth is expressed as

$$D_{\text{dot}} = a - 2W/\tan(\theta), \quad (1)$$

where W is the growth thickness on the opened area, a is the width of the opened area, and θ is the angle between the {111}B facets and (001) surface ($=54.7^\circ$). This equation indicates that the dot size can be controlled by adjusting growth thickness as well as the mask pattern and is smaller the thicker the growth layer. In contrast, the length of the tunnel barrier or the distance between the dot and wire (L_t) is approximately expressed as

$$L_t = W/\tan(\theta), \quad (2)$$

i.e., L_t becomes longer as thickness W is increased. Therefore, it is hard to compromise to obtain small dots and tunnel barriers with optimized tunnel resistances, and requires strict mask design. In addition, we need finite W as a buffer layer in electronic devices like SETs.

With the present structure, D_{dot} can also be controlled by adjusting the growth thickness, i.e., Eq. (1) applies. In addition, before the appearance of the self-limited region, L_t is independent of the growth thickness and depends only on the mask pattern, as shown in Fig. 9(b). Therefore, we can independently control the size of the dots and resistance of the tunnel barriers. The reduction in dot size depends on the

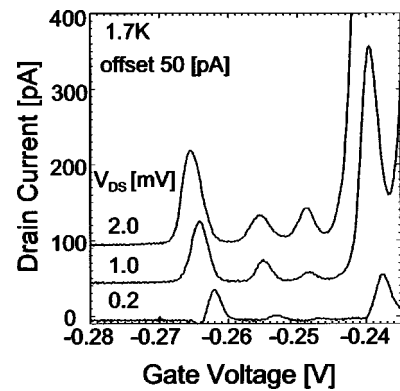


FIG. 10. Gate voltage vs drain current characteristics of SET at 1.7 K. Drain voltage was varied from 0.2 to 2.0 mV.

growth rate difference between the {111}B and {110} facets. Because the growth rate of the facets can also be controlled by adjusting the growth conditions, such as the temperature and AsH_3 partial pressure, the size of the dots can be controlled without limiting of the mask design or growth thickness.

B. Transport properties

We measured the transport properties of a SET shown in Fig. 8 at low temperatures. Figure 10 shows drain current I_D versus gate voltage V_G characteristics at 1.7 K. Drain voltage V_{DS} was varied from 0.2 to 2.0 mV. Periodic and stable conductance oscillation was observed near the pinch-off gate voltage at the all drain voltages. Oscillation was observed up to 20 K.

Figure 11 shows the differential conductance, dI_D/dV_{DS} vs V_{DS} . The differential conductance is plotted on a gray-scale as a function of both V_{DS} and V_G . Clear Coulomb diamonds were observed, indicating that a single electron transistor was fabricated. The width of Coulomb gaps E_C was of the order of 3 mV. We estimated dot radius R of the SET from the Coulomb gap by using $E_C = e/C$ and $C = 4\pi\epsilon\epsilon_0 R$. The results are summarized in Table I. The dot diameter (~ 60 nm) was smaller than the geometrical size of 150 nm due to the expansion of the depletion layers as they spread from the sidewalls due to the application of a negative

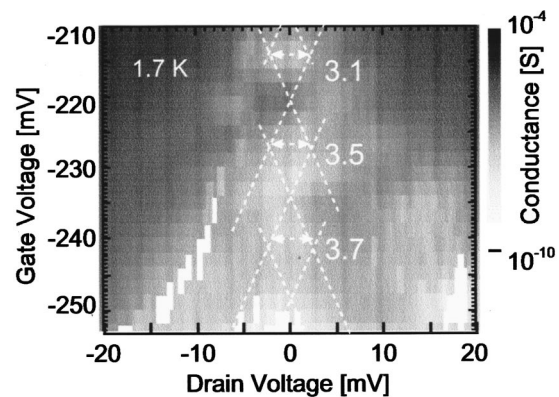


FIG. 11. Gray scale plot of dI_D/dV_{DS} for drain voltage and gate voltage characteristics.

TABLE I. Measured Coulomb gap, estimated self-capacitance of dot, and dot radius based on results shown in Fig. 11.

E_C (mV)	C (aF)	R (nm)
3.1	52	35
3.5	46	31
3.7	43	29

gate voltage. As the negative voltage sent to the Schottky gate increased, the depletion layer expanded from the sidewall facets, until finally a dot and tunnel barriers were formed near the pinch-off voltage due to the sharp channel modulation.

V. PROPOSAL OF SET STRUCTURES

To improve the performance of SETs for high temperature operation, it is necessary to fabricate high tunneling barriers and small dots. The design of a SET with the present dot-wire coupled structure with a self-limited ridge region is schematically shown in Fig. 12. A GaAs dot is formed on the small (001) terraces, and GaAs wires are formed on the large ones similar to the SET shown in Fig. 8(a), and these are almost completely buried in the AlGaAs. This structure can be made using SA-MOVPE because the growth rate in the self-limited ridge region is much slower than that in the dot region, as described in Sec. III B. Therefore, we can expect strong lateral confinement in GaAs dots by AlGaAs barrier material.

At the same time, high self-aligned tunnel barriers are formed at the ridge regions. Because the tunnel barriers are naturally formed by AlGaAs without applying the negative bias voltage at Schottky gates, the operation range of the SETs should be wider. This is another advantage for applications.

The geometrical size of the dot diameter is also reduced due to the self-limiting growth condition, as shown in Fig. 9(b). Because all the structures are formed close to the tops

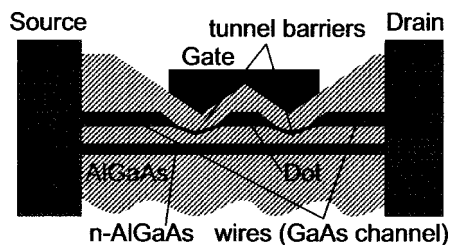


FIG. 12. Schematic cross-sectional view of single electron transistor with dot-wire coupled structures with self-limited region for lateral confinement.

of ridges, an inverted modulation doped heterostructure would be more feasible for ensuring carrier supply from the thick doped layer.

A variety of structures can be fabricated using SA-MOVPE with the appropriate mask design. It is also possible to form multiple dot structures with multiple tunnel junctions (MTJs). Typical application of MTJ structures are single electron turnstile and pump devices, which can produce a current that is clocked electron by supplying an electron using an external periodic signal. These structures are also applicable to SETs with MTJs, which should reduce the probability of cotunneling. They can be achieved by simply reducing the distance between dots in the dot arrays shown in Fig. 1, that is, by adjusting the mask design. In short, the principle for the device design described in Sec. IV A is applicable to SET with MTJs.

VI. SUMMARY

We described dot array and dot-wire coupled structures having periodic nanofacets formed using SA-MOVPE. The formation process was examined using spectrally and spatially cathodoluminescence. Single electron transistors were fabricated by applying the dot-wire coupled structure, and clear Coulomb blockade oscillation was observed at 1.7 K. We also described a SET and MTJ devices with stronger lateral confinement as applications of our dot-wire coupled structure.

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