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A Novel InGaAs/InAlAs Insulated Gate Pseudomorphic HEMT with a Silicon Interface Control Layer Showing High DC- and RF-Performance

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Abstract—A novel InGaAs/InAlAs insulated gate pseudomorphic HEMT (IG-PHEMT) utilizing a silicon interface control layer (Si ICL) was successfully fabricated and its DC and RF performances were characterized. The device showed high transconductance of 177 mS/mm even for a gate length of 1.6 μm . As compared with the conventional Schottky gate PHEMTs, the gate leakage current was reduced by 4 orders of magnitudes and the gate breakdown voltage was increased up to 39 V. Well-behaved RF characteristics with the current gain cutoff frequency, f_T , of 9 GHz and the maximum oscillation frequency, f_{max} , of 38 GHz were obtained for the 1.6 μm -gate-length device.

Index Terms—Fermi level pinning, gate leakage, InGaAs, insulated gate, interface control, interface states, PHEMT.

I. INTRODUCTION

DUE to its excellent high frequency performance, the InP-based InGaAs/InAlAs pseudomorphic HEMT (PHEMT) is a promising candidate for the key device in next generation ultra-high-speed wireless and optical communication systems [1], [2]. Unfortunately, however, the conventional PHEMT has a Schottky gate (SG) structure which tends to cause various problems particularly in high power applications. Namely, the problems are large DC leakage currents, low breakdown voltages, poor RF power handling capability, poor reproducibility and reliability, all of which are due to the low and unstable barrier height at the Schottky interface as well as to forward conduction inherent in the Schottky gate.

To solve these problems, use of an insulated gate (IG) structure is a promising approach. However, realization of a good IG structure on III-V compound semiconductors has been known to be difficult due to strong Fermi level pinning which takes place at the insulator-III-V compound semiconductor interface due to high-density interface states [3], [4]. Thus, previous insulator gate field effect transistors (IGFETs) suffered from problem such as poor gate controllability, large drain current drift and poor reliability.

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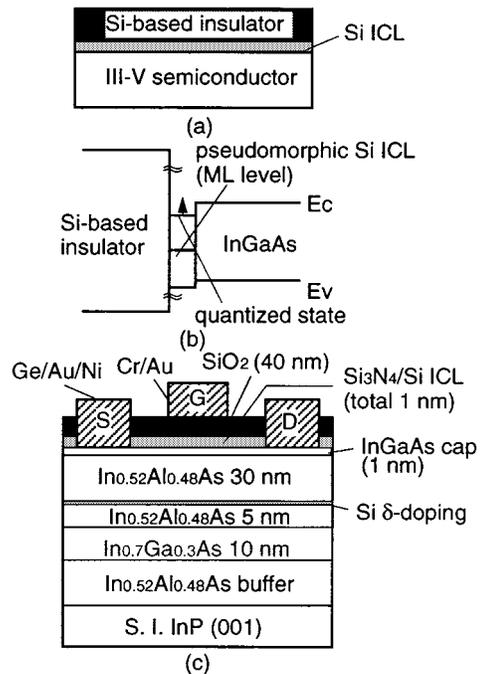


Fig. 1. (a) A basic insulator-III-V semiconductor structure utilizing Si ICL, (b) a band diagram of an insulator/Si ICL/InGaAs system and (c) cross-sectional structures of an InGaAs/InAlAs insulated gate (IG)-PHEMT.

In this letter, we report on successful fabrication and DC and RF characterization of an InGaAs/InAlAs IG-PHEMT having a novel IG structure utilizing a silicon interface control layer (Si ICL) [5]–[7]. In this structure, an ultrathin pseudomorphic Si layer grown by molecular beam epitaxy (MBE) is inserted between a Si-based insulator and the III-V compound semiconductor, as shown in Fig. 1(a). The pseudomorphic Si/InGaAs coherent interface combined with a Si-based insulator/Si interface having low-density interface states can realize ordered and coherent bonding transition from the III-V semiconductor to the Si-based insulator, thereby removing interface gap states. To make this scheme work for wide-gap materials, one should pay attention to the band gap narrowing of the Si ICL due to tensile stress. This potential problem can be avoided by using an ultrathin Si ICL where the electron and hole band states pushed out from the ultra-narrow Si surface quantum well [7], as shown in Fig. 1(b).

Effectiveness of the Si ICL technology has been confirmed in a macroscopic way by dramatic increase of photoluminescence intensity from near-surface AlGaAs/GaAs quantum well [8] and InAlAs/InGaAs quantum wires [9] as well as by realization of stable InGaAs metal-insulator-semiconductor (MIS) FETs [10]. More recently, a scanning tunnel microscopy (STM)/scanning tunnel spectroscopy (STS) study also has confirmed its effectiveness in a microscopic scale [11].

II. DEVICE STRUCTURE AND FABRICATION

The cross-sectional structure of the novel InP-based IG-PHEMT is shown in Fig. 1(c). The device has a novel insulated gate structure where a partially nitrated ultrathin Si layer is inserted between a gate insulator, SiO₂, and the standard PHEMT wafer with an InGaAs cap layer. Partial nitridation of the Si layer was done to control the Si ICL thickness precisely in monolayer level to push out Si band states.

The InGaAs/InAlAs PHEMT wafer was grown by the conventional MBE. The channel layer was a 10 nm pseudomorphic In_{0.7}Ga_{0.3}As layer whose Hall mobility and sheet carrier density at 300 K were 7700 cm²/Vs and 1.9×10^{12} cm⁻², respectively. The device isolation etching and formation of Ge/Au/Ni source and drain electrodes were done in air. After the removal of an oxide layer on the InGaAs cap layer by HF treatment in N₂ ambient, the sample kept in the N₂ ambient was quickly loaded into the MBE chamber. A pseudomorphic 1 nm thick Si layer below the critical thickness of the Si on InGaAs was grown by MBE at a substrate temperature (T_{sub}) of 290 °C. Then, the sample was transferred into an ECR plasma CVD chamber without breaking ultrahigh vacuum. Partial nitridation of the Si ICL was done by irradiating the surface by the N₂ plasma in order to obtain an optimum ultrathin SiN_x/Si structure [5] where *in-situ* XPS measurements were used for *in-situ* process monitoring and optimization. Then, a 40 nm SiO₂ was deposited by the plasma CVD as the gate insulator. A 10 nm Cr/100 nm Au gate electrode was formed by standard photolithography and lift-off process. The fabricated devices had gate length, L_G , of 1.6 μm and effective gate width, W_G , of 65 μm × 2. To clearly see the effect of insertion of the Si ICL, IG-HEMT devices with the SiO₂ gate insulator only and without the SiN_x/Si structure were also fabricated.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows $I_{\text{DS}}-V_{\text{DS}}$ characteristics of the fabricated IG-PHEMTs with and without Si ICL. The insulated gate devices without Si ICL were very fragile and easily broke down. Thus, they could be characterized at only small drain voltages. Without Si ICL, the IG-PHEMT showed very poor gate controllability and small drain currents. The channel could not be pinched off either. These are due to presence of strong Fermi level pinning. The obtained maximum transconductance, g_m , of the device without Si ICL was 7 mS/mm.

On the other hand, insertion of the Si ICL dramatically improved the DC performance, showing excellent gate control and complete channel pinch-off. The maximum drain currents became 4 times larger than those of the IG-PHEMT without Si ICL. Source-drain currents could be well controlled up to

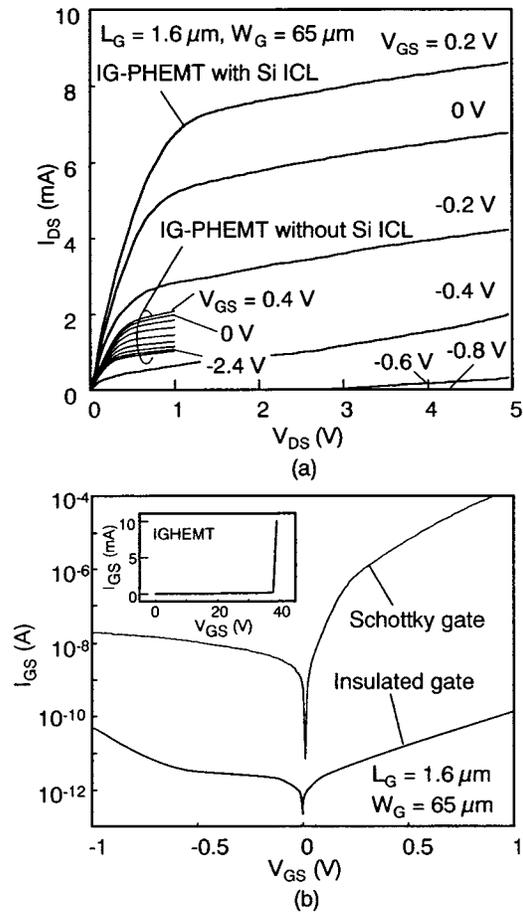


Fig. 2. (a) $I_{\text{DS}}-V_{\text{DS}}$ characteristics of IG-PHEMTs with and without Si ICL. I_{DS} : drain current, V_{DS} : drain to source voltage, V_{GS} : gate to source voltage, and (b) gate leakage current characteristics of the IG- and SG-PHEMTs.

$V_{\text{DS}} = 5$ V without any kink effects. No $I-V$ hysteresis effect was seen. A maximum transconductance of 177 mS/mm was achieved at $V_G = 0$ V. This is 20 times larger than the best g_m value of 7 mS/mm of the IG-PHEMT without Si ICL. All these improvements are due to the removal of the Fermi level pinning.

The best values of g_m of the conventional Schottky gate (SG)-HEMTs reported in the literature [12], [13] is 210–377 mS/mm for $L_G = 1$ μm. Thus, the g_m value of 177 mS/mm obtained in the present device for $L_G = 1.6$ μm is comparable to that of the SG-HEMTs. Further increase of g_m values to those comparable with commercial sub-micron SG-HEMTs seems feasible by reducing the gate length. It should be also noted that the present IG-PHEMTs allow operation under positive gate voltages, whereas SG-HEMTs usually do not, due to forward conduction.

Gate leakage currents of the IG-PHEMT with Si ICL and a SG-PHEMT are compared in Fig. 2(b). The reverse leakage current of the IG-PHEMT at $V_G = -0.5$ V was less than 0.01 nA, which was four orders of magnitude smaller than that of the SG-PHEMT. The forward gate current remained below 1 nA even at $V_G = +1$ V, which was six orders of magnitude smaller than that of the SG-PHEMT. Obtained low gate leakage current characteristics not only reduce DC power consumption, but also allow operations under large gate rf voltage swings since swings

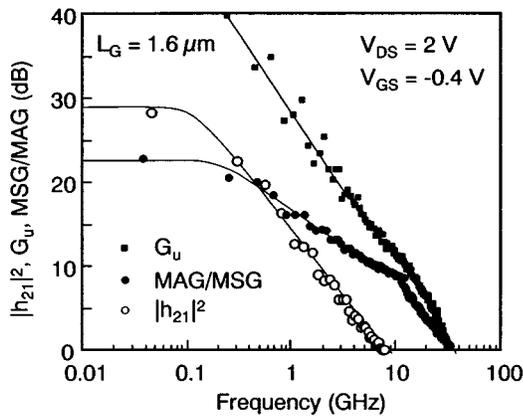


Fig. 3. On-wafer RF characteristics.

into positive gate voltages are acceptable. The off-state gate-source and gate-drain hard breakdown voltages were as high as 38 V and 39 V, respectively, as shown in the inset of Fig. 2(b). These values were much larger than those of the SG-PHEMTs.

With the fabricated long-gate devices, it is difficult to verify that the present IG structure improves on-state breakdown voltage of submicron HEMT devices where impact ionization within the InGaAs quantum well channel limits the breakdown voltage. However, in SG gate devices, surface state charging is known to cause inhomogeneous field distributions with strong local fields near the drain edge [14]. Thus, we expect that removal of surface states with the present IG technology will substantially also increase the on-state breakdown voltage.

Fig. 3 shows the on-wafer RF characteristics of the IG-PHEMT with Si ICL. In spite of a long gate length of $L_G = 1.6 \mu\text{m}$, the device showed respectable RF characteristics. The 0 dB-frequency for the unilateral power gain, G_U , and that for the maximum available gain, MAG, were the same. The current gain cutoff frequency, f_T , was 9 GHz and the maximum oscillation frequency, f_{max} , was 38 GHz at $V_{GS} = -0.4 \text{ V}$ and $V_{DS} = 2 \text{ V}$, respectively. These values of f_T and f_{max} somewhat inferior to the reported best values of the conventional SG-HEMT with $L_G = 1 \mu\text{m}$ mentioned previously which showed $f_T = 25\text{--}60 \text{ GHz}$ and $f_{\text{max}} = 120 \text{ GHz}$. However, these values seem to be respectable as the first attempt, because, in addition to a longer gate length of $1.6 \mu\text{m}$, device design was not optimized with respect to insulator thickness and parasitic elements in the present device. Further improvement of RF performance should be also achieved by reducing the gate length to sub-micrometer and optimizing the gate design and insulator thickness.

Reliability is an important issue for III-V FETs. Surface states have been reported to cause in SG and IG FETs various unwanted effects such as I - V hysteresis, drain current kink [15], drain current drift [10], g_m dispersion, gate lag [16], low S-D breakdown voltage [14], etc. We expect that successful removal of surface state effects by the present Si ICL technology will substantially improve device reliability and power performance. A preliminary drain-current drift test under pulsed gate voltage showed only a small and saturated drift below 0.7% after 10^4 s . This value is similar to what we

achieved for InGaAs MISFET with Si ICL reported previously [17].

In conclusion, a novel InGaAs/InAlAs IG-PHEMT utilizing Si ICL was successfully fabricated, the devices showed excellent and stable DC characteristics, respectable RF performances, much reduced gate leakage current and very high off-state breakdown voltages.

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