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Characterization and control of insulated-gate interfaces
on AlGa_N/Ga_N heterostructures

(AlGa_N/Ga_N ヘテロ構造に形成した絶縁ゲート界面の
評価と制御)

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Dedicate to

my family, Noriko, Takashi, and Momo Hori

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Chapter 1.

Introduction

1.1. Background of this study

Global warming is one of the serious problems that need to be solved to ensure the survival of the human race. It is said that the primary cause of global warming is the increasing concentration of greenhouse gases (GHGs) produced by our life style, activities, and industries. Indeed, GHG emissions have increased with the world population and development, mainly due to increasing energy consumption. Therefore, it is imperative for scientists, physicists and engineers to establish anti-global-warming measures for saving energies and controlling GHG emission. Fig. 1-1 shows the change of the total amount of CO₂ emission for the last decade reported by National Institute for Environmental Studies of Japan. While the CO₂ emission has been almost constant, the emission from the “energy conversion” category mainly due to power plants has gradually increased with time and reached more than 40 % for the year 2012. Indeed, since the Great East Japan Disaster of 2011, the number of operations of thermal power plants has drastically increased, resulting in approximately 10%-increase of CO₂ emission from the energy conversion category. Those facts suggest that our electric power consumption occupies at least 50% of the total CO₂ emission. Therefore, saving energy in electronics fields is a crucial way to solve the global-warming problem.

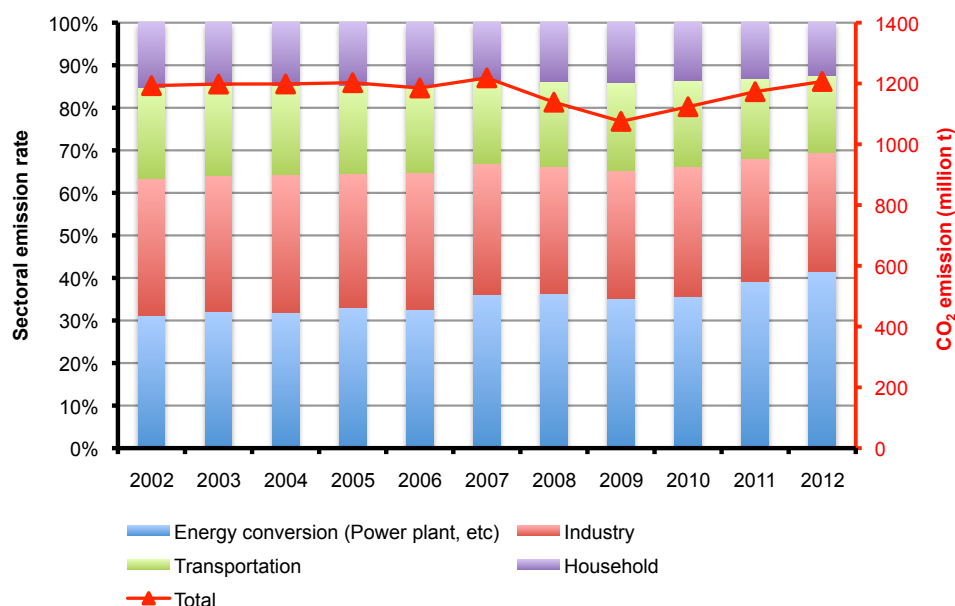


FIG. 1-1. Change of the CO₂ emission and its sectoral rate.

In electronic devices, power consumption is managed by a “power electronic system”. Power electronics is the technology associated for controlling and converting electric power, which is applied to power source units in every electronic device or system such as electric trains, vehicles, data centers, and all consumer electronics. Recently, electric vehicles (EVs) and hybrid-electric vehicles (HEVs) equipped with power electronic systems have been dramatically developed. In EVs and EHV, for example, the power conversion systems are used to drive their motors with supplying AC power source converted from DC voltage of installed batteries. In the actual conversion process, however, not all the electric power is converted because of the associated power loss in the system. To save energies in the electronic devices, not only reducing the power consumption but also controlling the power loss is quite important. Making those power electronic systems more efficient can also reduce the total electric power consumption, saving the energy in our everyday life. Nowadays, such power electronic circuits consist of various power semiconductor devices, which actually manage the efficiencies of the systems. Thus, continuous and robust development of the power semiconductor device technologies is necessary for the saving energy for the future of mother earth.

1.2. Requirements for power conversion circuits

Fig. 1-2 shows circuit diagram of DC-DC boost converter and three-phase DC-AC

inverter which are typically used to drive motors in EVs and HEVs. The circuit consists of the power transistors and diodes. The boost converter part pulls up battery voltages, and the DC-AC inverter part transforms the supplied DC voltage to AC signal with various frequencies and peak voltages. In this circuit, the transistors simply act as a switch. In the boost converter circuit, the switching transistor on the low side supplies the voltage to the inductance LI intermittently. The transistor on the high side is used for lowering the voltage that comes back from the motor as regenerative energy. In the inverter circuit, pairs of high side and low side switching transistors are alternatively turned on, realizing bi-polar voltage vibrations from single-polar DC power sources.

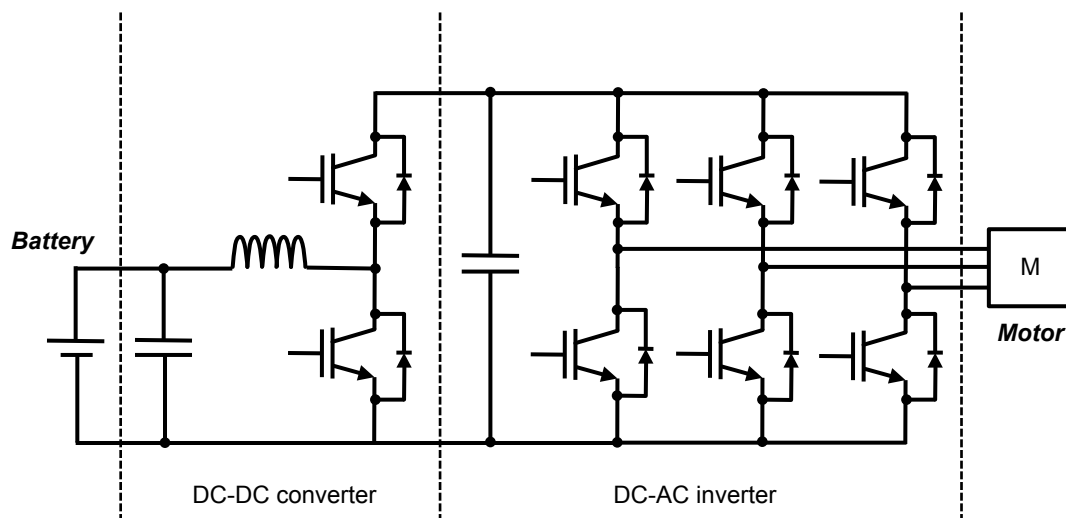


FIG. 1-2. Circuit diagram of DC-DC boost converter and three-phase DC-AC inverter.

To understand the basics operation of the switching transistors and diodes in the power conversion circuits, a circuit diagram of single-phase inverter and a resulting voltage waveform applied to the inductive load are shown in Fig. 1-3. $HS1$ and $LS2$ switches make positive-voltage on, while $HS2$ and $LS1$ apply negative-voltage to the load. In this case, tuning a duty cycle (= a ratio of on-duration to off-duration) can make AC signal and realize the DC-AC conversion using pulse-width modulation (PWM) as shown in Fig. 1-3(b).

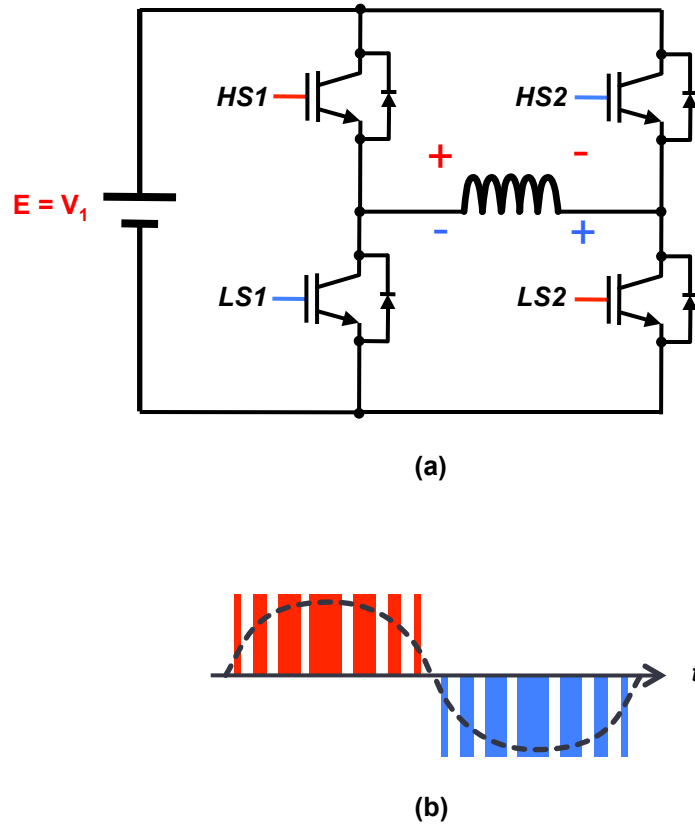


FIG. 1-3. (a) Single phase DC-AC inverter circuit. (b) Converted ac signal.

Now let us understand what is required for both of transistors and diodes to improve efficiencies of the power electronic systems.

(A) Transistors

As shown in Figure 1-4(a), a switch in electric circuits just makes on-state ($R = 0$) or off-state ($R = \infty$). Fig. 1-4(b) shows the voltage-drop vs the current-flow at the switch. In the ideal switching process, as indicated by the broken lines in Fig. 1-4(b), there are neither voltage drop nor leakage current. The broken lines in Figs. 1-5(a)-(c) show the waveforms of the voltage drop V , the current I , and the power loss P of the ideal switch. Note that P is the product of V and I . In the ideal case, P is always zero. However, the real switch has finite resistance for the on-state voltage and conductance for the off-state current, as indicated by solid lines in Fig. 1-4(b). In the V , I , and P waveforms, the finite resistance causes the voltage drop and the power loss during on-state. In this case, the resistance and the power loss are called “on-state resistance” and “conduction loss”, respectively. In addition to them, the real switch has the finite transient characteristics of voltage and current changes during turning-on and turning-off, as indicated in Figs. 1-5(a) and (b), respectively. The increased power loss

during the turning-on and turning-off transitions is called ‘switching loss’. Longer transients make the switching loss larger. Moreover, the total amount of switching loss also can be larger in the higher-frequency operation. Thus, from the viewpoint of the circuit requirements, it is vital to realize switching transistors having lower on-state resistance, lower leakage current, and higher-speed switching properties.

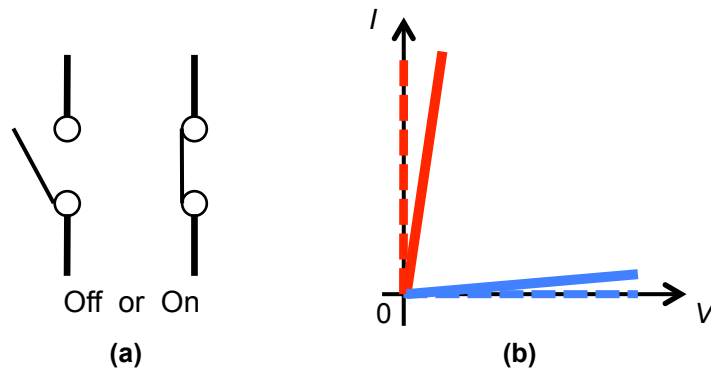


FIG. 1-4. I - V characteristics of the switching transistor.

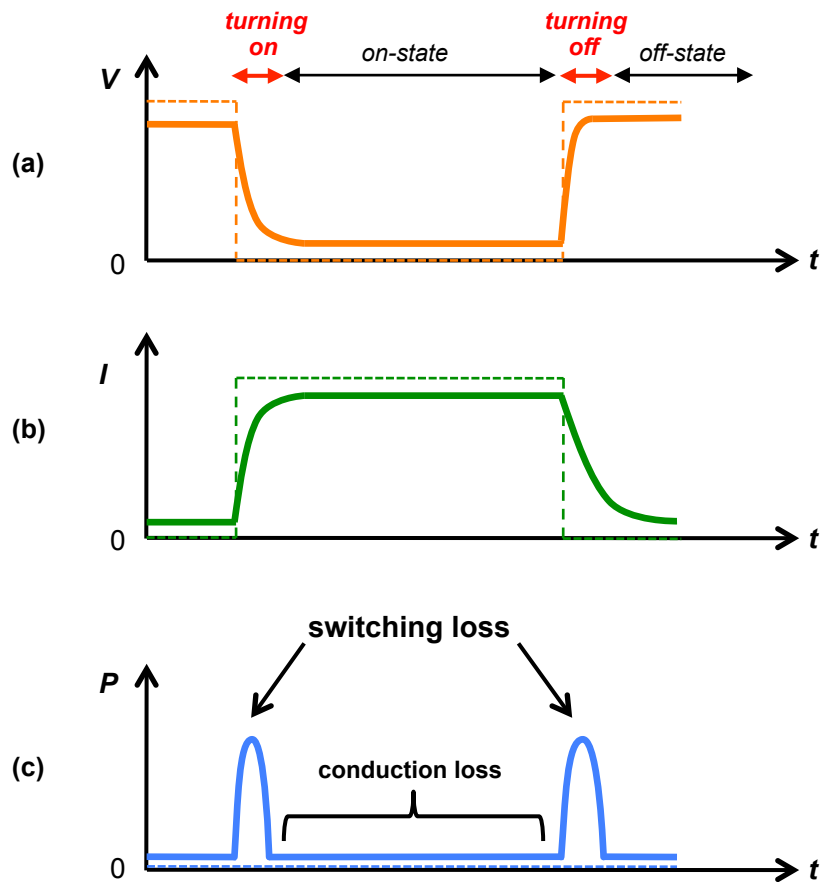


FIG. 1-5. (a) Voltage drop, (b) current, and (c) power loss waveforms of the switching transistor.

(B) Diodes

In the power conversion circuits, diodes are usually connected parallel to the transistors, which are called free-wheeling-diodes (FWDs) after their operations. To simplify their operation, Fig. 1-6 shows the circuit having two pairs of transistor and FWD connected to the inductor, which is just a part of the single-phase DC-AC inverter shown in Fig. 1-3. If the duty cycle is fixed, the circuit operates as a step down DC-DC converter. While the switch on the high side is on and the voltage is applied to the load, both FWDs are in 'off-state' due to applying the reverse bias. When the high-side switch is turned off, the inductor develops a counter electromotive force to oppose the current reducing while the voltage of the battery is also applied to the switch. Unless the switching transistor has the FWD, a critical high voltage is suddenly applied to the transistors. The FWD, however, can draw current in the continuous loop which is made by the FWD itself until the magnetic energy of L is dissipated through loss in the FWD. The current and the time to dissipate the energy with are called 'free-wheeling current' and 'free-wheeling time', respectively. The free-wheeling time, in particular, causes a dead time in the switching operation. For realizing high-frequency switching circuits, therefore, diodes are also required to have a lower resistance because the higher free-wheeling current makes the free-wheeling time shorter.

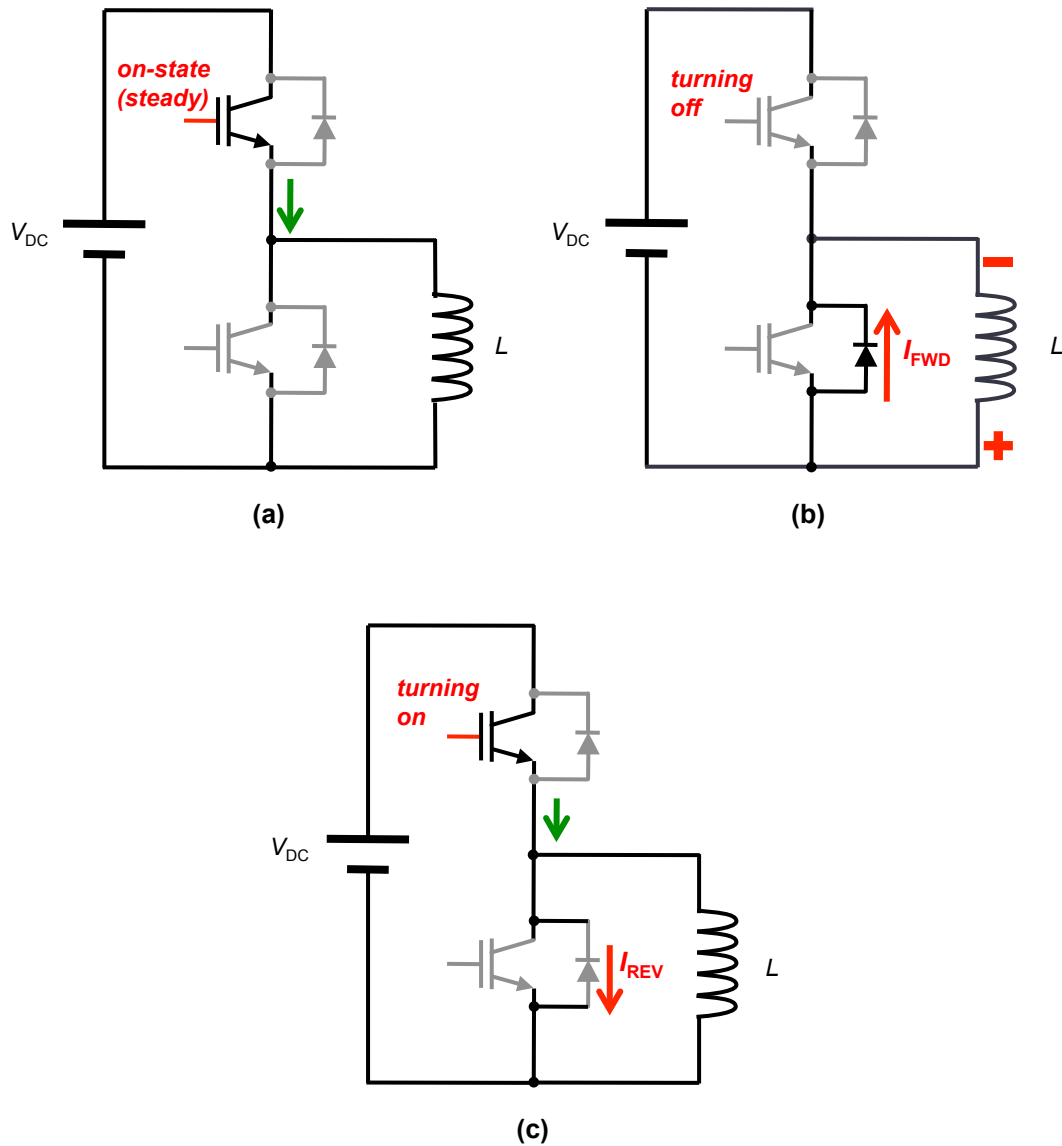


FIG. 1-6. Simplified circuit of transistors and FWDs under (a) steady on-state, (b) transient from on- to off-state, and (c) transient from off- to on-state of the switch on the high side.

Next, let us consider the transient from off-state to on-state. Once the switch on the high side is turned on again, as shown in Fig. 1-6(c), the current starts to flow through the transistors with the reverse recovery current I_{REV} in the diode on the low side. Fig. 1-7 shows the typical current waveform of the diode. In the real case, turning off the diode, I_{REV} flows mainly owing to the finite leakage current and the redistribution of carriers in the semiconductor. As a result, as shown in Fig. 1-7(b), the switching loss increases with I_{REV} . Thus, from the viewpoint of the requirements in the switching circuits, it is necessary to prepare the diodes having not only the low on-state resistance but also the low reverse recovery current.

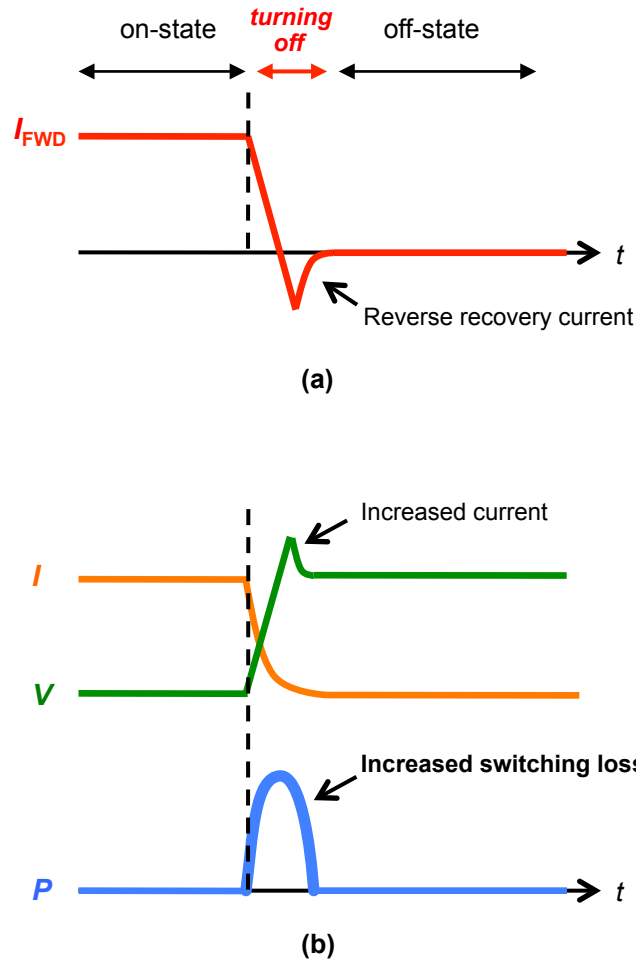


FIG. 1-7. (a) Typical current waveform of the diodes. (b) Power loss waveform at the switch affected by reverse recovery current.

(C) Example of Si-based transistors and diodes

At the moment, the power conversion circuits are usually designed using Si semiconductor transistors and diodes. Indeed, it is because Si is the most stable and reliable semiconductor in the world. Here, we introduce the actual Si power semiconductor devices that are commonly used in recent circuits. There are mainly two types of device structures and their combinations, low-voltage and high-voltage operations.

Figure 1-8 shows the example of Si transistors for low-voltage operation. The device is a typical n-channel MOSFET using n-type epi-layer, p, and n+ diffused layers prepared on a high-doped n+Si substrate. When the positive bias is applied to the gate, the p-Si layer underneath the gate is inverted into n-channel, then turning on the MOSFET. Because the current density of the device is dependent on the area of inversion layer, the integration of diffused regions can realize a higher current density. The on-state resistance can be decreased

by thinner drift region. However, the thinner drift region also makes higher electric field at the interface, resulting in lowering the critical voltage of the device.

Si-MOSFETs also have the parasitic pn diodes, which are called ‘body diodes’ between the p diffused region and the n drift layer. This parasitic diodes can act as FWDs in the switching circuits. Therefore, Si-MOSFETs themselves can realize a pair of transistor and FWD without external diodes.

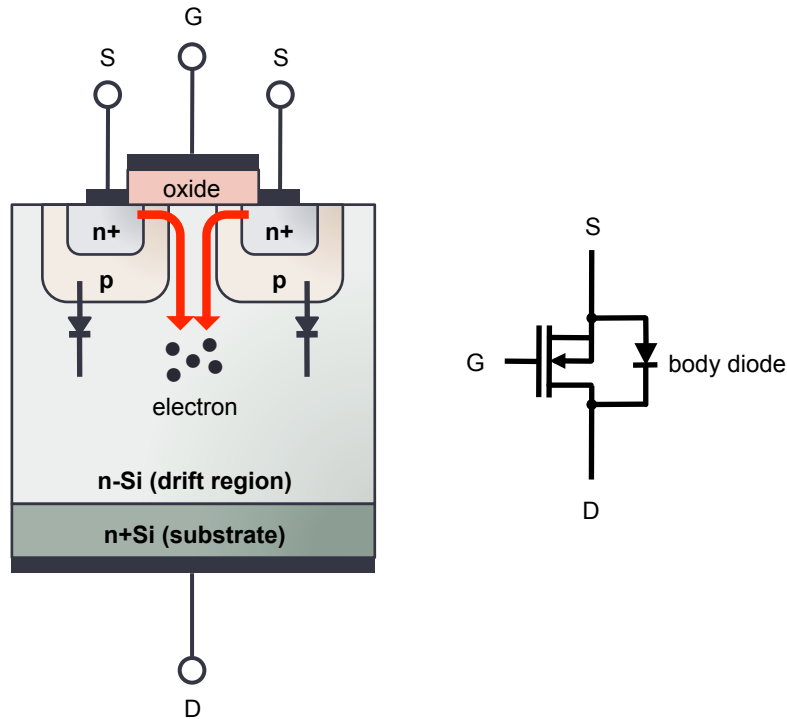


FIG. 1-8. Schematic illustration of Si-DMOSFET

For the high-voltage operation, on the other hand, the drift region must be thicker than that of the low-voltage devices. In this case, however, the on-state resistance increased with the thickness of the drift region. If the operation voltage increases by 10 times, the resulting on-state resistance then increases by approximately 300 times. To achieve lower on-state resistance for high blocking voltage operation, insulated-gate-bipolar transistors (IGBTs) which use both of electrons and holes as conductive carriers have been developed. As shown in Fig. 1-9, the device structure of IGBTs is the quite the same as those in the n-channel MOSFET, except for the p+Si substrate. In the IGBTs, when the device is turned on, the conductivity modulation which is caused by minority carrier injection from the p+-substrate to n-drift region can lower the resistance even under the high-voltage operation by using both the electrons and holes. Indeed, IGBTs are used widely in the power conversion circuits for

the EVs, HEVs, and electric trains.

When IGBTs operate under the conductivity modulation, however, the dynamics of recovery current and recovery time cannot be ignored. Mainly due to holes flowing into the n-region, the recovery time has to be greater than that of the MOSFETs. Moreover, the recovery current in the IGBTs also flows higher. As already mentioned above, the switching frequency in the circuit is limited due to such dynamics of the bi-polar devices. Indeed, the present high-voltage power conversion circuits operate with the switching frequency up to 10 kHz. Moreover, because IGBTs do not have the body diodes, the external diodes are absolutely necessary as FWDs. For realizing the on-state resistance as low as IGBTs, PiN diodes which have the intrinsic layer between the pn junction are widely used in the circuits. Those bi-polar diodes also limit the switching frequency because of the increase of the switching loss.

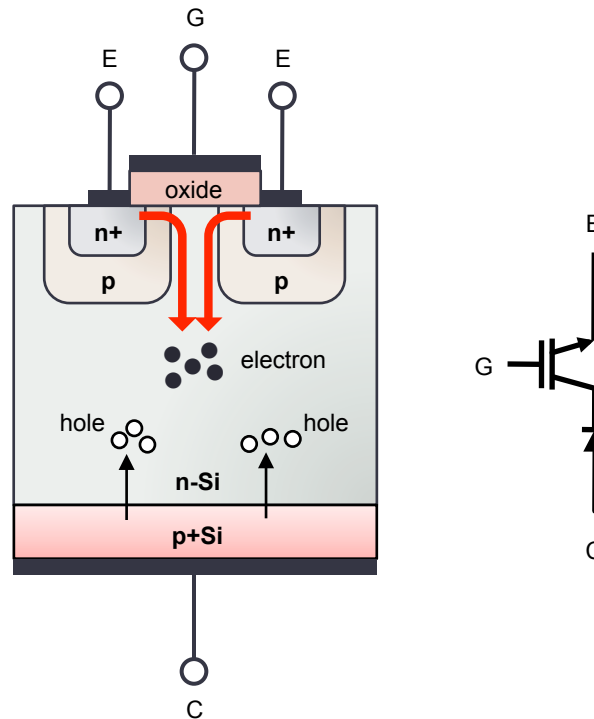


FIG. 1-9. Schematic illustration of Si-IGBT

1.3. Advantages of nitride semiconductors in power conversion systems

1.3.1. Physical properties of Si, SiC, and GaN

As mentioned in the previous section, from the viewpoint of the requirement for the

power conversion circuits, transistors are required to have the lower on-state resistance and the higher-speed switching characteristics. Besides, diodes are also required to have not only low on-state resistance but also the small recovery characteristics. From the viewpoint of the requirement for the power electronics systems, higher-voltage operation devices with the lower on-state resistance can also simplify the cooling devices. If the devices can operate under higher temperatures, furthermore, the reduced cooling systems can realize not only lowering the cost and volume of the systems but also improving the efficiency owing to the reduction of heat loss in the power electronic systems.

Wide-gap semiconductors such as GaN and SiC are currently attractive materials for realizing the next generation power conversion systems by replacing Si devices. Table I compares bandgap, breakdown electric field, electron mobility, electron saturation velocity, and permittivity of Si, GaN, and SiC taken from Refs. 1-5. The bandgap of both GaN and SiC are 3 times as large as that of Si, leading to the ten times higher breakdown electric field. Although the electron mobility of GaN and SiC showed lower values than that of Si, effects of the mobility on the on-state resistance can be suppressed using optimum device structures. GaN and its related materials, in particular, can realize various kinds of heterostructures which have much more high electron mobility than those of Si and SiC owing to less impurity scattering.³ Furthermore, GaN-based heterostructures generally show approximately ten times high electron density on their channels.

Here, let us consider what merits can be provided by those physical properties of wide-gap materials in the power semiconductor device application.

TABLE I. Physical properties of Si, GaN, and 4H-SiC

	Si	GaN	4H-SiC
Bandgap, E_G (eV)	1.1	3.4	3.3
Effective density of states in conduction band, N_C (cm ⁻³)	$6.2 \times 10^{15} \times T^{3/2}$	$4.3 \times 10^{14} \times T^{3/2}$	$3.25 \times 10^{15} \times T^{3/2}$
Effective density of states in valence band, N_V (cm ⁻³)	$3.5 \times 10^{15} \times T^{3/2}$	$8.9 \times 10^{15} \times T^{3/2}$	$4.8 \times 10^{15} \times T^{3/2}$
Breakdown electric field, E_{BD} (MV/cm)	0.3	3.3	3.0
Electron mobility, μ_e (cm ² /Vs)	1350	1200 (bulk) 2000 (HEMT)	700
Electron saturation velocity, v_e (cm/s)	1.0×10^7	2.5×10^7	2.0×10^7
Permittivity, ϵ_s	11.8	9.5	10.2

1.3.2. Intrinsic carrier concentration

The larger bandgap can realize the higher temperature operation owing to the low intrinsic carrier densities even at high temperatures. The intrinsic carrier concentration n_i in the semiconductor can be described by Eq. (1.1)

$$n_i = \sqrt{N_C N_V} \exp\left(\frac{-E_G}{2kT}\right), \quad (1.1)$$

where N_C and N_V are the effective density of the states in the conduction band and the valence band, respectively. T and k are the temperature and Boltzmann constant, respectively. E_G is the bandgap of the semiconductor. Fig. 1-10 shows the n_i of Si, GaN, and SiC as a function of $1000/T$. Parameters assumed in the calculations are summarized in Table I. For Si, n_i at room temperature are estimated to be 10^{10} cm⁻³, whereas GaN and SiC showed much more lower n_i around 10^{-10} cm⁻³. Because carriers in semiconductors are generated from electron-hole pairs, the product of electron density n and hole density p is fixed by n_i , as follows,

$$np = n_i^2. \quad (1.2)$$

Looking at Si, at room temperature ($T = 300$ K), when the electron density of the n-type semiconductor is 10^{15} cm⁻³, the minor carrier density, the hole density, is estimated to be 10^5

cm^{-3} , which is 10 orders lower than the electron density. At 200 °C ($T = 473\text{K}$), however, the hole density becomes only 3 order higher magnitude than the electron density. In this case, the existence of the minority carriers cannot be ignored. In general, high-power devices are designed using a drift region with a lower major carrier density in order to obtain higher blocking voltages. Therefore, for the Si system, the lower concentration of major carrier also leads to the small difference between the electron and hole densities at high temperatures. In contrast, GaN and SiC can keep the minority carrier density much more lower than that of Si even at 500 °C, as shown in Fig. 1-10. Wide-gap semiconductors are expected to have greater advantages for high temperature operation than Si. If the devices can operate stably up to 200 °C, the present water-cooling system in the EV and HEV systems can be replaced with an air-cooling system.

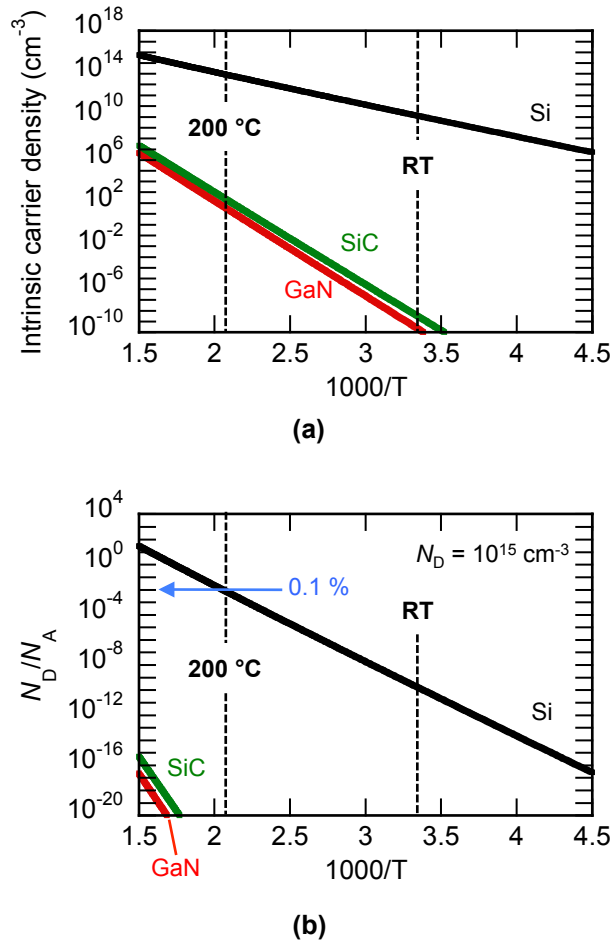


FIG. 1-10. (a) Intrinsic carrier concentrations of Si, GaN, and 4H-SiC.

1.3.3. On-state resistance vs. blocking voltage

Figure 1-11(a) shows the example of the I - V curve of n-type Schottky diode. The slope in the positive bias (on-state) corresponds to the on-state resistance per cm^2 , $R_{\text{on}} A$. When the critical voltage V_{BD} is applied to the diode, on the other hand, the device goes to breakdown as shown in the negative bias region. Let us consider the vertical Schottky diode structure prepared on the n-type semiconductor as shown in Fig. 1-11. The resistivity ρ of the semiconductor is expressed using ionized donor concentration N_D and electron mobility μ_e ,

$$\rho = (q\mu_e N_D)^{-1}. \quad (1.3)$$

$R_{\text{on}} A$ is described using the drift-region thickness W_{drift} and ρ , as follows,

$$R_{\text{on}} A = W_{\text{drift}} \rho. \quad (1.4)$$

Thus, $R_{\text{on}} A$ is inversely proportional to N_D and proportional to W . When the negative V_{BD} is applied, as shown in Fig. 1-11(c), the depletion region is increased with the maximum width W_{MAX} as expressed by Eq. (1.5),

$$W_{\text{MAX}} = \sqrt{\frac{2\varepsilon V_{\text{BD}}}{qN_D}}, \quad (1.5)$$

where ε is permittivity of the semiconductor. Accordingly, the electric field indicated by the red broken line has the peak intensity at the surface. The maximum electric field intensity E_{MAX} is described using applied V_{BD} and W_{MAX} as follow,

$$E_{\text{MAX}} = \frac{V_{\text{BD}}}{W_{\text{MAX}}}, \quad (1.6)$$

Using Eqs. (1.5) and (1.6), the specific on-state resistance per cm^2 , $R_{\text{on}} A$, is then given by the following equation,

$$\begin{aligned} R_{\text{on}} A &= \frac{W_{\text{drift}}}{q\mu_e N_D} \\ &= \frac{W_{\text{drift}}}{q\mu_e} \frac{qW_{\text{MAX}}^2}{2\varepsilon V_{\text{BD}}} \end{aligned} \quad (1.7)$$

Because W_{drift} is equal to W_{MAX} , the resulting $R_{\text{on}} A$ is obtained by Eq. (1.8),

$$\begin{aligned} R_{\text{on}} A &= \frac{W_{\text{drift}}}{q\mu_e N_D} \\ &= \frac{V_{\text{BD}}}{q\mu_e E_{\text{MAX}}} \frac{qV_{\text{BD}}^2}{2\varepsilon V_{\text{BD}} E_{\text{MAX}}^2} \\ &= \frac{V_{\text{BD}}^2}{2\varepsilon\mu_e E_{\text{MAX}}^3} \end{aligned} \quad (1.8)$$

Therefore, $R_{\text{on}} A$ is proportional to the blocking voltage and inversely proportional to the

breakdown electric field. Fig. 1-12 shows the calculated relationship between $R_{on}A$ and V_{BD} for the Si, GaN, and SiC. Note that the values shown in this figure is the theoretical limit of unipolar devices. Because GaN and SiC have ten times as large breakdown electric field as Si, $R_{on}A$ of those materials can be reduced by 3 order magnitude lower than that of Si at the same blocking voltage. The product in Eq. (1.8), $\epsilon\mu E_{MAX}^3$, is called Baliga figure of merit,² which compares the merit of those physical properties to the on-state resistance.

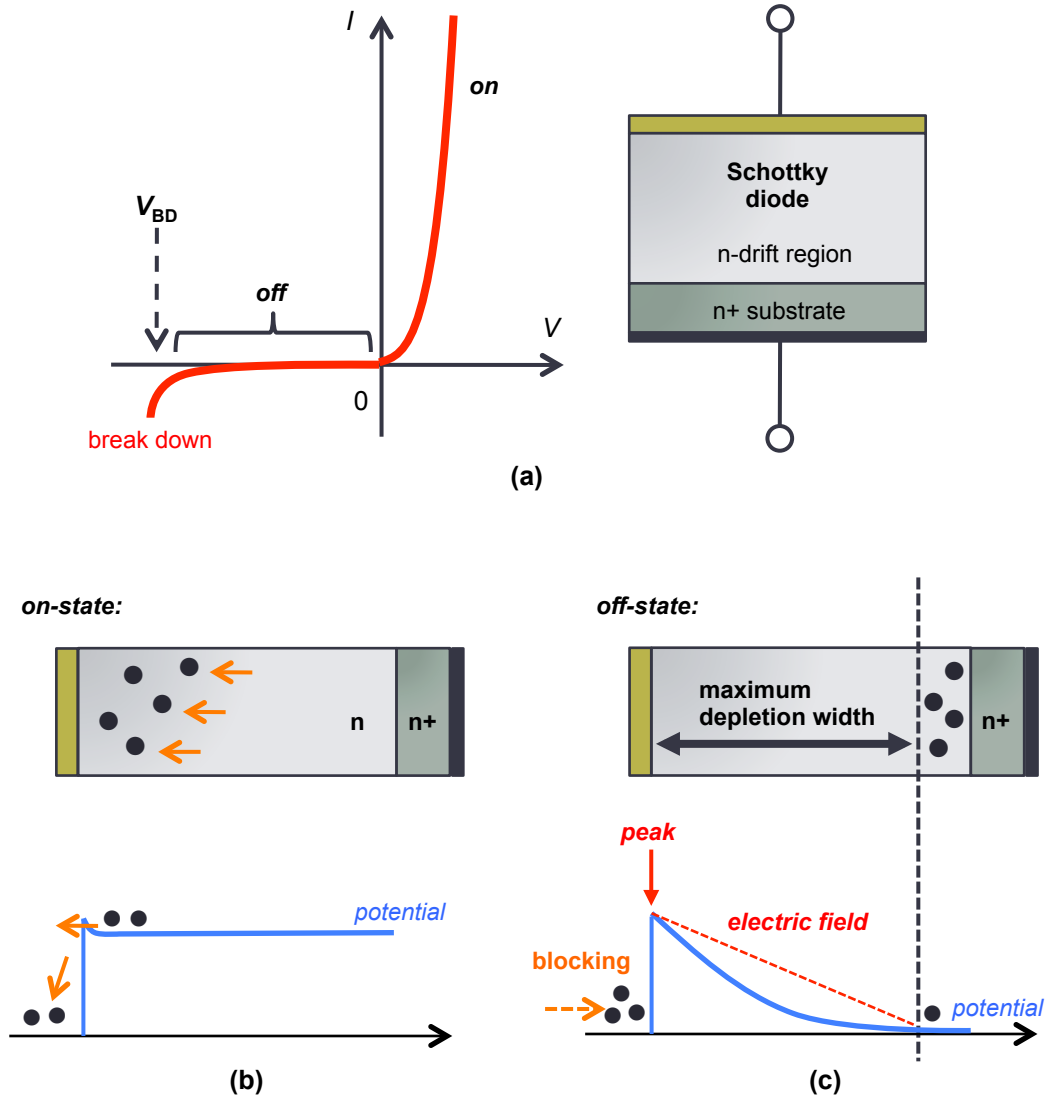


FIG. 1-11. R_{on} , I - V curves, and band diagrams of n-type Schottky diode.

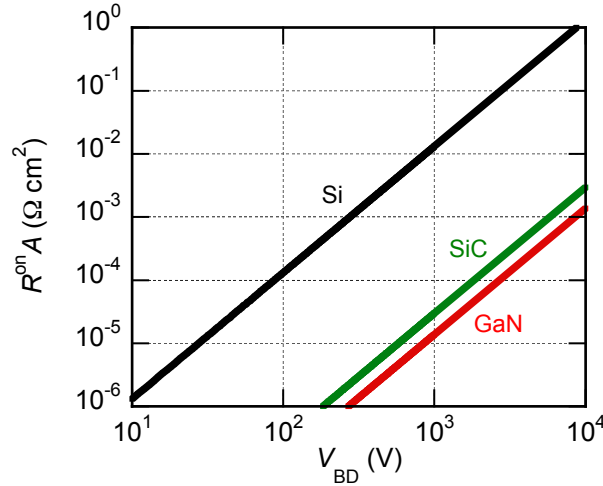


FIG. 1-12. $R_{on}A$ uni-polar limits of Si, GaN, and 4H-SiC as a function of V_{BD} .

1.3.4. Switching properties

As mentioned in the introduction of the present Si power devices, the devices have the parasitic recovery characteristics during turning-off. This also leads to limitation of switching frequencies. Fig. 1-13 schematically shows the band diagrams of the Schottky diode that is a uni-polar device. In this device, $R_{on}A$ is determined by Eq. (1.8). When turning off the device, the depletion width spreads toward the bulk region. In this case, if the no carrier transferring between the metal and semiconductor layers, there is not any current flowing. Fig. 1-14 shows, in contrast, the band diagrams of the pn diode that is a bi-polar device. As shown in Fig. 1-14(a), during on-state, additional electrons are injected from the n+ layer to the n-drift layer in order to cancel the excess hole flow, leading to decreasing the resistivity of the drift region, that is, $R_{on}A$. This is called the conductivity modulation, which is also introduced in the previous section. During turning-off, on the other hand, both electrons and holes that flow into the opposite layers have to return to the n- and p- region, respectively, by spreading the depletion width. Those carriers' flow leads to the reverse recovery current, as schematically shown in Fig. 1-14(b). Fig. 1-15 compares the typical recovery characteristics for the uni-polar and bi-polar devices. In general, the uni-polar devices have small recovery current and their recovery time is shorter owing to the fast redistribution of the electrons. In contrast, the bi-polar device has the larger recovery current than that of the uni-polar devices. The recovery time, in particular, is longer due to the smaller hole mobility. Note that this is not only the case for Si but also GaN and SiC. However, wide-gap materials can realize much more lower on-state resistance even using uni-polar devices. Thus, GaN and Si are very

attractive for high-speed switching operation with the lower on-state resistance.

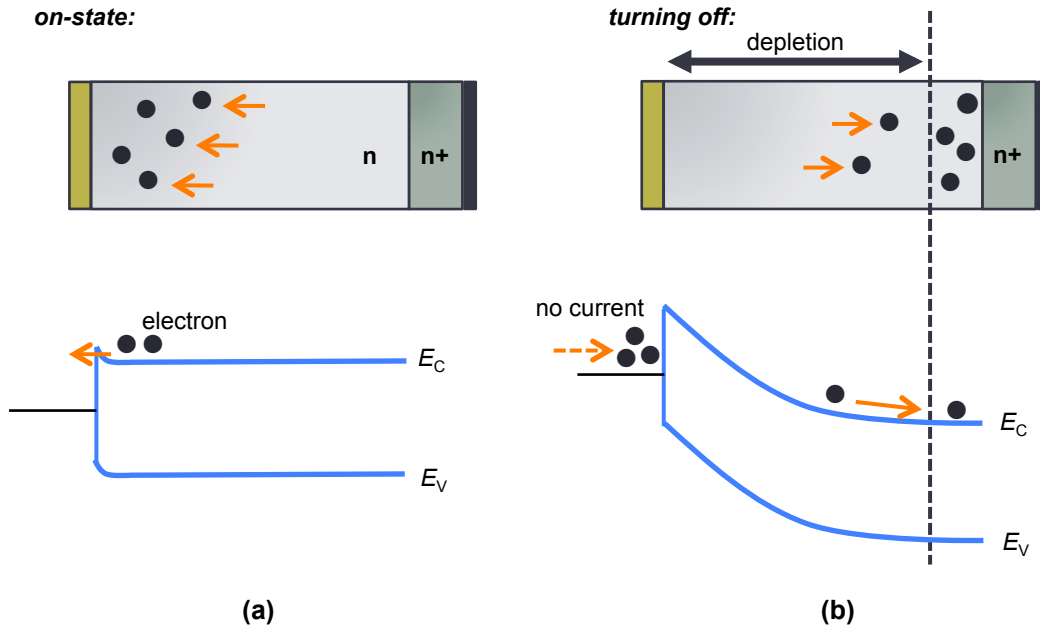


FIG. 1-13. Band diagrams of n-type Schottky junction during (a) on-state and (b) turning-off.

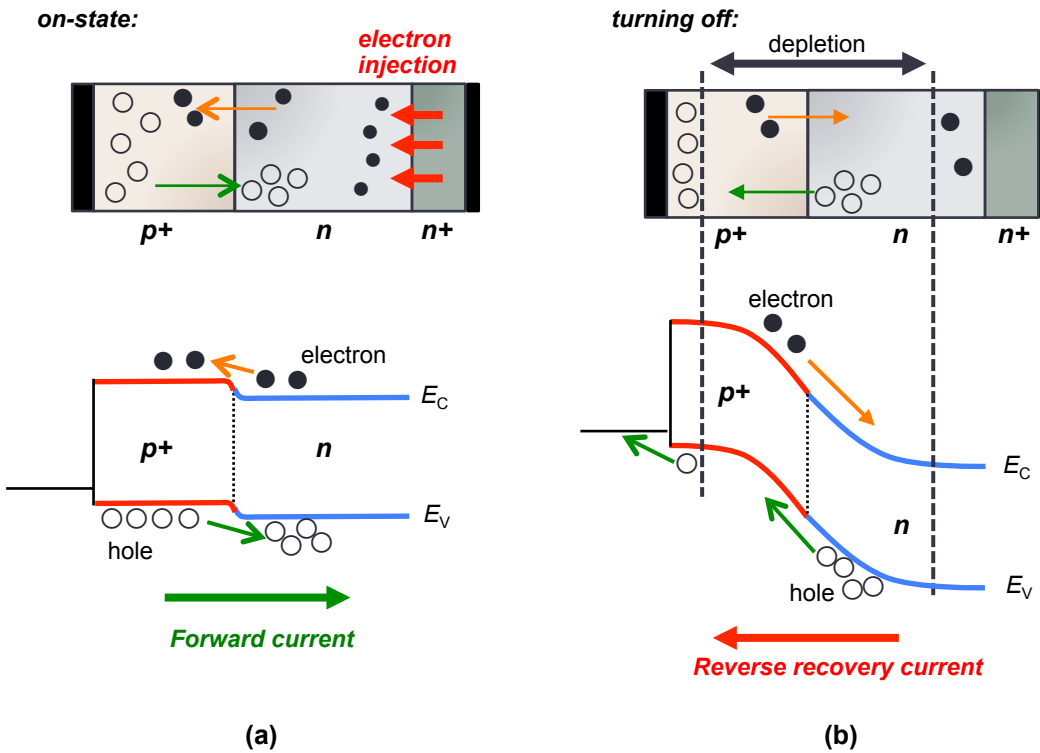


FIG. 1-14. Band diagrams of pn junction during (a) on-state and (b) turning-off.

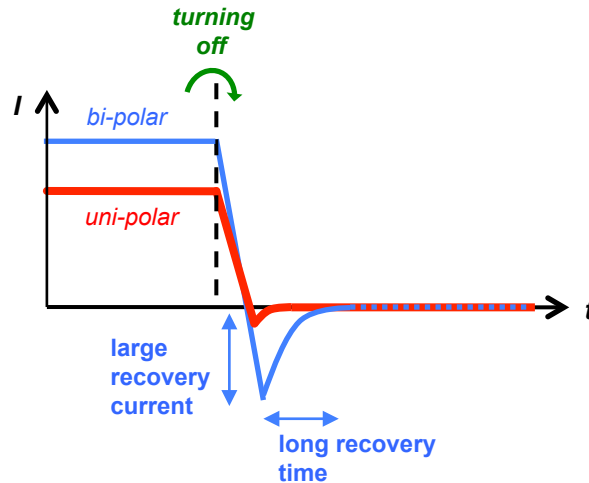


FIG. 1-15. Waveforms of reverse recovery current in Schottky and pn diodes having the same blocking voltages.

1.4. GaN-based transistors

1.4.1. High-electron-mobility transistors

As already introduced above, GaN and SiC are very attractive material which can realize high-frequency and high-power semiconductor devices which has extremely lower on-state resistance than that of Si-based devices. GaN and related-nitride materials, in particular enable us to prepare various types of heterojunctions using alloy semiconductors. Fig. 1-15 shows the typical structure and band diagram of the AlGa_N/Ga_N heterostructure. When the AlGa_N is grown on the Ga_N layer, the high-density and high-mobility electron channel can be generated at its heterointerface due to the spontaneous polarization and piezoelectric polarization. Those Ga_N and AlGa_N layers are generally grown without doping. Therefore, the electron mobility can be higher than that of SiC MOSFETs because there is no impurity scattering at the undoped-AlGa_N/Ga_N interface. Besides, the typical electron density is around 10^{13} cm^{-2} , which is approximately one order higher magnitude than that accumulated at the inversion layer of Si-MOSFETs. The devices having such heterostructure are called “high-electron-mobility transistors (HEMTs).”

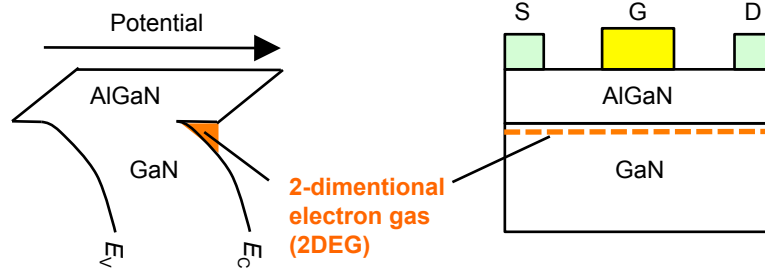


FIG. 1-16. Cross sectional view and band diagram of the AlGaIn/GaN heterojunction.

1.4.2. Insulated-gate structures for GaN-based HEMTs

The as-grown AlGaIn/GaN structure has the 2DEG at equilibrium due to the spontaneous and piezoelectric polarization, resulting in “normally-on” devices. Fig. 1-17 shows the transfer characteristics of the normally-on (depletion-mode) and normally-off (enhancement-mode) devices. In the normally-on device, the drain-source current flows without applying the gate voltage. From the viewpoint of the application to the power conversion circuits such as inverters and converters, however, normally-off operation is absolutely necessary for fail-safe operation.

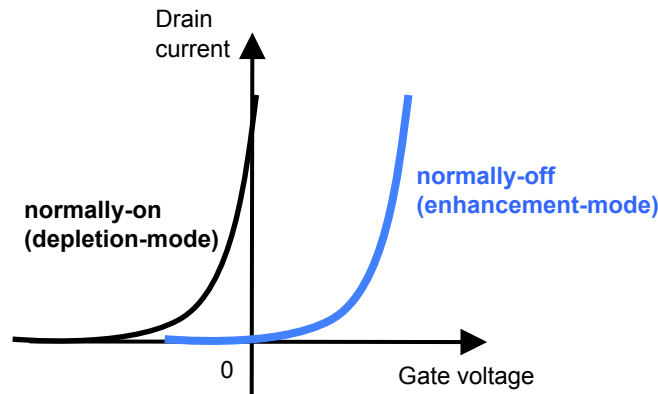


FIG. 1-17. Transfer characteristics of (a) normally-on and (b) normally-off transistors.

In the normally-off operation, the positive gate bias is applied to turn the device on-state. Fig. 1-18 shows the band diagrams of the Schottky and insulated-gate AlGaIn/GaN HEMTs during on-state. The conduction-band discontinuity between $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ and GaN is approximately 0.3 eV, which cannot block the electron flows in the positive bias condition. This leads to the severe increase of gate leakage current in the Schottky HEMTs. As shown in Fig. 1-17(b), on the other hand, the gate insulator can reduce gate leakage current even for the

positive bias owing to the large conduction-band offset at the insulator/AlGaIn interface. As a consequence, the insulated-gate structure realizes the wider dynamic range of the positive gate bias than that for the Schottky HEMTs. Thus, the insulated gate structure is very important for the improvement of operational performance.

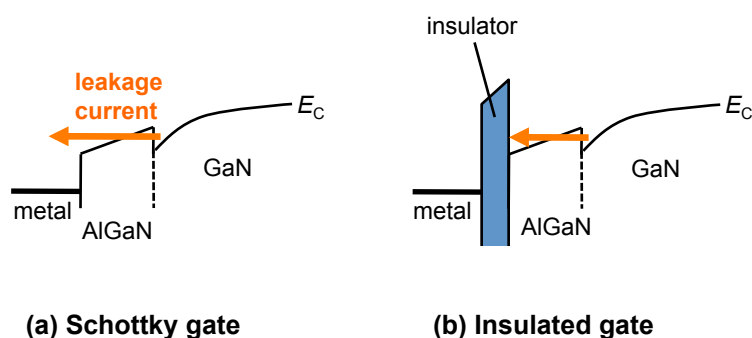


FIG. 1-18. Band diagrams of (a) Schottky HEMT and (b) insulated-gate HEMT under the forward gate bias.

For realizing a good insulated gate, some material properties of insulators should be considered: bandgap, band discontinuity against GaN and AlGaIn, breakdown field, and permittivity. Fig. 1-19 shows the band line up of GaN and major insulator materials: HfO_2 , ZrO_2 , La_2O_3 , Ga_2O_3 , Si_3N_4 , Al_2O_3 , and SiO_2 .⁶ To keep the leakage current low, the materials which have wider bandgap than those of GaN-based materials has to be chosen. High breakdown electric field is also required for operating under high voltage. Besides, because the gate insulator increases the distance between the gate metal and the channel, high permittivity of insulators which prevents pronounce decrease of transconductance is also necessary. SiO_2 has the largest bandgap among those materials in Fig. 1-19, but its permittivity is around 4. HfO_2 is known as a “high-k” material which has the permittivity higher than 20. However, the reported bandgap of HfO_2 film is around 5-6 eV, which cannot prepare enough large band offset against GaN-based materials. Ga_2O_3 is the only material originating from GaN. The reported bandgap of Ga_2O_3 prepared by electro chemical oxidation of GaN, however, showed relatively small bandgap as well as Si_3N_4 and HfO_2 .

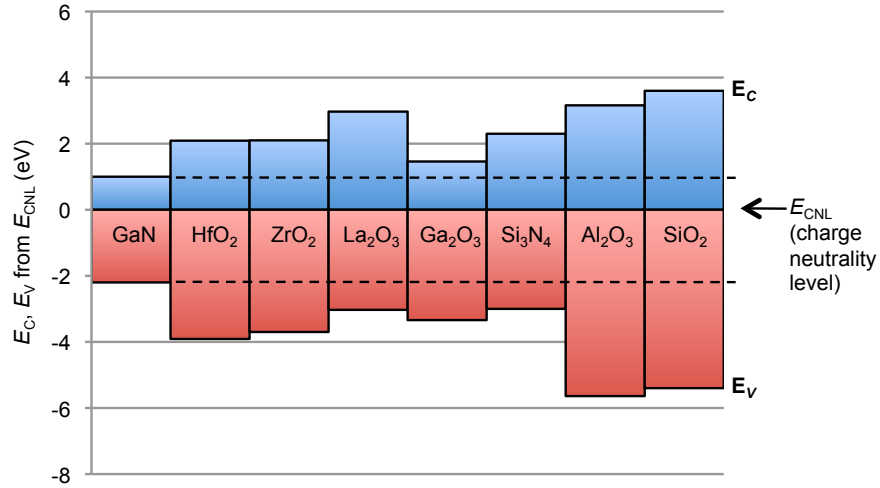


FIG. 1-19. Band lineup of GaN, AlGaIn and major insulators materials.

In addition to those properties, low electronic state densities at the insulator/semiconductor interface are absolutely necessary. The electronic states can be formed in the bandgap of the interface states, which are generally caused by the disorder and reconfiguration of chemical bonding structures and chemical reactions between the insulator and the semiconductor. If the unintentional exchange of the carriers at those electronic states, they may affect various characteristics of the devices. Therefore, it is indispensable to realize well controlled interface properties in the insulated-gate devices.

1.5. Objective

GaN-based HEMTs are very attractive for realizing the ultra low-loss power transistors which are applicable next generation power electronic systems owing to their excellent physical properties. To achieve normally-off operation, insulated-gate structures absolutely necessary for suppressing gate leakage current under a forward gate bias operation. Al₂O₃ is one of the best candidates for gate insulators in GaN-based devices. As shown in Figs. 1-19, the typical values of bandgap for the Al₂O₃ film are 7 – 9 eV and its permittivity has been estimated to be 8 – 10. Recently, GaN-based metal-oxide-semiconductor (MOS) HEMTs using the Al₂O₃ as an insulator have been demonstrated by many groups. However, the properties of the Al₂O₃/GaN-related material interfaces have not been understood, and the fabrication process is not well established yet. Besides, in the MOS-HEMT structures, the insulator/semiconductor interface is usually formed on the AlGaIn/GaN heterostructures, resulting in the existence of two interfaces under the gate electrode. In this case, it is rather difficult to characterize interface states in the MOS-HEMT structures compared with

standard MOS structures having a single semiconductor layer. Moreover, the wide bandgap of GaN-based materials also make the evaluation of interface state difficult due to the extremely low emission rate of electrons trapped at the interface states. Indeed, there are few reports on the MOS interface states in the GaN-based MOS-HEMTs and their relationship to the device characteristics.

In this thesis, the effects of fabrication processes on the electrical properties of $\text{Al}_2\text{O}_3/\text{GaN}$ structures prepared by atomic layer deposition (ALD) are investigated, which include interface state densities. The interface state density distributions of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs also attempt to be determined. The relationship between the evaluated interface states and the resulting electrical properties are then discussed.

1.6. Outline

The rest of this thesis is organized as follows.

Chapter 2 explains basics on physical properties of GaN-related semiconductors and AlGaIn/GaN heterostructures. Furthermore, proposed device structures, processes, and issues of GaN-based HEMTs are introduced.

Chapter 3 introduces the origin and effects of the electronic states induced at the interfaces between the insulators and GaN-based materials. In addition to the basic theory of metal-oxide-semiconductor (MOS) structures, the effects and evaluation method of the interface states are explained, focusing on the capacitance-voltage (C - V) characteristics of the MOS structures.

Chapter 4 explains the model of atomic layer deposition method used for depositing the Al_2O_3 gate insulator, followed by the characterization of optical and chemical properties of Al_2O_3 films prepared by ALD.

Chapter 5 investigates the effects of fabrication processes on the electrical properties of $\text{Al}_2\text{O}_3/\text{n-GaN}$ MOS structures prepared by ALD, including the interface state densities. The ohmic-first process with a SiN surface protection is proposed both for suppressing gate leakage current and realizing low electronic state densities at the $\text{Al}_2\text{O}_3/\text{n-GaN}$ interface. Furthermore, an additional surface control process using an N_2O -radical treatment is demonstrated, leading to a marked decrease of the interface states.

Chapter 6 discusses the relationship between the interface state densities and the electrical properties of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs. The N_2O -radical treatment is also applied to the MOS-HEMT for reducing the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states. To estimate the interface states on the AlGaIn/GaN heterostructures, two types of C - V analyses are

proposed: the photo-assisted and frequency dependent $C-V$ measurements. The reduced interface state densities in the MOS-HEMTs are estimated to be 40 % compared to those without the N_2O -radical treatment. The impact of the reduced interface states on the electrical properties of the MOS-HEMTs is then investigated. The higher maximum drain-source current density and the stable threshold voltage variation are obtained for the N_2O -radical treated MOS-HEMTs.

Chapter 7 summarizes the results presented in this thesis.

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Chapter 2.

Physical properties and device structures of GaN and related heterostructures

2.1. Basic properties of III-N semiconductor materials

2.1.1. Crystal structures

GaN and related materials, III-N semiconductors, have the hexagonal wurtzite structure due to the relatively strong ionicity of chemical bonds between cation and anion atoms (e.g. Ga and N, respectively) in the crystals. Fig. 2-1 schematically compares unit cells of the wurtzite and zincblende structures. In the wurtzite structure, the cation and anion atoms align in the same direction (vertically, in this case), while in the zincblende structure they align rotating by 60 degrees. Such symmetrical configuration with the ionic alignment leads to characteristic polarization effects which will be introduced later in this chapter.

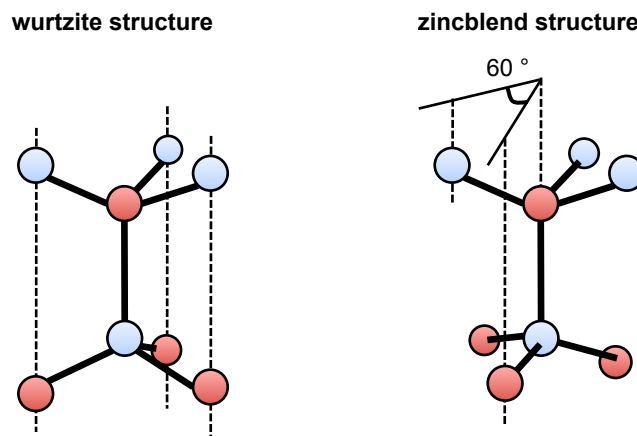


FIG. 2-1. Schematic illustrations of wurtzite and zinc blende crystal structures.

Figure 2-2 shows the definition of lattice constants and orientations in the hexagonal wurtzite crystal. Note that $[0001]$, the “c-axis” direction as shown in this figure, is the same as that in which the strong ionicity exists. Therefore, the polarization characteristics can be obtained along the c-axis. Accordingly, the (0001) orientation perpendicular to c-axis, “c-plane”, is called the “polar plain” after the polarization effects. Indeed, GaN-based HEMTs are generally produced on the c-plane of GaN-related materials. On the other hand, the normal direction of c-axis defined as a-axis and other direction weaken the ionicity in the crystal. As shown in Fig. 2-2(b), the $(11-20)$ and $(1-100)$, “non-polar” orientations, called a-plane and m-plane, respectively, do not show the polarization effects because of their atom configurations. Furthermore, the $(10-12)$ orientation is called a “semi-polar plane”, which is defined using a- and c-axes. Those a-, m-, and r-planes are utilized in III-V LEDs and LDs for controlling the polarization to suppress carrier separation due to the internal electric field.

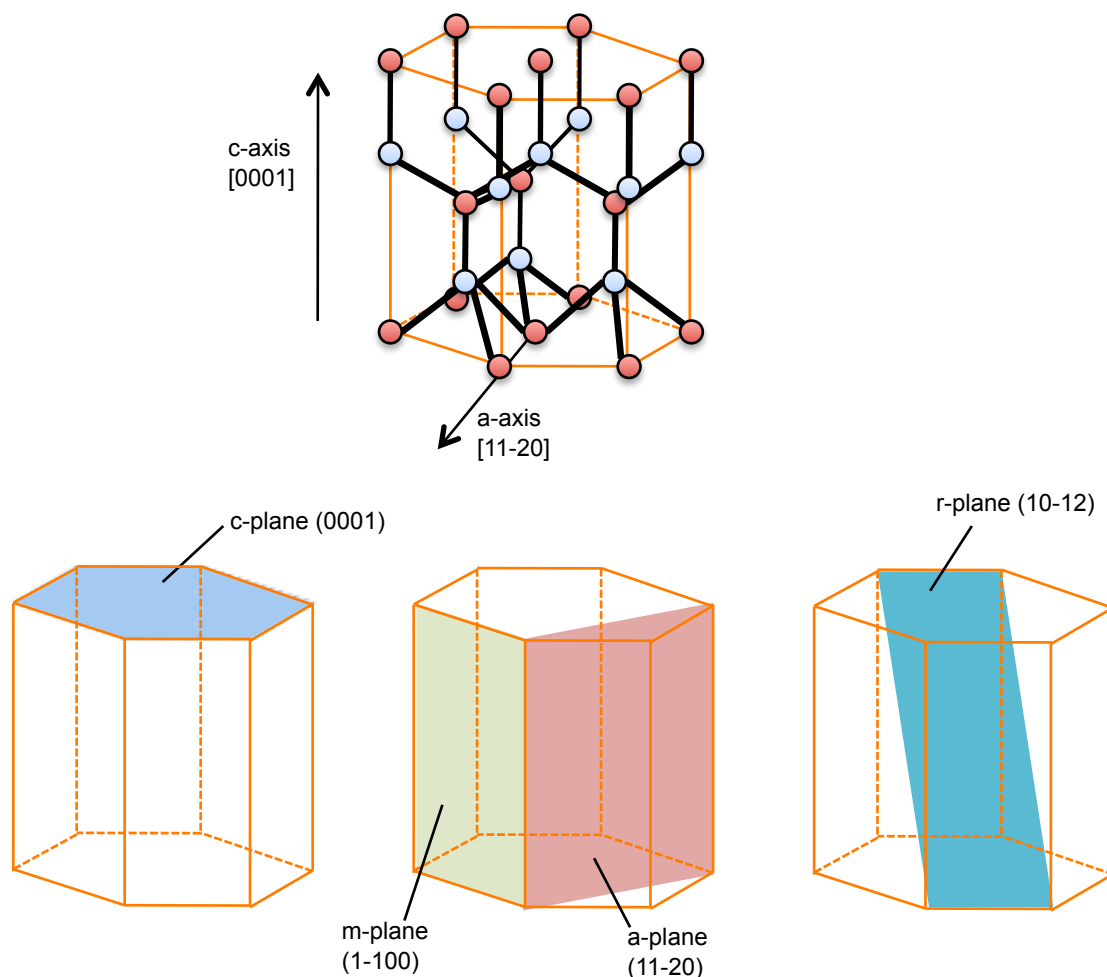


FIG. 2-2. Schematic illustrations of wurtzite crystal and its directions and orientations.

Also as shown in Fig 2-3, lattice constants of the wurtzite crystal are also defined as two ways, a and c . Each lattice constant is dependent on the ionicity in the crystal. The ionic strength between cations and anions in the III-N family are obtained as follow,

$$\text{AlN} > \text{GaN} > \text{InN}.$$

In general, the stronger ionicity leads to a smaller lattice constant. Table I shows the lattice constants, c and a , in the III-N crystals, GaN, AlN, and InN.¹

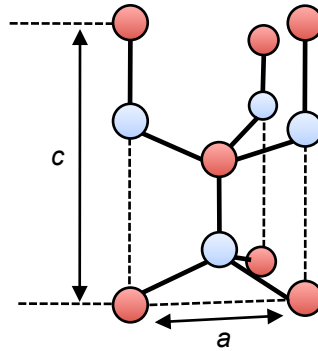


FIG. 2-3. Definition of lattice constants of wurtzite crystal.

Table I. Lattice constants of III-N semiconductors.

	GaN	AlN	InN
a (Å)	3.189	3.112	3.533
c (Å)	5.186	4.982	5.693

2.1.2. Physical properties of III-N semiconductors

Table II summarizes the bandgap, the intrinsic carrier density, the transition type, the electron mobility, and the saturation electron velocity of Si and III-N semiconductors. As already mentioned in Chapter 1, the bandgap of GaN is approximately three times as large as that of Si. In addition, the stronger ionicity in the semiconductor leads to the larger bandgap. Therefore, AlN shows the largest bandgap in the III-N family, while InN shows the smallest one. The larger bandgap shows the lower concentration of intrinsic carriers, leading to the stable operation at high temperatures. Besides, the breakdown electric fields increase with their bandgap. Consequently, AlN shows the highest breakdown electric field in those semiconductors.

GaN and other III-Ns have the direct bandgap, while Si, GaAs, and SiC have the indirect one. In the direct bandgap, photons can be emitted from the valence band to the conduction band without any phonons. This is the important factor for realizing the efficient LEDs. Although the electron mobilities of the III-Ns are inferior to that of Si, the hexagonal wurtzite structures generally show the higher electron saturation velocities than those of Si and other compound semiconductor materials having the zincblende structures, as shown in Fig. 2-4. As already mentioned in Chapter 1, the higher saturation velocity and the higher breakdown electric field also give the superior transport properties in the high electric field condition, that is, the high-frequency operation.

Table II. Physical properties of Si and III-N semiconductors.

	Si	GaN	AlN	InN
Bandgap, E_G (eV)	1.1	3.4	6.0	0.8
Intrinsic carrier density, n_i (cm^{-3} , at RT)	1.4×10^{10}	1.8×10^{-10}	2.23×10^{-31}	1.29×10^{12}
Transition type	indirect	direct	direct	direct
Electron mobility, μ_e (cm^2/Vs)	1350	1200	300	250
Electron saturation velocity, v_e (cm/s)	1.0×10^7	2.5×10^7	-	4.0×10^7

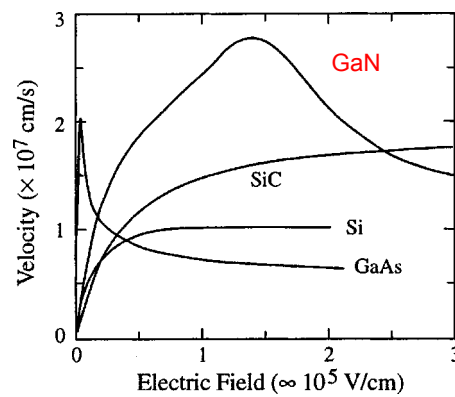


FIG. 2-4. Electron velocity vs. applied electric field taken from Ref. 1.

2.2. AlGaN/GaN heterojunction

2.2.1. Alloys and heterojunctions using III-N semiconductors

III-N semiconductors also enable us to realize various types of III-N alloys having different bandgap and lattice constant. Fig. 2-5 shows the relationship between lattice constant and bandgap for GaN, AlN, InN, and their alloys. In InGaN, the bandgap can be modulated from that of InN to that of GaN, that is, 0.7 – 3.4 eV, which corresponds to the photon energy range between infrared and ultra-violet (UV) regions. Indeed, InGaN is expected to be applied to the LEDs, LDs, and solar cells for the wide photon energy range. InAlN, in addition, covers deep UV range due to the wide bandgap of AlN. InAlN has an additional unique feature for HEMTs. When the In composition ratio is 13 %, the lattice constant a of $\text{In}_{0.13}\text{Al}_{0.87}\text{N}$ is in accordance with that of GaN can be prepared on the c-plane of GaN layer. Besides that, the large conduction-band offset at the InAlN/GaN interface can be a big merit for the HEMT application. At the moment, however, it is rather difficult to growth high-quality InGaN and InAlN with the high In composition ratio.

AlGaN is an alloy of AlN and GaN, which covers the photon energy range corresponding to blue and deep-UV ranges. Although deep-UV LEDs using AlGaN have been reported recently, the AlGaN/GaN heterojunction are the most popular application for the HEMTs shown in the previous chapter. Comparing with the InAlN/GaN system, AlGaN and GaN have no lattice-matching selections, resulting in the tensile-straining in the AlGaN/GaN heterostructures. This feature also leads to the polarization effects being explained in the following section.

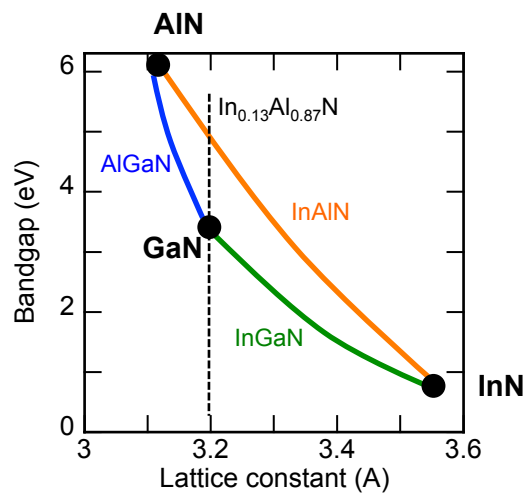


FIG. 2-5. Lattice constant vs. bandgap relations for III-N semiconductors.

2.2.2. Polarization effects in III-N heterojunctions

As shown in Fig. 2-2(a), III-Ns grown on the c-plane leads to the “spontaneous” polarization due to the symmetric configuration of cations and anions in the c-axis direction. The calculated spontaneous polarization charge densities P_{sp} for GaN, AlN, and InN taken from Ref. 2 are

$$\text{GaN: } P_{sp} = -1.8 \times 10^{13} \text{ /cm}^2,$$

$$\text{AlN: } P_{sp} = -5.1 \times 10^{13} \text{ /cm}^2,$$

$$\text{GaN: } P_{sp} = -2.0 \times 10^{13} \text{ /cm}^2.$$

The polarization charges are induced both on the c-plane and the opposite c-plane, as shown in Fig. 2-6. At the (0001) Ga-face surface, the negative charges are induced by the cation atoms, Ga, Al, and In, resulting in the internal electric field in the [000-1] direction. At the (000-1) N-face surface, on the other hand, the internal electric field shows the [0001] direction.

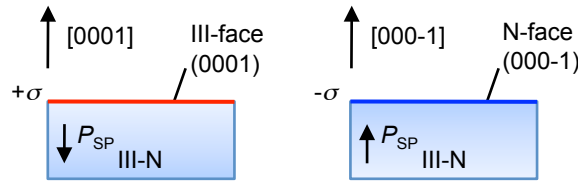


FIG. 2-6. Spontaneous polarization and internal electric fields in III-N semiconductors.

In addition to the spontaneous polarization, the lattice strain and compression due to the lattice-mismatched junction lead to the piezoelectric polarization. Let us consider this polarization effect in the AlGaN/GaN heterojunction. As schematically shown in Fig. 2-7, the AlGaN layer which has the smaller lattice constant a than that of GaN is the strained in the horizontal direction so that it cancels the lattice constant difference. Consequently, the compression of the AlGaN in the horizontal (c-axis) direction leads to the internal electric field due to the piezoelectric polarization. As shown in Fig. 2-7, in the heterojunction grown on the (0001) orientation, the piezoelectric field shows the [000-1] direction which is the same as that of the spontaneous polarization. Therefore, by either those spontaneous or piezoelectric polarization or by both of them, the potential of the heterojunction is bended downward, leading to accumulation of the two-dimensional electron gas (2DEG).

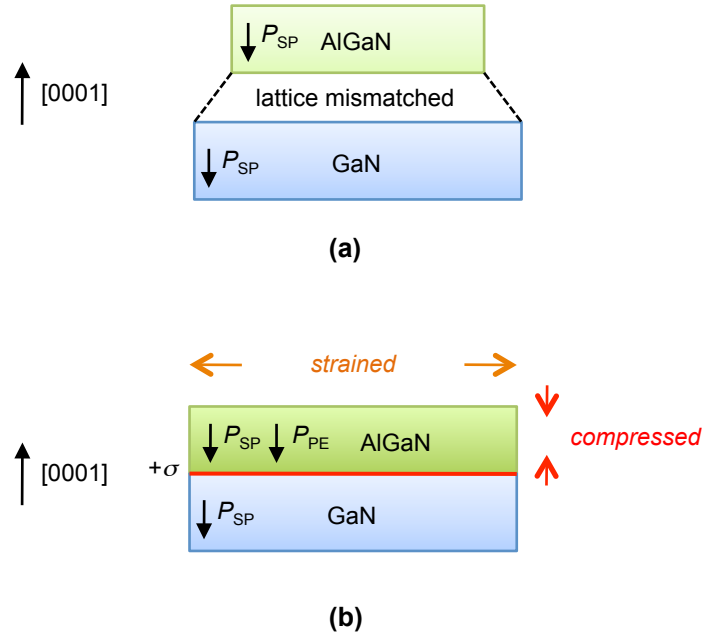


FIG. 2-7. Piezoelectric polarization in III-N heterostructures.

2.2.3. Two-dimensional electron gas induced at III-N heterointerfaces

Figure 2-8 shows the band diagram of the AlGaN/GaN heterojunction at equilibrium. As mentioned above, the band bended downward by the internal electric fields create the potential quantum well at the AlGaN/GaN interface. As a result, the 2DEG with the high electron density is induced at the heterointerface. The electron mobility of such 2DEG is not affected by the impurity scattering because those internal electric fields are induced even in un-doped III-N systems. Note that the origin of 2DEG has not been cleared yet but under discussion. The III-N electron devices utilizing such 2DEG are known as “heterojunction-fieled-effect transistors (HFETs)” or “high-electron-mobility transitors (HEMTs)”.

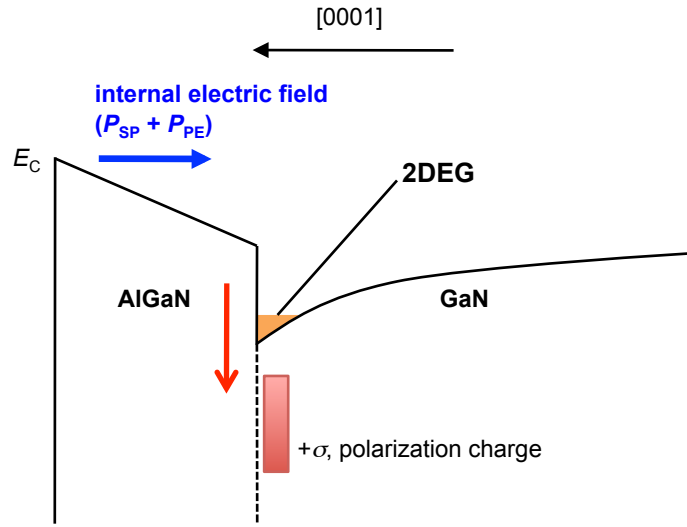


FIG. 2-8. Conduction-band diagram of AlGaN/GaN heterostructure.

Table III shows the polarization charge density and the conduction-band offsets reported for the AlGaN/GaN, InAlN/GaN, and InAlN/InGaN heterostructures.³ ΔP_0 is the spontaneous polarization charge density difference between the barrier and channel layers. P_{total} is the total polarization charge density at the heterointerface as described using ΔP_0 and the piezoelectric polarization charge density P_{PE} ,

$$P_{\text{total}} = \Delta P_0 - P_{\text{PE}}.$$

When the Al composition ratio is 20 % in the AlGaN/GaN heterostructure, the resulting P_{total} is $1.18 \times 10^{13} \text{ cm}^{-2}$, which is one order of magnitude higher than the inversion carrier densities at Si and SiC MOS interfaces. Using $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ as a barrier layer of HEMTs, the lattice-matched InAlN/GaN heterojunction shows the P_{PE} of zero. However, the higher P_{SP} of the InAlN gives the positive ΔP_0 with the two times higher density compared with that of AlGaN, resulting in P_{total} of $2.73 \times 10^{13} \text{ cm}^{-2}$. The larger conduction-band offset at the InAlN/GaN interface is also expected to suppress the gate leakage current under a forward gate bias. In Ref. 3, Kuzmik also mentioned that the piezoelectric polarization of the InGaN channel layer may realize the much more higher-density 2DEG and the higher band offset as compared with other III-N heterostructures.

Table III. Polarization effect parameters and conduction-band offset of III-N heterostructures taken from Ref. 3.

	ΔP_0 (cm ⁻²)	ΔP_{PE} (cm ⁻²)	ΔP_{total} (cm ⁻²)	ΔE_c (eV)
Al _{0.2} Ga _{0.8} N/GaN	6.5×10^{12}	5.32×10^{12}	1.18×10^{13}	0.3
In _{0.17} Al _{0.83} N/GaN	2.73×10^{13}	0	2.73×10^{13}	0.68
In _{0.17} Al _{0.83} N/In _{0.1} Ga _{0.9} N	2.71×10^{13}	1.1×10^{13}	3.81×10^{13}	>0.68

In case of the AlGaN/GaN heterojunction, the P_{SP} is proportional to the Al composition ratio of AlGaN, leading to the higher-density 2DEG. The typical Al composition ratio of AlGaN which is usually used for the HEMTs is around 20 – 30 %, resulting in the 2DEG density of around 10^{13} cm⁻². Fig. 2-9 shows the relationship between the 2DEG density and the thickness of AlGaN with the Al composition ratio of 24 %.⁴ Ideally, the 2DEG density increases with the AlGaN thickness due to the increase of P_{PE} . In the real case, the lattice strain can be relaxed with the thicker growth of AlGaN, resulting in the saturation of the 2DEG density. Furthermore, the thinner AlGaN also relaxes the compression of itself, leading to decrease of P_{PE} . As a consequence, when the resulting ΔP_0 is zero, the heterojunction system does not create the 2DEG channel. In the AlGaN/GaN heterostructure, thus, the 2DEG density can be modulated utilizing the Al composition ration and the thickness of AlGaN barrier layer. In particular, the 2DEG density controllability is the one of the important factors to obtain a normally-off operation.

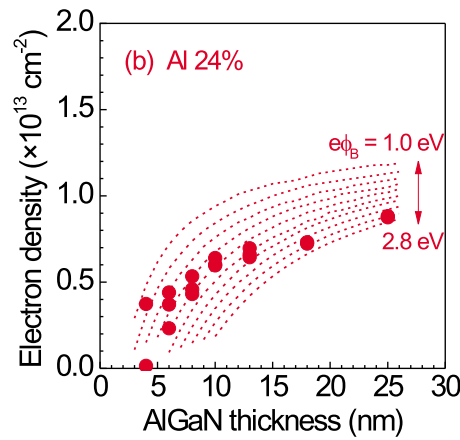


FIG. 2-9. Sheet charge density vs. AlGaN thickness taken from Ref. 4.

2.3. Device structures and current issues of GaN HEMTs

2.3.1. Vertical structures vs. lateral structures

Two types of GaN-based HEMT structures have been proposed: the vertical and the horizontal structures. Figs. 2-10(a) and (b) show the vertical and horizontal GaN-based HEMTs. For the both structures, the blocking voltage is applied between the source and drain electrodes during the off-state. The vertical device has the similar structure to that of Si MOSFETs.⁵ The maximum blocking voltage is dependent on the thickness of the GaN drift layer. As mentioned in the previous chapter, the thickness of the drift layer can be thinner at the same blocking voltage owing to the high breakdown electric field of GaN, leading to the extremely low on-state resistance with the higher blocking voltage as compared to the Si MOSFETs and IGBTs. However, this device is fabricated on the GaN substrate with the thickness of 300 - 500 μm . At the moment, it is rather difficult to fabricate such thick GaN substrate with appropriate diameters and costs. On the other hand, the lateral GaN devices can be grown on not only the GaN substrate but also other materials such as Si, sapphire, and SiC. Si substrate, in particular, is the most convenient material of the semiconductors. In addition, as compared with the vertical device, the lateral device has the 2DEG region not only underneath the gate electrode but also at the access region, leading to the lower on-state resistance and higher-frequency characteristics. Using such lateral devices, the monolithic integration of GaN-HEMTs has been demonstrated by Panasonic as shown in Fig. 2-11.⁶ They have demonstrated “1-chip inverter circuit” with the blocking voltage of 600 V. This is the only case of the lateral GaN-devices. However, in the lateral devices, the high blocking voltage is applied laterally between the source and drain. In this case, the peak electric field is applied at the gate edge, leading to hard breakdown of the devices. Consequently, the blocking voltage of the lateral devices should be lower than that of the vertical devices. Furthermore, when the substrate is Si, sapphire, SiC or other materials in lattice-mismatched, the various types of dislocation can be induced, leading to the unexpected degradation of the device operation.

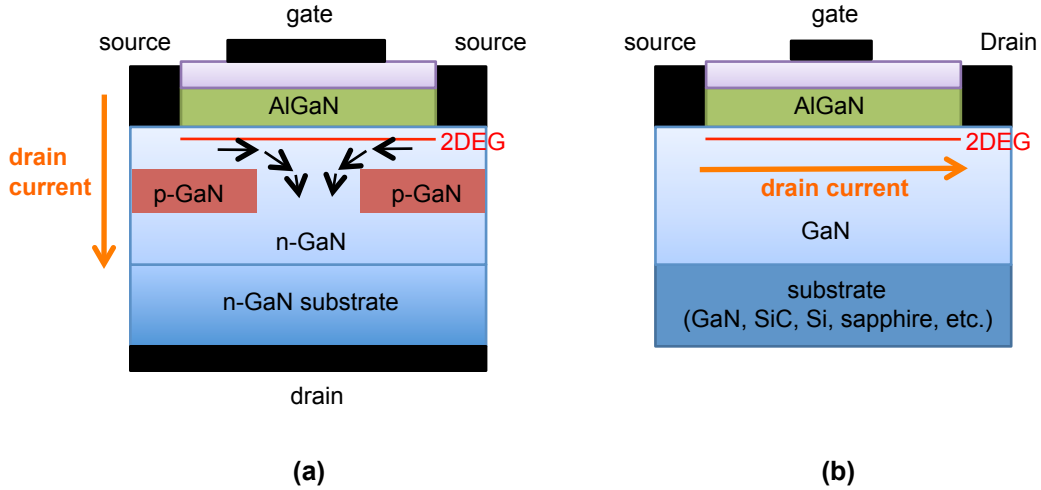


FIG. 2-10. (a) Vertical device and (b) lateral devices using AlGaN/GaN heterostructures.

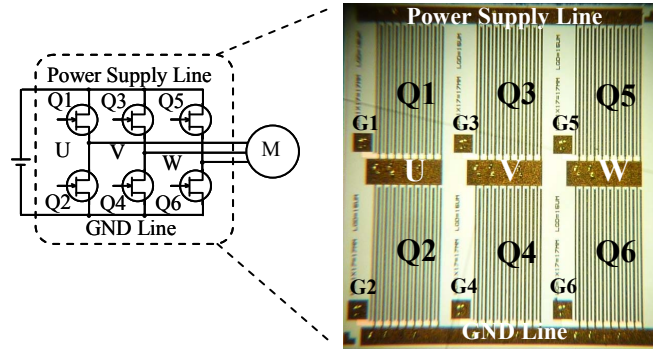


FIG. 2-11. 1-chip inverter using monolithic integration of GaN-HEMTs reported by Panasonic taken from Ref. 6.

2.3.2. Proposed structures for normally-off GaN HEMTs

As already mentioned in the previous section in this chapter, the as-grown AlGaN/GaN structure has the 2DEG at equilibrium due to the spontaneous and piezoelectric polarization, resulting in “normally-on” characteristics. From the viewpoint of the application to the power conversion circuits such as inverters and converters, however, normally-off operation is absolutely necessary for fail-safe operation. The normally-off GaN-HEMTs can be realized using the appropriate structures or circuits which have been reported by many groups. Here, Fig. 2-12 summarizes the reported structures for the GaN-HEMTs.

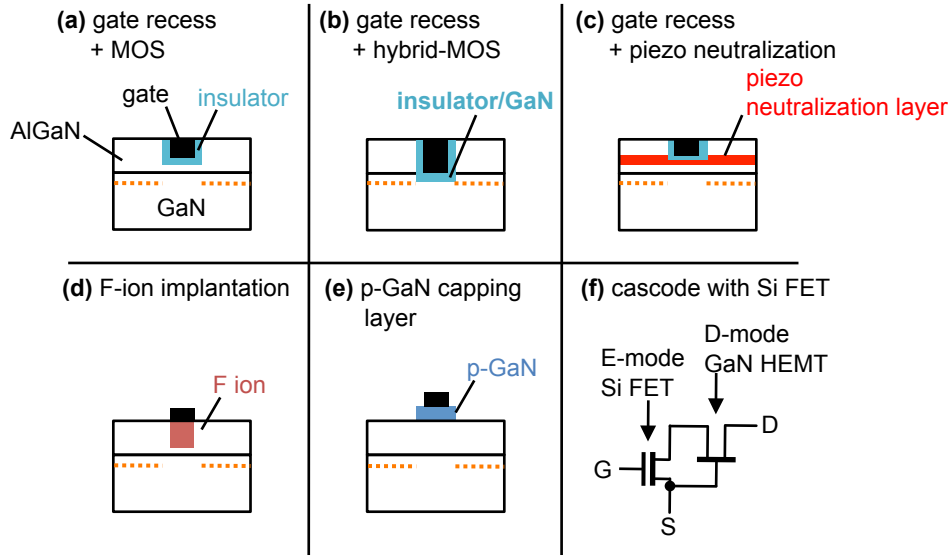


FIG. 2-12. Proposed device and circuit structures for realizing normally-off characteristics.

(a) Gate recess + MOS-HEMTs

Thinner AlGaN barrier layer cannot produce 2DEG because of weakened polarization. Using this feature, the selective-area cancellation of 2DEG can be realized by etching the thick barrier layers or re-growing on the thin layers. In general, the selective-area etching with the dry process is often used for realizing normally-off operations. Fig. 2-13 shows the state-of-the-art normally-off GaN-HEMT reported by Fujitsu.⁷ They also used the inductively coupled plasma process for etching the barrier layers. However, it is not easy to control the etching thickness precisely using the dry etching. Indeed, the current recess gate technology has the threshold-voltage instability issues. The dry etching often induces the degradation of chemical bonding structures at the semiconductor surfaces. Note that such operational issues are probably due to the surface or interface states.

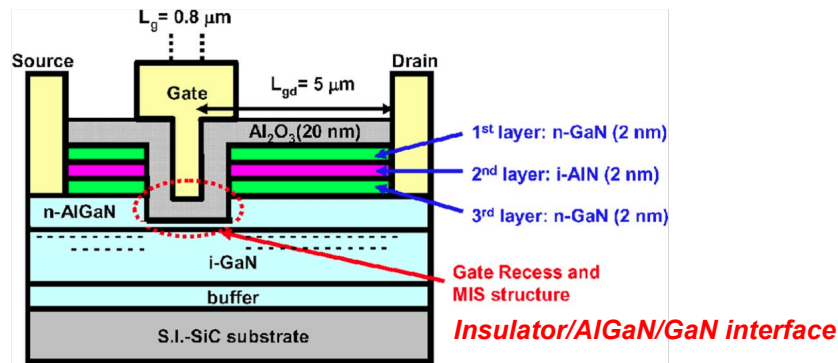


FIG. 2-13. Gate recess + MOS gate structure taken from Ref. 7.

(b) Gate recess + hybrid MOS-FETs

As shown in Fig. 2-14, if the AlGa_N is etched totally, the MOS interface is formed at the oxide/GaN. Such devices are called “hybrid-MOSFETs” as recently reported by Furukawa Electric⁸ and Rohm⁹. In this case, the threshold voltage is rather stable as compared to the recessed HEMTs. However, its electron mobility should be lower than that of the HEMTs.

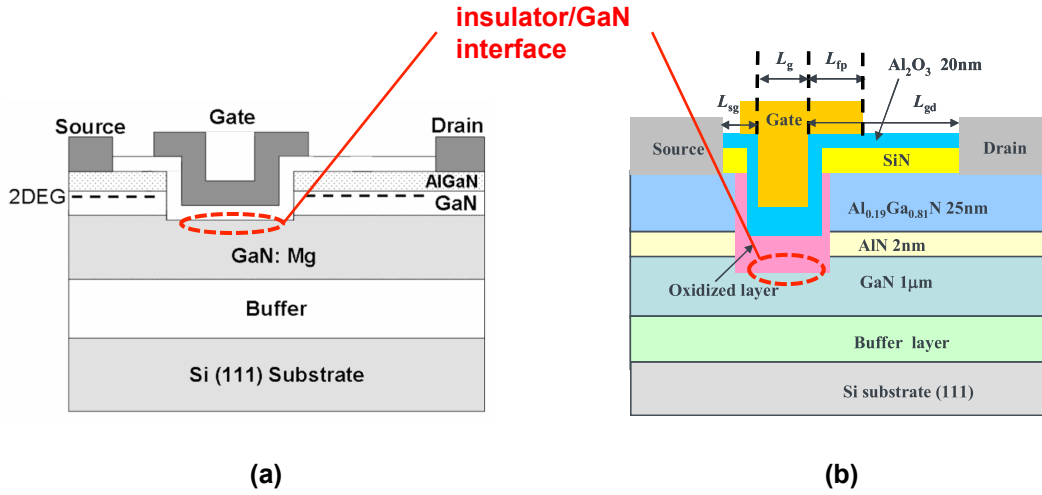


FIG. 2-14. Gate recess + hybrid MOS gate structures taken from Refs. 8 and 9.

(c) Piezo neutralization structure

NEC has proposed the unique structure for the barrier layers to obtain the less threshold voltage variation than the conventional recess technique.¹⁰ As shown in Fig. 2-15, the piezo neutralization (PNT) layer is formed as an additional barrier layer between 1st and 2nd AlGa_N layers. The Al composition ratio of the PNT layer is 7 %, which can neutralize the piezo electric fields of the 1st AlGa_N layer. If the 2nd layer is removed by the etching process, the PNT layer cancels the 2DEG, resulting in the normally-off operation. Interestingly, the resulting threshold voltage does not depend on the thickness of the PNT layer. However, the obtained threshold voltage is +0.3 V, which is lower than that of the conventional Si MOSFETs.

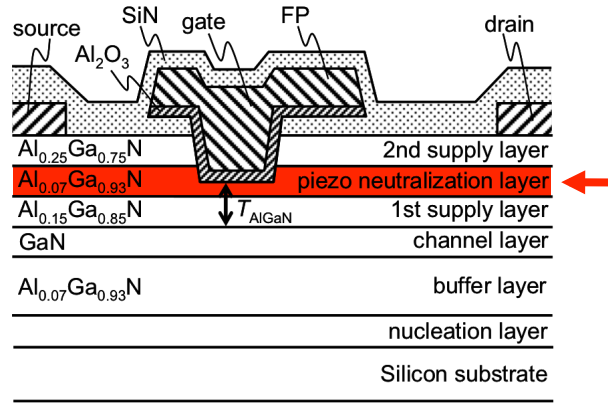


FIG. 2-15. Cross-sectional view of normally-off GaN-HEMT having piezo neutralization layer taken from Ref. 10.

(d) F-ion implantation + MOS-HEMTs

When the AlGaIn barrier layers are implanted with F ions, the negative charges of F ions can raise up the potential of AlGaIn, leading to the depletion of 2DEG. Using such a technique, Cai *et al.*¹¹ has been proposed the normally-off GaN HEMTs having F-ion implantation for the channel region. Etching-free process, in particular, is the big advantage for realizing the normally-off operation.

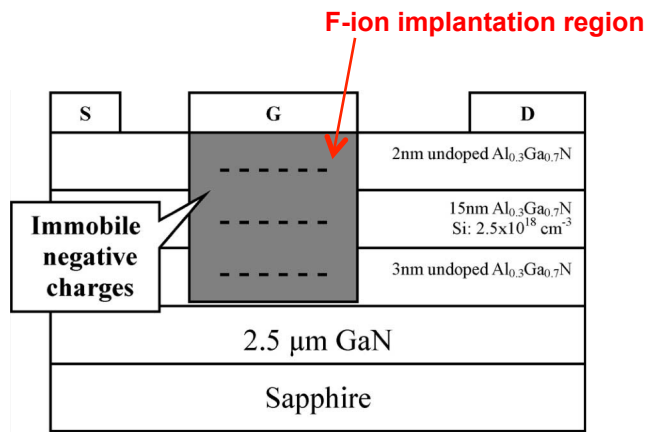


FIG. 2-16. Proposed normally-off structure having F-ion implantation region taken from Ref. 11.

(e) p-GaN or AlGaIn capping layer on GaN-HEMTs

In addition to the F-ion implantation, there is another way to achieve the normally-off operation without etching processes. Using a p-GaN capping layer over AlGaIn/GaN heterostructure, the potential is lifted up as shown in Fig. 2-17(a). When the capping layer is prepared on the channel layer, this leads to selective depletion of 2DEG, that is, the

normally-off operation. Uemoto et al.¹² have reported the normally-off GaN-HEMT with selectively regrown a p-AlGaN layer, as shown in Fig. 2-17(b). They also mentioned the conductive modulation by the hole injection from p-type layer. Therefore, such devices are called “gate injection transistors (GITs)”. Although the reliability issues on regrowth of p-type layers still remain, there is an advantage that the GIT can realize the normally-off operation without insulated-gate structures because of the relatively high Schottky barrier height in the p-GaN gate structures.

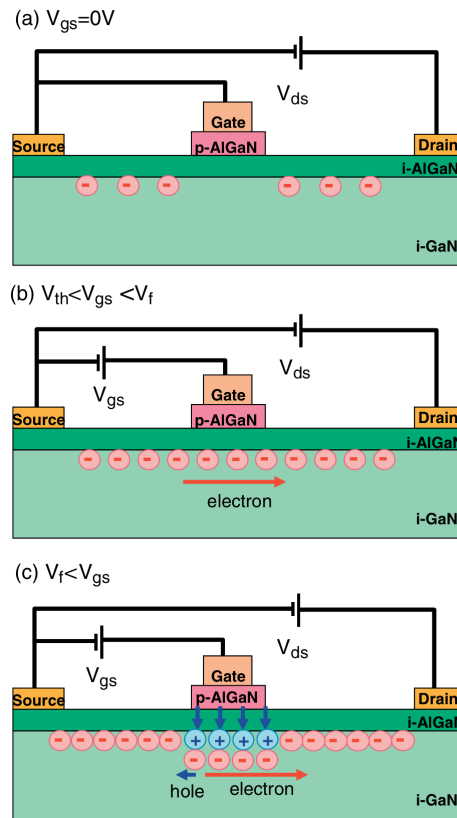


FIG. 2-17. Gate injection transistors (GITs) having p-AlGaN capping layer taken from Ref. 12.

(f) Cascode to Si MOSFETs

There is a unique way to achieve the normally-off characteristics using normally-ON GaN-HEMTs. As shown in Fig. 2-18, cascode circuit using normally-off devices can realize the normally-off operation even with the normally-on GaN HEMTs.¹³ In this circuit, standard Si MOSFET is connected to the GaN-HEMT which has the similar on-state resistance. Although the blocking voltage of the Si MOSFET is much more smaller than that of the GaN-HEMT which has the same on-state resistance, the critical voltage under the off-state is applied only between the gate and drain terminals in the GaN HEMT. Therefore, the blocking

voltages are governed by those of GaN-HEMTs. This unique cascade circuit can allow for standard gate driver circuit used in Si-based power electronics systems. However, Si MOSFETs also manage their high-temperature capabilities in the circuits even if the GaN-devices have the potential for high-temperature.

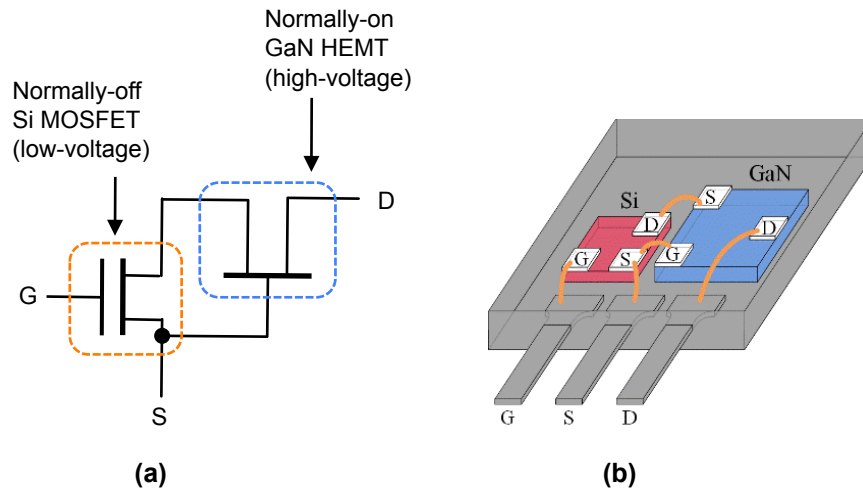


FIG. 2-18. (a) Circuit diagram of cascode configuration realizing normally-off operation.

2.3.3. Current issues in GaN-based HEMTs

As mentioned above, the GaN-based HEMTs have very attractive potential for realizing the high-power, high-frequency and low-loss devices owing to their superior physical properties. For the practical use of the GaN-HEMTs, however, there still remain several problems to solve. Most of them are arising from electronic states in the semiconductors, the main objective of this thesis. The electronic states are distributed in various parts in the devices such as barrier layer, channel layer, surface, and interface. They may also lead to the degradation of the electrical properties of the HEMTs due to unexpected exchange or transfer of charges in the devices. Here, some of the possible causes for the reported degradation of the GaN-HEMTs are introduced.

(A) Epitaxial growth on different-group materials

As mentioned in the previous section for the vertical structure, GaN substrates, at the moment, cost extremely expensive. For larger mass productions, it is necessary to make devices on low-cost and large-diameter substrates. Sapphire has been widely used as a substrate since Amano et al.¹⁴ first reported the epitaxial growth of GaN. SiC is one of the attractive substrates because it has the hexagonal crystal structure. Si is the most popular

material, which easily leads to the low-cost and large-diameter. However, they are in lattice-mismatched with GaN. Even if the buffer layers are prepared at the interface between the substrate and the epitaxial layer, the grown layers must have various types of defects and dislocation. If they reach the heterointerface or the surface, not only the electrons at the 2DEG channel but also the surface (or interface) states may be affected by the quality of the epitaxial layers. Besides, the electronic states induced at the substrate/epi-layer interface may also lead to the leakage current (called “buffer leakage current”). Some groups have reported that the intentional carbon doping is effective in reducing such leakage current, but the mechanism for this has not been discussed theoretically yet.

(B) Surface passivation

In case of the lateral GaN-HEMTs, the 2DEG is located in parallel to and close to the surface, making the electrons more sensitive to the condition of the surface. Therefore, the passivation of the devices are absolutely necessary to control the electrical performance of the GaN-HEMTs. In general, a “good” passivation prevents semiconductor surfaces from changing their chemical bonding structures. As a result, the passivation can also control the surface states. The resulting surface corresponds to the “interface”, in this case.

As Tajima and Hashizume reported¹³, the highest peak of electric field is applied to the gate edges in the lateral GaN-HEMTs. Such high electric fields can inject hot electrons into the surface states, resulting in the virtual gate bias applied in the access region which leads to the “current collapse” phenomena. They also reported the reduced current collapse using the Al₂O₃ passivation effect due to the reduction of the surface states at the AlGaN. However, the reduced state density at the surface has not been provided at that moment.

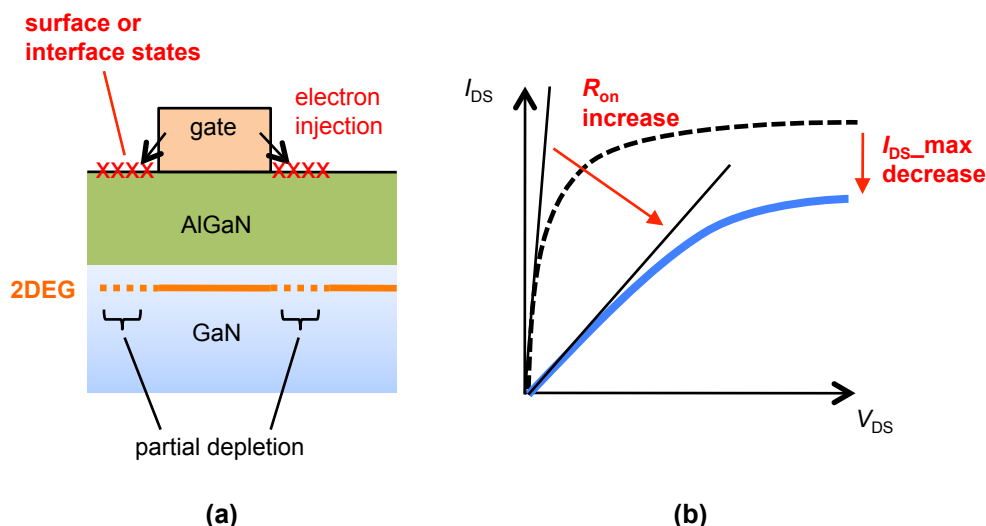


FIG. 2-20. Model for current collapse phenomenon of AlGaIn/GaN HEMTs.

(C) Reliability issues in the insulated-gate HEMTs

As introduced in the previous section, most of the normally-off GaN-HEMTs require the insulated-gate structure to suppress the gate leakage under the forward gate bias. However, there are operational stability and reliability issues of the insulated-gate GaN HEMTs. Ozaki *et al.*¹⁶ reported on the threshold voltage instability in the insulated-gate HEMTs which was induced by applying the negative gate bias stress. They said, this is probably due to the charge emission and trapping at the insulator/heterostructure interface. Their study focused on the relatively short-term reliability, while the long-term drift degradation may occur due to such high interface trap states. The interface states should be distributed in the access regions in the HEMTs, probably leading to the current collapse phenomena due to the electron injection into those interface states. As Tajima and Hashizume reported in Ref. 13, the insulated-gate structure succeed in reducing the current collapse but it still remains, indicating that the state density at the insulator/AlGaIn interface is still high. However, there are few reports on the state densities in the insulated-gate GaN-HEMTs because it is rather difficult to evaluate them at the moment.

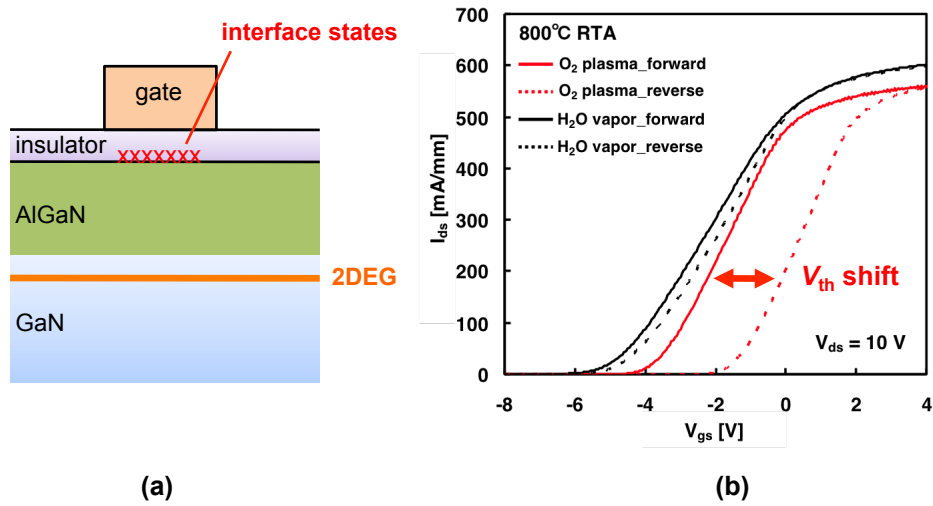


FIG. 2-21. Threshold voltage shifts in MOS-HEMTs reported in Ref. 16.

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Chapter 3.

Basics on metal-oxide-semiconductor structure

3.1. Introduction

A metal-oxide-semiconductor (MOS) structure is one of the key structures for MOS field effect transistors (FETs). In this chapter, basics on the interface states and their effects are introduced using some theories. The band diagrams, capacitance-voltage characteristics, and the behavior of electronic states are also explained, especially focusing on MOS diode structures for GaN-based materials. Furthermore, the theories to characterize the interface states in the MOS structures are derived. Note that the n-type semiconductor is mainly considered here because all the semiconductor materials used in this thesis have n-type conductivity (or unintentionally n-doped).

3.2. Surface and interface states

3.2.1. Origin of surface and interface states

At the surface of semiconductor or the interface between semiconductor and other materials, electronic states are formed within the bandgap due to the termination of the periodic atomic configuration. The electronic states can trap or emit electrons even in the bandgap, leading to the operational stability and reliability issues. Here, the origin of such electronic states is introduced.

Even in the bulk region, the electronic states can be created due to the degradation of the atomic configurations, which is “doping”. For example, when impurities are introduced into a pure Si crystal which has periodic configuration, the impurity level can be formed in

the bandgap and distributed through the bulk. This is mainly due to the substitution of the impurities for some of the Si atoms. If the reconfiguration of atoms is simple such as doping, only the single level is formed.

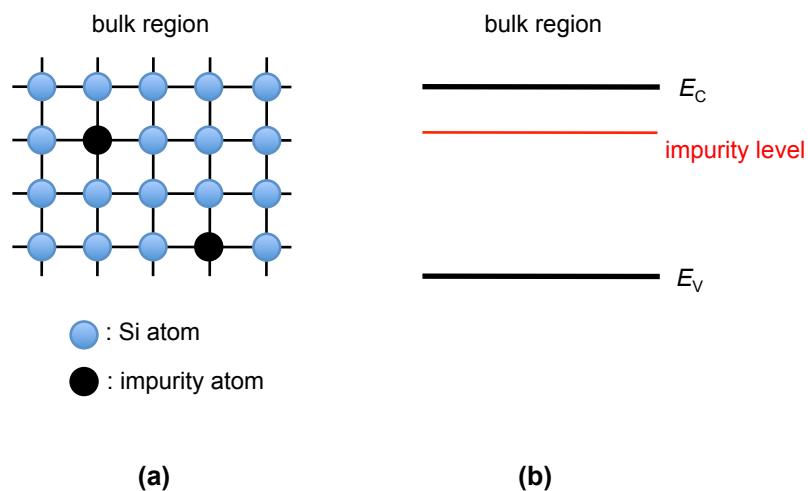


FIG. 3-1. (a) Schematic illustration of dopant atoms distributed in the Si crystal. (b) shows the dopant level generated in the Si bandgap.

Next, let us consider the intrinsic surface, that is, the vacuum/semiconductor interface. The termination of the periodic atomic configuration can prevent the formation of the conduction- and valence-band edge. In this case, only the termination of the crystal can create new states even within the bandgap. Those states are called intrinsic states, because they are originating from clean and well-ordered surface.^{1,2} At the real surface or interface, however, not only the simple reconfiguration but also the various types of degradation and disorder should be induced. Also, they consist of the interface between the semiconductor and metal, oxide, or atmosphere and their internal or external chemical reactions. The electronic states caused by those degradation and disorder are called extrinsic surface/interface states.³ Supposing the real interface has the various types of disorder originating the termination of order in the semiconductor, in particular, the interface states should be created in accordance with the unified disorder induced gap state (DIGS) model, which has been proposed by Hasegawa and Ohno in 1986.⁴

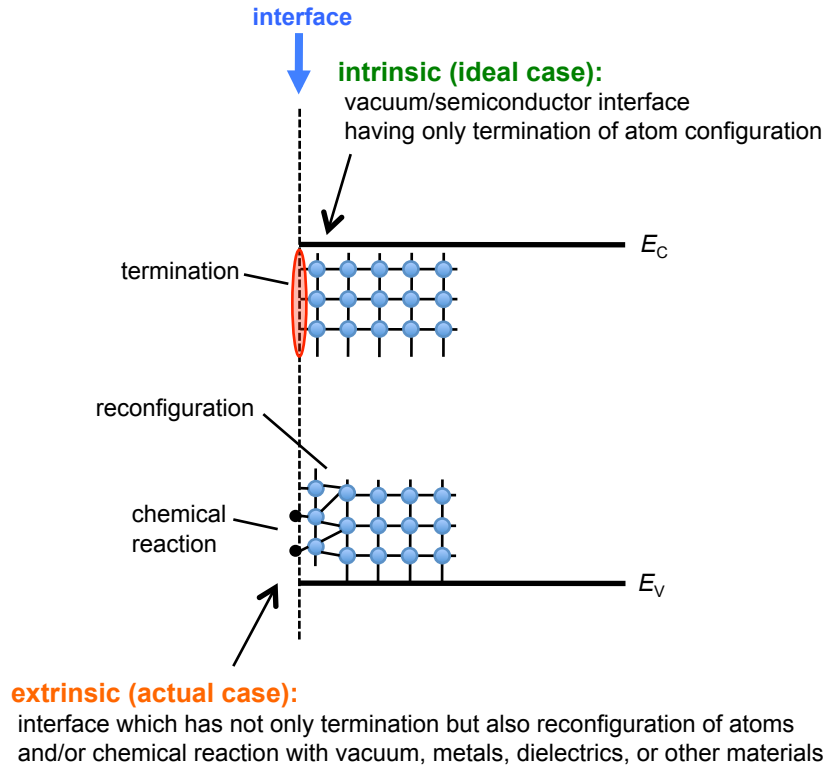


FIG. 3-2. Schematic illustration of intrinsic and extrinsic interfaces.

Fig. 3-3 shows the interface state density distribution based on the DIGS model. The DIGS density distribution consists of two types of states, bonding (donor-like) states and antibonding (acceptor-like) states, as shown in Figs. 3-3(a) and (b), respectively. Supposing that the origin of those states is the disorder of the atom configurations at the semiconductor surface, the separation of the conduction and valence band edges should not be plain. In the upper range of the bandgap, the created bonding states must succeed the conduction-band's properties, which have the highest density of the states near the band edge. In the lower range, on the other hand, the antibonding states must represent the valence-band's properties. In this case, when the electrons occupy the both types of the states, the bonding and antibonding states are in negative and in positive, respectively. Therefore, those states are called "acceptor-like" and "donor-like". At the energy represented by the charge neutrality level E_{CNL} , the state density shows the minimum. As a result, the interface has the U-shaped density distribution, as shown in Fig. 3-3(c).

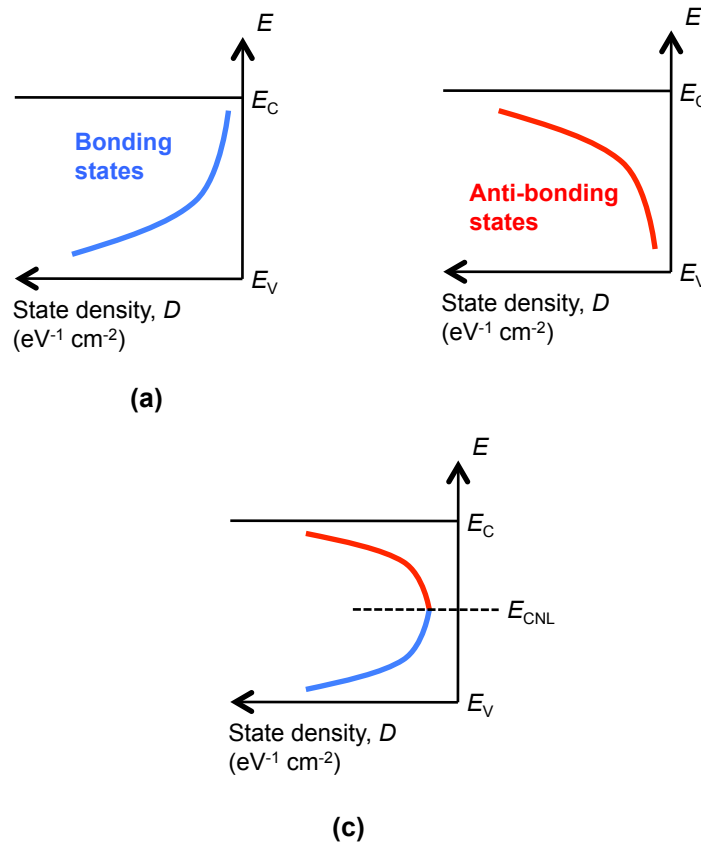


FIG. 3-3. (a) Bonding- and (b) antibonding-states of the DIGS model. (c) shows the resulting U-shaped interface state density distribution.

3.2.2. Shockley-Read-Hall statistics

Electronic states can transfer carriers to or from the conduction and valence bands, with trapping and emitting (= detrapping) the carriers. Therefore, it is important to consider such transferring processes and their probability of carriers. Shockley *et al.*⁵ have proposed the method to describe those processes at the electronic states as a statistics. In this section, their SRH (Shockley Read Hall) model is introduced in detail.

Fig. 3-4 shows the four simple process for transferring carriers between one electronic state and each band:

- (a) emitting electron from the electronic state to the conduction band
- (b) capturing electron of the conduction band at the electronic state
- (c) emitting electron from the electronic state to the valence band
- (d) capturing electron of the valence band at the electronic state.

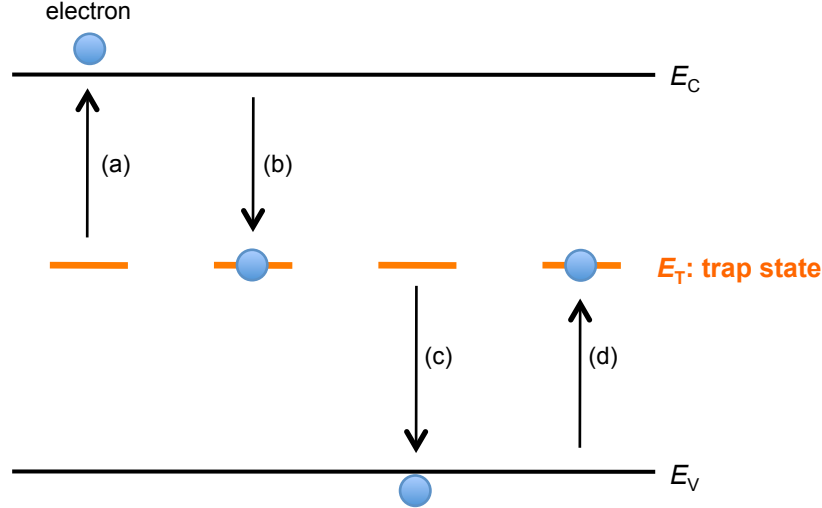


FIG. 3-4. Four processes of SRH-statistics: (a) electron emission from the trap state to the conduction band, (b) electron trapping at the trap state, (c) electron emission from the trap state to the valence band, and (d) electron trapping at the trap state.

Considering (a) and (b) processes, the rate equation for free electrons can be described by the following equation,

$$-\frac{dn}{dt} = C_n(N_T - n_T)n - e_n n_T, \quad (3.1)$$

where n is the concentration of free electrons in the semiconductor, N_T is the density of the electronic states, n_T is the density of the electrons captured at the electronic state. C_n and e_n are the capture coefficient and the emission rate of electrons, respectively. At equilibrium, the rate equation is given by Eq. (3.2),

$$C_n(N_T - n_T)n = e_n n_T. \quad (3.2)$$

n_T is the Fermi-dirac function, as described by Eq. (3.3),

$$n_T = N_T \left[1 + g \exp\left(\frac{E_T - E_F}{kT}\right) \right], \quad (3.3)$$

where E_F and E_T are the energies of the Fermi level and the electronic state, respectively. g is the degeneration factor of the electronic state. Also, n can be expressed using the effective density of the conduction band N_C and the following equation,

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT}\right), \quad (3.4)$$

where the E_C is the energy of the conduction band edge. Using Eqs. (3.2), (3.3), and (3.4), the relationship between emission rate and capture coefficient can be obtained as follows,

$$e_n = C_n N_C g^{-1} \exp\left(-\frac{E_C - E_F}{kT}\right). \quad (3.5)$$

Here, C can be expressed using the capture cross section of the electronic state σ ,

$$C = \sigma v_{th}, \quad (3.6)$$

where the v_{th} is the thermal velocity of electrons in the semiconductor as given by Eq. (3.8),

$$v_{th} = \sqrt{\frac{3kT}{m^*}}, \quad (3.8)$$

where m^* is the effective mass of electrons in the semiconductor.

The time constant τ for electron emission from the electronic state to the conduction band can be expressed as the reciprocal of e_n , as follows,

$$\tau \sim \frac{1}{e_n}. \quad (3.9)$$

In case that $g = 1$, thus, τ can be obtained as Eq. (3.10),

$$\tau = \frac{1}{\sigma v_{th} N_C} \exp\left(-\frac{E_C - E_F}{kT}\right). \quad (3.10)$$

This relation is called ‘‘SRH-statistics’’. As indicated by this model, τ is exponentially proportional to the energy depth of the electronic states. In the widegap materials, in particular, this relation must be considered to characterize the electron emission from the electronic states.

3.3. Band diagram of MOS junction

Figure 3-5 shows band diagrams of the ideal MOS structures. In the ideal case, we assumed that the work function of the gate metal is equal to that of the semiconductor, resulting in the ‘flat-band’ condition at the equilibrium state (Fig. 3-5(a)). In addition, it should be supposed that there are no exchanges of carriers through the insulator. At $V_G > 0$, as shown in Fig. 3-5(b), energy bands bend upward, leading to ‘accumulation’ of electrons at the insulator/semiconductor interface without any leakage flow. At $V_G < 0$, on the other hand, bands bend downward with moving down E_F , resulting in the ‘depletion’ of electrons in the semiconductor layer (Fig. 3-5(c)). In the deep reverse bias condition, two cases should be considered. When the reverse bias increased, minority carriers (holes, in this case) may be generated, leading to accumulation of holes at the interface. This phenomenon is called the ‘inversion’ condition, as shown in Fig. 3-5(d), because the conductivity of the semiconductor is inversed to be a p-type. Unless holes can be generated, the ‘depletion’ without any carrier accumulation continues with increasing the reverse bias, which is called the ‘deep-depletion’

condition (Fig. 3-5(e)). The effects of these two phenomena will be introduced later in this chapter.

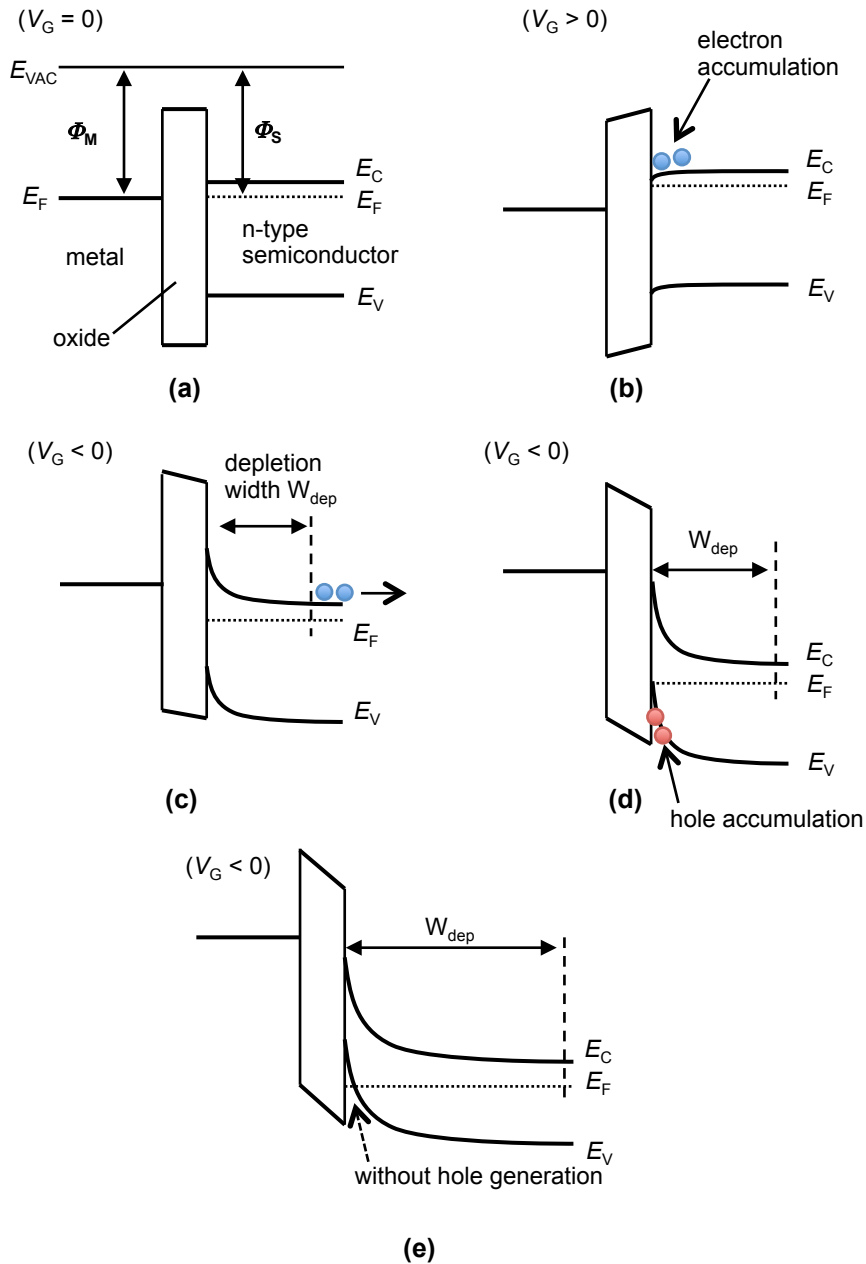


FIG. 3-5. Band diagrams of ideal MOS junction at equilibrium.

In reality, there can be energy difference between work functions of gate metals and semiconductors.⁶ Moreover, additional charges placed in the junctions, such as interface state charges and fixed/mobile charges distributed in the oxide layer or near the interface, may also affect their band bending. When the work function of the gate metal is larger than that of the semiconductor and there are negative charges at the oxide/semiconductor interface as shown

in Figs. 3-6(a) and (b), respectively, the energy bands at the interface bend upward, leading to the ‘depletion’ condition at the zero bias. In the opposite conditions, as shown in Figs. 3-6(c) and (d), the energy bands bend downward at the equilibrium state. In those cases, the flat-band voltage V_{FB} , which should be applied in order to flatten the bands, can be described by Eq. (3.11),

$$V_{FB} = W_M - W_S - \frac{Q_{it}}{C_{ox}}, \quad (3.11)$$

where W_M and W_S are the work functions of the gate metal and the semiconductor, respectively, and Q_{it} is the fixed interface charge (C/cm^2) at the oxide/semiconductor interface. C_{ox} is the insulator capacitance per unit area (F/cm^2).

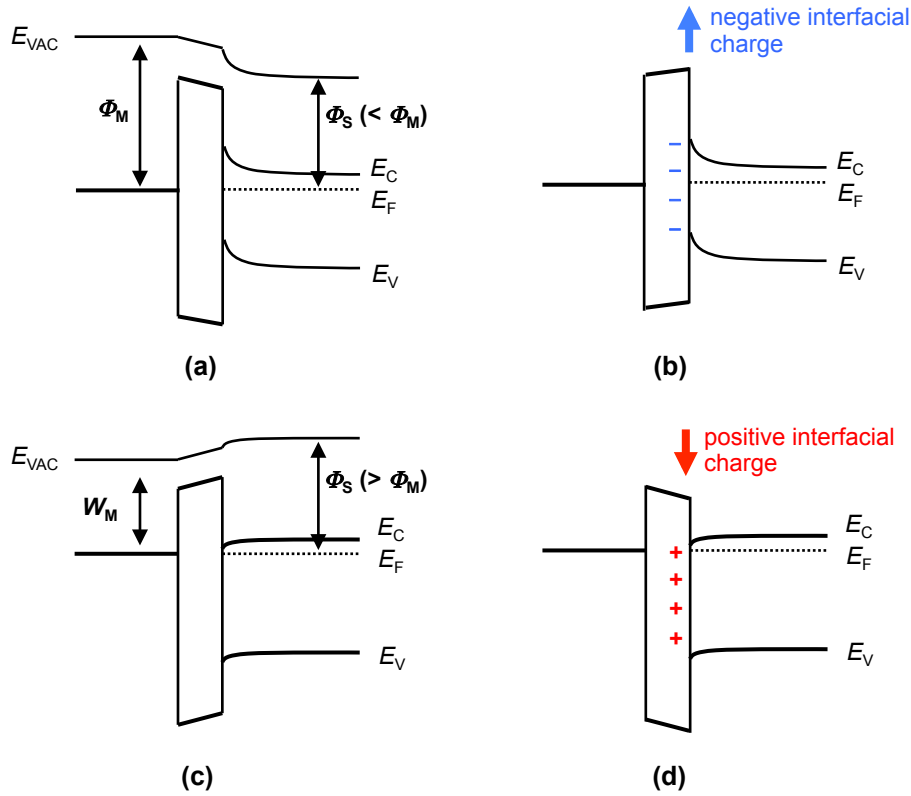


FIG. 3-6. Band diagrams of MOS structures for real cases.

3.4. Capacitance-voltage characteristics of MOS structures

To obtain the ideal C - V curve of the MOS structure, the relationship between surface potential, space charge, and electric field has to be derived. Fig. 3-7 shows the detail band diagram of the n-type semiconductor under the negative gate bias condition.⁷ n_n and p_n are the densities of electrons and holes, respectively, and N_D and N_A are donor and acceptor

concentrations in the semiconductor, respectively. The potential $\phi_p(x)$ at each position is defined using the conduction-band edge E_C relative to that of the bulk region,

$$\phi_p(x) = \frac{E_C(\infty) - E_C(x)}{q}. \quad (3.12)$$

Especially, the surface potential ϕ_s ($x = 0$) is defined as follows,

$$\begin{aligned} \phi_s &= \phi_p(0) \\ &= \frac{E_C(\infty) - E_C(x)}{q}. \end{aligned} \quad (3.13)$$

Once ϕ_s is determined, electric field and charge distributions in the semiconductor can be obtained using Poisson equation, as shown in Fig. 3-8(b). The integrated charge in the semiconductor is equivalent with the surface charge Q_s , resulting in the capacitance of the depletion region in the semiconductor. Surface electric field E_s is also obtained from ϕ_s , giving gate voltage V which is applied to the MOS structure. Deriving them, as a result, the ideal C - V - ϕ_s relationship will be extracted.

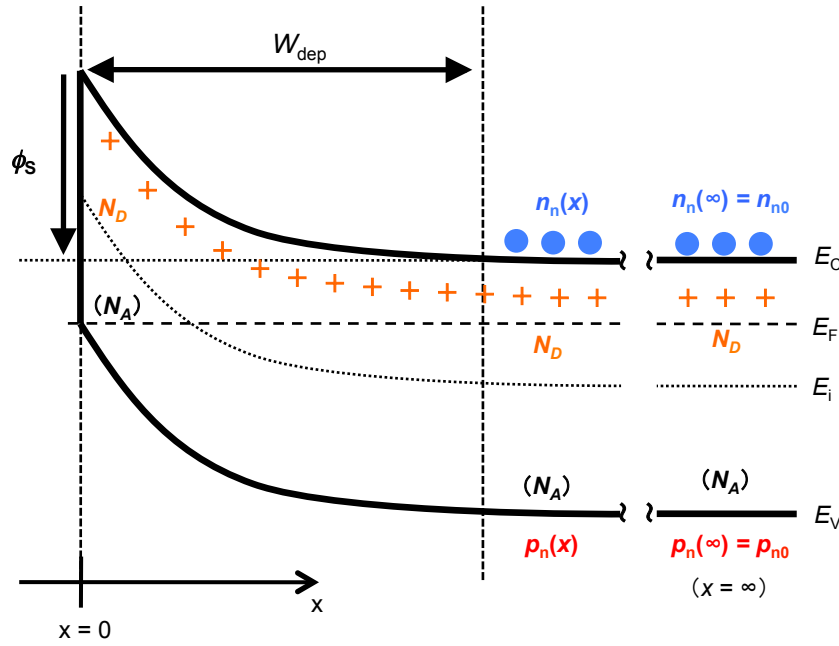


FIG. 3-7. Band diagrams and charge distributions of n-type semiconductor.

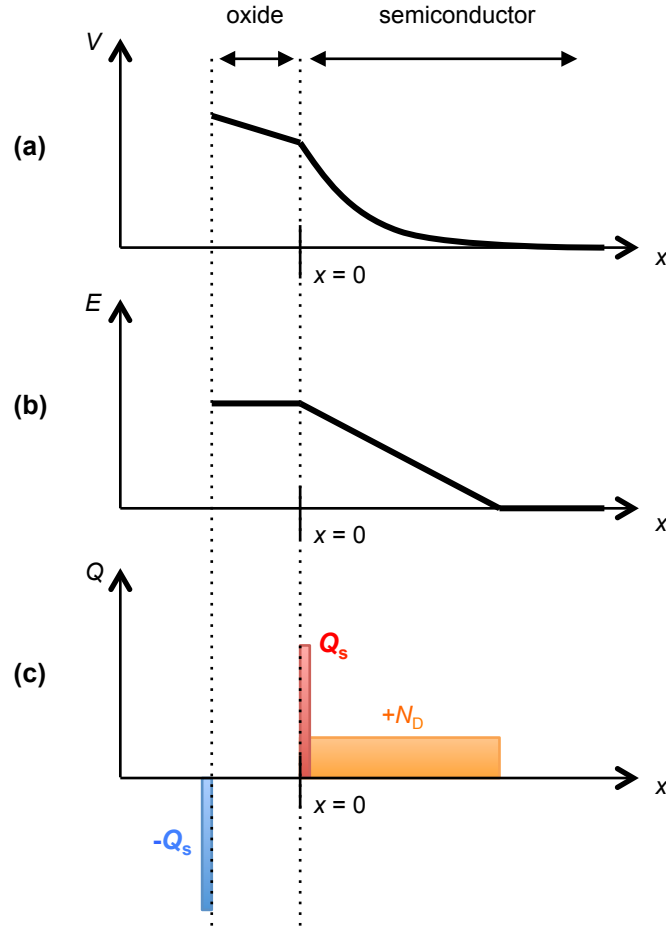


FIG. 3-8. (a) Potential, (b) electric field, and (c) charge distributions in the MOS structure.

(A) Relationship between surface potential and surface charge density

The potential $\phi_p(x)$ is defined as the intrinsic Fermi energy relative to that grounded, $\phi_p(\infty) = 0$. The relationship between $\phi_p(x)$ and carrier concentrations of electrons and holes can be described as follows:

$$n_n(x) = n_{n0} \exp(\beta \phi_p(x)) \quad (3.14)$$

$$p_n(x) = p_{n0} \exp(-\beta \phi_p(x)) \quad (3.15)$$

$$\beta = \frac{q}{k_B T} \quad (3.16)$$

where n_{n0} and p_{n0} are the equilibrium densities of electrons and holes, respectively. β is the constant value using temperature, boltzman constant and charge of single electron. In the bulk region, that is $x = \infty$, ϕ_p goes to zero, giving electron and hole densities,

$$n_n(\infty) = n_{n0} \quad , \quad (3.17)$$

$$p_n(\infty) = p_{n0} \quad . \quad (3.18)$$

At the surface ($x = 0$), on the other hand, densities for both carriers are given by the following equations,

$$n_n(0) = n_{n0} \exp(\beta\phi_s) \quad , \quad (3.19)$$

$$p_n(0) = p_{n0} \exp(-\beta\phi_s) \quad , \quad (3.20)$$

where ϕ_s is the surface potential ϕ_s . ($\phi_s = \phi_p(0)$ from Eq. (3.13))

A one dimensional Poisson equation is given by:

$$\frac{d^2\phi_p}{dx^2} = -\frac{\rho(x)}{\epsilon_s\epsilon_0} \quad , \quad (3.21)$$

where ρ is the charge density. Supposing that all the donors and acceptors are ionized, ρ is then described,

$$\rho(x) = q(N_D^+ - N_A^- + p_n(x) - n_n(x)) \quad . \quad (3.22)$$

When the charge neutrality condition is considered in the bulk region ($x = \infty$), we obtain Eq. (3.23),

$$\begin{aligned} \rho(\infty) &= 0 \\ \Rightarrow N_D^+ - N_A^- + p_n(\infty) - n_n(\infty) &= 0 \\ \Rightarrow N_D^+ - N_A^- &= n_n(\infty) - p_n(\infty) \quad . \end{aligned} \quad (3.23)$$

The Poisson equation is then described using Eqs. (3.21) and (3.23),

$$\frac{d^2\phi_p}{dx^2} = -\frac{q}{\epsilon_s\epsilon_0} \left(n_{n0} - p_{n0} + p_{n0} \exp(-\beta\phi_p) - n_{n0} \exp(\beta\phi_p) \right) \quad . \quad (3.24)$$

Integrating Eq. (3.24) from the surface to the bulk,

$$\int_0^{\frac{d\phi_p}{dx}} \left(\frac{d\phi_p}{dx} \right) d\left(\frac{d\phi_p}{dx} \right) = -\frac{q}{\epsilon_s\epsilon_0} \int_0^{\phi_p} \left\{ p_{n0} \left[\exp(-\beta\phi_p) - 1 \right] - n_{n0} \left[\exp(\beta\phi_p) - 1 \right] \right\} d\phi_p \quad . \quad (3.25)$$

Using the electric field $E \left(= -\frac{d\phi_p}{dx} \right)$, Eq. (3.25) is expressed as a relation between E and ϕ_p ,

$$\begin{aligned}
E^2 &= -\left(\frac{2}{\beta}\right)^2 \left(\frac{qn_{n0}\beta}{2\varepsilon_s\varepsilon_0}\right) \left\{ \frac{p_{n0}}{n_{n0}} \left[\exp(-\beta\phi_p) + \beta\phi_p - 1 \right] + \left[\exp(\beta\phi_p) - \beta\phi_p - 1 \right] \right\} \\
&= -\frac{2}{\beta^2 L_D^2} F^2 \left(\beta\phi_p, \frac{p_{n0}}{n_{n0}} \right),
\end{aligned} \tag{3.26}$$

where the Debye length L_D in the semiconductor and factor F are,

$$F\left(\beta\phi_p, \frac{p_{n0}}{n_{n0}}\right) = \sqrt{\frac{p_{n0}}{n_{n0}} \left[\exp(-\beta\phi_p) + \beta\phi_p - 1 \right] + \left[\exp(\beta\phi_p) - \beta\phi_p - 1 \right]}, \tag{3.27}$$

$$L_D = \sqrt{\frac{kT\varepsilon_s\varepsilon_0}{n_{n0}q^2}}. \tag{3.28}$$

The electric field E is then given by,

$$E(x) = \pm \frac{\sqrt{2}}{\beta L_D} F\left(\beta\phi(x), \frac{p_{n0}}{n_{n0}}\right). \tag{3.29}$$

Note that E is positive at $\phi_p > 0$. When the $\phi_p = \phi_s$, the surface electric field $E_s (= E(0))$ is given by Eq. (3.30),

$$E_s = \pm \frac{\sqrt{2}}{\beta L_D} F\left(\beta\phi_s, \frac{p_{n0}}{n_{n0}}\right). \tag{3.30}$$

Using Gauss's law, the charge density at the surface Q_s is given as follows,

$$\begin{aligned}
Q_s &= -\varepsilon_s\varepsilon_0 E_s \\
&= \mp \frac{\sqrt{2}\varepsilon_s\varepsilon_0}{\beta L_D} F\left(\beta\phi_s, \frac{p_{n0}}{n_{n0}}\right).
\end{aligned} \tag{3.31}$$

As shown in Fig. 3-9, the relationship between Q_s and ϕ_s is successfully derived.

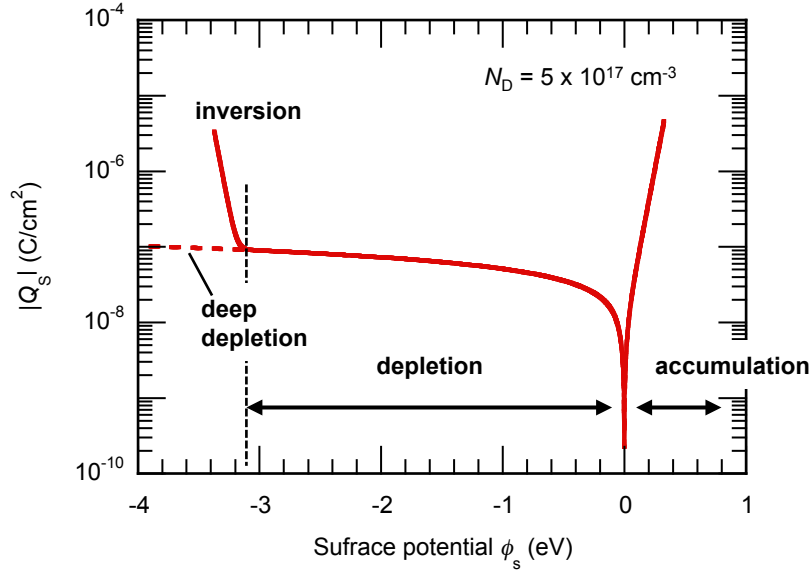


FIG. 3-9. Surface potential vs. surface charge.

(B) Relationship between surface potential and gate voltage

In the MOS structure, the gate voltage V is divided by the insulator and semiconductor. V is then given by,

$$V = V_{ox} + \phi_s, \quad (3.32)$$

where the V_{ox} is the voltage applied to the insulator as described,

$$V_{ox} = -\frac{Q_s}{C_{ox}}. \quad (3.33)$$

As expressed by Eq. (3.31), Q_s is the function of ϕ_s . Once ϕ_s given, the relationship between V and ϕ_s is then determined as shown in Fig. 3-10.

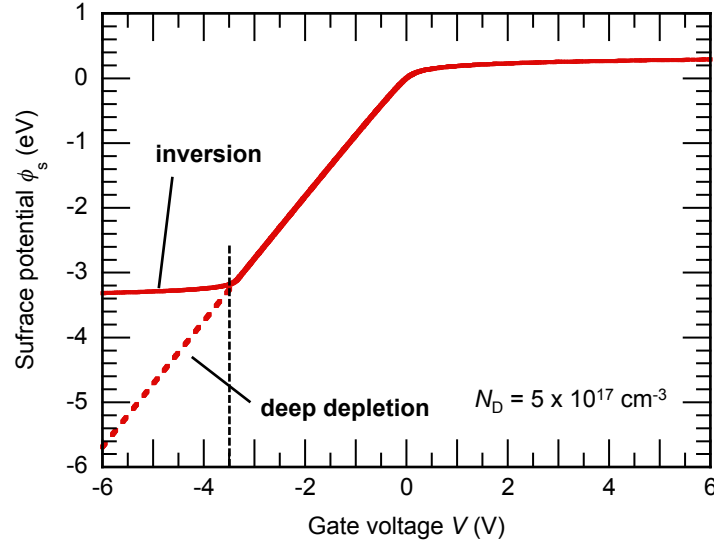


FIG. 3-10. Surface potential vs. gate voltage.

(C) Relationship between depletion capacitance and surface potential

The depletion capacitance C_{dep} can be obtained by differentiating the Q_s with ϕ_s ,

$$C_{\text{dep}} = \frac{dQ_s}{d\phi_s}. \quad (3.34)$$

However, C_{dep} is not only dependent on the bias but also the frequency and the sweep-rate. Therefore, three types of C_{dep} have to be considered as follows:

low-frequency mode,

high-frequency mode,

deep-depletion mode.

In the low- and high-frequency mode, generated holes accumulate at the insulator/semiconductor interface, leading to ‘inversion’ condition. For both modes, because holes can shield the electric field from the gate electrode, the depletion width is no longer a function of gate bias. In contrast, if the sweeping rate is faster than the hole generation rate, the depletion width can spread with respect to applying the gate voltages. This phenomenon is called ‘deep depletion’ mode.

C_{dep} for each mode is now described as follows.

(a) Low-frequency mode

When the frequency is slower than the hole generation rate, the hole generation and recombination can respond to the ac signal. In Eq. (3.27), the 1st term in the root square corresponds to the hole density in the semiconductor. Therefore, the depletion capacitance

C_{dep} without considering the hole density is given by Eq. (3.35),

$$C_{dep} = \frac{dQ_s}{d\phi_s} = \frac{\epsilon_s \epsilon_0}{\sqrt{2}L_D} \frac{(p_{n0}/n_{n0})[1 - \exp(-\beta\phi_s)] + \exp(\beta\phi_s) - 1}{F_{low}}, \quad (3.35)$$

where F_{low} is the F function for the low-frequency mode given as follows,

$$F_{low} = \sqrt{\frac{p_{n0}}{n_{n0}} \left[\exp(-\beta\phi_p) + \beta\phi_p - 1 \right] + \left[\exp(\beta\phi_p) - \beta\phi_p - 1 \right]}. \quad (3.36)$$

In this case, the high-density hole generation impedes the spread of the depletion region, giving the maximum depletion width W_{MAX} as expressed by Eq. (3.37),

$$W_{MAX} = \sqrt{\frac{4\epsilon_s \epsilon_0 \ln(N_D/n_i)}{q^2 N_D}}. \quad (3.37)$$

(b) High-frequency mode

When the hole generation rate is slower than the frequency, the hole generation and recombination can respond to the ac signal. In this case, the differentiating the 1st term in the root square of F is zero. C_{dep} can be obtained using the following equation,

$$C_{dep} = \frac{dQ_s}{d\phi_s} = \frac{\epsilon_s \epsilon_0}{\sqrt{2}L_D} \frac{\exp(\beta\phi_s) - 1}{F_{high}}, \quad (3.38)$$

where F_{high} is F function for the high-frequency mode,

$$F_{high} = \sqrt{\left[\exp(\beta\phi_p) - \beta\phi_p - 1 \right]}. \quad (3.39)$$

Even if the generation and recombination of minority carriers cannot respond to the ac signal, however, the accumulation of minority carriers can occur. Thus, the spread of the depletion layer is limited to W_{MAX} , as well as the low-frequency mode, given by Eq. (3.37).

(c) Deep-depletion mode

In case the bias sweep rate is faster than the generation rate of minority carriers, the hole generation cannot follow the gate bias change, spreading the depletion layer as a function of the gate bias. F is given by the Eq. (3.40) as well as that of the high-frequency mode,

$$F_{deep} = \sqrt{\left[\exp(\beta\phi_p) - \beta\phi_p - 1 \right]}. \quad (3.40)$$

Therefore, C_{dep} can be obtained by the following Eq. (3.41),

$$C_{dep} = \frac{\epsilon_s \epsilon_0}{\sqrt{2} L_D} \frac{\exp(\beta \phi_s) - 1}{F_{deep}}. \quad (3.41)$$

(D) Relationship between gate capacitance and gate voltage

The total capacitance C is given using C_{ox} and C_{dep} as described in the following equation,

$$C = \frac{C_{dep} C_{ox}}{C_{dep} + C_{ox}}. \quad (3.42)$$

As already derived, C_{dep} can be obtained giving ϕ_s in Eqs. (3.35), (3.38), and (3.41). The gate voltage V is also given by Eq. (3.43),

$$V = -\frac{Q_s}{C_{ox}} + \phi_s. \quad (3.43)$$

Therefore, giving ϕ_s , both C and V can be obtained. Fig. 3-11 shows the ideal C - V characteristics for low frequency mode, high frequency mode, and deep-depletion mode.

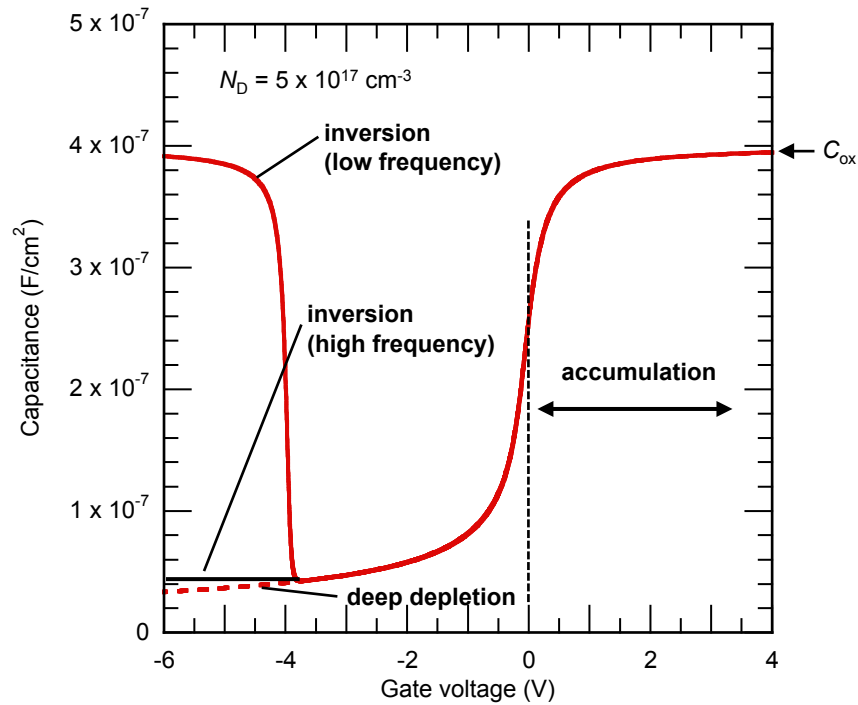


FIG. 3-11. C - V characteristics of the ideal MOS structure.

3.5. Interface states in MOS structures

3.5.1. Basic behavior of electronic states at oxide/semiconductor interfaces

As mentioned in the previous paragraph, interface states are formed at the oxide/semiconductor interfaces with various densities and distributions in the real MOS structures. At first, let us consider a simple case as shown in Fig. 3-12. $T1$ and $T2$ are acceptor-like and donor-like interface states, respectively. Assume that electron captured at the states only can be emitted to the conduction band. If electrons occupy both states, $T1$ and $T2$ have negative and positive charges, respectively. The occupation rate of each state is subject to the Fermi-dirac function. When the Fermi level E_F moves below $T1$, as shown in Fig. 3-12(c), $T1$ emits the electron to the conduction band and turns neutral, while $T2$ is in neutral. When $T2$ emits the electron, $T2$ then turns positive.

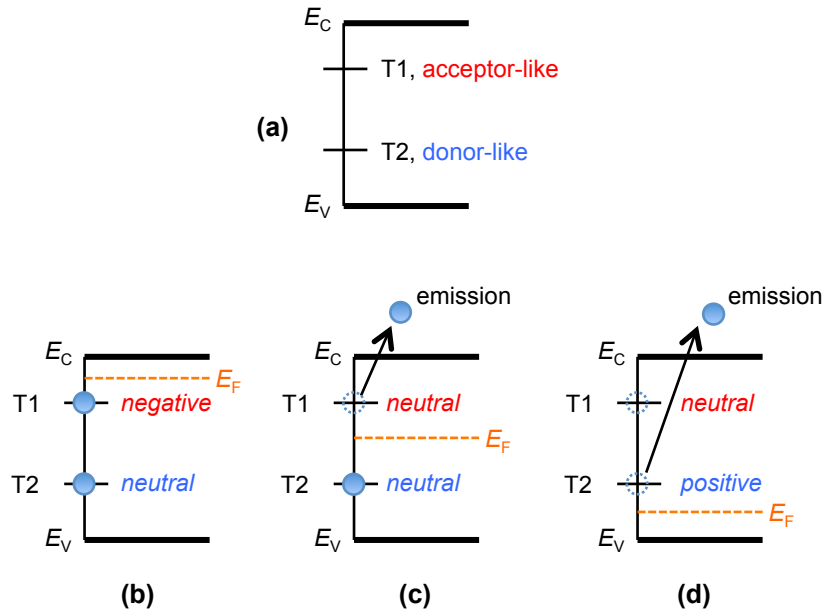


FIG. 3-12. Schematic illustrations of assumed two interface states. (b), (c), and (d) describe E_F moving and electron emission from the interface states.

As a result, the electron trapping and emission at the interface states lead to the change of the interface charge. Fig. 3-13(a) shows the resulting charge distributions in the MOS structure. Considering the interface state charge Q_{it} , the affected surface charge Q_s' is given by the original surface charge Q_s added to Q_{it} as follows,

$$Q_s' = Q_s + Q_{it}. \quad (3.44)$$

Let us suppose the charge polarities corresponding to Figs. 3-12(b), (c) and (d) are in

negative, in neutral, and in positive, respectively. Those polarities depend on the position of the Fermi level at the interface, that is, the surface potential. The resulting change of the interface state charge affects the C - V characteristics of the MOS structures.

Furthermore, in case that the charge emission and trapping can respond to the ac bias signal, the interface states are detected as the capacitance and conductance as shown in Fig. 3-13(b). Here, the interface state conductance R_{it} corresponds to the charge emission rate of the electron from the interface states.⁸

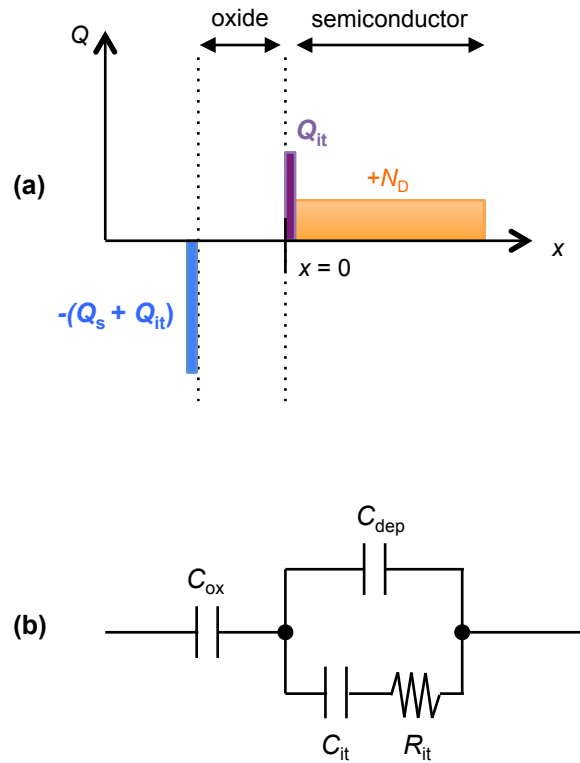


FIG. 3-13. Effect of the interface states on (a) charge distributions and (b) equivalent circuits of the MOS structure.

Considering those two models for the behavior of the interface state, we attempt to derive the effects of the interface states on the C - V characteristics of the MOS structures.

First, let us consider the effects of the interface state charge on the gate voltage change. As shown in Eq. (3.44), the interface state charge Q_{it} is considered in the MOS structures. Using Q'_s , the voltage applied the gate insulator is given by the following equation,

$$V_{ox} = -\frac{Q'_s}{C_{ox}}. \quad (3.45)$$

The resulting relationship between the surface potential and the gate voltage is then described

by Eq. (3.46),

$$\begin{aligned}
 V &= -\frac{Q'_s}{C_{ox}} + \phi_s \\
 &= -\frac{Q_s + Q_{it}}{C_{ox}} + \phi_s
 \end{aligned} \tag{3.46}$$

Therefore, when the interface states $T1$ and $T2$ emit the electron due to the ϕ_s change, the resulting change of Q_{it} gives the change of the gate voltage, as schematically shown in Fig. 3-14.

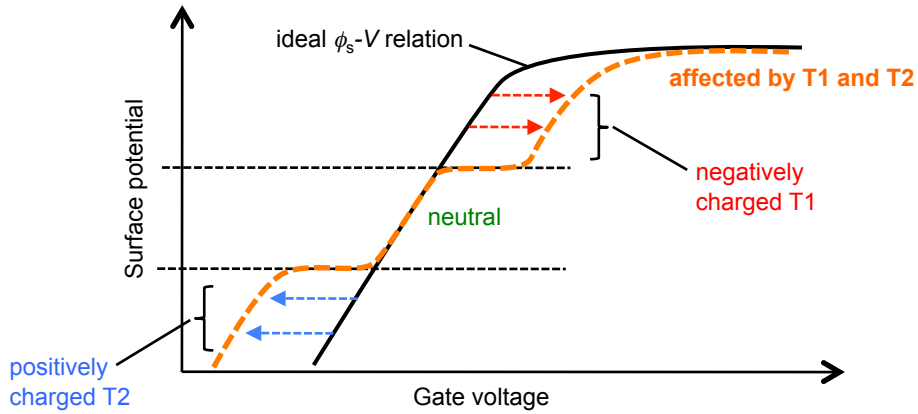


FIG. 3-14. Schematic illustration of surface potential vs. gate voltage affected by assumed two interface states.

Next, let us consider the effects of the interfaces states on the capacitance. In the case of Fig. 3-15(a), Q_{it} is fixed because the variation of E_F cannot affect the charging condition of $E1$. The depletion capacitance C'_{dep} is then described by the following equation,

$$\begin{aligned}
 C'_{dep} &= \frac{dQ'_s}{d\phi_s} \\
 &= \frac{dQ_s}{d\phi_s}
 \end{aligned} \tag{3.47}$$

Therefore, $E1$ cannot affect the capacitance. On the other hand, if E_F reaches $E1$, the capture and emission of electrons follows the variation of E_F . In this case, the resulting capacitance is given as follows,

$$\begin{aligned}
C'_{dep} &= \frac{dQ'_s}{d\phi_s} \\
&= \frac{dQ_s}{d\phi_s} + \frac{dQ_{it}}{d\phi_s}
\end{aligned} \tag{3.48}$$

The interface state capacitance C_{it} can be described by Eq. (3.49),

$$C_{it} = \frac{dQ_{it}}{d\phi_s}, \tag{3.49}$$

which corresponds to the equivalent circuit shown in Fig. 3-13(b). The response rate of emitting the electrons is dominantly governed by the time constant of electron emission from the interface states, which can be expressed using SRH statistics. The time constant τ_1 of electron emission from E_1 can be described by Eq. (3.50),

$$\tau_1 = \frac{1}{\sigma N_C v} \exp\left(\frac{E_C - E_1}{kT}\right). \tag{3.50}$$

τ_1 is equal to the product of C_{it} and R_{it} defined in Fig. 3-13(b). The equivalent circuit shown in Fig. 3-15(a) represents that in Fig. 3-13, where C_p and G_p are described as follows,

$$\begin{aligned}
C_p &= C_{dep} + \frac{C_{it}}{1 + \omega^2 \tau_1^2}, \\
\frac{G_p}{\omega} &= \frac{C_{it} \omega \tau_1}{1 + \omega^2 \tau_1^2}, \\
\omega &= 2\pi f.
\end{aligned} \tag{3.51}$$

The total capacitance C as given by Eq. (3.52) can be obtained below,

$$\begin{aligned}
C &= \left[C_{ox}^{-1} + \left(C_{dep} + \frac{C_{it}}{1 + \omega^2 \tau_1^2} \right)^{-1} \right]^{-1} \\
\frac{G_p}{\omega} &= \frac{C_{it} \omega \tau_1}{1 + \omega^2 \tau_1^2}, \\
V &= -\frac{Q_s + Q_{it}}{C_{ox}} + \phi_s
\end{aligned} \tag{3.52}$$

where the measurement frequency nears the electron emission rate of the interface states. If the frequency is much more lower than the emission rate ($\tau_1 < 1/2\pi f$), that is the low-frequency limit, the total capacitance is then given by Eqs. (3.53),

$$\begin{aligned}
C_{LF} &= \left[C_{ox}^{-1} + (C_{dep} + C_{it})^{-1} \right]^{-1} \\
G_p &= \infty \\
V &= -\frac{Q_s + Q_{it}}{C_{ox}} + \phi_s
\end{aligned} \tag{3.53}$$

If the frequency is much more faster than the emission rate ($\tau_1 > 1/2\pi f$), on the other hand,

the variation of E_F cannot lead to the emission of electrons at the interface, resulting in $C_{it} = 0$. This situation is called the high-frequency limit. The total capacitance C is then given as follows,

$$\begin{aligned} C_{HF} &= (C_{ox}^{-1} + C_{dep}^{-1})^{-1} \\ G_p &= 0 \\ V &= -\frac{Q_s + Q_{it}}{C_{ox}} + \phi_s \end{aligned} \quad (3.54)$$

The resulting equivalent circuits for the high-frequency limit and the low-frequency limit are shown in Figs. 3-15(a) and (b), respectively.

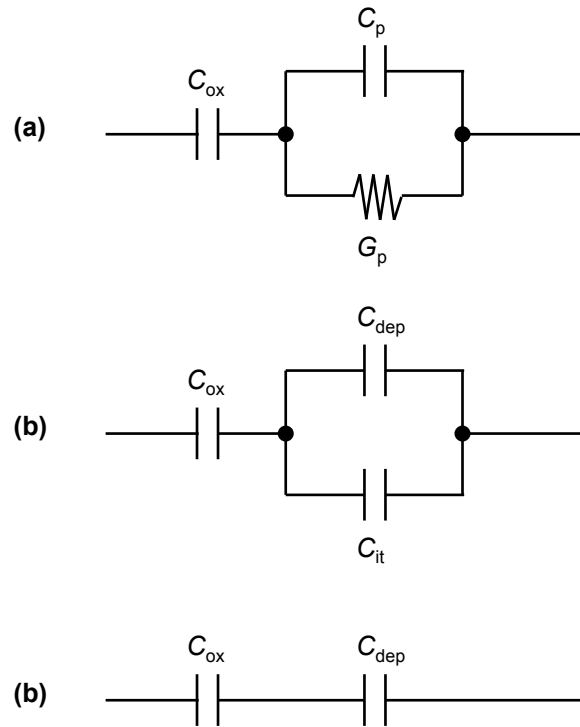


FIG. 3-15. (a) Equivalent circuits of interface states. (b) and (c) indicates the circuit for high-frequency and low-frequency limits, respectively.

Now, let us consider the continuously distributed interface states, as shown in Fig. 3-16. Supposing that the states in the upper and lower ranges are the acceptor-like and donor-like states, respectively, the total interface state charge Q_{it} can be described as follows,

$$Q_{it} = -q \int_{E_v}^{E_c} D_{it}^A f dE + q \int_{E_v}^{E_c} D_{it}^D (1-f) dE, \quad (3.56)$$

where f is the Fermi-dirac function as a function of the surface potential ϕ_s . As shown in Fig. 3-17(a), the change of Q_{it} impedes the surface potential control by the gate voltage V . As a result, the continuous distributed interface states cause the “stretch-out” behavior of C - V curves, as shown in Fig. 3-17(b).

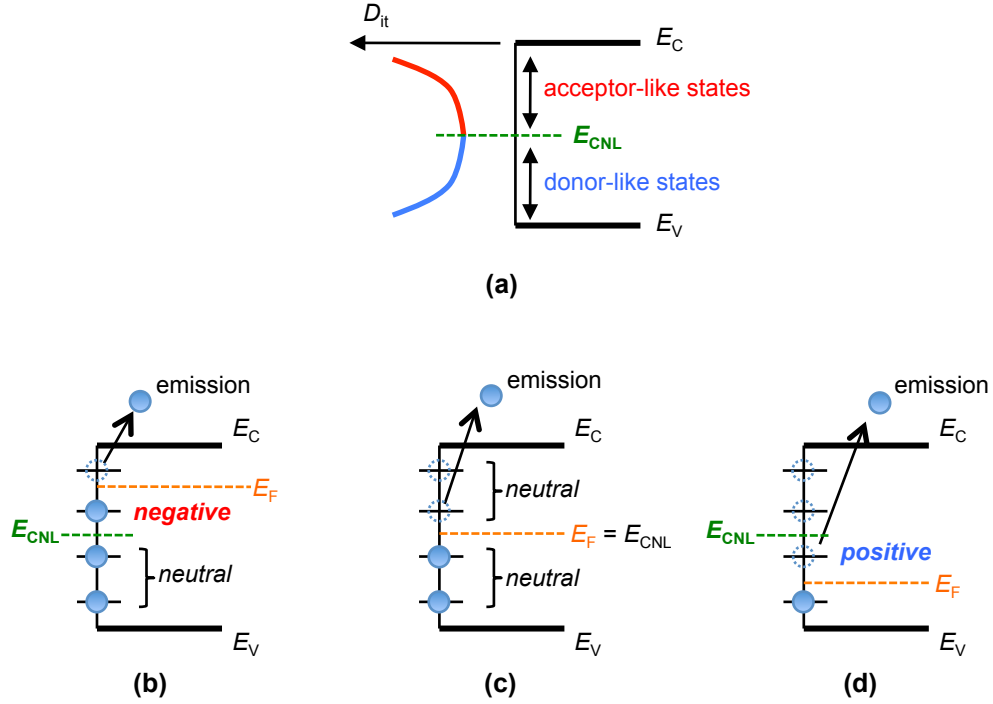


FIG. 3-16. (a) Schematic illustration of U-shaped interface state distribution.

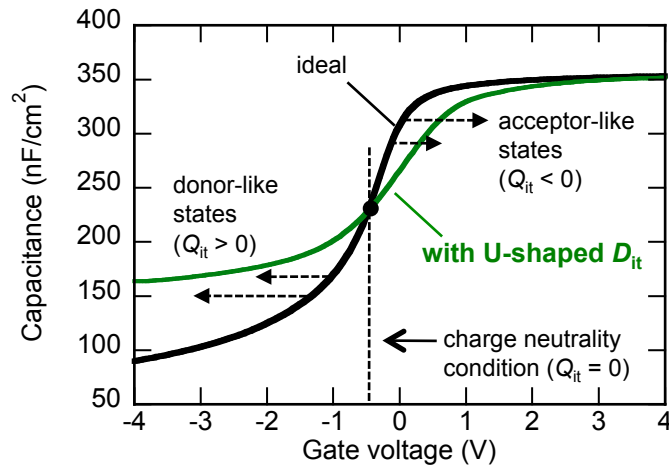


FIG. 3-17. C - V characteristics affected by the U-shaped distributed interface states.

3.5.2. Effects of interface states in widegap materials

As described in Eq. (3.10), the time constants τ for electron emission from the interface states is exponentially proportional to the energy depth of the trap. The typical oxide/GaN system has the time constant of 1 month for the electron emission from the interface state with the trap depth of 1 eV at RT. In the widegap MOS structures, therefore, not all the interface states can emit the electron due to the longer τ compared to the actual C - V measurement time. Using τ , the emission efficiency of the trapped electrons can be expressed by the following equation,⁹

$$\eta = 1 - \exp\left(-\frac{t_{\text{meas}}}{\tau}\right), \quad (3.57)$$

where t_{meas} is the measurement time. The interface state charge density can be obtained by Eqs. (3.57) and (3.58),

$$Q_{it} = q \int_{E_v}^{E_c} D_{it}^D [1 - f_0(1 - \eta_e) - \eta_e f] dE - q \int_{E_v}^{E_c} D_{it}^A [f_0(1 - \eta_e) + \eta_e f] dE. \quad (3.58)$$

Fig. 3-18 shows the emission efficiency at the oxide/GaN interface calculated for RT, 100 °C, and 200 °C. In Fig. 3-19, the effects of the interface states on C - V characteristics are compared between the calculation with and without assuming the emission efficiency. If the interface states can emit all the electrons during the C - V measurement (i.e. without assuming the emission efficiency), the resulting C - V curve shows the stretch-out toward both the negative and positive bias directions. If the emission efficiency assumed, in contrast, the stretch-out only toward the positive direction was observed in the C - V curve. This is because the limited number of acceptor-like states can emit the electron during t_{meas} . In the case of oxide/GaN, the limited number of the interface states can be detected during the standard C - V measurements.

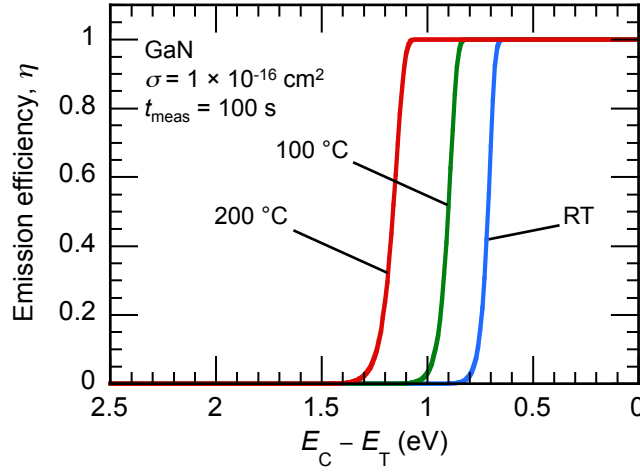


FIG. 3-18. Emission efficiencies of insulator/GaN interface at RT, 100 °C, and 200 °C.

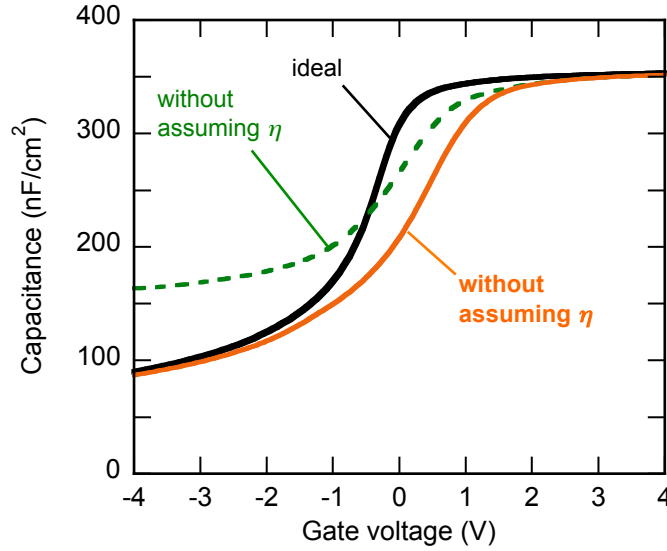


FIG. 3-19. Typical C - V characteristics of the wide-gap material assuming emission efficiency.

3.5.3. High-frequency method ('Terman method')

As described by Eq. (3.54), in the high-frequency limit, the effects of the interface stats just appear in the dc gate bias change. This means that the capacitance measured in the high-frequency limit does not have any errors from the interface states. Therefore, C_{dep} can be directly extracted from the measured capacitance C_{HF} using Eq. (3.54), as follows,

$$C_{dep} = \left(C_{HF}^{-1} + C_{ox}^{-1} \right)^{-1}, \quad (3.59)$$

where C_{ox} is the oxide capacitance (needed to be given). The depletion width W_{dep} is then

given using C_{dep} ,

$$W_{dep} = \frac{\epsilon_s \epsilon_0}{C_{dep}}. \quad (3.60)$$

The surface potential ϕ_s can also be extracted using C_{dep} ,

$$\phi_s = \frac{\epsilon_s \epsilon_0 q N_D}{2C_{dep}^2}, \quad (3.61)$$

where the N_D is the density of the majority carriers, electrons. Therefore, in the high-frequency limit, the experimental C - V - ϕ_s relations can be obtained using those equations. Here, let us differentiate the gate bias change affected by the interface states, Eq. (3.54). The resulting equation is,

$$\frac{dV}{d\phi_s} = \frac{1}{C_{ox}} \frac{dQ_s}{d\phi_s} + \frac{1}{C_{ox}} \frac{dQ_{it}}{d\phi_s} + 1. \quad (3.62)$$

Using Eq. (3.38), Eq. (3.62) is

$$\frac{dQ_{it}}{d\phi_s} = C_{ox} \left(\frac{dV}{d\phi_s} - 1 \right) - C_{dep}. \quad (3.63)$$

Using these relations, Eqs. (3.64) and (3.65),

$$dQ_{it} = qD_{it}dE, \quad (3.64)$$

$$dE = qd\phi_s, \quad (3.65)$$

the left term in Eq. (3.63) can be described as follow,

$$\frac{dQ_{it}}{d\phi_s} = q^2 D_{it}. \quad (3.66)$$

Thus, D_{it} can be expressed by the following equation,

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{dV}{d\phi_s} - 1 \right) - \frac{C_{dep}}{q^2}. \quad (3.67)$$

Using this equation, the interface state density can be extracted from experimental C - V curves. This is commonly called high-frequency method, also known as ‘‘Terman method’’.³

To apply Terman method to experimental C - V data, the appropriate value of C_{ox} has to be assumed at the beginning. Using Eq. (3.35) or (3.38), the relationship between C_{dep} and ϕ_s corresponding to the experimental C - V relation can be extracted. Then, using Eq. (3.67), D_{it} can be calculated. The differentiating V can be obtained the difference between the successions of V - ϕ_s relation in the experimental data. The energy position of the resulting interface states also is extracted as the average of those two successions of ϕ_s . Note that considering the frequency used in C - V the measurement is necessary to exclude the estimated

D_{it} data in the high-frequency limit. Therefore, in the actual analyses, the densities for very shallow states just near the conduction-band edge cannot be obtained due to the lower rate for the electron emission than the measurement frequency.

3.5.4. High-low method

D_{it} can also be extracted from the frequency dispersion of C - V curves between the high- and low- frequency limits.⁹

From the Eq. (3.53), C_{it} is extracted using the measured capacitance in the low-frequency limit C_{LF} as follows,

$$C_{it} = C_{dep} - (C_{LF}^{-1} - C_{ox}^{-1})^{-1}. \quad (3.68)$$

Using Eq. (3.59), C_{it} is expressed using C_{HF} , C_{LF} , and C_{ox} ,

$$C_{it} = (C_{HF}^{-1} - C_{ox}^{-1})^{-1} - (C_{LF}^{-1} - C_{ox}^{-1})^{-1}. \quad (3.69)$$

Then, the D_{it} can be obtained by Eq. (3.70),

$$\begin{aligned} D_{it} &= \frac{C_{it}}{q^2} \\ &= \frac{1}{q^2} (C_{HF}^{-1} - C_{ox}^{-1})^{-1} - \frac{1}{q^2} (C_{LF}^{-1} - C_{ox}^{-1})^{-1}. \end{aligned} \quad (3.70)$$

Here, ΔC is defined as the difference between C_{HF} and C_{LF} as given by Eq. (3.71),

$$\Delta C = C_{HF} - C_{LF}. \quad (3.71)$$

D_{it} is then obtained using the following equation,

$$D_{it} = \frac{\Delta C}{q^2} \left(1 - \frac{C_{HF} + \Delta C}{C_{ox}} \right)^{-1} \left(1 - \frac{C_{HF}}{C_{ox}} \right)^{-1}. \quad (3.72)$$

This extraction is called “High-low” method.

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Chapter 4.

Atomic layer deposition of Al_2O_3

4.1. Introduction

Atomic layer deposition (ALD) method is one of chemical vapor deposition (CVD) methods. In general CVD methods, two or more chemicals (gas, metal organic, or plasma) are introduced into a reactor at the same time. In contrast, ALD is based on the sequential injection of each chemical, leading to a monolayer-level deposition. Repeating the sequences, a thin film can be deposited by ALD method. According to a review by Parsons *et al.*,¹ the principle model for ALD was first proposed as “Molecular Layering” by Aleskovskii *et al.* in 1952.² The practical technology was then developed and published by Suntola in 1977.³ Nowadays, the ALD technique is widely used in the various semiconductor device manufactures such as Si complementary metal-oxide-semiconductor (CMOS), thin-film-transistor (TFT), and solar cell applications.

The advantages of ALD method are the thickness controllability and the large area capability with excellent uniformity because of simple chemical reactions. Theoretically, the thickness of the films can be determined only by the number of ALD cycles. This also leads to the reproducibility. The typical minimum thickness is around 0.1 nm, which is angstrom level. Also, ALD can realize the multilayer stack with different materials (SiO_2 , Al_2O_3 , HfO_2 , ZrO_2 ...). On the other hand, the slow reaction is sometimes likely to be disadvantage for depositing thicker films by ALD because the typical deposition duration for one cycle is 5 – 10 s.

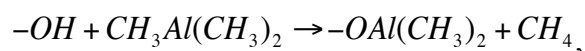
Park *et al.* first applied ALD method to GaN related materials in 2003.⁴ They fabricated GaN MIS-HEMTs using Al_2O_3 prepared by ALD for the first time. Since their

report, the number of studies on the ALD Al_2O_3 - and HfO_2 -based MIS-HEMTs has been gradually increased. We then have started to research regarding ALD for the GaN based electronic devices since 2008.

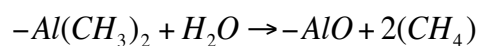
In this chapter, the principle of ALD is explained, mainly focusing on the model for depositing Al_2O_3 . The experimental procedures and results on the optical and chemical characterization of Al_2O_3 films used in this study are then introduced.

4.2. Model for atomic layer deposition of Al_2O_3

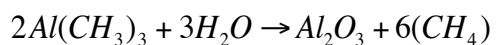
Fig. 4-1 schematically shows the model for atomic layer deposition of Al_2O_3 films. In the ALD process for depositing Al_2O_3 , trimethylaluminum (TMA) and water vapor H_2O are typically used as Al and O sources, respectively. N_2 or Ar gas is also used as a carrier gas. First, (a) when H_2O introduced, hydroxyl (OH) groups chemisorb on the Si surface. In the ideal case, chemisorption of OH groups can be saturated when the reaction sites at the surface are completely filled. This phenomenon is called “self-limiting reaction”. The excess H_2O molecules are then removed by evacuation of the reactor or by flowing the carrier gas. After evacuating, (b) TMA is then introduced. TMA can react only with OH groups on the surface prepared during the process (a). The possible reaction is described as follows,



which is also self-limited when all the OH groups react with introduced TMA as shown in the process (c). The excess TMA molecules and byproduct CH_4 are also removed. When (d) next H_2O injected to the reactor, H_2O can react only with the methyl (CH_3) group at the surface. The reaction of this process is described by the following formula,



As a result, one layer of Al-O can be formed on the surface. After reaching self-limiting condition, (e) evacuating the excess H_2O molecules and CH_4 are carried out. The OH groups left at the surface can be also used as reaction sites for next TMA injection. Those processes (b) - (e) correspond to 1 cycle for the ALD reaction, as expressed by the following formula,



Repeating this cycle, ALD can form the Al_2O_3 film in a layer-by-layer fashion, as shown in Fig. 4-1 (f). In the ideal ALD methods, the resulting thickness can be determined only by the number of cycles. Therefore, ALD methods have the advantage for controlling and reproducing thicknesses with a wide area, as compared with other deposition methods.

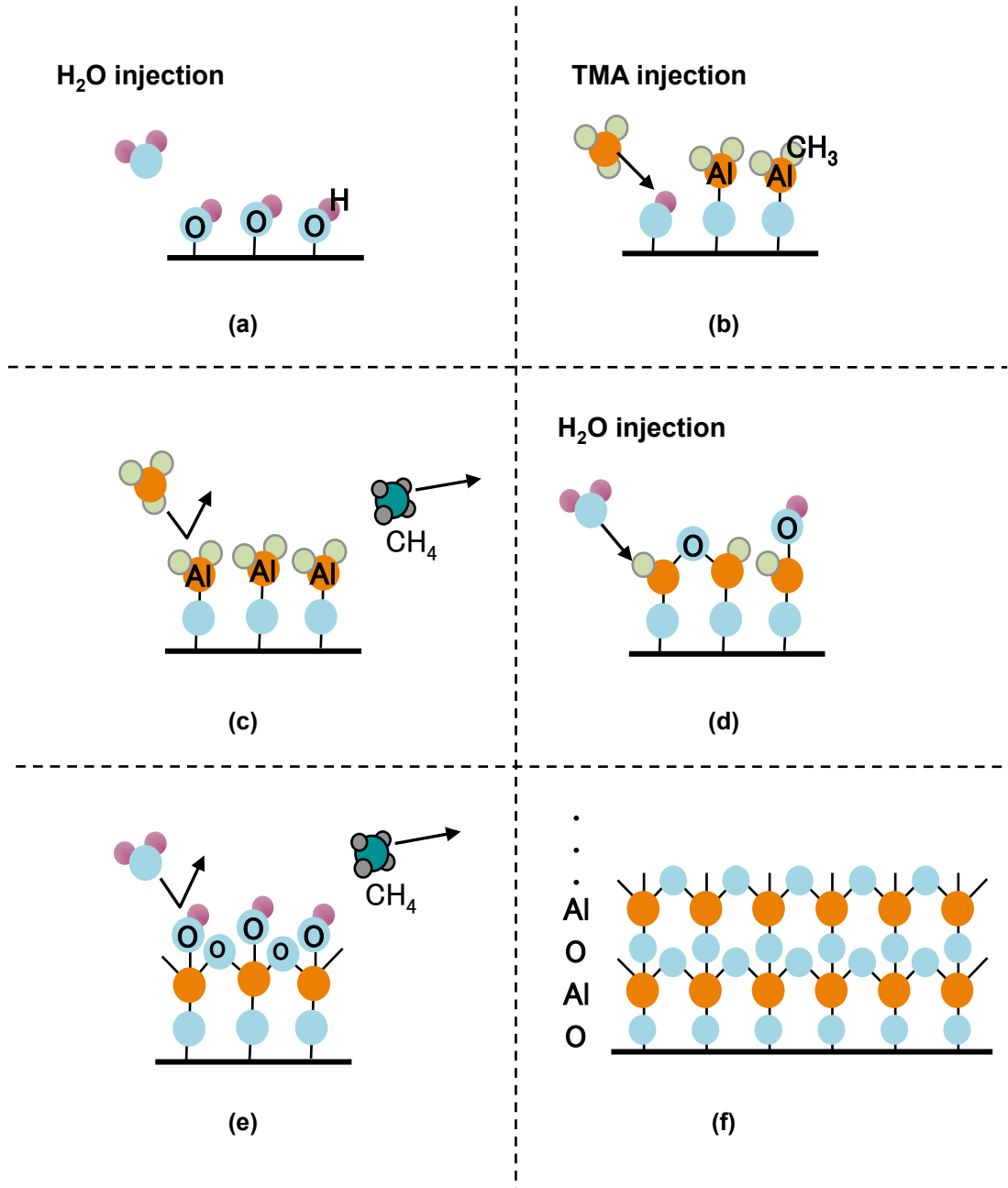


FIG. 4-1. Schematic illustrations of the ALD reactions for the deposition of the Al_2O_3 .

4.3. Experimental

4.3.1. Setup of ALD system

Fig. 4-2 schematically shows the basic setup for ALD system. In this study, the N_2 carrier gas continuously flows into the reactor chamber using a mass flow controller with the constant flow rate of 20 sccm. The reactor is also evacuated by a vacuum pump. Two precursor cylinders are attached to the N_2 flow line. Between the cylinders and the gas line,

Swagelok Diaphragm Valve for ALD equipped with Solenoid Pilot Valve Assembly is connected, which leads to pulse-like open/close to introduce each precursor for a very short time. The minimum pulse time is 10 ms. ALD valves and their connections are covered with a heater in order to keep them 150 – 160 °C. For depositing Al_2O_3 , each precursor is not necessary to be heated. The precursors and N_2 carrier gas are introduced to the heated stage. The typical temperature for the ALD Al_2O_3 is 250 – 350 °C. Fig. 4-3 show an example of the ALD sequence and its pressure waveform. In this case, each precursor is introduced in alternate pulse forms, resulting in the formation of Al_2O_3 in a layer-by-layer fashion as already mentioned above. The purging time 5 s is reasonable in removing the excess molecules and the byproducts entirely for the both precursors.

In this study, two types of ALD systems are used. Savannah S-100 made by Cambridge Nanotech was mainly used for the study in Chapter 5. For the research in Chapter 6, the new ALD system, model SAL1500, was developed by SUGA. Here, the basic properties for both ALD Al_2O_3 films are characterized in the following section. Table I shows the typical conditions for the both ALD processes.

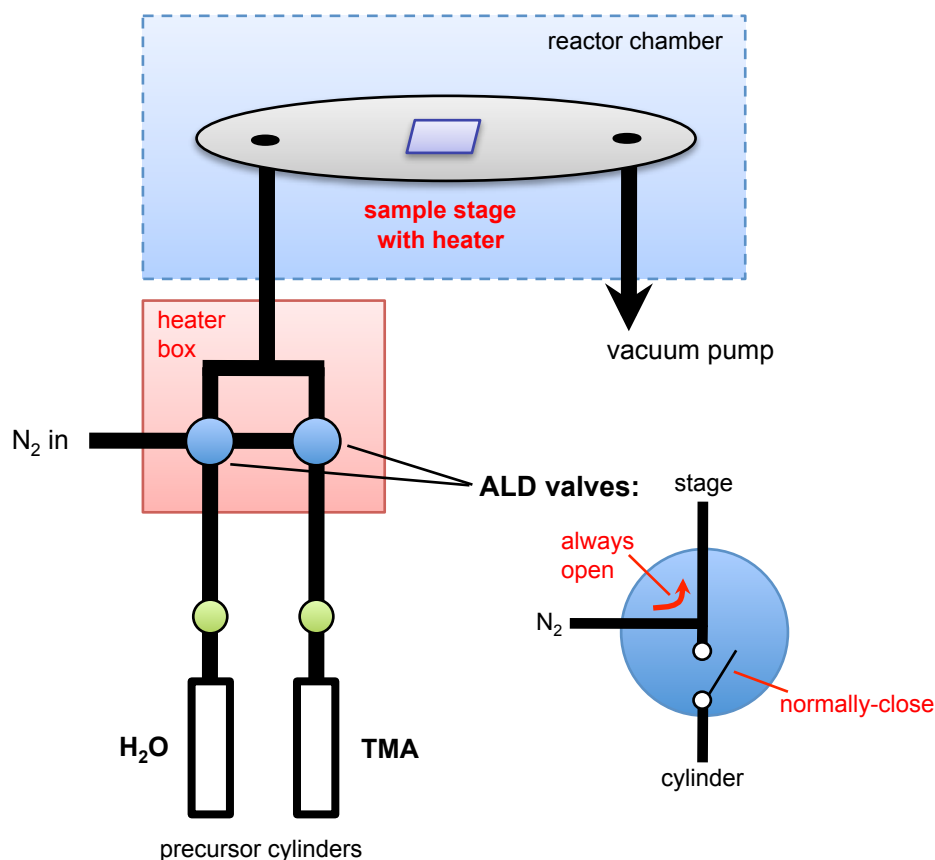


FIG. 4-2. Schematic illustration of the typical ALD system layout.

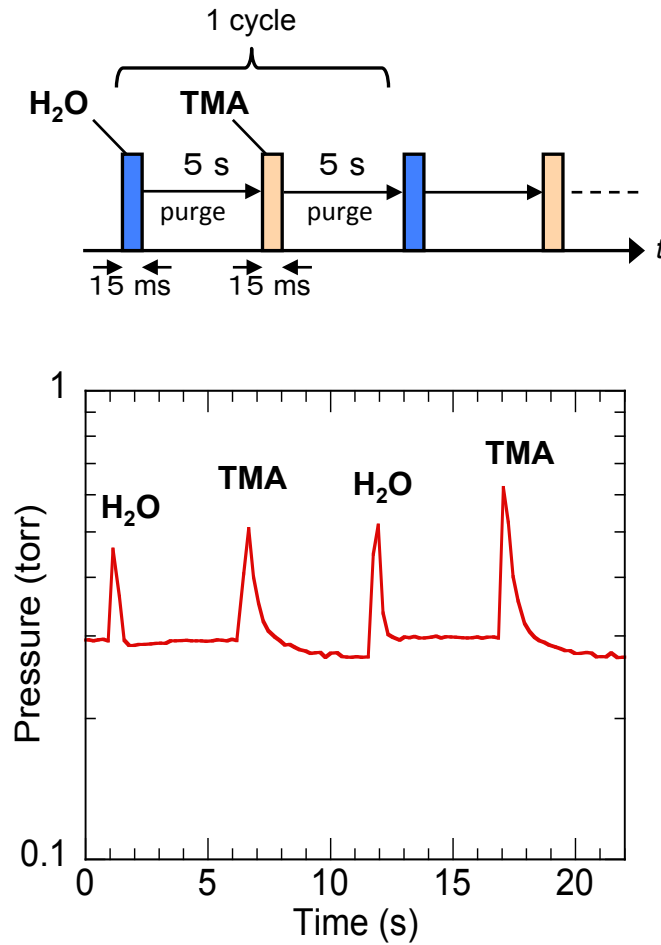


FIG. 4-3. Typical ALD sequence and corresponding pressure waveform.

4.3.2. Ellipsometry

To characterize optical properties of Al₂O₃ films prepared by the ALD systems, the ellipsometry is used. Fig. 4-4 schematically shows the measurement setup for the ellipsometry. Linearly polarized laser with a wavelength of 632.7 nm is injected to the sample. The injection angle is set to 70 °. If the reflection and/or transmission lead to the change of polarization, the amplitude component psi and the phase difference delta are measured at the detector. Assuming the optical properties, the used wavelength, and the thickness for the structure having one substrate and one film shown in Fig. 4-4, the one theoretical pair of psi and delta can be obtained by a known formula. Comparing the theoretical and experimental psi-delta relations, the thickness and optical properties of the film on the substrate can be estimated. In this study, ULVAC ESM-1AT is used as the ellipsometer. The measurements are carried out for Al₂O₃/Si structures.

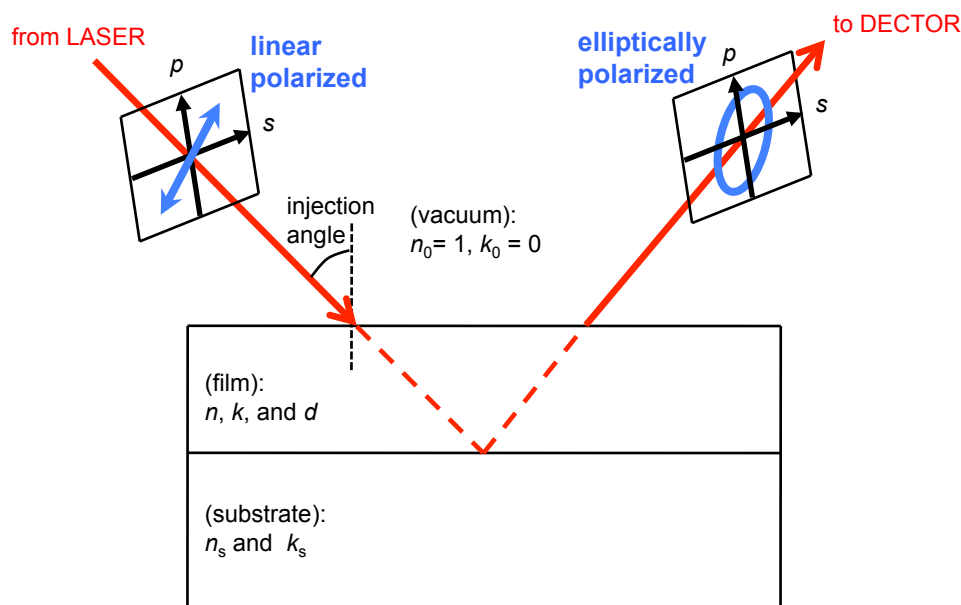


FIG. 4-4. Schematic illustration of the ellipsometry.

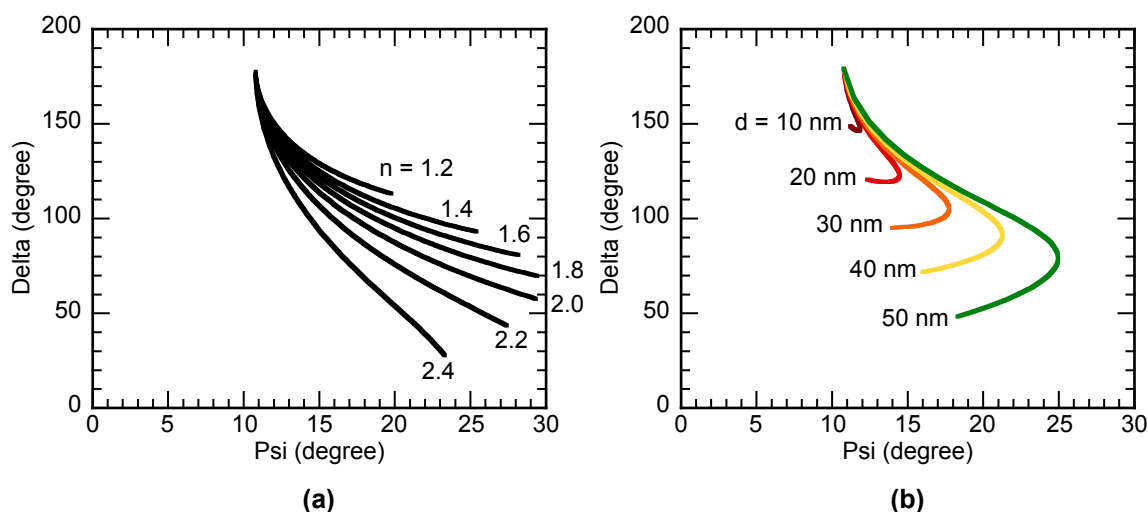


FIG. 4-5. Typical psi vs. delta relations for the oxide/Si structures.

4.3.3. X-ray photoelectron spectroscopy

Chemical properties of the Al_2O_3 films are characterized by x-ray photoelectron spectroscopy (XPS) using Perkin-Elmer PHI 1600C equipped with a spherical capacitor analyzer and a monochromated Al K α radiation source ($h\nu = 1486.6 \text{ eV}$). In XPS analyses, x-ray is applied to the sample surface in a vacuum chamber, leading to the photoelectron emission from the binding states in the sample as shown in Fig. 4-6. The kinetic energy of photoelectrons E_k corresponds to the binding energy E_b as described in the following

equation,

$$E_b = E_x - E_k - \Phi_s,$$

where E_x is the energy of induced x-ray and Φ_s is the workfunction of detector. Because the mean free path of the photoelectron is generally 1 – 4 nm, the chemical bonding properties near the sample surface can be characterized using the XPS measurements.

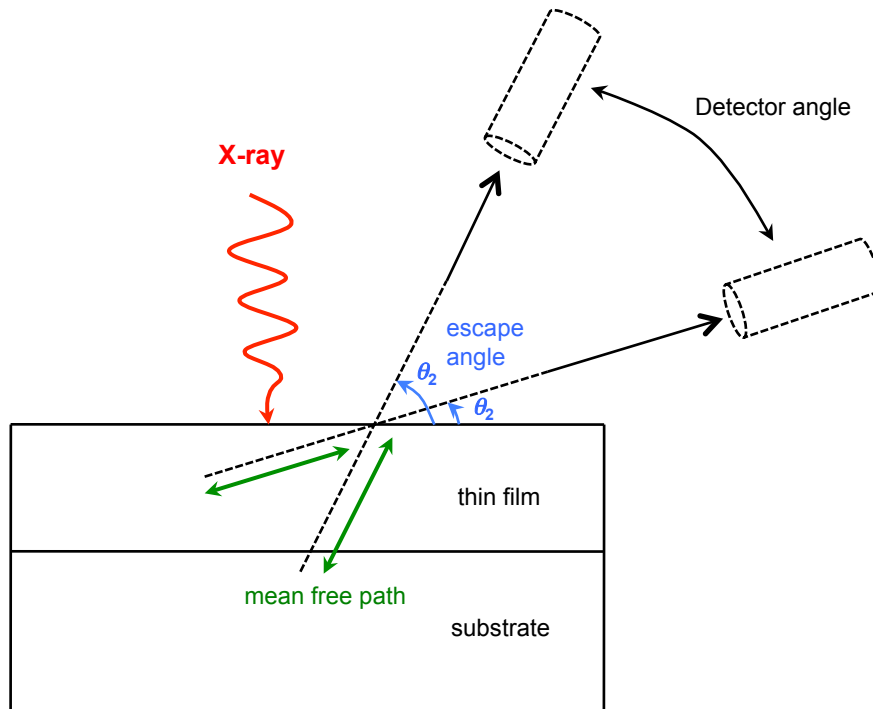


FIG. 4-6. Schematic illustration of x-ray photoelectron spectroscopy.

4.4. Results and discussion

4.4.1. Optical properties: refractive index, thickness, and deposition rate

Figure 4-7 shows the psi-delta relations obtained from the Al_2O_3 film deposited at 300 °C using Savannah S-100. The deposition of this Al_2O_3 was carried out at 300 °C. The refractive index of the Al_2O_3 film is estimated to be 1.65, which is close to typical values reported for the Al_2O_3 films prepared by the oxidation of thin metallic Al and other ALD methods. For the sample of 450 cycles, the obtained thickness is 42 nm, resulting in the deposition-rate of 0.093 nm/cycles. The psi-delta relations for the Al_2O_3 film deposited at 350 °C using SUGA SAL1500 are also shown in Fig. 4-8. The refractive index is similar to that of the Al_2O_3 prepared by Savannah S-100. The average deposition-rate of the Al_2O_3 films is approximately 0.106 nm/cycle, which is close to that for Savannah S-100. Fig shows the thickness distribution map of the Al_2O_3 film deposited for 457 cycles at 300 °C by

Savannah S-100. The ALD Al_2O_3 showed a good thickness uniformity within ± 1 nm.

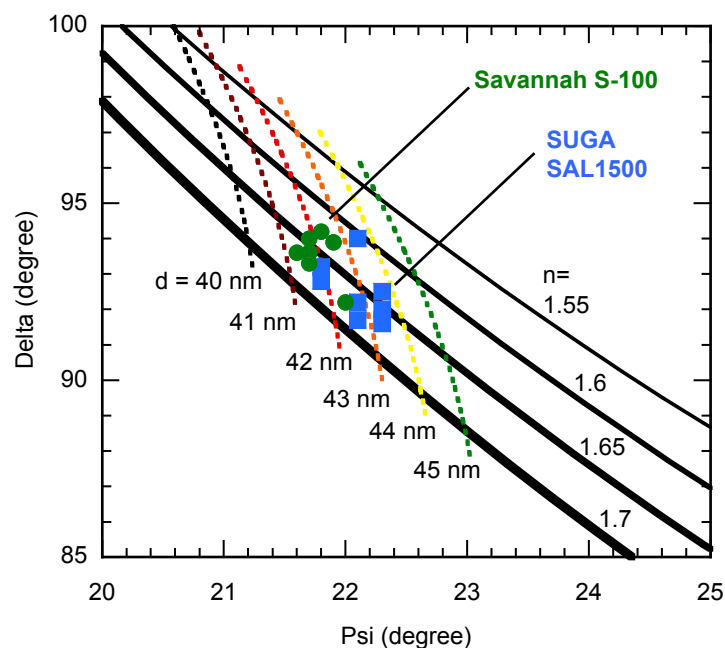


FIG. 4-7. Psi and delta relations obtained from the Al_2O_3 film prepared by Savannah S-100 for 450 cycles and SUGA SAL1500 for 405 cycles.

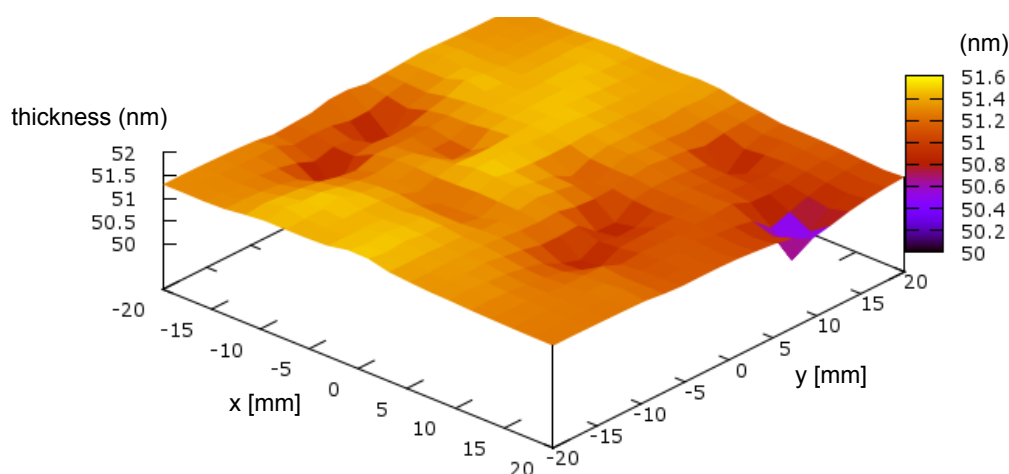


FIG. 4-8. Thickness distribution map of the Al_2O_3 film deposited for 457 cycles by Savannah S-100.

4.4.2. Chemical properties: composition, impurities, and bandgap

(a) Chemical composition of the Al_2O_3 films

Fig. 4-8 shows the XPS wide-scan spectra obtained from the Al_2O_3 prepared by Savannah S-100 and SUGA SAL1500. The spectrum obtained from the crystalline sapphire

is also plotted as a reference. The both ALD systems showed the similar spectra of sapphire, indicating that the main compositions of the deposited films are Al and O. The Al 2p spectrum of ALD Al_2O_3 was compared with that of crystalline Al_2O_3 (sapphire) in Fig. 4-10(a). The peak positions of both spectra were very close. This feature is also observed in XPS O 1s spectra as shown in Fig. 4-10(b). These indicate that the Al-O bond is dominant in atomic configuration. The linewidth of ALD Al_2O_3 was slightly wider than that of the reference sapphire, probably arising from the amorphous phase of ALD Al_2O_3 .

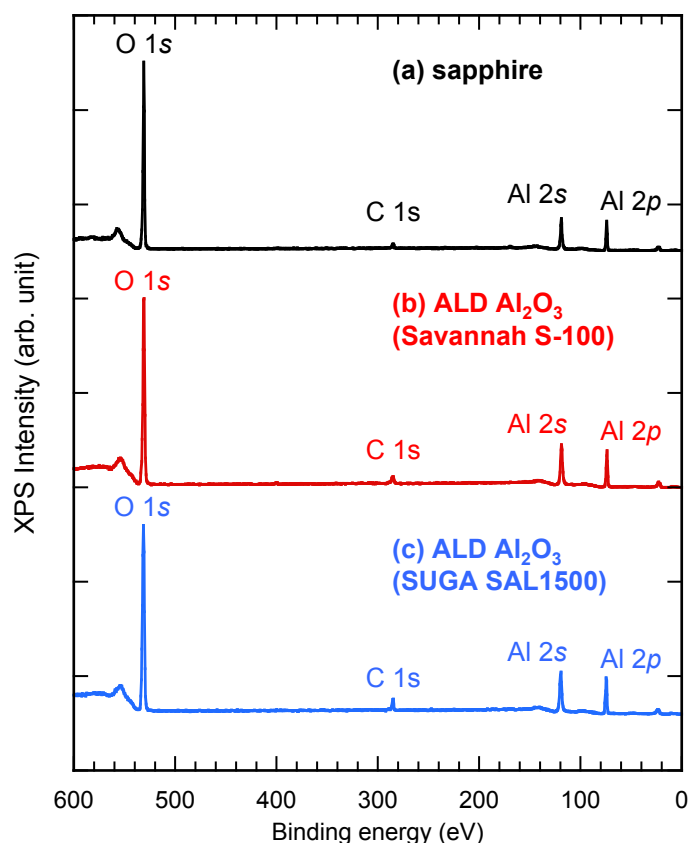


FIG. 4-9. Wide-scan spectra obtained from the Al_2O_3 films prepared by Savannah S-100 and SUGA SAL1500.

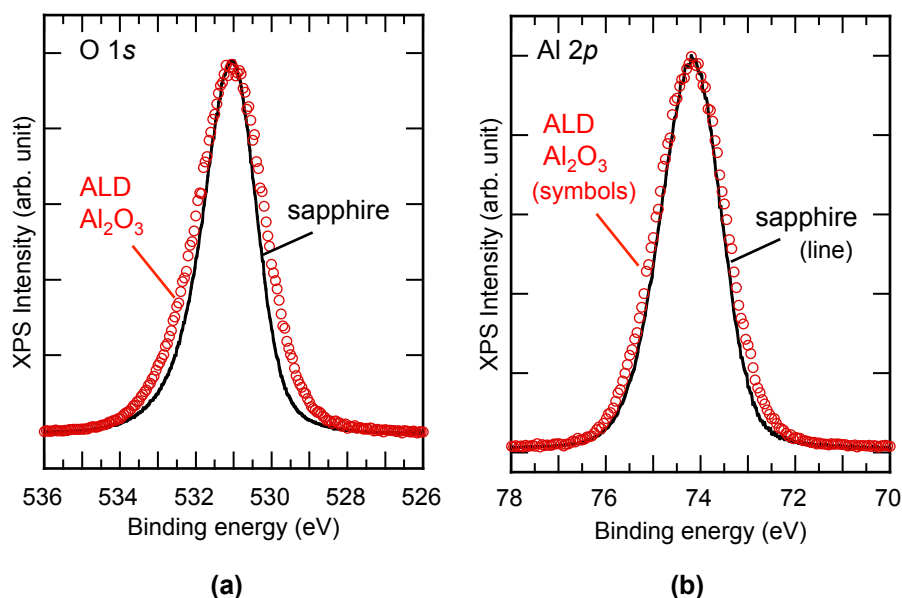


FIG. 4-10. (a) O 1s and (b) Al 2p spectra obtained from the Al₂O₃ film prepared by Savannah S-100.

(b) Impurities in the Al₂O₃ films

Figures 4-11(a) compares the XPS O 1s spectra obtained from 1nm-thick and 20nm-thick of Al₂O₃ deposited on n-GaN taken at the escape angle of 45 °. For the both escape angles, the spectrum of the 1nm-thick Al₂O₃ showed the higher peak energy position and the broader linewidth. There is a possibility that some kinds of C-O bonds originating from methyl group are incorporated into Al₂O₃ at an initial stage of the ALD process. The Ga 3d spectra of the n-GaN surface with and without the 1nm-Al₂O₃ layer are shown in Fig. 4-11 (b). Both spectra are almost the same, indicating that the ALD process did not cause significant degradation on the chemical bonding structure of n-GaN surface.

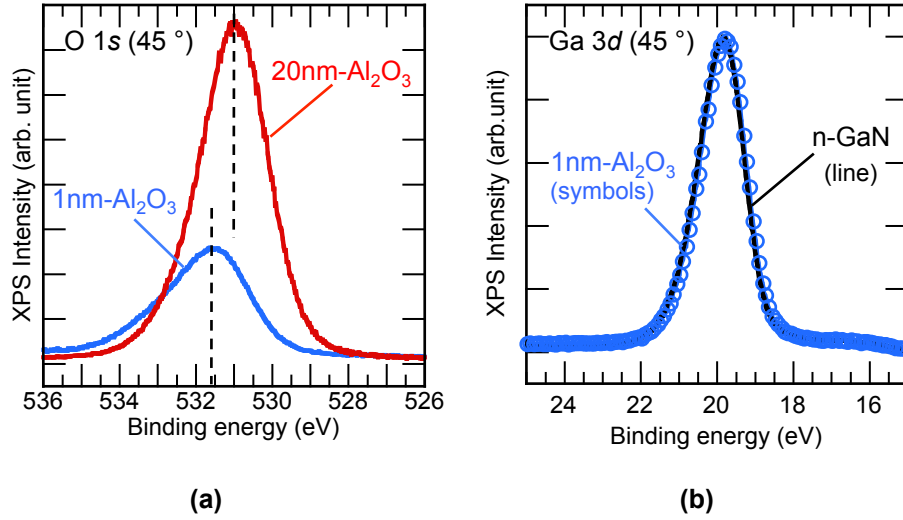


FIG. 4-11. (a) O 1s and (b) Ga 3d spectra obtained from 3nm-Al₂O₃/n-GaN interface prepared by Savannah S-100.

To characterize the impurity profiles of the Al₂O₃, the secondary ion mass spectroscopy (SIMS) analysis was performed. Cs⁺ ions were applied to the samples with an acceleration voltage of 3 keV. Figures 4-12 and 4-13 show the SIMS profiles of the 45nm-thick Al₂O₃ films deposited on Si prepared by Savannah S-100 and SUGA SAL1500, respectively. To quantify the densities of the impurities, the sensitive factors for the sapphire (crystalline Al₂O₃) were used as reference values. For both samples, the densities of C and H showed almost constant values of 1×10^{20} atoms/cm³ and 5×10^{21} atoms/cm³, respectively, throughout the deposited Al₂O₃ layers. The marked high density of H impurities is the characteristic feature for the ALD Al₂O₃ using H₂O vapor, probably arising from –OH groups in the film.⁵ Note that there is highly possibility that the high densities of H lead to an error in the quantity of impurities.

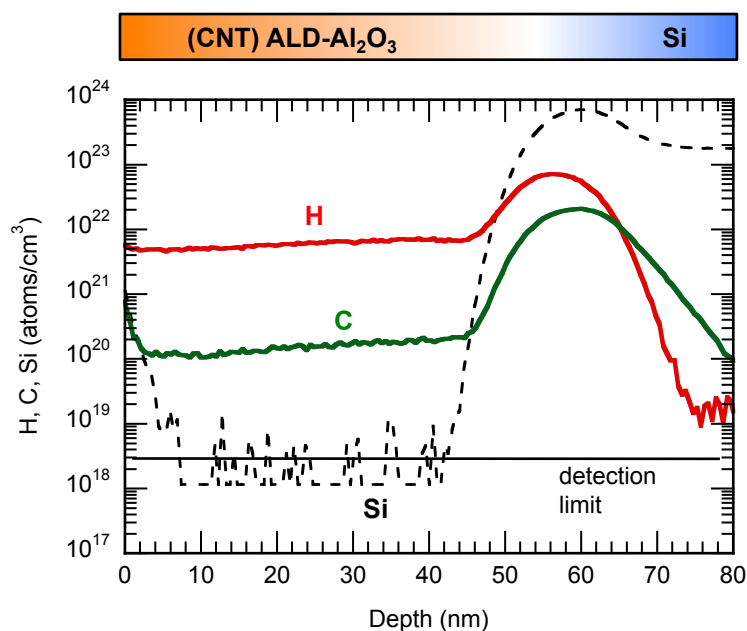


FIG. 4-12. SIMS profiles of the Al_2O_3 films prepared by Savannah S-100 at 250 °C.

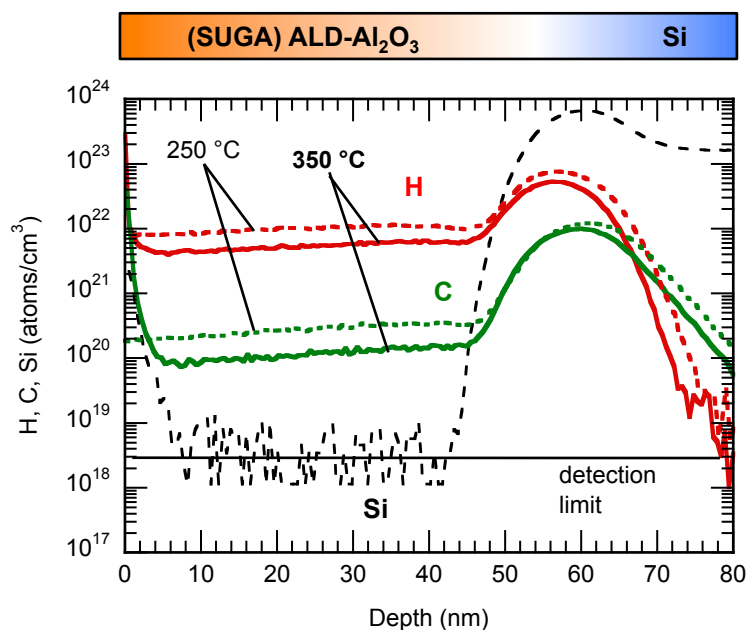


FIG. 4-13. SIMS profiles of the Al_2O_3 films prepared by SUGA SAL1500 at 250 °C and 350 °C.

(c) Bandgap of the Al_2O_3 films

The bandgap, E_G , of Al_2O_3 was estimated from the energy-loss peak in the O 1s spectrum.⁶ As shown in Fig. 4-14, the onset of the loss-peak line gave $E_G = 6.7$ eV, which is close to the data reported for thin Al_2O_3 layers prepared by the oxidation of metallic Al and the ALD method.⁶⁻⁹

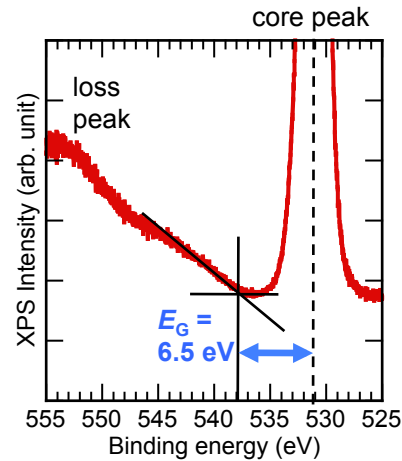


FIG. 4-14. O 1s spectra including energy loss peak obtained from the Al_2O_3 films prepared by Savannah S-100 and SUGA SAL1500.

4.5. Summary

In Chapter 4, the principle of the ALD method and the basic properties of the Al_2O_3 films prepared by ALD are introduced. The deposition rate was estimated to be 0.1 – 0.11 nm/cycle, which is typical value reported for the ALD methods. The refractive index of the ALD Al_2O_3 was in good agreement with that of AlO_x films prepared by other methods. Besides that, the results obtained from XPS analysis indicated that Al and O are the main composition of the deposited films. The major impurities distributed in the ALD Al_2O_3 were C and H. The H density, in particular, showed higher than that of C, indicating that the post annealing process is probably necessary for reducing impurities and their related charges. The bandgap of ALD Al_2O_3 was estimated to be 6.7 eV, which probably leads to the conduction-band offset large enough against GaN-related widegap materials. The following Chapter 5 and 6 investigate the electrical properties and interface state properties of $\text{Al}_2\text{O}_3/\text{GaN}$ and $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ structures prepared by those ALD techniques.

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Chapter 5.

Process conditions for improvement of electrical properties of $\text{Al}_2\text{O}_3/\text{n-GaN}$ metal-oxide-semiconductor structures

5.1. Introduction

GaN and its related heterostructures are very promising for high-power and high-frequency devices owing to their excellent properties, such as a high breakdown field and a high saturation electron velocity. A SiN-based structure is currently the standard used for the surface passivation of AlGaN/GaN high-electron mobility transistors (HEMTs) because of good interface properties between SiN and GaN-based semiconductors.¹⁻³ However, the bandgap of SiN (~5 eV) is not high enough to keep sufficient barriers against the conduction and valence bands of wide-gap semiconductors, which leads to severe leakage phenomena in a gate structure, particularly at a forward bias.² Indeed, for realizing high-power switching devices, it is essential to make robust and reliable insulated-gate structures with low interface state densities.

Aluminum oxide (Al_2O_3) has relatively high permittivities (8–10) and large bandgap (7–9 eV), which are very attractive for gate-structure application in field effect transistors (FETs) and HEMTs.⁴⁻¹⁰ However, the properties of the $\text{Al}_2\text{O}_3/\text{GaN}$ interface have not been well understood, and the fabrication process is not well established yet.

In this chapter, we report the effects of fabrication processes on the electrical properties of $\text{Al}_2\text{O}_3/\text{GaN}$ structures, including interface state densities, prepared by atomic layer deposition (ALD). We then demonstrate control of interface states in $\text{Al}_2\text{O}_3/\text{n-GaN}$ system.

5.2. Measurements

5.2.1. Current-voltage measurement

In this chapter, current-voltage (I - V) measurements are performed using Agilent 4156C Semiconductor Parameter Analyzer. 4156C is connected to a probe station with Triaxial (TXA) cables. The instrument is entirely controlled by the computer with Agilent Desktop EasyEXPERT.

5.2.2. Capacitance-voltage measurement and analysis

Yokogawa-Hewlett-Packard 4192A Impedance Analyzer is used for capacitance-voltage measurements in this chapter. After connecting the instrument to the probe station, open- and short-calibrations must be done correctly. To obtain proper measurement results, ‘averaging’ mode without ‘high speed’ scan is chosen on the front panel of the instrument. The resulting measurement duration and resolution are approximately 1.1 s/step and 0.1 pF, respectively. The instrument is also connected to the computer using GPIB interface. Measurements are automatically carried out using a control-software which is developed with National Instrument LabVIEW.

To estimate interface states from C - V results, ‘Terman method’ mentioned in the previous chapter is used in this chapter. The analysis is performed using a computer. Fig. x shows the flowchart of ‘Terman method’ program. At first, ideal capacitance-voltage-surface potential C - V - ϕ_s relation is calculated using the equations shown in Chapter 3. A division of ϕ_s is set to 0.001 eV in the calculation. Comparing ideal and experimental C - V data, ϕ_s of the experimental capacitance at each gate bias is stored to a data array.

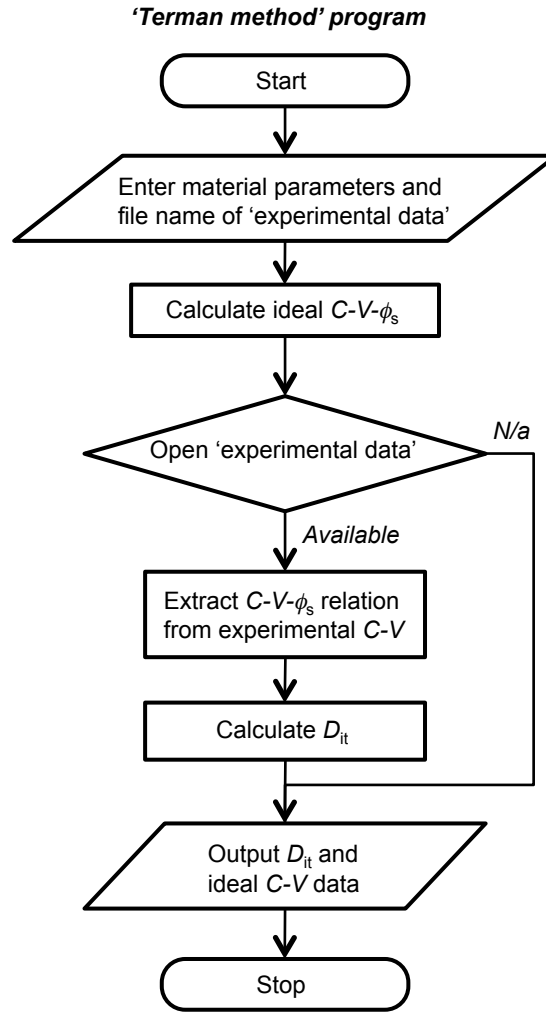


FIG. 5-1. Flowchart of the “Terman method” program.

5.3. ‘Deposition-first’ process

5.3.1. Fabrication process

Figures 5-2 and 5-3 show the sample structure and fabrication process that is firstly applied to an $\text{Al}_2\text{O}_3/\text{n-GaN}$ diode structure, respectively. We used n-GaN with an electron density of $5 \times 10^{17} \text{ cm}^{-3}$ grown on a sapphire substrate by metal organic chemical vapor deposition. After the pretreatment of the n-GaN surface in a 30% HF solution for 5 min, we deposited an Al_2O_3 layer on the GaN surface by ALD using Savannah-S100 (Cambridge NanoTech). In the ALD process, water vapor (H_2O) used as an O source and trimethylaluminum (TMA) used as an Al source were introduced into a reactor chamber in alternate pulse forms, resulting in the formation of Al_2O_3 in a layer-by-layer fashion. The N_2 carrier gas continuously flowed into the reactor, and the base pressure in the reactor was

approximately 40 Pa. Each precursor was injected into the reactor for 15 ms, and the purging time was set to 5 s. As already mentioned in chapter 3, the growth rate was estimated to be 0.11 nm/cycle. The deposition was carried out at 250 °C for 182 cycles, resulting in an Al_2O_3 thickness of 20 nm. By ellipsometry measurement using 632.8 nm light, the refractive index was estimated to be 1.55–1.60 which is close to the values of 1.60–1.65 reported for the amorphous Al_2O_3 films produced by the sputtering and ALD methods.^{11,12} A Ti/Al/Ti/Au (=20/50/20/100 nm) multilayer structure was deposited on the n-GaN surface as a ring-shaped ohmic contact, followed by annealing at 800 °C for 1 min in N_2 ambient. A circular Ni/Au (=20/50 nm) structure with a diameter of 200 μm was deposited on the Al_2O_3 surface as a gate electrode. The space between gate and ohmic electrodes is set to 100 μm .

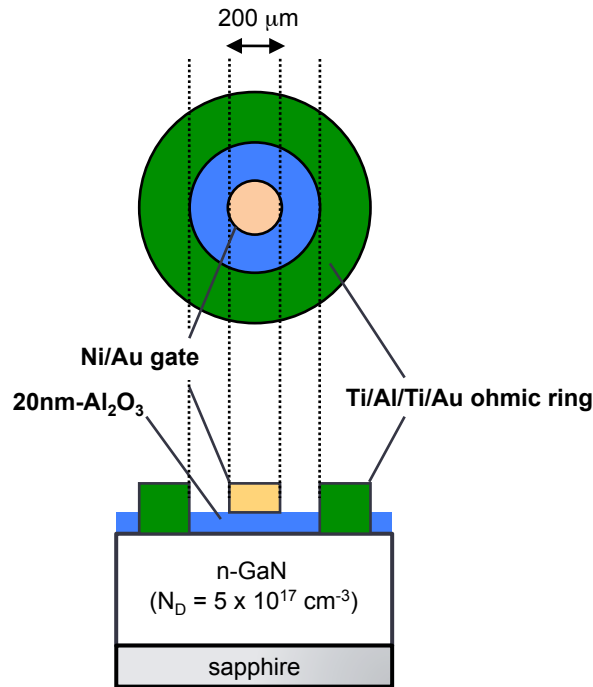


FIG. 5-2. Schematic illustrations of the ALD- Al_2O_3 /n-GaN diode structure.

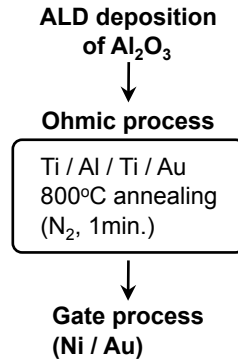
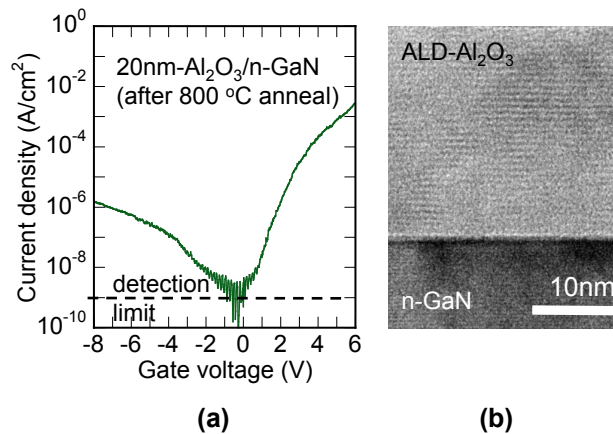
'Deposition-first' process

FIG. 5-3. Flowchart of the “deposition-first” process.

5.3.2. I - V characteristics

A typical current-voltage (I - V) curve of the $\text{Al}_2\text{O}_3/\text{GaN}$ structure is shown in Fig. 5-4(a). Unexpectedly, a very leaky behavior similar to that of a Schottky diode was observed. In fact, high leakage currents impeded the control of the surface potential of GaN in the forward bias region. To understand such a serious problem, we carried out the transmission electron microscopy (TEM) analysis of the $\text{Al}_2\text{O}_3/\text{GaN}$ interface. As shown in Fig. 5-4(b), microcrystallization regions were distributed throughout the Al_2O_3 layer. They were probably generated during the annealing process at 800 °C for the ohmic electrode formation. The grain boundaries in the Al_2O_3 layer can serve as high-leakage paths, leading to the Schottky-like I - V curve shown in Fig. 5-4(a).

FIG. 5-4. (a) I - V characteristics and (b) TEM image of the ALD- $\text{Al}_2\text{O}_3/\text{n-GaN}$ structure.

5.4. ‘Ohmic-first’ process

5.4.1. Fabrication process with SiN surface protection

To overcome the problem mentioned in the previous section, we employed the “ohmic-first” process for the fabrication of the $\text{Al}_2\text{O}_3/\text{GaN}$ structure, as shown in Fig. 5-5. For comparison, two kinds of samples were prepared: samples with and without a surface protection layer for the first ohmic annealing process. The former sample has a 10-nm SiN film as a surface protection layer that was deposited on the GaN surface at 260 °C by electron cyclotron resonance chemical vapor deposition. After the ohmic electrode process, we removed the SiN protection layer using a buffered HF solution, followed by the deposition of Al_2O_3 on the GaN surface.

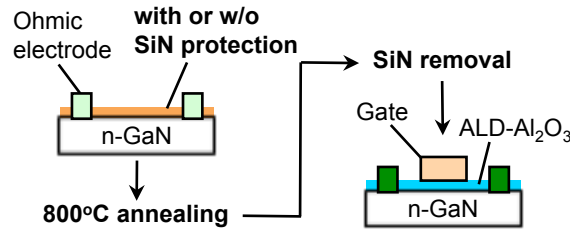


FIG. 5-5. Flowchart of the “ohmic-first” process.

5.4.2. Improved I - V characteristics

The I - V curve of the $\text{Al}_2\text{O}_3/\text{GaN}$ structure prepared by the ohmic-first process is shown in Fig. 5-6(a). We observed low leakage currents (close to the detection limit) except for forward voltages larger than 3.5 V. The TEM image of this sample is shown in Fig. 5-6(b). The interface between ALD- Al_2O_3 /n-GaN was very flat. In addition, an amorphous phase was kept in the atomic bonds of Al_2O_3 , resulting in the suppression of leakage current. The increase in current at a forward bias larger than 3.5 V can be governed by the Fowler-Nordheim (FN) tunneling mechanism, because we confirmed the linear relation of $\log(J/E^2)$ vs $1/E$ (here, J is the current density and E is the electric field),^{2,16} as shown in the inset of Fig. 5-6(a). From such FN plots, we estimated 2.2 eV for the conduction band offset, ΔE_C , between Al_2O_3 and GaN, which is close to the expected values of 2.0–2.5 eV.^{4,17}

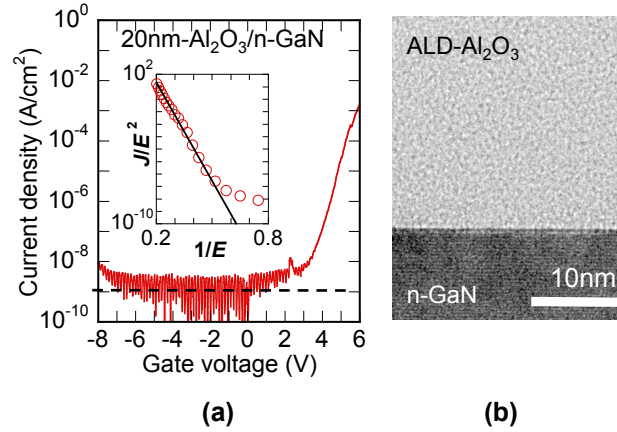


FIG. 5-6. (a) I - V characteristics and (b) TEM image of the ALD- $\text{Al}_2\text{O}_3/\text{n-GaN}$ structure prepared by the “ohmic-first” process. The inset in (a) indicates Fowler-Nordheim (FN) plots.

5.4.3. C - V characteristics and D_{it} distributions

Figure 5-7 shows the typical C - V characteristics of the $\text{Al}_2\text{O}_3/\text{n-GaN}$ structures prepared by the ohmic-first process. From the maximum capacitance, the permittivity of ALD- Al_2O_3 was estimated to be 9.5, being a typical value reported for amorphous aluminum oxides. For the sample using the SiN protection layer, the measured C - V curve was very close to the ideal one (deep-depletion mode) calculated without assuming interface states. The deep-depletion behavior in the negative bias region is the characteristic feature of wide-gap semiconductors, mainly due to the extremely low generation rate of minority carriers (holes in this case) at RT.^{18,19} On the other hand, the sample without the surface protection layer showed poor C - V behavior. In particular, a nearly plateau region appeared in the negative bias range, indicating the inhibition of surface potential control due to the existence of high-density electronic states at the $\text{Al}_2\text{O}_3/\text{n-GaN}$ interface.

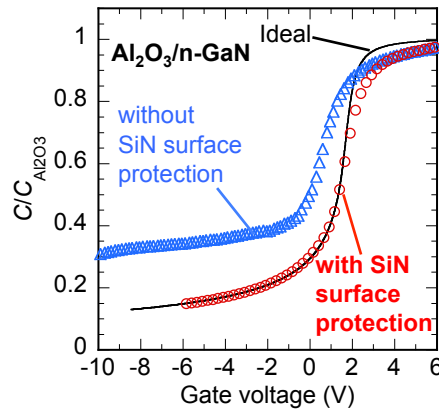


FIG. 5-7. C - V characteristics of the ALD- $\text{Al}_2\text{O}_3/\text{n-GaN}$ structures prepared by the “ohmic-first” process with and without the SiN protection layer.

Figure 5-8 shows the electronic state density distributions of the ALD- $\text{Al}_2\text{O}_3/\text{GaN}$ interfaces calculated by applying the Terman method to the measured C - V data.²⁰ Note that the time constant of electron emission is extremely long at RT for interface states with deep energies from the conduction band edge.^{2,21,22} We thus plotted the calculated data within $E_C - 1.0$ eV in Fig. 5-8. The ohmic annealing process at 800 °C without the SiN protection layer caused a high interface state density, particularly at energies from 0.5 to 1.0 eV. It was likely that the high-temperature annealing induced the preferential desorption of N atoms from the GaN surface, leaving N-vacancy-related defect states at the surface.²³ In comparison, low interface state densities of less than $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ were observed in the sample with the SiN protection layer. The SiN layer can suppress N desorption and related chemical disorder at the GaN surface even during high-temperature annealing. Although interface states at the lower half of the bandgap will be characterized by using separate techniques, e.g., monochromatic photon-assisted admittance spectroscopy, the ALD- Al_2O_3 -based gate structure prepared with a suitable surface control process is promising for a reliable and stable operation of GaN-based transistors.

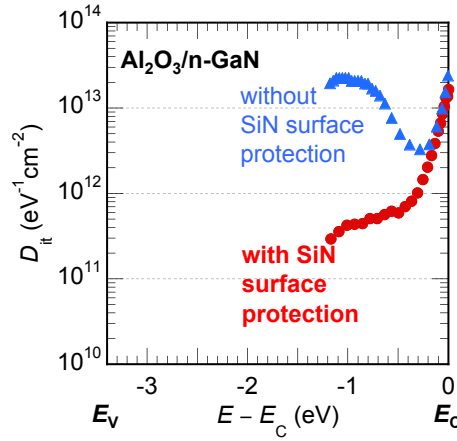


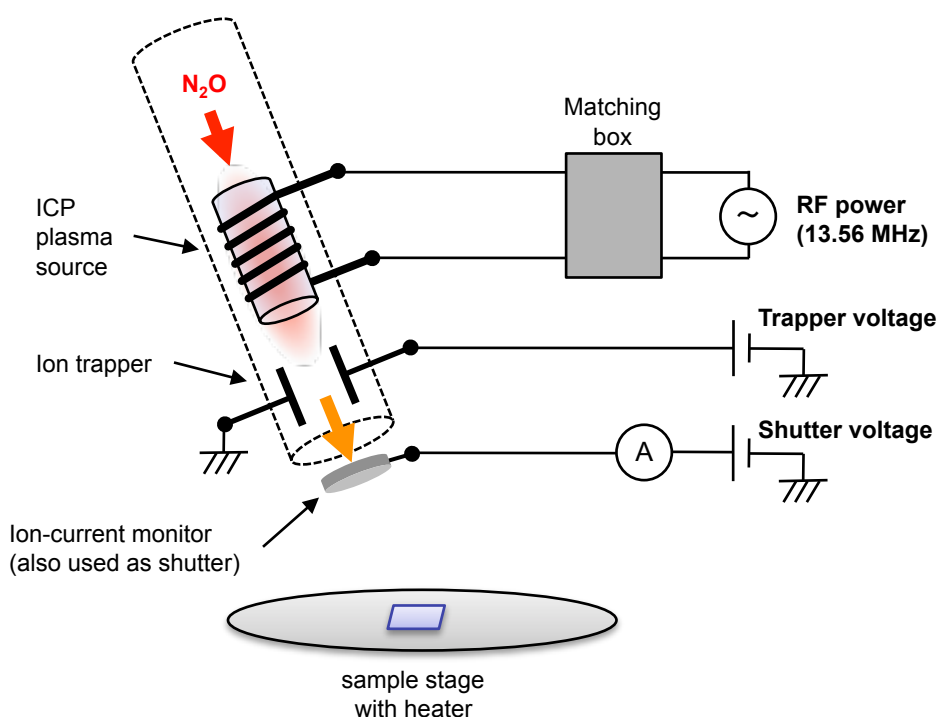
FIG. 5-8. Interface state density distributions of the ALD-Al₂O₃/n-GaN structures prepared by the “ohmic-first” process with and without the SiN protection layer.

5.5. Control of interface states using N₂O-radical treatment

5.5.1. Process condition

As an additional surface control process just prior to the deposition of Al₂O₃, an N₂O-radical treatment was performed in a vacuum chamber equipping EIKO ER-1000 Radical Beam Source. Fig. 5-9 shows the schematic illustration of the inductively coupled (ICP) plasma source with a radio frequency (RF) power source, matching box, ion trapper, and ion-current monitor. N₂O gas is introduced into the chamber with a constant flow rate of 1.1 sccm. Applying the RF power of 200 W, N₂O plasma is produced in the plasma source. The ion trapper is equipped near the exit of plasma source to capture produced electrons and ions, leading to carrying radicals without any electrons or ions to the sample surface. Before opening the shutter, the ion current can be monitored using the shutter as an electrode. In this study, the trapper voltage of 550 V is applied, resulting in the ion current of almost zero. The substrate temperature and exposure time were set to 300 °C and 10 min, respectively. In this experiment, the ohmic-first process with the SiN protection is employed, as indicated in Fig. 5-5. After removing the SiN surface protection layer in BHF solution, the sample was immediately loaded to the chamber and treated using the N₂O-radical beam source. After the treatment, the sample was carried through ex-situ, and the Al₂O₃ film was then deposited on the treated n-GaN by ALD. In this experiment, the deposition was carried out using SUGA-SAL1500 at 350 °C for 170 cycles. The resulting thickness of the Al₂O₃ film was estimated to be 20 nm.

EIKO ER-1000 Radical Beam Source

FIG. 5-9. Schematic illustration of radical beam source for the N_2O -radical treatment.

5.5.2. Improved C - V characteristics and D_{it} distributions

Figure 5-10 shows the C - V characteristics of the Al_2O_3/n -GaN diode structures fabricated with and without the N_2O -radical treatment. For the sample without the surface treatment, the measured C - V slope was different from the ideal one. On the other hand, the N_2O -radical treatment realized good C - V behavior close to the ideal curve.

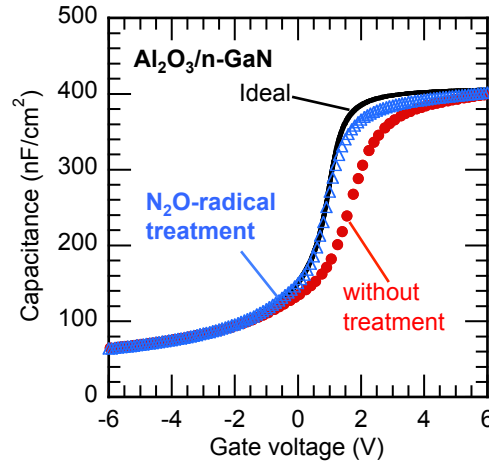


FIG. 5-10. C - V characteristics of $\text{Al}_2\text{O}_3/\text{n-GaN}$ structures without and with the N_2O -radical treatment.

Figure 5-11 shows the electronic state density distributions of the $\text{Al}_2\text{O}_3/\text{n-GaN}$ interface estimated by applying the Terman method to the measured C - V data. The calculated data was plotted within $E_C - 1.0$ eV, because the time constant of the electron emission is extremely large at RT for the interface state with deep energies from the conduction band edge. The sample without the surface treatment showed state densities of around $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at energies from -0.4 to -1.0 eV, which is similar to the result shown in Fig. 5-8. For the N_2O -radical treated sample, in comparison, very low state densities with values of equal to or below the detection limit were observed.

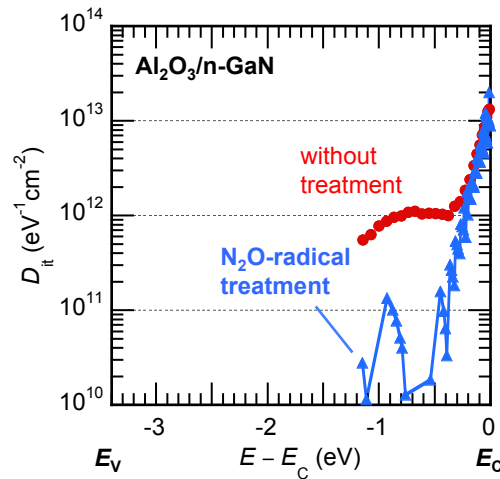


FIG. 5-11. D_{it} distributions at $\text{Al}_2\text{O}_3/\text{n-GaN}$ interfaces without and with the N_2O -radical treatment.

5.5.3. Chemical analysis of N₂O-radical treated GaN surface

X-ray photoelectron spectroscopy analysis of the GaN surface subjected to the N₂O-radical treatment was also performed. Fig. 5-12 shows the O 1s, N 1s and Ga 3d spectra obtained from the GaN surfaces before and after the N₂O-radical treatment. Each spectrum was taken with a photoelectron escape angle of 45° and normalized to the Ga 3d peak. In the Fig. 5-12(b), the enhancement of O 1s spectrum is probably arising from an oxidation of the GaN surface due to the N₂O-radical treatment. Indeed, the chemical shift probably due to the GaO_x bonds was observed in the Ga 3d spectra (Fig. 5-12(c)). In the N 1s spectra, on the other hand, there are not pronounced chemical shifts or broadening for both samples, indicating that there is no degradation of chemical bonds in the GaN layer. The results also indicated that the present N₂O-radical treatment formed the GaO_x layer with a thickness of 1 nm or less. Bae *et al.*²⁴ reported that an ultra thin Ga-oxide interfacial layer prepared by the remote plasma-assisted oxidation process achieved a low interface state density for the SiO₂/n-GaN system. In our case, it is likely that the monolayer-level formation of a Ga-oxide layer prepared from the N₂O-radical treatment is effective in the reducing interface states in the Al₂O₃/n-GaN structure. The thickness of the oxidation layer was also confirmed in next section using the TEM observation.

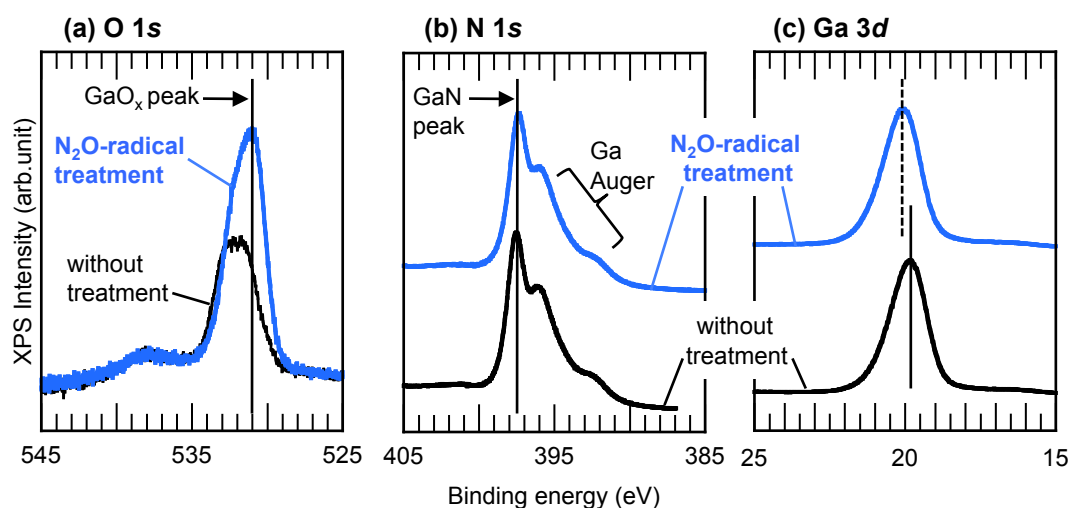


FIG. 5-12. (a) O 1s, (b) N 1s, and (c) Ga 3d spectra obtained from n-GaN surfaces before and after the N₂O-radical treatment.

5.5.4. TEM observation of N₂O-radical treated Al₂O₃/GaN interface

Figures 5-13(a) and (b) show the TEM images of 2-nm-thick Al₂O₃/n-GaN structures

without and with the N₂O-radical treatment, respectively. For both samples, the interface between Al₂O₃ and GaN was flat, as also confirmed in the previous experiment (Fig. 5-6(b)). However, there were no significant differences in both images. For further confirmation, Figs. 5-13(c) and (d) show the brightness profiles of the arrows indicated in Figs. 5-13(a) and (b), respectively. Note that each profile was averaged within a 10-nm width. For both samples, periodic contrast changes correspond to the periodic Ga and N distributions in the GaN layer. On the other hand, not periodic contrast near the sample surfaces is probably arising from the amorphous phase in the Al₂O₃ region. For the sample without the treatment shown in Fig. 5-13(c), the periodicity in the GaN layer steeply disappeared at the interface, indicating that there is no interlayer between the Al₂O₃ and GaN layers. As shown in Fig. 5-13(d), in contrast, the N₂O-radical treated interface has a darker non-periodic region than that in the Al₂O₃ layer, probably due to the GaO_x layer. The thickness of the interlayer was estimated to be 0.7 nm, which is consistent with the results of XPS analysis shown in Fig. 5-12.

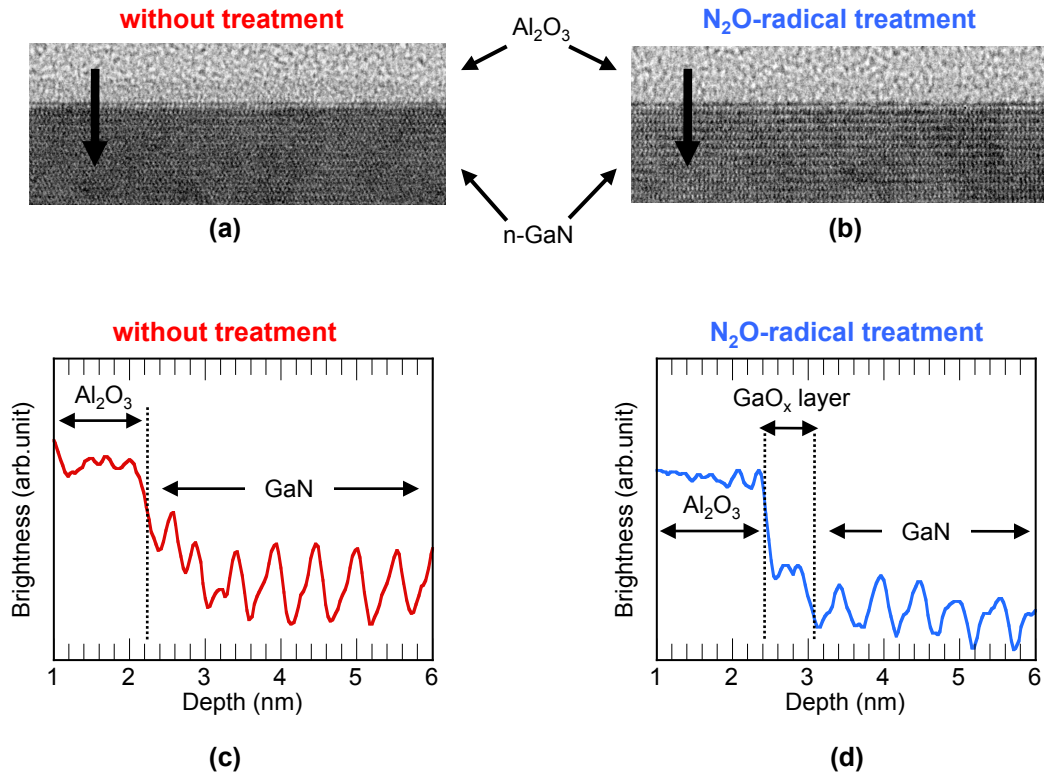


FIG. 5-13. TEM images of 2-nm-thick Al₂O₃/n-GaN interfaces (a) without and (b) with the N₂O-radical treatment. Average line profiles of image brightness obtained from the TEM images (a) without and (b) with the N₂O-radical treatment.

5.6. Summary

We have investigated the effects of fabrication processes on the electrical properties of $\text{Al}_2\text{O}_3/\text{GaN}$ structures prepared by ALD. When the ohmic annealing process at 800°C was carried out after the Al_2O_3 deposition on GaN, we observed a large number of microcrystallization regions in Al_2O_3 , causing the pronounced leakage in the I - V characteristics of the $\text{Al}_2\text{O}_3/\text{GaN}$ structure. To overcome this problem, the “ohmic-first” process with a SiN protection layer was employed. The ohmic-first process maintained the amorphous phase in the atomic configuration of Al_2O_3 , leading to the sufficient suppression of leakage current at the $\text{Al}_2\text{O}_3/\text{GaN}$ interface. In addition, low electronic state densities of less than $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ were observed at the interface, indicating that the ALD- Al_2O_3 -based gate structure prepared with a suitable surface control process is promising for a reliable and stable operation of GaN-based transistors. To control the interface states, the N_2O -radical treatment was then applied. The N_2O -radical treated $\text{Al}_2\text{O}_3/\text{AlGaN}$ structure showed lower state density than that of the sample without the surface treatment. The results presented in this chapter indicated that the combination of “ohmic-first” process with the SiN protection and the N_2O -radical treatment is effective in reducing the interface states. Those processes seem to be applicable to the AlGaN/GaN system, which is discussed in next chapter.

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Chapter 6.

Characterization and control of Al₂O₃ gate interfaces on AlGaN/GaN heterostructures for improved electrical properties of high-electron-mobility transistors

6.1. Introduction

GaN and related-material high-electron-mobility transistors (HEMTs) are promising for high-power and high-frequency device applications, owing to their good physical properties.¹ In particular, high-density and high-mobility two dimensional electron gas (2DEG) generated at the AlGaN/GaN interface enables us to realize power switching transistors having extremely low on-state resistance applicable to next generation power conversion systems.²⁻⁵ For realizing a good insulated gate, we should consider material properties of insulators: wide bandgap leading to large band offset against GaN-based-materials, high breakdown field, and high permittivity. In addition, low-density electronic states at the insulator/GaN-based-material interfaces are also necessary because interface states may cause various operational stability and reliability issues in GaN-based MOS-HEMTs such as threshold voltage instability and current collapse phenomenon. To address these issues, it is essential to investigate not only the densities of electronic states at the insulator/GaN-based-material interfaces but also the various process conditions to control them.

As already discussed previously in this thesis, Al₂O₃ is one of the leading candidates for gate insulators in GaN-based devices. GaN-based MOS-HEMTs using an Al₂O₃ as the insulator have been demonstrated by many groups.^{3,4,6-9} The typical values of bandgap and permittivity reported for the Al₂O₃ film are 7-9 eV and 8-10, respectively.⁶⁻¹⁰ The Al₂O₃ film

prepared by atomic layer deposition (ALD), in particular, showed relatively low electronic state densities in the $\text{Al}_2\text{O}_3/\text{n-GaN}$ system.^{9,11-13} However, in the MOS-HEMT structures, the insulator/semiconductor interface is usually formed on the AlGaIn/GaN heterostructures, resulting in the existence of two interfaces under the gate electrode. As shown in Fig. 6-1(a), because those two interfaces make potential control rather complicated during capacitance-voltage (C - V) measurements, it is difficult to characterize interface states in the MOS-HEMTs compared with MOS structures having a single semiconductor layer (e.g. the $\text{Al}_2\text{O}_3/\text{n-GaN}$ structure). Moreover, the wide bandgap of GaN-based materials also leads to extremely low emission rate of electrons captured at the interface states, making the evaluation of interface state densities difficult. Fig. 6-1(b) shows the example of the time constant of electron emissions from an insulator/AlGaIn interface. A typically used AlGaIn with an Al composition ratio of around 25 % has a bandgap of approximately 4.0 eV. Accordingly, the time constant for thermal electron emission from its midgap (~ 2.0 eV) is estimated to be several years at room temperature. It means that only a limited number of the interface states can be detected during the standard C - V measurements even at high temperatures. Although several groups have proposed new methods to characterize electronic states in the MOS-HEMT structures,¹⁴⁻¹⁷ there have been few reports on MOS interface state densities of the GaN-based MOS-HEMTs and their relationship to the resulting electrical properties has not been discussed in detail.

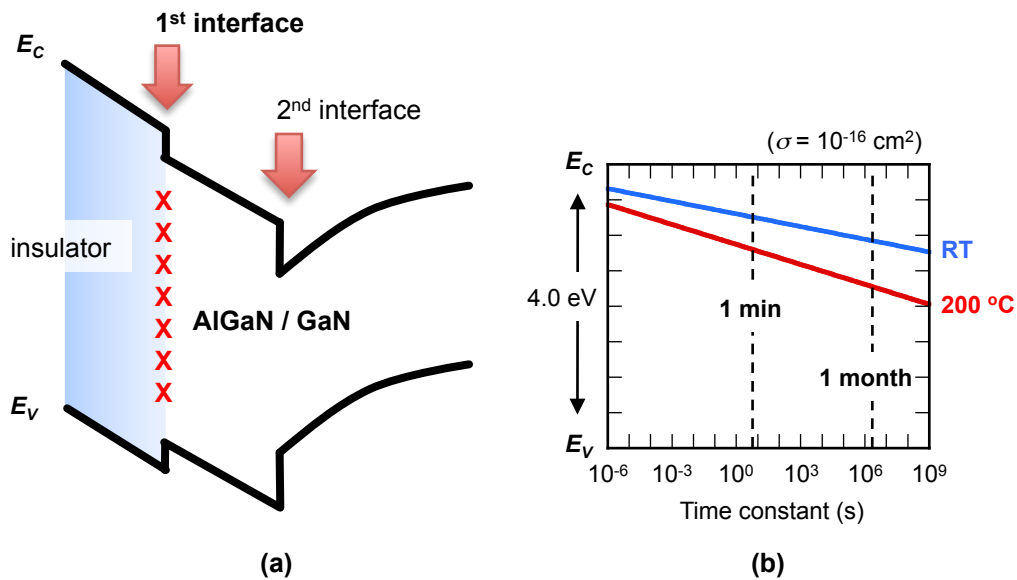


FIG. 6-1. Band diagram of insulated-gate on the AlGaIn/GaN heterostructure. (b) Time constants for electron emission from the insulator/AlGaIn interface.

In this chapter, we have attempted to determine interface state density distributions of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MOS-HEMTs using two types of C - V analysis, the photo-assisted measurement and the frequency dispersion characterization. We then discuss the relationship between the interface states and resulting electrical properties including threshold voltage instability of the MOS-HEMTs.

6.2. Fabrication process

Figure 6-5 schematically shows the structure of the fabricated $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MOS-HEMT. We used an $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}/\text{GaIn}$ heterostructure grown on a sapphire substrate by metal organic chemical vapor deposition. Sheet resistance and electron mobility of the heterostructure were estimated to be $440 \, \Omega/\text{sq}$ and $1770 \, \text{cm}^2/\text{Vs}$, respectively. We employed the ‘ohmic-first’ process to prevent damage to the Al_2O_3 film during ohmic annealing.¹¹ After the pretreatment of the sample surface in a 30%-HF solution for 5 min, we deposited a 10 nm SiN as a surface protection layer by electron cyclotron resonance chemical vapor deposition. Ti/Al/Ti/Au (= 20/50/20/100 nm) source and drain electrodes were then deposited on the AlGaIn surface, followed by ohmic annealing at $800 \, ^\circ\text{C}$ for 1 min in N_2 ambient. Device isolation was performed in a reactive ion beam etching chamber using CH_4 -based plasma. After removing the SiN layer with a buffered HF, we applied an N_2O -radical treatment to the AlGaIn surface.¹⁸ A 10-nm-thick Al_2O_3 gate insulator was then deposited at $350 \, ^\circ\text{C}$ by ALD (SUGA-SAL1500) using trimethylaluminum and water vapor as precursors. To improve the interface properties, we also performed post deposition annealing at $450 \, ^\circ\text{C}$ for 15 min in N_2 ambient. Finally, a Ni/Au (= 20/50 nm) gate electrode was deposited on the Al_2O_3 layer. Gate length L_G and width W of the MOS-HEMTs were 3 and $100 \, \mu\text{m}$, respectively. For C - V characterization, we also fabricated $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ diode structures having circular gate and ring-shaped ohmic electrodes on the same chip.

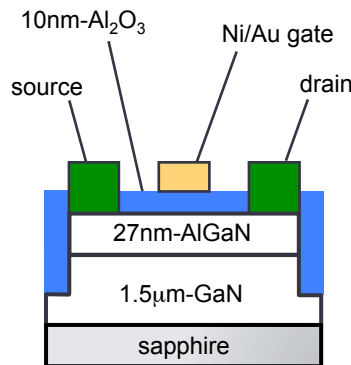


FIG. 6-5. Schematic cross-sectional view of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MOS-HEMT structure.

6.3. Measurements

6.3.1. Capacitance-voltage measurement

In this chapter, we used Yokogawa-Hewlett-Packard 4280A C meter/ C - V plotter for the standard and photo-assisted C - V measurements. Figure x schematically shows the measurement setup of 4280A. As a light source, we used ASAHI-SPECTRA MAX-302 that has Xe light and a set of eight band-pass filters ($h\nu = 1.26 - 2.43$ eV) to obtain monochromatic lights with. The computer connected with GPIB and RS-232C interfaces controls 4280A and MAX-302, respectively. The instrument is also connected to a probe station using the two-terminal connection. On the front panel of the instrument, the cable length is set to 1 m. After connecting the instrument to the probe station, the ‘zero’ calibration for the instrument and probes must be performed. Fig. 6-3 shows the flowchart of the C - V measurements programmed with National Instrument LabVIEW software. The step time is approximately 300 ms/step. For the photo-assisted measurements, in particular, the software automatically turns on the light source at the ‘Stop’ bias while keeping the voltage for ‘photo time’, and then restarts sweeping toward the ‘Start’ bias.

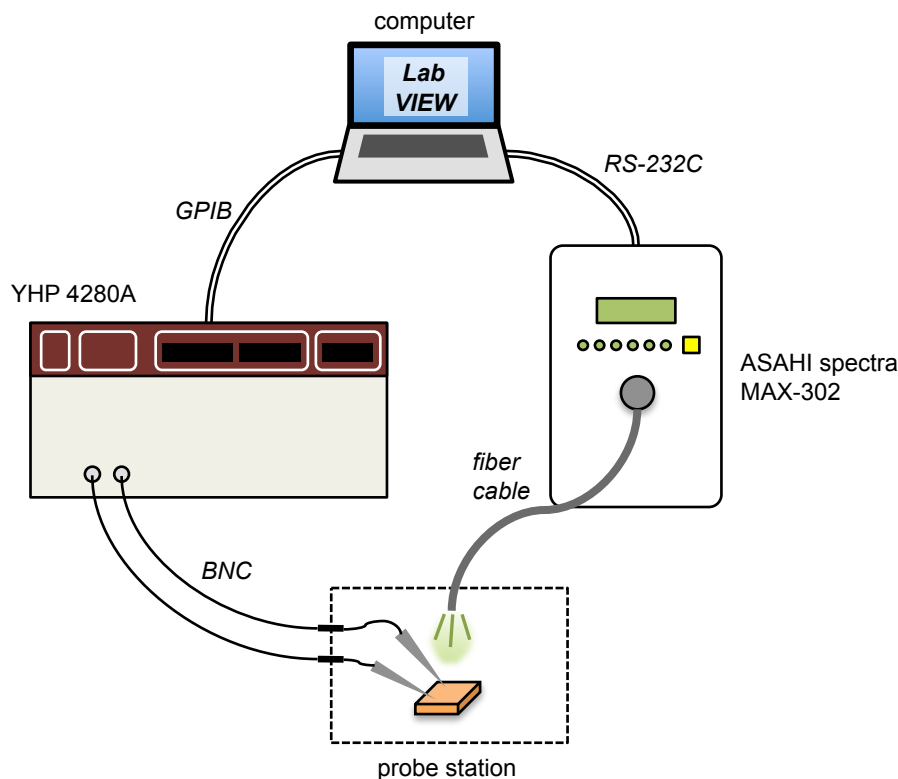


FIG. 6-2. Schematic illustration of measurement setup using 4280A and MAX-302.

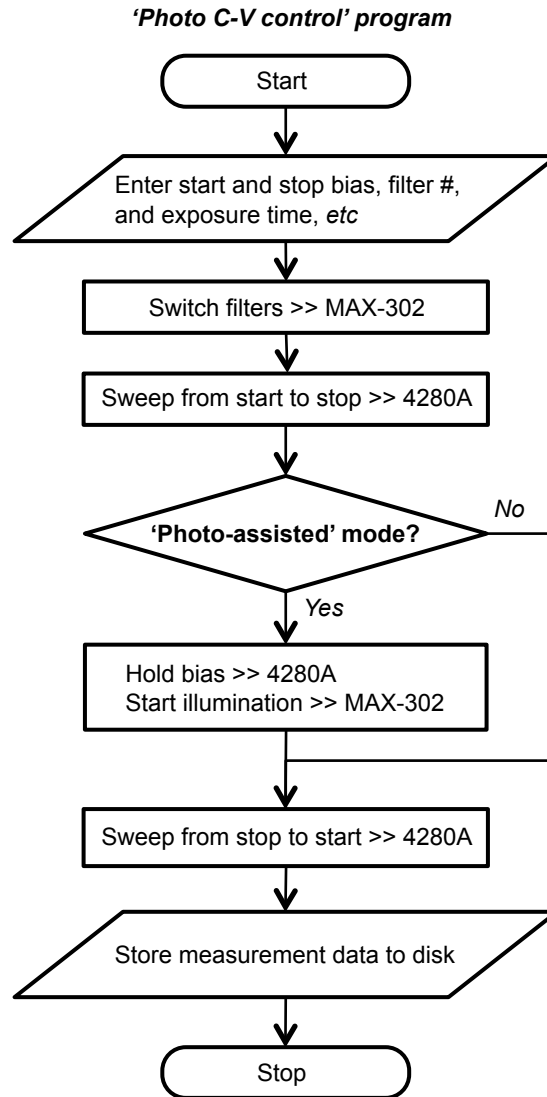


FIG. 6-3. Flowchart of the “photo- C - V control” program.

In 4280A, only one frequency source of 1 MHz is equipped. Therefore, Agilent 4294A Precision Impedance Analyzer is employed for the frequency dependent C - V measurement. Before connecting the instrument, a proper calibration using open-, short-, and load-adapters must be done. To obtain accurate measurement results, basic parameters shown in Table I are set to the instrument. The bandwidth of ‘5’ realizes the most precise measurement. In addition, ‘point averaging ”on” with “4” counts (= point averaging factor)’ makes C - V curves noise-free at low frequencies ($\Rightarrow$ 1 kHz) with appropriate measurement durations (approximately 300 ms/step). The instrument is also connected with a computer using GPIB interface.

TABLE I. Parameters set in 4294A.

Parameter name	Value
Oscillation level	0.02
Bandwidth	5
Point averaging	<i>on</i>
Point averaging	4

6.3.2. Pulsed current-voltage measurement

For pulsed I-V measurements, we used Agilent B1500A Semiconductor Device Analyzer with B1525A High Voltage Semiconductor Pulse Generator Unit (HV-SPGU). The instrument is totally operated with Agilent EasyEXPERT software installed in B1500A itself. In HV-SPGU, synchronized two channel pulse sources are equipped with DC bias source from +40 to -40 V. Fig. 6-4(a) shows the typical waveform of the single pulse and the parameters used in this study. The minimum pulse width is 5 μ s, and the transition time for turning-on and turning-off is set to 90 ns. The base and destination voltages can be set individually. Fig. 6-4(b) shows the example of the sequence in the pulsed I - V measurement. Each pulse between channel 1 and channel 2 is synchronized with a pulse period of 0.5 s. In Fig. 6-4(b), the destination voltage of channel 1 (drain-source voltage V_{DS}) is constant for each pulse, while that of channel 2 (gate-source voltage V_{GS}) is falling down. This sequence leads to the I_{DS} - V_{DS} measurement. For both channel, the base voltages also can be set individually as V_{DS} and V_{GS} with any stress bias condition.

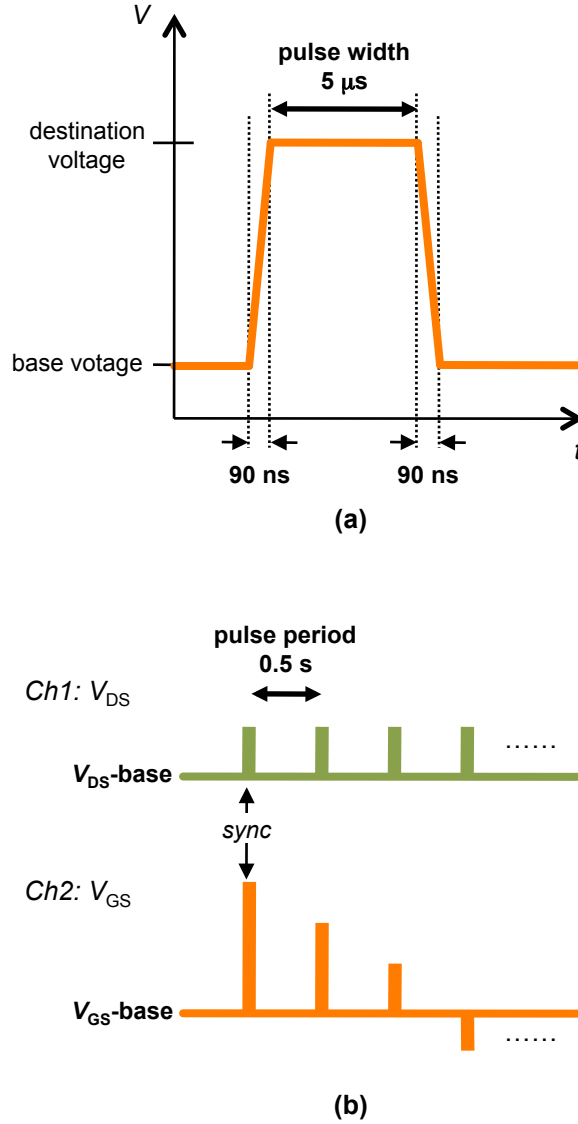


FIG. 6-4. (a) Typical waveform of single pulse generated with HV-SPGU B1525A. (b) Sequence example of pulsed I - V measurements. Schematic indicates the pulsed measurement for transfer characteristics.

6.4. C-V characteristics of MOS-diode structures

6.4.1. Typical C-V characteristics

Figure 6-6 shows the C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ diode structures without and with the N_2O -radical treatment prepared on the same chip as the MOS-HEMTs. We carried out C - V measurements using Agilent 4294A Precision Impedance Analyzer. The gate bias was swept from +4 to -8 V with a 0.05V-step. The sweep rate was approximately 300 ms/step. The measurement frequency was 1 MHz. For both samples without and with the N_2O -radical treatment, we obtained peculiar C - V curves having a two-step capacitance change, which is the characteristic feature of the MOS-HEMT structure having two

interfaces.¹⁴ The nearly flat capacitance $C_{2\text{DEG}}$ around zero bias indicates that the 2DEG accumulates at the AlGaIn/GaN interface. When we apply the positive gate bias, electrons start to distribute in the AlGaIn layer, leading to the increase of capacitance to the insulator capacitance $C_{\text{Al}_2\text{O}_3}$. Because the maximum gate bias was limited to +4 V by the gate leakage current, $C_{\text{Al}_2\text{O}_3}$ corresponding to the 10-nm-thick Al_2O_3 was not observed here. However, $C_{2\text{DEG}}$ around the zero bias is in accordance with the series capacitance of the 10-nm-thick Al_2O_3 and the 27-nm-thick AlGaIn. When the gate bias nears the threshold voltage (V_{th}) in the negative bias range, the depletion of the 2DEG leads to the steep decrease of capacitance, corresponding to the 2nd C - V step.

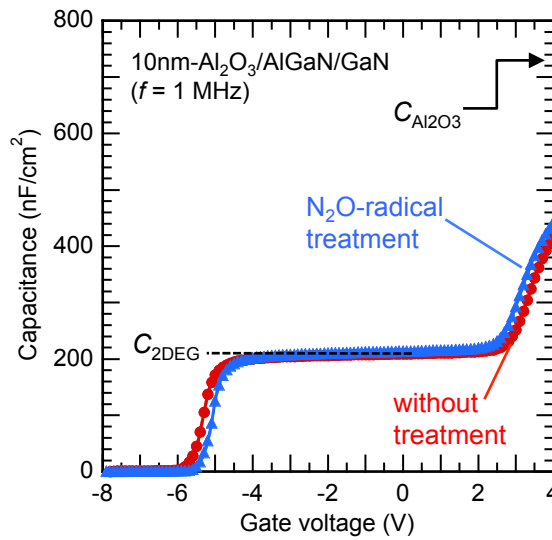


FIG. 6-6. C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS diode structures without and with the N_2O -radical treatment.

6.4.2. Effect of MOS interface states on C - V characteristics of heterostructures

To understand the basic behavior of interface states in the measured C - V curves of the MOS-HEMT structures, we calculated the C - V characteristics of the MOS-HEMTs using a numerical solver of the one-dimensional Poisson equation designed by Miczek *et al.*¹⁹ In the calculation, the high-frequency limit is assumed, in which all the interface states cannot respond to the ac signal but only follows the dc gate bias change. Fig. 6-7(a) shows the calculated C - V characteristics of 10nm-AlGaIn/GaN structures assuming physical parameters summarized in Table II. As indicated by the solid line, the ideal C - V curve shows a two-step capacitance change which is also observed in the experimental data. $C_{2\text{DEG}}$ is also in agreement with those in Fig. 6-6. The two broken lines show an example of the C - V

calculation assuming the two typical interface state density D_{it} distributions, D_{it1} and D_{it2} ($> D_{it1}$) shown in Fig. 6-7(b). In the D_{it} distributions, the charge neutrality level E_{CNL} is a branch point for acceptor- and donor-like interface states having a U-shaped distribution which is in accordance with the disorder-induced gap state model. As defined in Ref. 19, D_{it} distributions assumed in the calculation are expressed using Eq. (6.1)

$$D_{it}^{A,D}(E) = D_{it0} \exp \left[\left(\frac{|E - E_{CNL}|}{E_{0A,0D}} \right)^{n_{A,D}} \right], \quad (6.1)$$

where E_{0A} and n_a are the curvature of the acceptor-like D_{it}^A branch, E_{0D} and n_d are the curvature of donor-like D_{it}^D branch, respectively, and D_{it0} is the minimum density at E_{CNL} . Additionally, we also took into account time constants for electron emission from the interface states using the Shockley-Read-Hall (SRH) statistics. Time constant τ as a function of the trap energy level E_T can be calculated using the following equation,

$$\tau = \frac{1}{\sigma N_C v} \exp \left(\frac{E_C - E_T}{kT} \right), \quad (6.2)$$

where k , T , and σ are the Boltzmann constant, temperature, and the capture cross section of the interface states, and N_C and v are the effective density of states in the conduction band of the AlGaIn and the thermal velocity of electrons, respectively. Due to the exponentially increased time constants, only some of electrons can be emitted from the interface states during the measurement duration, which is determined by the emission efficiency. Using the actual C - V measurement time t_{meas} , the emission efficiency η_e is given by Eq. (6.3),

$$\eta = 1 - \exp \left(-\frac{t_{meas}}{\tau} \right). \quad (6.3)$$

Figure 6-8 shows the calculated η_e as a function of E_T . In the calculation, the resulting charge Q_{it} in the interface states at each gate bias can be estimated using η_e , D_{it} distributions, and the following equation,

$$Q_{it} = q \int_{E_V}^{E_C} D_{it}^D [1 - f_0(1 - \eta_e) - \eta_e f] dE - q \int_{E_V}^{E_C} D_{it}^A [f_0(1 - \eta_e) + \eta_e f] dE \quad (6.4)$$

where the f_0 and f are the Fermi-Dirac function at the start bias (+4 V, in this case) and at each bias, respectively.

In Fig. 6-7(b), E_{Tm} is the deepest energy of the state which can respond during t_{meas} . E_{Tm} can also be described by using SRH statistics as follows:

$$E_{Tm} = kT \ln(\sigma N_C v t_{meas}). \quad (6.5)$$

Assuming that σ is $1 \times 10^{-16} \text{ cm}^2$ and t_{meas} is 100 s, E_{Tm} was estimated to be 0.8 eV from the conduction-band edge in the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ system. It means, therefore, that only 25% or less

of the interface states can be detected while the others are in ‘frozen states’ which cannot de-trap electrons during the C - V sweeping at room temperature. As shown in Fig. 6-7(a), the interface states led to on-set voltage shifts toward the positive direction and stretch-out of C - V curves in the positive bias range. This is due to the change of the interface state charge within the ‘effective states’ when the Fermi level E_F is moving between the conduction-band edge E_C to E_{Tm} , as shown in Fig. 6-9(a). In the negative bias range, in contrast, only parallel voltage shifts were observed. As shown in Fig. 6-9(b), when E_F moves down toward the valence-band edge E_V at the $Al_2O_3/AlGaN$ interface, the ‘frozen states’ in the energy range of E_{Tm} to E_V cannot change their electron occupation rate because their corresponding time constants are longer than the sweeping time of 100 s. Because the interface charge density is not a function of the gate bias during the negative bias sweep, the interface states do not cause the stretch-out behavior. It follows, therefore, that the detection of the interface states using the standard C - V technique in the negative bias region is difficult.

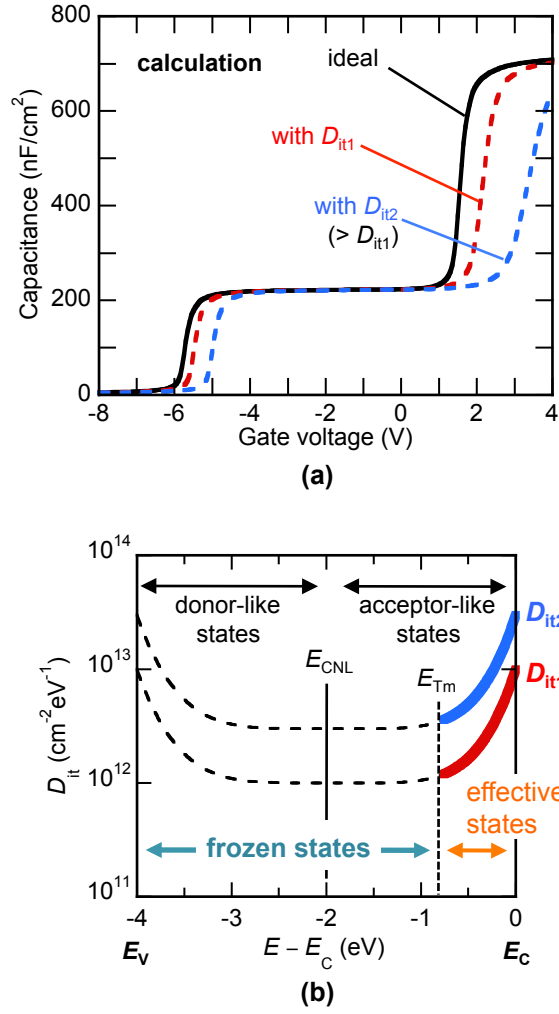
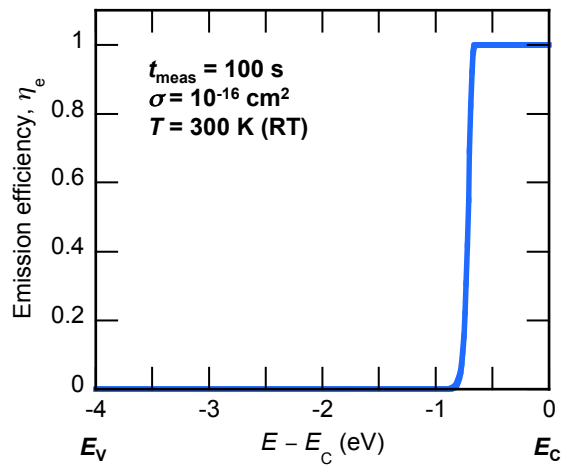


FIG. 6-7. (a) Calculated C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ structures. (b) $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface density distributions assumed in the calculation.

TABLE II. Parameters assumed in the C-V calculation.

Parameter name	Value
Bandgap (eV)	3.4 (GaN)
	4.0 (AlGaN)
	6.7 (Al ₂ O ₃)
Effective mass of electron	0.2 (GaN)
	0.23 (AlGaN)
Effective mass of hole	0.8 (GaN, AlGaN)
Permittivity	9.5 (GaN)
	9.25 (AlGaN)
	8.5 (Al ₂ O ₃)
Doping density (cm ⁻³)	10 ¹⁵ (GaN, AlGaN)
Band offset (eV)	0.384 (AlGaN/GaN)
	2.2 (Al ₂ O ₃ /AlGaN)
Surface barrier height (eV)	4.5 (Ni/Al ₂ O ₃)
2DEG density (cm ⁻²)	1.0 × 10 ¹³
E_{CNL} (eV)	$E_{\text{C}} - 1.9$
D_{it0} (cm ⁻² eV ⁻¹)	1 × 10 ¹² (D_{it1})
	3 × 10 ¹² (D_{it2})
$E_{0\text{A}}$	1.608090
n_{A}	5
$E_{0\text{D}}$	1.7773631
n_{D}	5
σ (cm ²)	10 ⁻¹⁶ (Al ₂ O ₃ /AlGaN)
t_{meas} (s)	100

**FIG. 6-8. Calculated emission efficiency η_e as a function of E_T .**

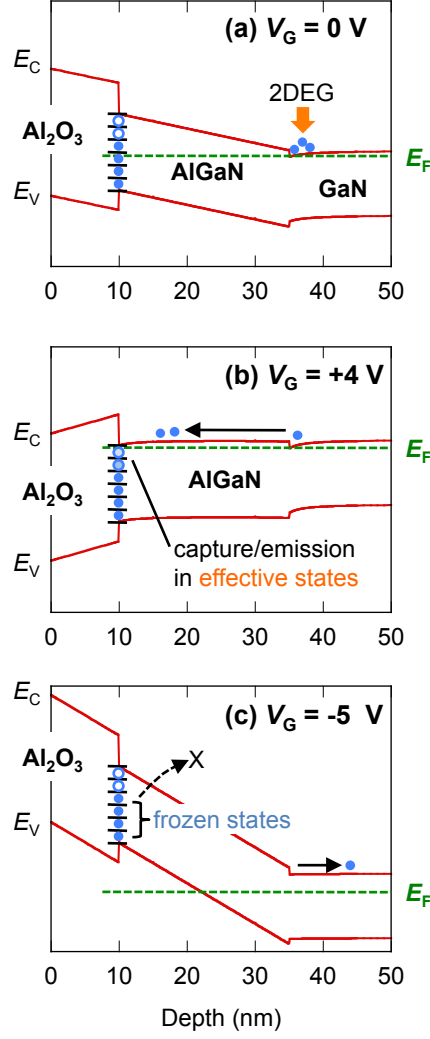


FIG. 6-9. Band diagrams of the $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ structure at (a) $V_G = 0$ V, (b) $V_G = +4$ V, and (c) $V_G = -5$ V.

For the sample subjected to the N_2O -radical treatment, as shown in Fig. 6-6, the smaller on-set voltage in the positive bias region probably indicates the reduction of the $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface states. However, the slopes of both C - V curves were not so different from each other. In the MOS-AlGaN/GaN systems, it is rather difficult to apply Terman method²⁰ to the interface state characterization, because we cannot determine one surface potential in the MOS-HEMT structures having two interfaces from one gate capacitance value. Fagerlind *et al.*²¹ utilized the frequency dispersion characteristics of the C - V curves in the positive bias range for estimating interface state densities. They evaluated the MIS interface state densities near the conduction-band edge for SiN/AlGaN/AlN/GaN structures. Mizue *et al.*¹⁴ developed the photo-assisted C - V measurement using monochromatic lights with photon energies less than the bandgap of the AlGaN. They analyzed photo-induced V_{th} shifts in the negative bias range, and reported the MOS interface state densities around the

midgap of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ structure for the first time. In this study, we have employed the combination of those techniques, the frequency dispersion method and the photo-assisted measurement, for the characterization of the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states of the MOS-HEMTs.

6.4.3. Photo-assisted C - V measurement

To characterize interface states near the midgap, the photo-assisted C - V measurements are performed using Yokogawa-Hewlett-Packard 4280A C meter/ C - V plotter and ASAHI Spectra MAX-302 monochromatic light source. Fig. 6-10(a) shows the schematic illustrations of the photo-assisted C - V characteristics before and after illuminations with two different photon energies ($h\nu_1$, $h\nu_2$). At first, the gate bias is swept from +4 to -8 V under dark condition. While holding the bias at -8 V, the sample surface is then exposed to the monochromatic light with the photon energies of less than the bandgap of AlGaIn for 2 min. This leads to the photo-assisted electron emissions from the interface states with the energy range corresponding to the photon energy as shown in Fig. 6-10(b). After switching off the light, the C - V sweeping is restarted toward +4 V. Then, V_{th} shift toward the negative bias direction can be obtained in the negative bias range. This mainly arises from the photo-assisted electron emissions from the interface states. When the higher photon energy ($h\nu_2$) is applied, the larger amount of photo-assisted electron emission causes the larger V_{th} shift in C - V curves. The V_{th} difference (ΔV_{th}) between two photon-energies corresponds to the interface charge difference (ΔQ_{it}) in the energy range of $E_{\text{C}} - h\nu_1$ to $E_{\text{C}} - h\nu_2$. It follows, therefore, that the interface state density D_{it} is proportional to the ΔV_{th} .

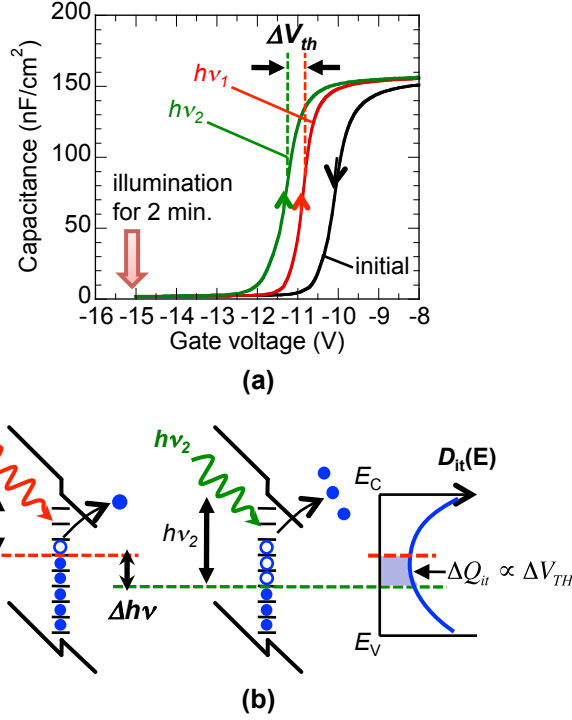


FIG. 6-10. Schematic illustration of (a) the photo-assisted C-V measurement and (b) photo-assisted electron emission from the interface states.

Figure 6-11 shows the photo-assisted $C-V$ characteristics of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ structures with and without the N_2O -radical treatment. For both samples, the parallel $C-V$ shifts toward the negative bias direction indicate that the interface states at $\text{Al}_2\text{O}_3/\text{AlGaIn}$ act as fixed charges in this bias range before and after the illumination. The illumination can also lead to the electron emission from the defect levels in the AlGaIn and GaN layers. However, the deep level densities reported for GaN are typically lower than $1 \times 10^{15} \text{ cm}^{-3}$, which corresponds to an area density of $1 \times 10^{11} \text{ cm}^{-2}$ with an assumption of 1mm-depletion layer width in the GaN layer at $V_G = -15 \text{ V}$. In case of AlGaIn, Ooyama *et al.* reported that the defect level densities of AlGaIn were estimated to be less than $5 \times 10^{16} \text{ cm}^{-3}$, which corresponds to an area density of $1.4 \times 10^{11} \text{ cm}^{-2}$ in the 27nm-AlGaIn layer. These densities are one order lower than the interface state densities ($\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$), so that the effect of those levels seems weak in this measurement.

For the sample with the N_2O -radical treatment as shown in Fig. 6-11(b), in particular, the smaller ΔV_{th} was observed between $h\nu = 1.4$ and 2.2 eV , indicating the lower density of interface states. The state density can be estimated from the observed ΔV_{th} using the following equation:

$$D_{it}(E = E_{AVG}) = \frac{C_{2DEG}}{q} \frac{\Delta V_{th}}{\Delta h\nu}, \quad (6.6)$$

where $\Delta h\nu$ is the difference between two photon energies ($= h\nu_2 - h\nu_1$) and E_{AVG} is the average energy position ($= h\nu_1 + \Delta h\nu/2$). Using six photon energies from 1.4 to 2.2 eV, we estimated the electronic state density distributions at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. When the photon energy is higher than half of the bandgap of AlGaIn ($h\nu = 2.0$ eV or higher), the electron excitation from the valence band to the interface states can occur, resulting in the hole generation. As a result, the accumulation of holes at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface also has an effect on the V_{th} shift, and there is a possibility of an overestimation of D_{it} in the energy range corresponding to the photon energy of 2.0 eV or higher.

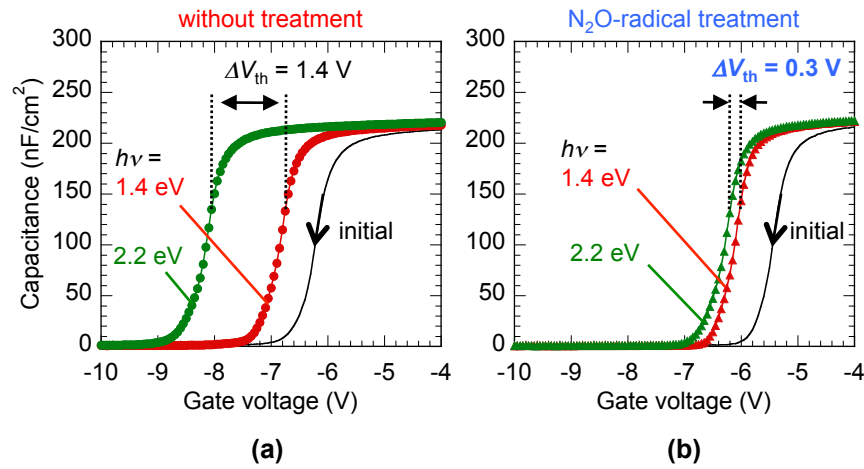


FIG. 6-11. Photo-assisted C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ structures (a) without and (b) with the N_2O -radical treatment.

6.4.4. Frequency dispersion in C - V characteristics

Figure 6-12 compares the frequency dispersion of the C - V characteristics of the MOS-HEMTs without and with the N_2O -radical treatment. The measurement frequencies were 1 kHz, 10 kHz, 100 kHz, and 1 MHz. In the positive bias range, we clearly observed frequency dispersion for the both samples probably caused by electron capture and emission at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states. For the N_2O -radical treated sample, in particular, the smaller dispersion between those frequencies indicates the reduction of interface states near the conduction-band edge.

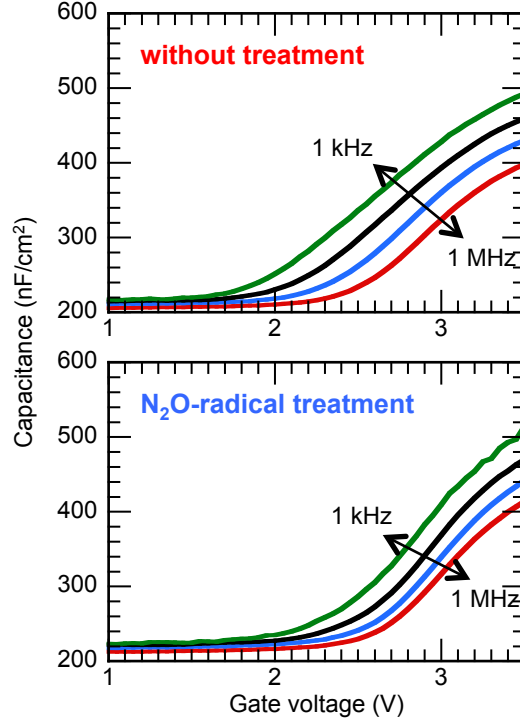


FIG. 6-12. Frequency dispersion of the C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS diode structures without and with the N_2O -radical treatment in the positive bias range.

The relationship between the time constant τ_1 and the frequency f_1 is given by Eq. (6.7)

$$\tau_1 = \frac{1}{2\pi f_1}, \quad (6.7)$$

and the trap energy depth E_1 corresponding to f_1 is expressed by the SRH statistics as follows:

$$E_1 = kT \ln \left(\frac{\sigma N_c v}{2\pi f_1} \right). \quad (6.8)$$

As schematically shown in Fig. 6-13, the interface states distributed within the bandgap can be divided into two parts by E_1 . In the upper energy range which has faster time constants than the measurement frequency ($\tau < 1/2\pi f_1$), electron capture and emission at the interface states can respond to the ac gate signal. In this case, the interface trap capacitance C_{it} and resistance R_{it} associated with electron capture and emission at the interface states are connected parallel to the depletion capacitance (the AlGaIn capacitance C_{AlGaIn} , in this case).²² Consequently, that leads to the overestimation of the measurement capacitance when the Fermi level is located in the energy range of E_C to E_1 . In the lower energy range which has longer time constants ($\tau > 1/2\pi f_1$), on the other hand, the C_{it} and R_{it} can be ignored because the interface states do not respond to the ac signal. Using a lower frequency f_2 , the trap energy depth E_2 at which C_{it} starts to be detected becomes deeper. This leads to the

overestimation of the capacitance at the smaller gate bias, causing a leftward on-set voltage shift for the lower frequencies in the positive bias region. Note that such overestimation of the capacitance is not observed in the C - V calculation shown in Fig. 6-7(a) because the present calculation does not take into account the frequency response of the interface states. To estimate D_{it} from the experimental data, we then focused on the on-set voltage shifts in the frequency dependent C - V curves.

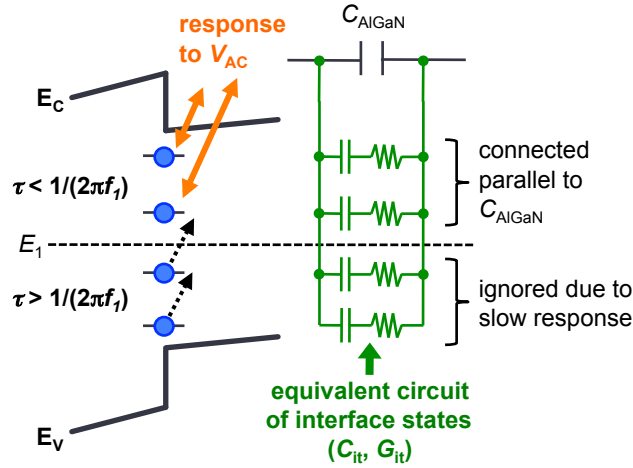


FIG. 6-13. Equivalent circuit of the interface states in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ structures during the C - V measurement.

Fig. 6-14(a) compares the C - V characteristics of the sample without the treatment measured at 100 kHz and 1 MHz in the positive bias range. The on-set voltage difference ΔV between two frequencies (f_1, f_2) corresponds to the interface charge density ΔQ_{it} in the energy range of E_1 to E_2 as schematically shown in Fig. 6-14(b). E_1 and E_2 were estimated to be 0.17 and 0.23 eV, respectively using Eq. (8), where f_1, f_2 and σ are 1 MHz, 100 kHz and $1 \times 10^{-16} \text{ cm}^2$, respectively. In this energy range, D_{it} can be estimated from the following equation:

$$\begin{aligned} D_{it}(E = E_{AVG}) &= \frac{C_{Al2O3}}{q} \frac{|V_2 - V_1|}{E_2 - E_1} \\ &= \frac{C_{Al2O3}}{q} \frac{\Delta V}{\Delta E}, \end{aligned} \quad (6.9)$$

where V_1 , and V_2 are the on-set voltages for f_1 and f_2 , respectively.²¹ E_{AVG} is the average energy between E_1 and E_2 , as described by Eq. (6.10)

$$\begin{aligned} E_{AVG} &= E_1 + \frac{E_2 - E_1}{2} \\ &= E_1 + \Delta E/2 \end{aligned} \quad (6.10)$$

Although we have to assume a value of σ in E_1 (as suggested in Eq. (6.8)) to determine the energy position of D_{it} , the energy difference ΔE , which is also used in Eq. (6.9), is independent of σ but dependent on T, f_1 and f_2 , as described by Eq. (6.11)

$$\begin{aligned}\Delta E &= E_2 - E_1 \\ &= kT \ln\left(\frac{\sigma N_c v}{2\pi f_2}\right) - kT \ln\left(\frac{\sigma N_c v}{2\pi f_1}\right) \\ &= kT \ln(f_1/f_2)\end{aligned}\quad (6.11)$$

Therefore, D_{it} can be evaluated using Eq. (6.9) without assuming a value of σ . Supposing that σ is constant for both samples without and with the N_2O -radical treatment, we can compare the D_{it} distributions of both samples in the same energy range.

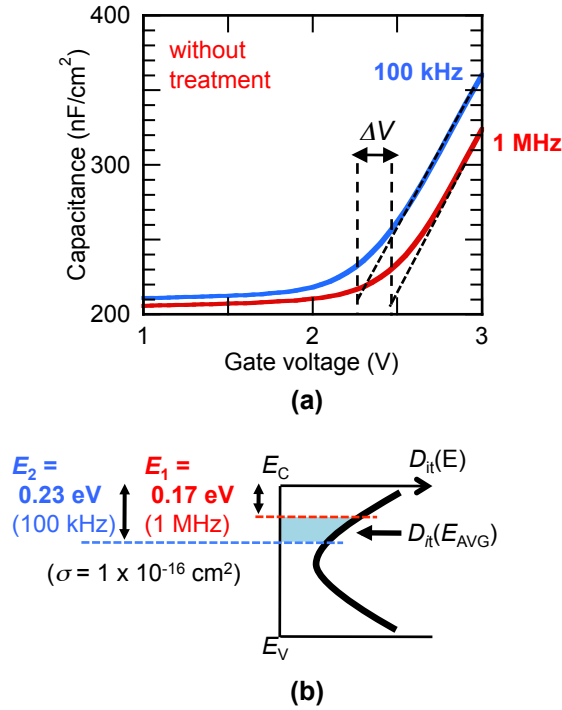


FIG. 6-14. (a) C - V curves of the sample without the surface treatment measured at frequencies of 100 kHz and 1 MHz. (b) Schematic illustration of D_{it} energy ranges corresponding to measurement frequencies.

6.5. Estimate of D_{it} in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs

Figure 6-15 shows the results of the D_{it} distributions at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface in the MOS-HEMT structures estimated using the combination of the frequency dispersion C - V method and the photo-assisted C - V measurement. In the frequency dispersion method, we assumed σ to be $1 \times 10^{-16} \text{ cm}^2$, giving values of D_{it} in the energy range of -0.2 to -0.32 eV from E_C . For the sample without the treatment, D_{it} near the conduction-band edge was

estimated to be $2 - 3 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, which is about one order higher than those reported for the $\text{Al}_2\text{O}_3/\text{n-GaN}$ system.¹¹ As Ooyama *et al.* reported in Ref. 23, the defect level densities of AlGaIn were about 10 times as high as those of GaN, probably due to high densities of defects related to nitrogen vacancy, oxygen impurity and their complexes.²⁴ It is likely that they also led to the higher densities of interface states in $\text{Al}_2\text{O}_3/\text{AlGaIn}$ compared with those in the $\text{Al}_2\text{O}_3/\text{n-GaN}$ system. We also carried out the photo-assisted $C-V$ measurement using monochromatic lights with photon energies of 1.4 - 2.2 eV.¹⁸ For the sample without the surface treatment, the minimum state densities around the midgap were estimated to be around $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which is in good agreement with the data reported for the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ structure.¹⁴

As already reported in Ref. 18, in comparison, the N_2O -radical treated sample showed a lower D_{it} distribution around the midgap with a minimum density of less than $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Moreover, the state densities near the conduction-band edge were estimated to be $8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the N_2O -radical treated $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. Supposing that the D_{it} distributions of both samples are U-shaped as indicated by the broken lines in Fig 6-15, the entire acceptor-like state density distribution of the N_2O -radical treated MOS-HEMT is expected to be reduced by approximately 40% compared with that of the sample without the treatment. Assuming those entire D_{it} distributions to the numerical solver, the calculated $C-V$ curves reasonably reproduced the experimental data for the both samples at 1 MHz. For further consideration of the D_{it} estimation, not only the methods presented here but also other approaches to $C-V$ analyses are necessary. However, the N_2O -radical treatment appears also to be effective in improving the electrical properties of the AlGaIn/GaN MOS-HEMTs.

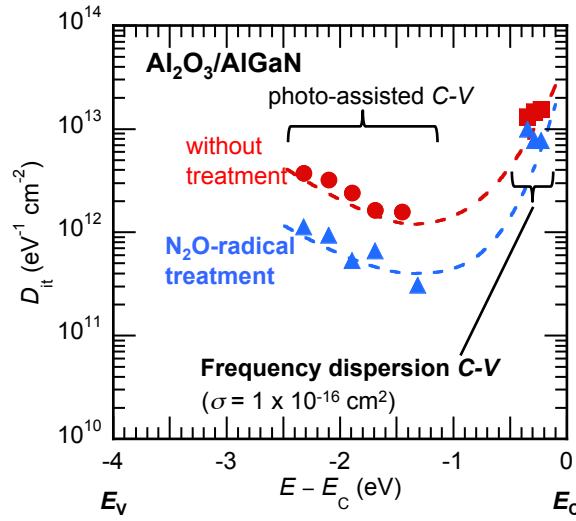


FIG. 6-15. Al₂O₃/AlGa_N interface state density distributions in the Al₂O₃/AlGa_N/Ga_N structures without and with the N₂O-radical treatment.

6.6. Chemical properties of N₂O-radical treated AlGa_N surface

To investigate the chemical bonding properties of the N₂O radical treated AlGa_N surface, we carried out X-ray photoelectron spectroscopy (XPS) analysis using a monochromatic Al K α radiation source ($h\nu = 1486.6$ eV). Figure 8 compares the O 1s and N 1s core-level spectra of the AlGa_N surfaces before and after the N₂O-radical treatment taken with a photoelectron escape angle of 15°. Note that each spectrum was normalized to the Ga 3d peak. As indicated by the broken line in Fig. 6-16(a), the increase of the AlGaO_x peak was observed for the N₂O-radical treated AlGa_N surface, probably arising from the oxidation of the AlGa_N due to the treatment.^{25,26} We also confirmed chemical shifts in the Ga 3d and Al 2p core-level spectra,²⁷ which is also confirmed in the N₂O-radical treated Al₂O₃/n-GaN system as mentioned in the previous chapter. In the N 1s spectra shown in Fig. 6-16(b), however, the AlGa_N peak at 397.0 eV is decreased for the N₂O-radical treated sample but still remains and overlaps with the broadened Ga LMM Auger spectra.²⁸ The broader linewidth and the chemical shift of Ga Auger signal were also observed in the GaO_x layer prepared by photoelectrochemical oxidation of GaN.²⁹ That is, the XPS spectra obtained from the N₂O-radical treated surface contain those of the AlGa_N and AlGa-oxide layers, suggesting the oxidation layer was very thin (1 nm or less). Bae *et al.*³⁰ reported that an ultra thin Ga-oxide layer prepared by the remote plasma-assisted oxidation process is effective in reducing interface states for the SiO₂/n-GaN system. Tajima *et al.*³¹ compared the oxidation processes for access regions in AlGa_N/Ga_N HEMTs using O₂- and N₂O-plasma treatments.

In their report, N_2O plasma promoted the oxidation of the AlGaIn surface with an N-O bonding network, which probably suppressed the defect formation in the AlGaIn layer during the oxidation process. As shown in Fig. 6-16(b), we also confirmed the small presence of the N-O bonding peak at around 402.5 eV for the N_2O -radical treated AlGaIn surface.^{27,31,32} Although the mechanism is not clear yet, it is likely that the monolayer-level formation of the AlGa-oxide layer prepared by the N_2O -radical treatment is effective in reducing electronic states at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface.

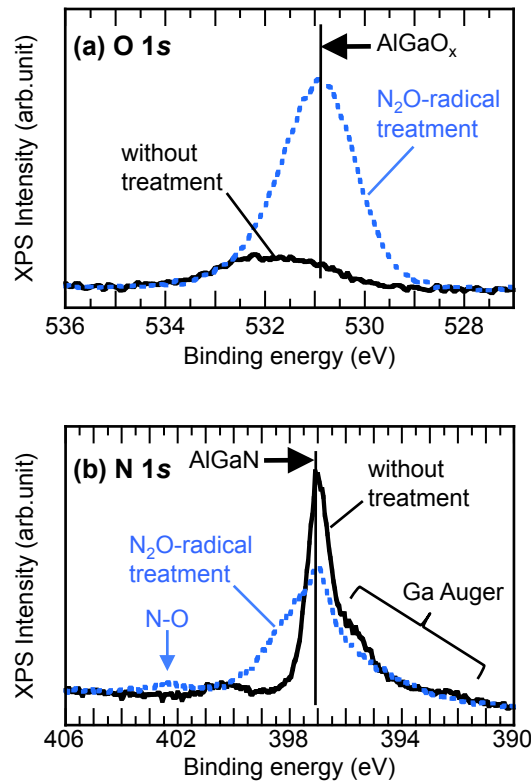


FIG. 6-16. (a) O 1s and (b) N 1s core-level spectra obtained from the AlGaIn surfaces before and after the N_2O -radical treatment.

6.7. Electrical properties of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MOS-HEMTs

Figure 6-17 shows the drain current-voltage ($I_{\text{DS}}-V_{\text{DS}}$) characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MOS-HEMTs without and with the N_2O -radical treatment. We used Agilent B1500A Semiconductor Device Analyzer with B1525A High Voltage Semiconductor Pulse Generator Unit for pulsed current-voltage measurements. Pulse width and period were 5 μs and 0.5 s, respectively. The drain-source and gate-source base-voltages were set to 0 V, ‘no-stress’ condition. At the gate-source voltage $V_{\text{GS}} = 0$ V, both samples show almost the

same current density, indicating no pronounced degradation of the 2DEG channel due to the N₂O-radical treatment. At $V_{GS} = +4$ V, in contrast, the N₂O-radical treated MOS-HEMT shows higher current density than the MOS-HEMT without the treatment. This tendency was also confirmed in the transfer characteristics in the saturation region, as indicated by the solid lines in Fig. 6-18. For the MOS-HEMT without the treatment, a marked decrease of transconductance was observed at high gate bias range. When the gate bias is positive, electron transfer from the AlGa_{0.3}N/GaN interface to the Al₂O₃/AlGa_{0.3}N interface occurs, which can be confirmed in the $C-V$ results in Fig. 6-6, resulting in the parasitic channel formation at the Al₂O₃/AlGa_{0.3}N interface. In this case, the relatively high-density interface states caused the degradation of electron mobility, leading to the decrease of transconductance. In comparison, the improvement of transfer characteristics of the N₂O-radical treated MOS-HEMT in the positive gate bias region is due to the reduction of interface states, also as confirmed in Fig. 6-15.

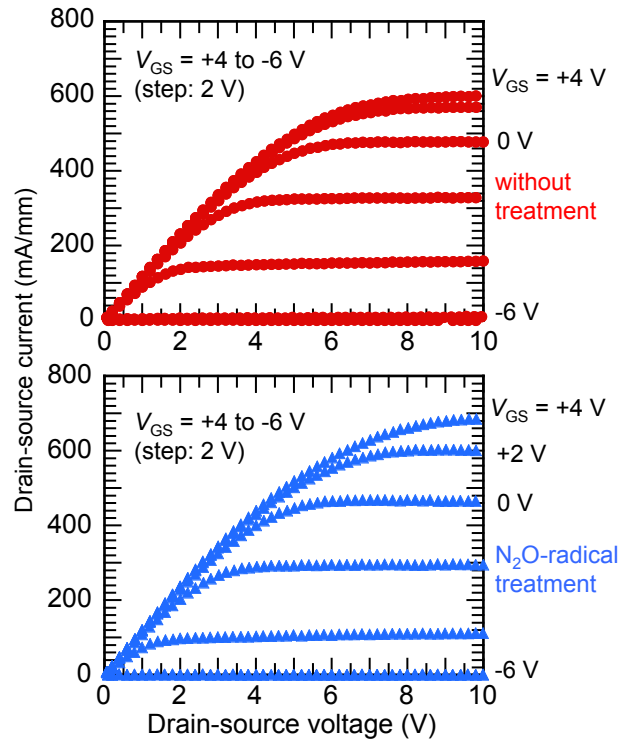


FIG. 6-17. I_{DS} - V_{DS} characteristics of the Al₂O₃/AlGa_{0.3}N/GaN MOS-HEMTs without and with the N₂O-radical treatment pulsed from ‘no-stress’ bias condition.

To investigate the operational stability of the MOS-HEMTs, we also performed negative-gate-bias-induced V_{th} instability measurements. In Fig. 6-18, the broken lines (‘gate-stress’) show transfer characteristics pulsed from negative-gate-bias stress condition,

$V_{GS} = -8$ V and $V_{DS} = 0$ V. For the sample without the treatment, we observed a threshold voltage shift ΔV_{th} of 0.7 V toward the negative bias direction, which is probably due to the negative-gate-bias-induced electron emission from the $Al_2O_3/AlGaN$ interface. Figure 6-19 shows the potential profile of the $Al_2O_3/AlGaN/GaN$ structure calculated by using the numerical Poisson solver. At $V_{GS} = -8$ V, E_F is located far below the valence-band edge at the $Al_2O_3/AlGaN$ interface. In this case, electron at the shallow states which have shorter time constants can be emitted, resulting in the V_{th} shift toward the negative bias direction. Using Eq. (1) and the pulse period of 0.5 s, E_{Tm} for the pulsed measurement can be estimated to be 0.6 eV. When we integrated the expected D_{it} distribution determined in Fig. 6-15 from E_C to E_{Tm} , the resulting charge density is in good agreement with the charge difference ΔQ_{it} ($= C_{Al_2O_3} \Delta V_{th}/q$), $3.2 \times 10^{12} \text{ cm}^{-2}$, corresponding to 0.7 V-shift. In contrast, the suppressed V_{th} shift for the N_2O -radical treated MOS-HEMT is clearly due to the reduction of the interface states. For this sample, ΔQ_{it} was estimated to be $1.4 \times 10^{12} \text{ cm}^{-2}$ with ΔV_{th} of 0.3 V, which is approximately 40%-less compared with that of the MOS-HEMT without the treatment.

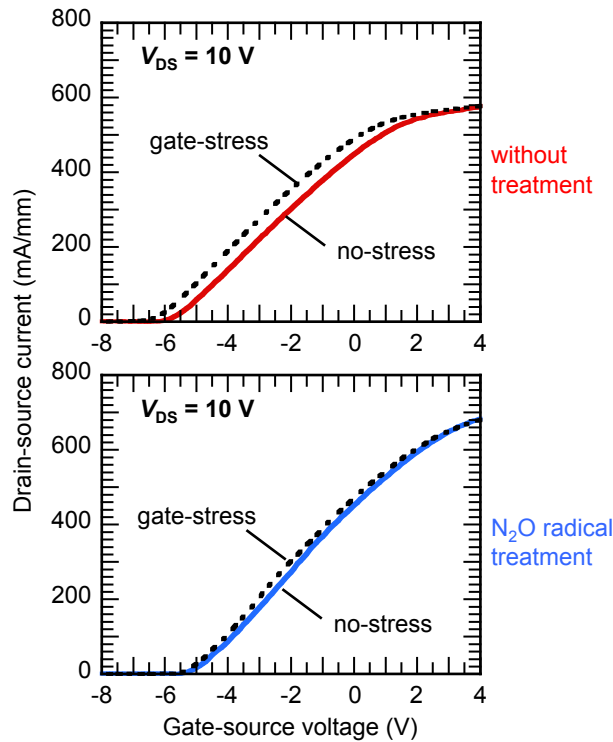


FIG. 6-18. Transfer characteristics of the $Al_2O_3/AlGaN/GaN$ MOS-HEMTs without and with the N_2O -radical treatment pulsed from ‘no-stress’ (solid lines) and ‘gate-stress’ (broken lines) bias condition.

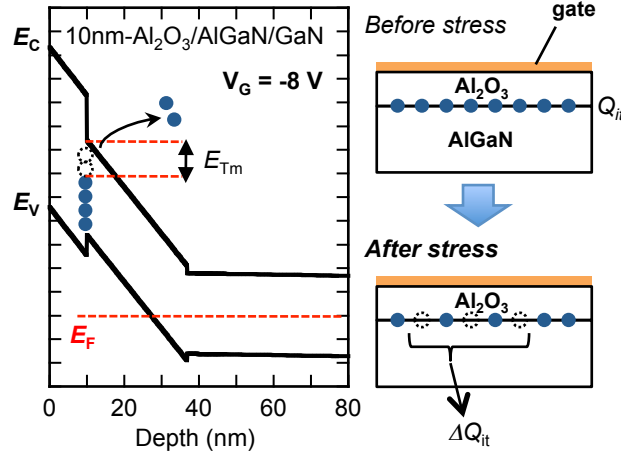


FIG. 6-19. Calculated potential profile of the Al₂O₃/AlGa_N/Ga_N at $V_{GS} = -8$ V and schematic illustration of the possible mechanism for the negative-gate-bias-induced V_{th} shifts.

Figure 6-20 shows the results on the negative-gate-bias-induced V_{th} shifts of the MOS-HEMTs measured at room temperature (RT), 100 °C, and 150 °C. For both samples, the amount of V_{th} shifts increased with increasing temperature. Because E_{Tm} is proportional to the temperature as described in Eq. (1), the larger amount of electron emission caused larger V_{th} shifts toward the negative bias direction. For the N₂O-radical treated MOS-HEMT, however, we observed the smaller V_{th} shift of less than 0.5 V even at 150 °C. The N₂O-radical treated MOS-HEMT shows more stable V_{th} under negative-gate bias stress at high temperatures due to the reduction of interface states. The results presented in this paper are the first report on the relationship between electrical properties of GaN-based MOS-HEMTs and experimental D_{it} distributions evaluated for the same structures. The N₂O-radical treatment is one of the effective processes for reducing the Al₂O₃/AlGa_N interface states and improving the electrical properties of the GaN-based MOS-HEMTs.

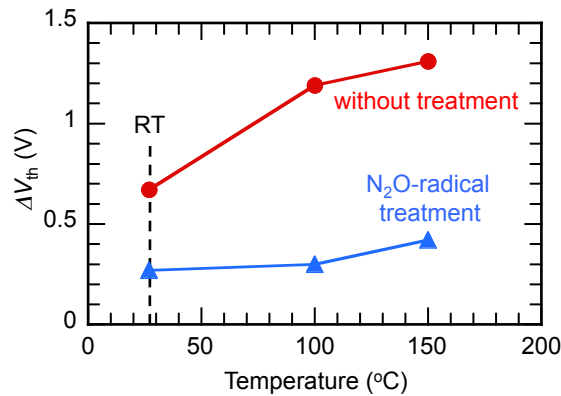


FIG. 6-20. Negative-gate-bias-induced V_{th} shifts of the MOS-HEMTs without and with the N₂O-radical treatment measured at RT, 100 °C, and 150 °C.

6.8. Summary

We have estimated the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface state density distributions in the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs using the combination of the frequency dependent and photo-assisted C - V methods. The N_2O -radical treated MOS-HEMT showed smaller photo-induced C - V shifts and smaller frequency dispersion of the C - V curves than those of the sample without the treatment, indicating the reduction of the interface states. The state densities were estimated to be $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ or less around the midgap and $8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ near the conduction-band edge, which is approximately 40% less than those in the MOS-HEMT without treatment. We then investigated the impact of the reduced interface state densities on the electrical properties of the MOS-HEMTs. In the transfer curves, the decrease of transconductance was observed at high gate bias range where the parasitic channel is formed at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface. In this case, the N_2O -radical treated MOS-HEMT having the reduced interface states showed higher current density than that of the sample without treatment. We also have performed the negative-gate-bias-induced V_{th} instability measurements at RT to 150 °C. For the N_2O -radical treated MOS-HEMT, the reduced interface states led to more stable V_{th} even at high temperatures. The results indicated that the N_2O -radical treatment is effective both in reducing the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states and improving the electrical properties of the MOS-HEMTs. Control of the MOS interface states is one of the key technologies for improving operational performance and stability of the GaN-based devices.

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Chapter 7.

Conclusion

This thesis aimed at the characterization and control of electronic states in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ metal-oxide-semiconductor structures for the application to the insulated-gate $\text{AlGaIn}/\text{GaIn}$ HEMTs considering various fabrication process conditions.

Chapter 1 started with the introduction of power electronic systems which are widely used in various electronics devices. GaN and related materials are attractive for the application to the semiconductor devices in the power electronics circuits owing to their superior physical properties. However, it is rather difficult to characterize and control electronic states, in particular, at the insulator/semiconductor interfaces in the insulated-gate GaN transistors because of their wide bandgap and complicated structure having two (or more) interfaces.

Chapter 2 explained the physical properties of III-N semiconductors and their heterostructures, followed by the introduction of proposed device structures, processes, and issues of the present GaN-based HEMTs. To achieve normally-off operation, most of the proposed structures require insulated-gates to suppress the gate leakage current under a forward gate bias. However, there are some problems regarding the degradation of electrical properties in the present insulated-gate HEMTs, mainly caused by the electronic states in the devices including insulator/semiconductor interfaces.

Chapter 3 discussed basic theories on the metal-oxide-semiconductor (MOS) structures which consist of electronic states and difficulties for characterizing the wide-bandgap interfaces. At the wide-bandgap interfaces, there are only 30 % or less interface states which can emit the electron during the standard C-V measurements. Thus, it is necessary to develop methods to characterize and control the electronic states in the wide

bandgap materials.

Chapter 4 introduced the experimental results obtained for this thesis. The Al_2O_3 films prepared by atomic layer deposition showed superior thickness uniformity, controllability, and optical properties, as confirmed by the ellipsometry. Using XPS analyses, the bandgap of the deposited Al_2O_3 was estimated to be 6.7 eV, which can lead to the conduction-band offset large enough against GaN and AlGaIn for the application to GaN-based HEMTs.

Chapter 5 investigated the effects of fabrication processes on the electrical properties of $\text{Al}_2\text{O}_3/\text{n-GaN}$ MOS structures prepared by ALD, including the interface state densities. The ohmic-first process with a SiN surface protection could suppress the increase of gate leakage current effectively. Furthermore, the SiN surface protection led to low electronic state densities less than $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at the $\text{Al}_2\text{O}_3/\text{n-GaN}$ interface. The N_2O -radical treatment was then applied as the additional surface treatment. The N_2O -radical treated $\text{Al}_2\text{O}_3/\text{AlGaIn}$ structure showed one order of lower magnitude state density ($1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) than that of the sample without the surface treatment.

Chapter 6 finally investigated the relationship between the interface state densities and the electrical properties of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs. The N_2O -radical treatment was also applied to the MOS-HEMT for reducing the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface states. To estimate the interface states on the AlGaIn/GaN heterostructures, two types of C - V analyses were applied: the photo-assisted and frequency dependent C - V measurements. The reduced interface state densities in the MOS-HEMTs were estimated to be 40 % compared to those without the N_2O -radical treatment. The impact of the reduced interface states on the electrical properties of the MOS-HEMTs was then investigated. The higher maximum drain-source current density and the stable threshold voltage variation were obtained for the N_2O -radical treated MOS-HEMTs. For further consideration of relationship between the D_{it} estimation, not only the methods presented here but also other approaches to C - V analyses are absolutely necessary. The results presented in this thesis indicate that control of the MOS interface states is one of the key technologies for improving operational performance and stability of the GaN-based devices.

List of publications/conferences/awards

Publications

Journals

- (1) Yujin Hori, Zenji Yatabe, and Tamotsu Hashizume, “Characterization of interface states in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ structures for improved performance of high-electron-mobility transistors”, [Journal of Applied Physics](#), Vol. 114, pp.244503-1-8 (2013).
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- (1) Yujin Hori, Taketomo Sato, and Tamotsu Hashizume, “Control of insulated gate interfaces on $\text{AlGaIn}/\text{GaIn}$ heterostructures for power devices”, Proc. of The 1st IEEE Workshop in Wide Bandgap Power Devices and Applications (WiPDA), pp. S10-003-1-4 (2013).
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Awards

- (1) 10th International Conference on Nitride Semiconductors Outstanding Poster Presentation Award
“Characterization and Control of MOS Interface States in GaN-based MOS-HEMTs Using Al₂O₃ Gate Insulator”
(2013 年 8 月 26 日)
- (2) 電子情報通信学会電子デバイス研究会発表奨励賞
“GaN および AlGaN/GaN 構造への絶縁ゲート形成と評価”
(2010 年 11 月 12 日)