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Recent progress in integration of III–V nanowire transistors on Si substrate by selective-area growth

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Abstract

We report on the recent progress in electronic applications using III–V nanowires (NWs) on Si substrates using the selective-area growth method. This method could align vertical III–V NWs on Si under specific growth conditions. Detailed studies of the III–V NW/Si heterointerface showed the possibility of achieving coherent growth regardless of misfit dislocations in the III–V/Si heterojunction. The vertical III–V NWs grown using selective-area growth were utilized for high performance vertical field-effect transistors (FETs). Furthermore, III–V NW/Si heterointerfaces with fewer misfit dislocations provided us with a unique band discontinuity with a new functionality that can be used for the application of tunnel diodes and tunnel FETs. These demonstrations could open the door to a new approach for creating low power switches using III–V NWs as building-blocks of future nanometre-scaled electronic circuits on Si platforms.

Keywords: III–V nanowires, epitaxy, FET, tunnel FET

(Some figures may appear in colour only in the online journal)

1. Introduction

III–V compound semiconductor nanowires (NWs) have attracted a lot of attention as building blocks for future electronic and optical devices [1–6]. InAs and InGaAs NWs are especially promising channel materials for next-generation field-effect transistors (FETs), because these III–V NWs have a lower electron effective mass and higher electron mobility, and their NW geometries are feasible for use in surrounding-gate architecture, in which all the surfaces around the NW are wrapped by gate metal. These III–V NWs can enhance the ON-state current under a lower supply voltage, and the surrounding-gate structure suppresses the OFF-state

leakage current as compared to that of Si metal–oxide–semiconductor FETs (MOSFETs) and Si fin FETs. The recent studies on III–Vs as alternative channels for future FETs have been exceedingly common in the field of Si complementary MOS (CMOS) technologies [7–9]. However, the vertical III–V NWs on Si substrates as alternative channel materials have not been aggressively investigated using the bottom-up growth approach [10–15], because the channel-formation technique had some difficulties in suppressing formation of crystal defects due to mismatches such as lattice constants and polarity. Mismatches in the lattice constant and thermal expansion coefficients form defects such as misfit and threading dislocations. The mismatches in polarity between polar III–V NWs and non-polar Si randomize the growth direction along an equivalent orientation and forms anti-phase defects.



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Recent progress in the heteroepitaxy of III–V NWs on Si such as metal-catalysed [16], self-catalysed vapour–liquid–solid (VLS) [17], and selective-area growth [18] have been solving these problems due to their nanometre-scale footprints. Since Mårtensson's pioneering works in 2004 [19], the heteroepitaxy of As/P/Sb-related III–V NWs on Si has been increasing. In 2011, we summarized the progress in the heteroepitaxy of III–V NWs on Si at that time, which mainly focused on selective-area growth and their device applications [20]. Topics concerning the III–V NWs on Si are attracting much attention today. Most of the reports have focused on the synthesis of the NWs on Si. So far, the growth of GaAs [21–24, 29–38, 53–62, 82–98, 118, 119, 126, 129], InP [49–52, 76–80, 108–112, 122, 123], InAs [10–12, 14, 15, 25–27, 39–47, 68–70, 73, 99–101, 124, 126, 130, 142, 144], InSb [117], and ternary alloys such as InGaAs [13, 48, 71–75, 102–107, 120, 121, 139], GaAsP [81, 114, 115], InAsP [113] and GaAsSb or InGaSb [116, 125] NWs on Si have been reported, and these NWs were grown by using metal-catalysed VLS [23, 24, 30, 31, 49–51, 55, 62, 65–67, 70, 77, 79, 81, 83, 104, 106, 109, 111, 112, 127–129], self-catalysed VLS [21, 22, 27–29, 32–38, 40, 41, 43–46, 50, 53, 54, 57–61, 63, 64, 71, 74, 78, 80, 82, 85, 86, 88–94, 96–98, 103, 105, 107, 108, 110, 113–119, 123–126], and catalyst-free selective-area growth [25, 26, 39, 47, 56, 68, 69, 72, 73, 75, 84, 87, 95, 99–102, 120–122, 142, 144]. The most interesting phenomenon of the nanometre-scaled epitaxy is suppression of misfit and threading dislocations, because the nanometre-scaled footprints moderately relax the lattice mismatches. For the selective-area growth, the formation of misfit dislocations in the III–V NWs on a Si substrate have been systematically characterized as a function of the NW diameter [130]. Also, the mask layer eliminates the propagation of threading dislocations inside the grown NW material.

The device applications can be divided into two categories: simple integration and fusion of III–V NWs with Si as a new heterointerface. Basic electronic and optical devices such as light-emitting diodes (LEDs) [34] and vertical FETs [10–15, 47, 75, 102] on Si have been reported as the simple integration, and high performance devices such as high-electron mobility transistors (HEMTs) [75, 102] have been demonstrated on Si substrates. In the fusion of III–V NWs with Si, heterojunctions of III–V/Si with fewer dislocations present a unique band discontinuity across the III–V NW/Si heterojunction. Electronic and optoelectronic devices using III–V NW/Si heterojunctions such as tunnel diodes [42, 73, 121, 144], and tunnel FETs (TFETs) [39, 68, 120, 130, 142, 144] have been demonstrated.

We are now reporting on our recent progress in the heteroepitaxy of III–V NWs on Si, specifically focusing on the details on the selective-area growth of vertical InGaAs NWs on Si and Zn-doped InAs NWs on Si substrates, and our demonstration of electronic devices such as vertical FETs, tunnel diodes, and TFETs using III–V NWs on Si and III–V NW/Si heterojunctions formed using selective-area MOVPE.

2. Selective-area growth of vertical InGaAs NWs on Si

The formation of a (1 1 1)B-oriented surface on a Si surface is important for aligning vertical III–V NWs on Si because almost all of the III–V NWs grow preferentially along the $\langle 111 \rangle$ direction. The (1 1 1)B-oriented surfaces on a Si(1 1 1) surface are the group-V incorporated Si(1 1 1) and group-III terminated Si(1 1 1) surfaces [131, 132]. These (1 1 1)B-oriented surfaces should be formed just before the growth of III–V NWs. The selective-area growth of III–V NWs on Si requires stricter conditions, since the surface area for NW growth is restricted to within the nanometre-scaled region. Moreover, the co-existence of the (1 1 1)B- and (1 1 1)A-oriented surfaces in the selective-area growth forms hillock structures instead of forming anti-phase defects. This growth behaviour can be prominently observed in the case of the selective-area growth of vertical InGaAs NWs on Si. We recently reported on how to align the vertical InGaAs NWs on Si substrates [75]. However, the detailed characterization of the InGaAs NWs on Si by using selective-area growth has not yet been reported on. In this section, we focus on the details of this selective-area growth.

InGaAs is widely used in high performance electronic devices such as planar HEMTs and optical devices used for infra-red lasers and passive devices such as APDs because of its band-gap engineering with In/Ga ratio variation. Once the heterogeneous integration of vertical InGaAs NWs is achieved on Si substrates, the possibility of NWs for the device applications briefly mentioned above will become reality. For example, the Fermi levels within the InGaAs NWs can be changed based on the composition of the In atoms [133]. This means that Schottky barrier height can be controlled by the composition. In addition, the InGaAs NWs are expected to be used in tandem-type solar cells because their nanometre-scaled cross-section would release interface strain and thus avoid introduction of misfit dislocations between the III–V/Ge interfaces. They also can be used for a wide range of wavelength charged-coupled devices (CCDs) in tandem with Si-based CCDs. Therefore, InGaAs NWs on Si would be better material systems because their one-dimensional structure and nanometre-scaled footprint can easily accommodate any lattice mismatches regardless of misfit dislocations. We investigate the epitaxial technique for aligning InGaAs NWs on Si the growth directions and positions for these applications to take full advantage of selective-area growth.

The growth conditions for the selective-area growth of vertical InGaAs NWs on Si(1 1 1) are slightly different from those for vertical InAs and GaAs NWs on Si. The low-temperature surface cleaning using AsH₃ at 400 °C and using the flow-rate modulation epitaxy (FME) mode were effective for forming a (1 1 1)B-oriented surface and aligning vertical InAs NWs on Si(1 1 1) for the selective-area growth of InAs NWs on Si [131]. The low-temperature surface cleaning effectively forms an As-incorporated Si surface that corresponds to the (1 1 1)B-oriented surface. The FME mode terminates the Si dangling bond and the incorporated As atoms by using the In atoms. In addition, the low-temperature surface cleaning by AsH₃ and the low-temperature buffer GaAs growth

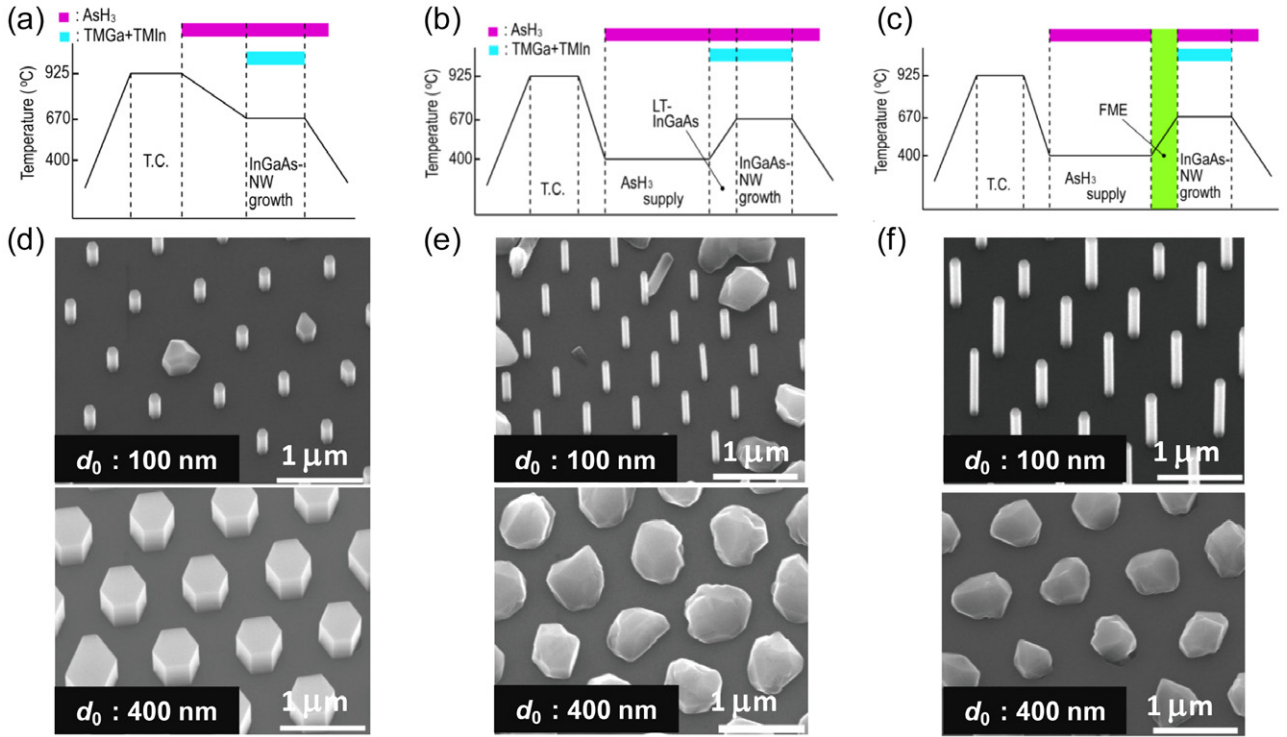


Figure 1. Growth sequences: (a) conventional sequence, (b) AsH_3 surface treatment at 400°C and low-temperature (LT) InGaAs growth, (c) AsH_3 surface treatment at 400°C and flow-rate modulation epitaxy (FME), and representative SEM images of InGaAs grown by using (d) the sequence in (a), (e) the sequence in (b), and (f) the sequence in (c).

were effective for aligning the vertical GaAs NWs on Si(1 1 1) [132]. The growth condition of the vertical InGaAs NWs on Si is slightly different from that for InAs and GaAs NWs on Si [131, 132]. In the InGaAs case, the bonding-energy difference of Ga–Si and In–Si should be taken into account for the formation of the (1 1 1)B-oriented surface.

The (1 1 1)-oriented Si substrates were used as the starting substrates. First, the substrates were etched using a hydrofluoric (HF) solution and then cleaned with a so-called RCA cleaning that uses SC1 and SC2 solutions ($1\text{NH}_4\text{OH} : 1\text{H}_2\text{O}_2 : 5\text{H}_2\text{O}$ and $1\text{HCl} : 1\text{H}_2\text{O}_2 : 6\text{H}_2\text{O}$ at 75°C) to remove any metal particles from their surfaces. For the selective-area growth of InGaAs NWs on Si(1 1 1), we used a lithography defined mask opening inside a $50 \times 50 \mu\text{m}^2$ square SiO_2 mask that was 20 nm thick. The opening diameter (d_0) was 100 or 400 nm. The SiO_2 film was made by using thermal oxidation at 950°C . The InGaAs NWs were grown in a low-pressure (76 Torr) horizontal metal-organic vapour phase epitaxy (MOVPE) system, supplying trimethylindium (TMIn), trimethylgallium (TMGa), and arsine (AsH_3) as source materials. The partial pressures of TMIn ([TMIn]), TMGa ([TMGa]), and AsH_3 ($[\text{AsH}_3]$) were 9.7×10^{-7} , 5.7×10^{-7} and 5.0×10^{-4} atm. The growth temperature (T_G) was 670°C , and the growth time was 20 min.

Figure 1 shows several growth conditions for the InGaAs NWs on a Si substrate by using selective-area growth and a summary of the representative growth results of InGaAs on Si with opening diameters of 100 and 400 nm under each growth condition. We commonly used thermal cleaning at 925°C in a H_2 ambient for each growth conditions, which is

necessary to thermally evaporate the native oxide and to form the Si(1 1 1) 1×1 surface reconstruction. In figure 1(a), the substrate was cooled to $T_G = 670^\circ\text{C}$ in the AsH_3 ambient, and then the InGaAs NW growth was resumed. Figure 1(b) shows a similar growth sequence to those of the selective-area growth of vertical GaAs NWs on Si [132]. The sequence contains the low-temperature surface cleaning by AsH_3 to form an As-incorporated Si(1 1 1) surface and low-temperature InGaAs growth. Figure 1(c) follows the growth sequence of the selective-area growth of vertical InAs NWs on Si using the FME mode [131].

Figure 1(d) shows the representative growth results of the growth sequence shown in figure 1(a). The NW growth yield when $d_0 = 100$ nm was 87% and the hillock growth yield was 13%. Among the NW growths, the vertical InGaAs NW growth direction percentage was almost 100%. The hillock growth resulted from the co-existence of the (1 1 1)A and (1 1 1)B orientations inside the openings. For $d_0 = 400$ nm, the faceting growth of non-uniformed hexagons appeared. These results indicate that the (1 1 1)B-oriented surface formation was insufficient when there was a small opening diameter and the As-terminated Si surface was formed during the cooling down process, but the formation of the (1 1 1)A-oriented surface was almost suppressed for the large openings. This implies that the In or Ga atom termination when forming a (1 1 1)B orientation was dominant under this growth sequence.

Figure 1(e) depicts the InGaAs growth results of the sequence in figure 1(b). Under the growth sequence for $d_0 = 100$ nm, the percentage of vertical and tilted InGaAs NW growths was 76 and 7%. The percentage of the

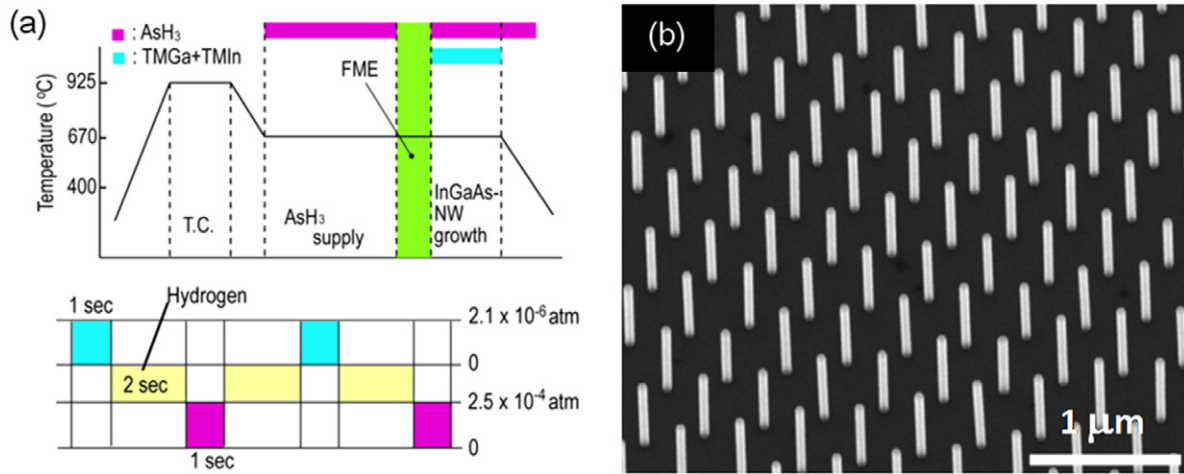


Figure 2. (a) Optimum growth sequence of aligning vertical InGaAs NWs on Si (adapted from [20]). (b) Representative SEM image showing vertical InGaAs NW array on Si (adapted with permission from [20], Copyright 2011 IEEE).

hillocks was 17%, and this percentage was dominant when $d_0 = 400$ nm. The growth yield of hillocks was almost the same as those shown in figure 1(d), but the percentage of the inclined NW growth was slightly increased, which means a (111)A-oriented surface formation was facilitated by the growth sequence. This indicates that 70–80% of the openings were changed into a (111)B-oriented surface during the low-temperature surface cleaning by AsH_3 , and the (111)A oriented surface was formed during the low-temperature InGaAs growth. The Ga–In alloy and Si were thought to enhance the thermal reactions and lead desorption. After the desorption, other (111)A surfaces were formed. The As termination against a dangling bond of Si(111) occurred during the low-temperature InGaAs growth.

Figure 1(f) shows the growth results for the growth sequence in figure 1(c). The percentage of vertical InGaAs NWs was almost 100% when $d_0 = 100$ nm. However, the diameter and height of the vertical InGaAs NWs were not uniform. In the case of $d_0 = 400$ nm, all of the grown materials were hillock structures. This indicates that the growth sequence can moderately form a (111)B-oriented surface and align the vertical InGaAs NWs when there is a small diameter, while the formation of a (111)B-oriented surface was insufficient and forms hillocks due to the coalescence of multi nuclei on the (111)A and (111)B surfaces when there is a large opening diameter. Since the role of the FME mode was to terminate the remaining dangling bond on a Si(111) surface by using group-III atoms, this mode seemed to be effective enough for terminating the dangling bonds created by In or Ga atoms for small openings. However, the termination when using group-III atoms was insufficient and As termination possibly occurred during the FME mode in case of the large openings.

According to these growth characterizations, the growth sequence in figure 1(a) and the FME in figure 1(c) are effective at forming a (111)B-oriented surface for aligning vertical InGaAs NWs on a Si(111) surface with small openings. Thus, the growth sequence was optimized, which is shown in figure 2(a) [20]. In this case, the combination of AsH_3

surface treatment and the FME mode at 670°C is important for aligning vertical InGaAs NWs on Si. The representative growth results are shown in figure 2(b). The percentage of vertical NW was almost 100%. A (111)B surface orientation due to the incorporation of group-V atoms and a Si^+ surface were thought to be formed under the sequence depicted in figure 2(a).

The yield of the vertical InGaAs NW growth strongly depended on $[\text{AsH}_3]$ during NW growth in the sequence depicted in figure 2(a). Figure 2(b) shows some typical growth results. The yield of the vertical InGaAs NWs increased to 100% when increasing $[\text{AsH}_3]$, as shown in figures 3 and 4. This indicates that the InGaAs NWs nucleation process proceeds well when using a high AsH_3 , and group-III atoms, which adsorbed into Si dangling bonds to form a (111)B-oriented surface, are easily desorbed from the Si surface at higher temperatures, but high As coverage of the In/Ga-terminated Si surface suppresses the desorption of the group-III atoms from the In–Si and Ga–Si bonding. For a lower $[\text{AsH}_3]$, the desorption process for the group-III atoms was enhanced with less As coverage and the NW growth in itself failed eventually suppressed. In addition, the NW growth yield decreased to 1%.

Figure 5(a) depicts a transmission electron microscopy (TEM) image of InGaAs NW with a diameter of 67 nm. The diameter of the InGaAs NW/Si heterointerface was 33 nm. The crystal structure of the InGaAs NW was a zinc-blende structure with many rotational twins. The frequency of the twin was distributed within three monolayers (MLs). Although the InGaAs NW had many rotational twins, no threading dislocation was observed in them. An energy dispersive x-ray (EDX) line-scan profile showed that the In composition was 70% [75] and there was no diameter dependence [120]. The In composition was higher than that of the In in the vapour phase (63%). This is because the surface diffusion lengths of In atoms on SiO_2 and sidewalls of an InGaAs NW were longer than those of Ga atoms. Then, the number of In adatoms increased in the InGaAs NW growth. Figure 5(b) depicts the ε_{xx} strain mapping of the InGaAs NW/Si heterointerface.

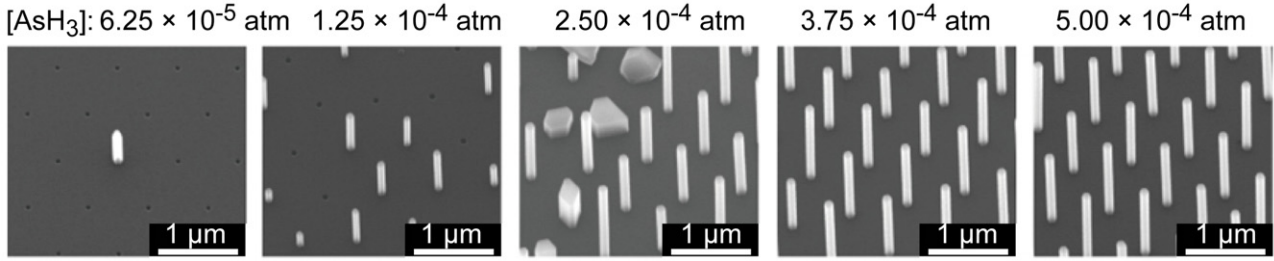


Figure 3. AsH₃ partial pressure ([AsH₃]) dependence of selective-area growth of InGaAs NWs on Si.

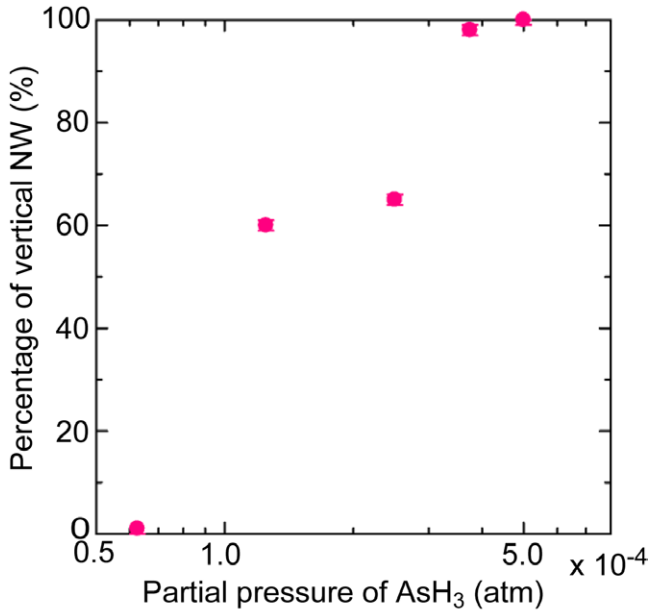


Figure 4. Percentage of vertical InGaAs NWs with variation of [AsH₃].

The xx direction corresponds to the $\langle -1\ 1\ 2 \rangle$ direction. The strain was calculated by using the peak-pair finding method [134]. The InGaAs NW/Si heterointerface had periodical misfit dislocations. The periodicity of the misfit dislocations was 41.3 ± 3 Å, which coincide with the calculated values from the lattice mismatch (43.1 Å). The number of dislocations per unit length is possibly decreased as the d_0 decreases. The d_0 dependence of the numbers of misfit dislocations across the III–V NWs/Si heterointerface has been investigated. The results showed that the number of misfit dislocations in the grown III–V NW/Si heterointerface falls appreciably below the calculated numbers from their lattice mismatch as diameter decreases [130]. This helped to predict that coherent growth can be achieved even in highly lattice mismatched systems for smaller diameter with selective-area growth. In fact, coherent growth has been achieved in GaAs NW/Si regardless of the misfit dislocations for $d_0 = 19$ nm [132].

3. Applications of vertical surrounding-gate FETs using III–V NWs on Si

Once vertical III–V NWs can be integrated on a Si substrate using selective-area growth with lithography defined

positioning, the grown III–V NWs can be directly be used as III–V channels for vertical surrounding-gate FETs [135]. Si-based CMOS technologies have recently been used to consider the possibility of creating surrounding-gate or gate-all-around structures to suppress the off-state leakage current and the III–V materials as alternative channel materials against the strained SiGe channels. These are needed to decrease the power consumption of electronic circuits by decreasing the off-state leakage current and enhancing the on-state current under low bias conditions. Furthermore, the vertical FET structures are expected as building blocks for future three-dimensional large-scale integrated circuit (LSI) chips [136]. Thus, the possibility of using vertical III–V NW channels as alternative channels on Si platforms has attracted a great deal of attention. In addition, these III–V NW channels grown by using selective-area growth would be used for high-performance back-end-on-line (BEOL) transistors as well as for front-end-on-line (FEOL) transistors such as Si-CMOS technologies.

A vertical FET using compound semiconductor NWs was firstly reported by Ng *et al* in 2004 [137]. As for As/P-related III–V NWs, VLS grown InAs NWs on InAs substrates were first studied for vertical FET applications [138] and InAs NWs wrapped-gate transistors were demonstrated on Si substrates [10]. Vertical surrounding-gate FETs using InAs NWs on Si, which are grown by using the selective-area method, have also been demonstrated [11]. In addition, InGaAs NW channels grown by using selective-area growth were recently achieved on Si substrates [13, 75].

The details of the device processes for these vertical surrounding-gate FET structures were previously reported [11, 13, 75]. We used a spin-coated low-dielectric insulating layer to isolate the source/gate/drain electrodes and an etch-back process using reactive-ion etching (RIE) to fabricate vertical surrounding-gate architecture. Figure 6 summarizes the recent progress made with vertical surrounding-gate FETs using InGaAs NW channels on Si [13, 75, 139]. The device had ten NWs connected in parallel with the drain metal. The measured current was divided by the number of NWs, and the current per NW was normalized by the outer perimeter of the gate metal. Table 1 summarizes the device parameters and performances for each device in figures 6(a)–(c). In figure 6(a), we first demonstrate characteristics of InGaAs NW FETs that were all doped by Si with a carrier concentration (n) of approximately $1 \times 10^{18} \text{ cm}^{-3}$ [13], which is similar to the junction-less transistor [140]. The threshold voltage (V_T) in this vertical FET was -0.37 V and the drain current (I_D) was modulated by the gate voltage (V_G) with a subthreshold slope

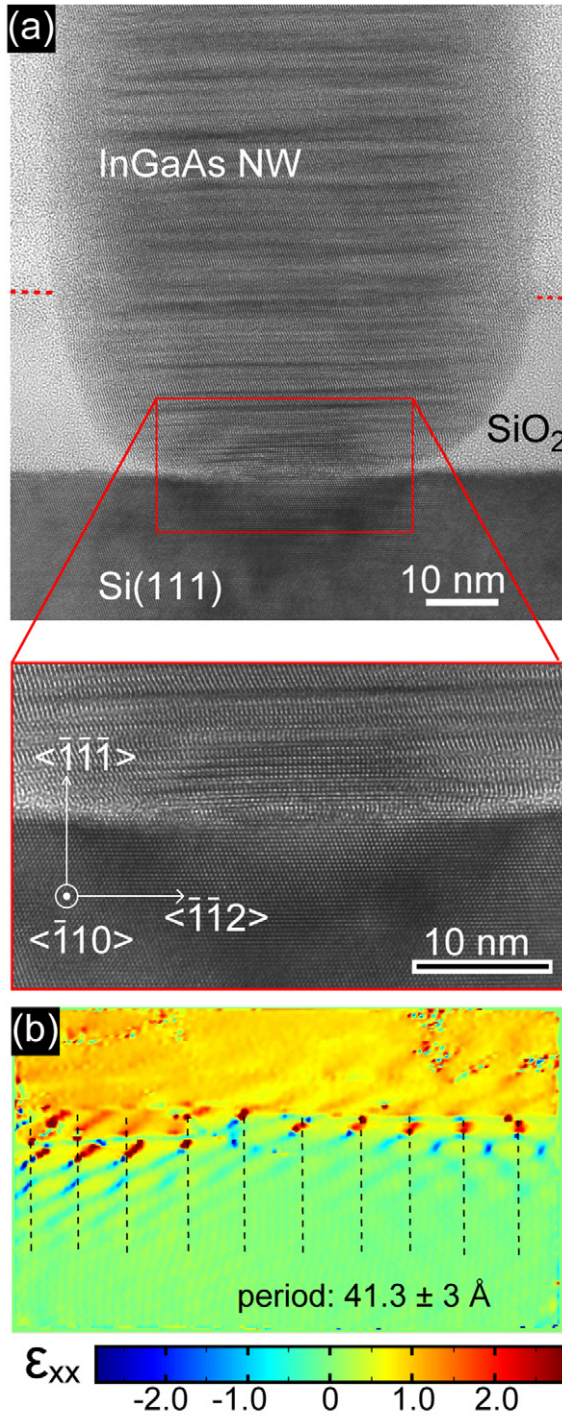


Figure 5. (a) TEM image showing InGaAs NW on Si. The NW is 76 nm in diameter and the heterointerface is 33 nm in diameter. Magnified TEM image of the red-square panel (bottom). (b) ϵ_{xx} strain mapping calculated from the red square in (a). The dashed lines denote the positions of misfit dislocations.

(SS) of 98 mV/decade. The drain-induced-barrier lowering (DIBL) was 165 mV/V. Next, the InGaAs NW channel was improved in figure 6(b). In this case, the InGaAs NW comprises Si-doped InGaAs ($1 \times 10^{18} \text{ cm}^{-3}$) stacked on undoped InGaAs ($5 \times 10^{16} \text{ cm}^{-3}$) and had a diameter of 60 nm [75]. The V_T of the FET shifts to positive to 0.18 V

due to the reduction of n in the NW-channel region and improves the SS by decreasing the NW capacitance. Then, V_T was shifted to 0.18 V. The SS and DIBL were improved to 85 mV/decade and 48 mV/V. Next we optimized the EOT of the InGaAs vertical surrounding-gate FET in figure 6(c). In this device, the oxide thickness was 4 nm and effect-oxide thickness estimated from the dielectrics was 0.75 nm. We introduced a gate-metal etching process to avoid as much process damage to the gate oxide as possible [139]. Eventually, we achieved moderate switching properties with an SS of 68 mV/decade and a DIBL of 33 mV/V. Through a series of device advances, the quality of the InGaAs/HfAlO interface was improved and the interface state density (D_{it}) ranged from 1.8 to $3.8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ with an EOT variation, and the I_D was increased to $0.07 \text{ mA } \mu\text{m}^{-1}$ at $V_{DS} = 0.50 \text{ V}$. However, the I_D for the InGaAs vertical surrounding-gate FETs was much lower than that of a Si-MOSFET. Moreover, further advanced techniques are required for higher I_D because future low operation power (LOP) devices that will be required in the year 2026 will require $0.66 \text{ mA } \mu\text{m}^{-1}$ at a supply voltage of 0.54 V [141]. Thus, we need novel techniques such as passivation and ballistic transport for the InGaAs vertical surrounding-gate FET in order to enhance the I_D at a lower supply voltage.

We designed the InGaAs–InP–InAlAs–InGaAs core-multishell (CMS) NW [14, 75] shown in figure 7(a). The InAlAs consisted of InAlAs/Si-doped InAlAs/InAlAs modulation-doped multi-layers and forms two-dimensional electron gas (2DEG) inside the core InGaAs NW under a positive V_G . Although the InAlAs shell layer without a modulation-doped layer was confirmed to have a passivation effect, the I_D and G_m were not markedly enhanced as compared to that of a bare-InGaAs NW channel. The 2DEG of the CMS NW enhances the I_D at a lower supply voltage. Figures 7(b)–(g) shows summaries of cross-section TEM images and the transfer characteristics of the vertical surrounding-gate FET of the CMS NWs [14, 75, 139]. For the thicker shell layer in figure 7(b), the SS was as large as 130 mV/decade, and the transfer curve in figure 7(c) showed kinks at around $V_G = -0.50 \text{ V}$, which were caused by the thickness fluctuation of the outer InGaAs shell layers in figure 7(b). The thickness fluctuation was caused by a slight difference in the nucleation process of the InGaAs on the InAlAs surface. The V_T was -0.07 V . The thickness for thin CMS layers was uniform and the SS was improved to 75 mV/decade, which is close to that of the bare InGaAs NW vertical surrounding-gate FET. V_T was 0.38 V, and I_D was increased to $0.45 \text{ mA } \mu\text{m}^{-1}$ at $V_{DS} = V_G - V_T = 0.50 \text{ V}$ [75]. The SS for the InGaAs CMS NW became 70 mV/decade by further decreasing the thickness of the outer InGaAs layer in figures 7(f) and (g). The I_D was slightly decreased to $0.43 \text{ mA } \mu\text{m}^{-1}$ at $V_{DS} = V_G - V_T = 0.50 \text{ V}$, which resulted from the increases in the InP and InAlAs thickness. The important point regarding the CMS NW is that Al segregation occurs at the corner of the CMS, which forms an Al-rich InAlAs layer and divides the radial HEMT layer into a six-sided HEMT layer. This helped to integrate six HEMTs on a single InGaAs NW.

Next, we characterized the oxide-thickness dependence of the vertical surrounding-gate FET using InGaAs CMS NWs.

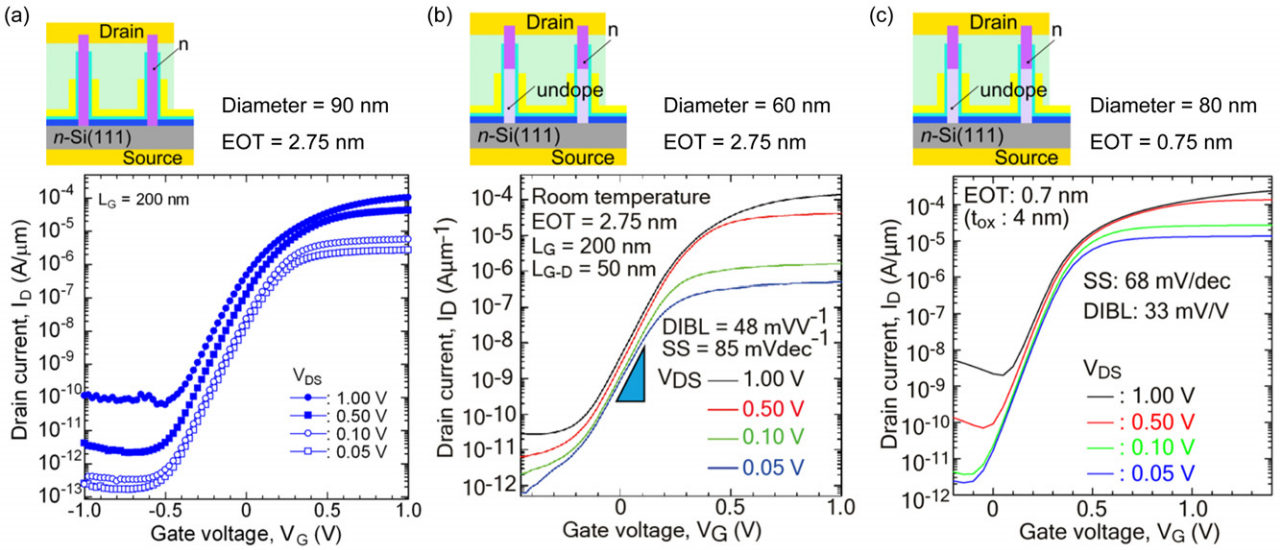


Figure 6. Transfer curves for surrounding-gate FETs using InGaAs NW channels: (a) Si-doped InGaAs NW channel (adapted with permission from [13], Copyright 2011 IEEE), (b) Si-doped InGaAs/undoped InGaAs axial NW channel (adapted with permission from [75], Copyright 2012 Nature) and (c) Si-doped InGaAs/undoped InGaAs axial NW channel with EOT = 0.75 nm (adapted with permission from [139], Copyright 2013 IEEE).

Table 1. Summary of device performance in figure 6.

Material	Sub.	EOT	d_{NW} (nm)	L_G (μm)	I_{DS} ($mA \mu m^{-1}$) at $V_{DS} = 1.00$ V	I_{DS} ($mA \mu m^{-1}$) at $V_{DS} = 0.50$ V	I_{off} ($nA \mu m^{-1}$) at $V_{DS} = 0.50$ V	I_{on}/I_{off} at $V_{DS} = 0.50$ V	SS (mV/dec)	DIBL (mV/V)
Figure 6(a)	Si	2.75	90	0.20	0.16	0.02	10^{-3}	10^7	97	160
Figure 6(b)	Si	2.75	60	0.15	0.25	0.04	10^{-2}	10^6	85	48
Figure 6(c)	Si	0.75	80	0.15	0.21	0.07	10^{-1}	10^6	68	33

Figure 8(a) depicts the transfer curves at $V_{DS} = 0.50$ V with EOT variation. In this characterization, the diameter of the NW was fixed to 100 nm and that of the core-InGaAs NW was fixed to 55 nm. Figure 8(b) shows the EOT dependence of SS and DIBL. We characterized ten devices for each EOT and plotted the averages in figure 8(b). The SS and DIBL decreased with decreasing EOT: 70 ± 3 mV/decade and 24 ± 4 mV/V were obtained for EOT = 0.75 nm. On the other hand, I_D was constant with the EOT variation. This was because the carrier density of the 2DEG was not changed by the difference in EOT.

The advantage of using the direct integration of III-V NWs on Si substrates by selective-area growth is that the radial growth mode such as that for the InGaAs-InP-InAlAs-InGaAs CMS NW can be distinctly formed around the sidewalls on the NW channel. Moreover, the III-V NW/Si heterojunction forms a large conduction band offset across the III-V NW/Si heterojunction. The band offset is convenient for high mobility channel materials such as InGaAs and InAs, whose channels always lead to a high off-leakage current with a low effective electron mass. In figure 8(a), the off-state leakage current was surely reduced to $10 pA \mu m^{-1}$, which was three orders of magnitude lower than that of future LOP transistors (the off-state leakage current is $5 nA \mu m^{-1}$). Instead, these III-V/Si heterojunctions tend to possess higher series resistance. The next challenges for the vertical FETs using III-V NW channels are reduction of resistance and demonstration of p-channel FETs.

4. Applications of tunnel FETs using III-V/Si heterojunction

In addition to the simple integration of vertical III-V NW channels on Si, the heterointerface across III-V NW/Si works as a specific tunnel junction when III-V NWs are grown on Si regardless of any defects such as threading dislocations and anti-phase defects. We have proposed the application of tunnel FETs using the III-V/Si heterojunctions [142] shown in figure 9, and first demonstrated the vertical tunnel FET using an InAs NW/Si heterojunction as a n-channel switch shown in figure 9(a) [39]. The big goal for the TFET for application in CMOS technologies is to achieve a steep SS of below 60 mV/decade and increase the tunnelling current. In the n-channel vertical TFET using III-V NW/Si heterojunctions, one must consider the series resistances of the device structure, which are (1) contact resistance, (2) channel resistance, and (3) junction resistance, in order to achieve a steeper SS. This is because the SS in a TFET can be expressed as a function of V_{DS} and V_G [143].

- (1) *Contact resistance.* The contact resistance should be lowered as far as possible because it affects the reverse bias. For steep SS switching, the reverse bias should be higher under a small V_{DS} . It is very difficult to decrease the contact resistance for a III-V NW with a small diameter. Thus, enlargement of the contact area was effective for reducing the series resistance, as mentioned in a previous

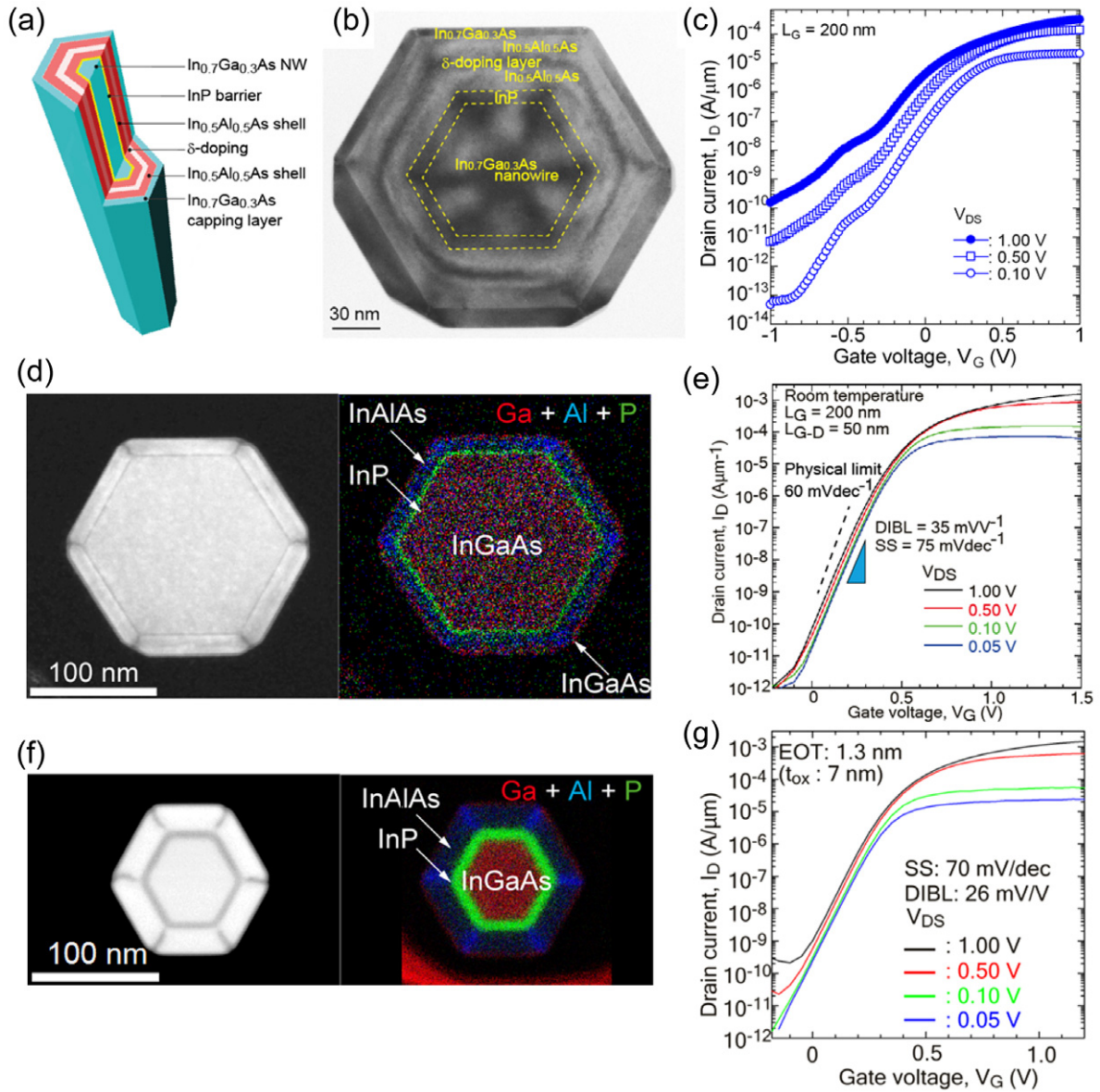


Figure 7. (a) Illustration of InGaAs-InP-InAlAs-InGaAs CMS NW. (b) Cross-section TEM image of CMS NW with thicker shell layers. (c) Transfer curves measured from surrounding-gate FET using the CMS NW in (b). (d) Bright-field scanning TEM (BF-STEM) image and EDX elemental mapping for Ga-Al-P of the CMS NW with thicker shell layers. (e) Transfer curves measured from CMS NW channel in (d). (f) BF-STEM image and EDX elemental mapping for Ga-Al-P of CMS NW with thinner shell layer. (g) Transfer curves measured from CMS NW channel in (f). (Adapted with permission from [13] Copyright 2011 IEEE, [75], Copyright 2012 Nature [139], Copyright 2013 IEEE).

report [142]. In addition, the formation of a Ni/III-V alloy was effective at reducing the contact resistance [144].

- (2) *Channel resistance.* This resistance should be higher to induce a large internal electrical field. Thus, the formation of intrinsic NWs is important. However, III-V NW channels formed using MOVPE intrinsically contain carbon impurities. For example, InAs has a carrier concentration of 10^{16} – 10^{17} cm⁻³, which results from the carbon impurity from the metal-organic precursor. It is very difficult to reduce the intrinsic carrier concentration in a very small nanostructure, since a single dopant atom provides a high carrier concentration at an order of 10^{17} cm⁻³ when the diameter of the III-V NW is below 30 nm. We introduced a pulsed-doping technique

of p-type impurities during the growth of the III-V NWs to compensate for residual donor impurities, and demonstrated the turn-on voltage shift of TFET using an InAs NW/Si heterojunction by decreasing the intrinsic carrier concentration [130]. In addition, steep SS was achieved in the vertical TFET using an InGaAs NW/Si heterojunction [120].

- (3) *Junction resistance.* The resistance should be the highest among the other series resistances because a higher junction resistance induces a larger internal electrical field under a lower V_G or V_{DS} . However, the III-V/Si heterointerface inherently forms misfit dislocation networks due to the lattice mismatch. The misfit dislocations form defect levels across the III-V/Si

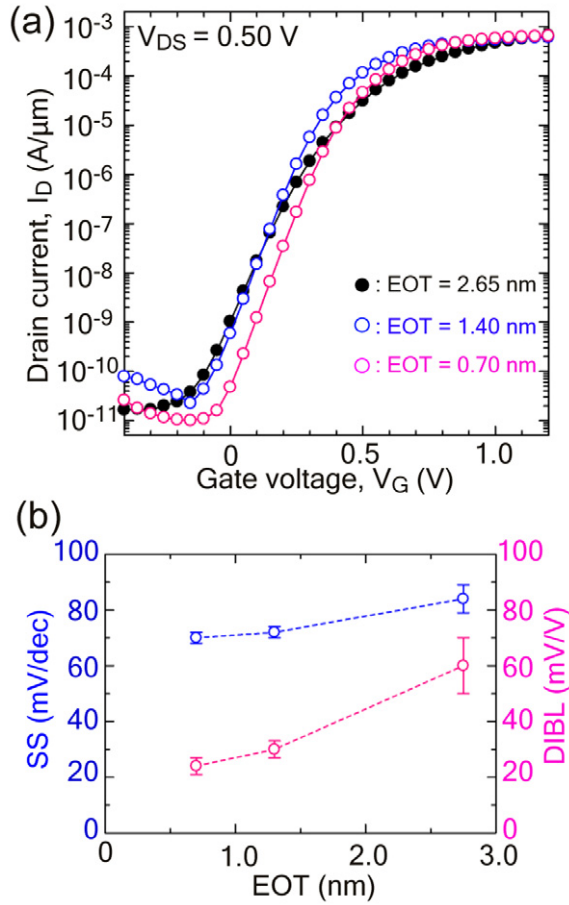


Figure 8. (a) EOT dependence of transfer curve of InGaAs CMS NW channel. $V_{DS} = 0.50$ V. (b) Average SS and DIBL of InGaAs CMS NW channel with variation of EOT.

heterojunction and a tunnelling transport process occurs through the defect levels, which is called trap-assisted tunnelling (TAT). When the TAT is the dominating process, the SS increases because the tunnelling leakage current is increased. The heterointerface should possess zero misfit dislocations in order to suppress the TAT process, and thus, coherent growth should be achieved with the integration of III–V NWs on Si. The reduction of the crystal growth area was recently proven effective at reducing the number of misfit dislocations across the III–V NW/Si heterointerface, and report on this also predicted the coherent growth mode was able to be achieved by decreasing the diameter of the openings [130], and reducing the diameter of heterointerface in practical TFETs using InAs NW/Si heterojunctions produced a steep SS turn-on switching with a minimum of 12 mV/decade at room temperature [130, 142].

We have also demonstrated n-channel vertical TFETs with III–V NW/Si heterojunctions. However, p-channel vertical TFETs with InAs NW/Si heterojunctions have been less investigated [68]. In particular, there has been no report regarding a p-channel TFET with p-type III–V NW/n-type Si heterojunctions like that shown in figure 9(b). Here we demonstrate the selective-area growth of p-type InAs NWs

on Si and the fabrication of vertical TFETs with p-InAs/Si heterojunctions as a p-channel switch.

The substrate was n-type Si(1 1 1) ($r = 0.1 \Omega \text{ cm}$). InAs NWs were grown in a low-pressure horizontal MOVPE system. The growth conditions included a partial pressure of TMIn, $[\text{TMIn}] = 4.87 \times 10^{-7} \text{ atm}$, a partial pressure of AsH_3 , $[\text{AsH}_3] = 1.25 \times 10^{-4} \text{ atm}$, growth temperatures of 540 and 560 °C, and a growth time = 7 min. We used diethylzinc (DEZn) for the p-type doping of the InAs NWs. The growth conditions for controlling the InAs NWs followed those in the previous report [131]. The $[\text{DEZn}]/[\text{TMIn}]$ ratio was 4.8. The carrier concentration of the planar p-InAs grown under the same conditions was approximately $1 \times 10^{18} \text{ cm}^{-3}$. The diameters of the openings were fixed to 70 nm.

Figure 10(a) shows Zn-doped InAs NWs on a Si substrate grown at 540 °C. The diameter of the grown InAs NWs was about 130 nm, which indicates that the lateral overgrowth along the $[-1 1 0]$ directions was enhanced even though there was optimum T_G for the InAs NW growth [145]. The rate of the lateral overgrowth was approximately 4.3 nm min^{-1} . The enhancement of the lateral overgrowth using Zn doping indicates that the nucleation process on the $\{-1 1 0\}$ side facets of the InAs NWs was increased. This means that the adsorption processes of the In atoms were enhanced due to the Zn atoms because the surface diffusion length of the In atoms shortened due to the Zn. Thus, the supersaturation of the In atoms increased on the $\{-1 1 0\}$ side facets with the growth of Zn-doped InAs NWs. It should be noted that the desorption process of the As adatoms on the $\{-1 1 0\}$ facets was not changed by any dopants. Figure 10(b) depicts the Zn-doped InAs NWs grown at 560 °C. The slightly increased T_G (> 540 °C) suppressed the lateral overgrowth of the Zn-doped InAs NWs. The lateral overgrowth for the InAs NWs was suppressed under the growth conditions. In this case, the desorption process of the As atoms was enhanced and the adsorption process was decreased under a higher T_G .

Next, we formed InAs NWs comprised of a Zn-doped InAs/Zn-pulse doped InAs axial junction. The purpose of the pulsed doping is to create an intrinsic layer by using the compensation effect. After growth of the Zn-pulse doped InAs NW at 540 °C for 5 min, the NW growth was resumed at 560 °C for 10 min using Zn doping to create pseudo-intrinsic InAs/ p^+ -InAs axial junctions on an n-Si substrate. The NW was 70 nm in diameter and 1.2 μm in height. The device processes for the vertical FET structure were the same as in previous reports [130]. We used a single InAs NW for the device. The gate oxide was $\text{Hf}_{0.8}\text{Al}_{0.2}\text{O}$ with a thickness of 10 nm, and the gate metal was tungsten. The gate length was 150 nm, the drain metal was a Ti–Pt–Au non-alloy Ohmic electrode and the source metal was a Ni–Au electrode. After depositions of the source and drain electrodes, the device was annealed at 330 °C for 5 min in N_2 .

Figure 11 shows the transfer curve of the device. The negative V_{DS} was reverse biased in the direction against the Zn-doped InAs/Zn-pulse doped InAs/n-Si junction because the source electrode was grounded. This curve indicates that the tunnelling current from the n-Si to the InAs NW was modulated by the negative V_G , which follows the simulation results in

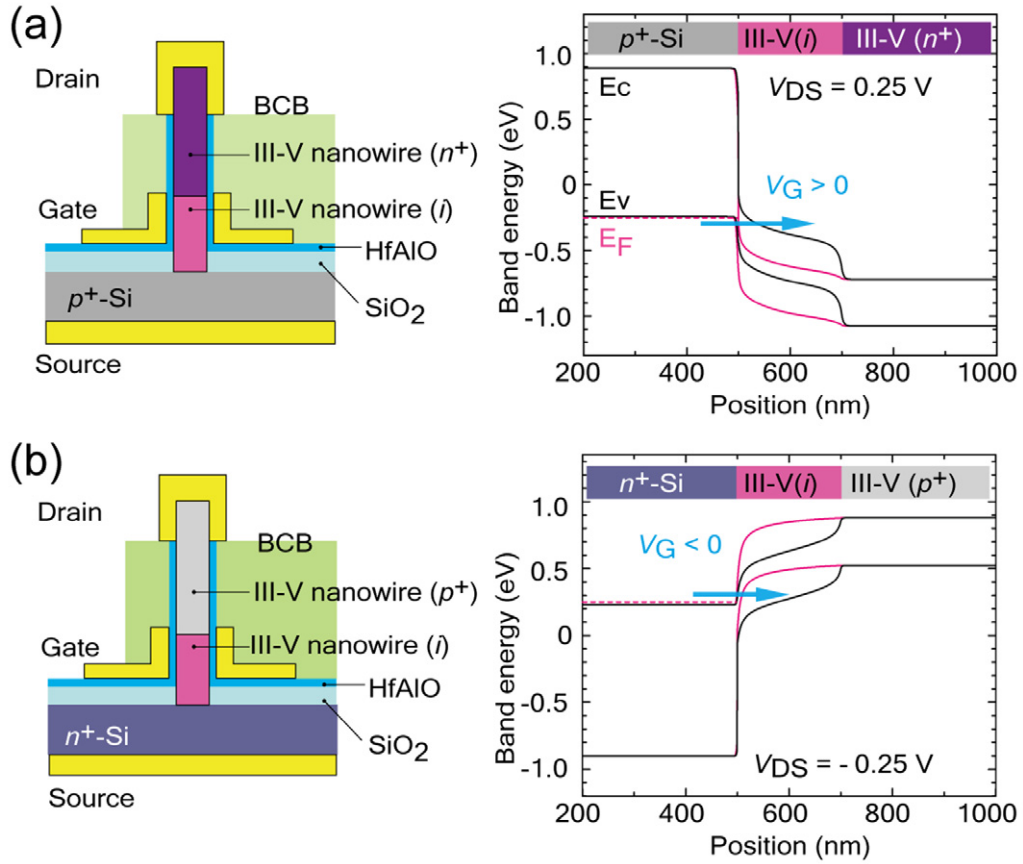


Figure 9. Device designs of vertical TFET using III-V NW/Si heterojunction: (a) n-channel TFET on Si(111) using III-V NW to serve as channel and drain and a one-dimensional Poisson–Schrödinger solver. At $V_{DS} = 0.25$ V, the positive gate bias (pink curve) induces Zener tunnelling transport from the p-Si to the III-V NWs. (b) p-channel TFET using III-V NW. At $V_{DS} = -0.25$ V, the negative V_G (pink curve) induces Zener tunnelling transport from the n-Si to the III-V NW.

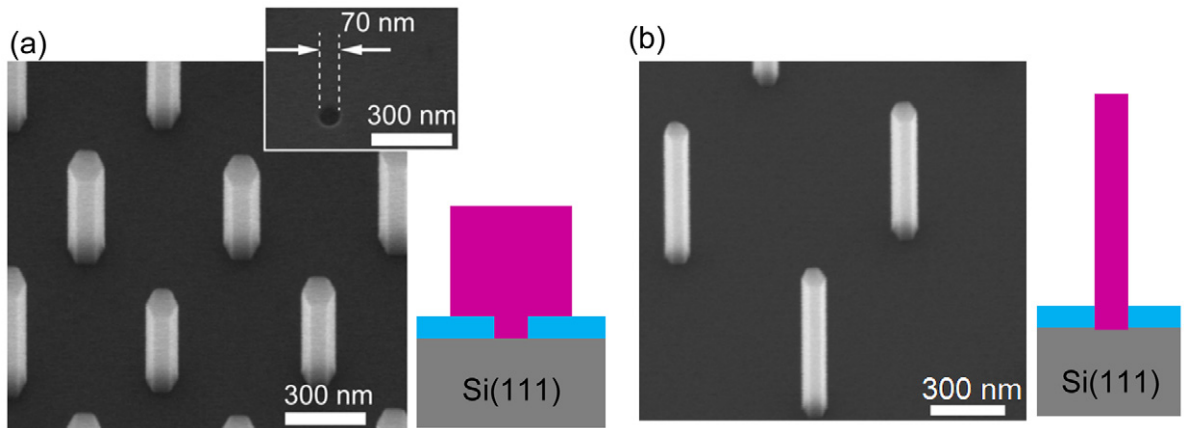


Figure 10. (a) SEM image showing Zn-doped InAs NWs on Si(111) grown at 540 °C. The inset shows the mask pattern. (b) SEM image showing Zn-doped InAs NWs on Si(111) grown at 560 °C.

figure 9(b). The SS was 86 mV/decade at $V_{DS} = -0.25$ V. I_{on}/I_{off} was about 10^4 at $V_{DS} = -0.25$ V. I_{off} was increased with increasing V_{DS} , and I_{on}/I_{off} decreased. This was because the Fermi level in the n-Si started to overlap that of the InAs due to the increase in V_G at a low V_{DS} . In this case, the tunnelling current is moderately modulated by V_G and the switching behaviour appeared, while at a high V_{DS} the Fermi level in the n-Si overlapped that of the InAs, and then the tunnel

current itself could be the leakage current. This resulted from the Zn interdiffusion that occurred from the Zn-doped InAs to Zn-pulse doped InAs channel region during the Zn-doped InAs NW growth, and the channel region became p-type InAs. Thus, voltage overlapping occurred in the InAs channel and drain regions under negative V_{DS} . This voltage overlapping due to the interdiffusion also degraded the SS, and thus a steeper SS below 60 mV/decade was not achieved in this case.

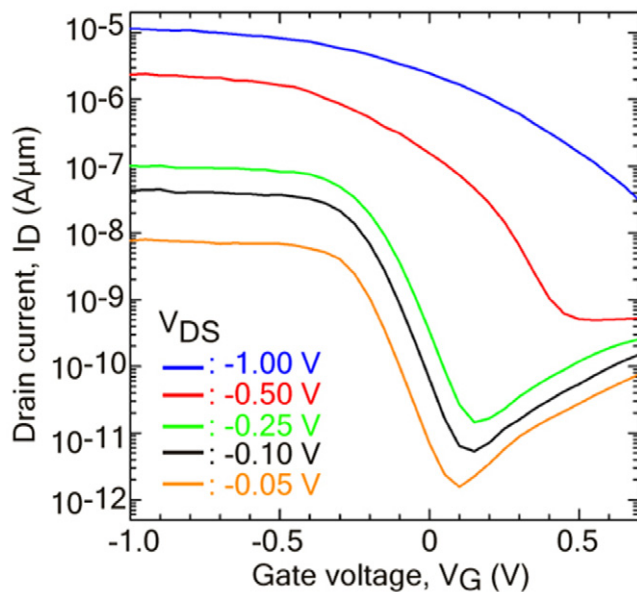


Figure 11. Transfer curve of p-channel TFET using Zn-doped InAs/Zn-pulse doped InAs/n-Si heterojunction at room temperature.

Although the device currently has degradation in the SS at $V_{DS} > -0.50$ V, the device is an attractive possibility for higher I_{on} current in the tunnel transport regime. I_{on} was $2 \mu\text{A} \mu\text{m}^{-1}$ at $V_{DS} = V_G = -0.50$ V, which is higher than that of a p-channel TFET using a III–V/Si heterojunction [68]. Further optimization of the device structure may be necessary to achieve both a high I_{on} and steep SS turn-on properties.

5. Summary

We have reviewed the recent progresses made with vertical III–V NWs, specifically the InGaAs and Zn-doped InAs NWs, on Si substrates by using selective-area growth. We also discussed vertical surrounding-gate transistors using III–V NW channels on Si as a first step towards attaining future vertical systems or integrating chips. The use of modulation-doped CMS NWs enhanced the performance of InGaAs NW-based surrounding-gate FETs on Si while maintaining an SS of 70 mV/decade. Finally, we reviewed the recent achievements made using TFETs with III–V NW/Si heterojunctions and discussed the application for p-channel TFETs by using Zn-doped InAs NW/Si heterojunctions for the first time. Our next target is to integrate these high-performance III–V NW surrounding-gate FETs and TFETs based on the III–V NW/Si junctions into a Si-LSI platform and to build low power electronic circuits.

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