Design and fabrication of 2.4 GHz pre-biased rectifier

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Abstract—A 2.4 GHz rectifier operating in a region of low RF input power was developed. The rectifier has a cross-coupled bridge configuration and is driven by a differential RF input signal. Since a rectifier needs an RF signal higher than the threshold voltage of transistors, we introduced a pre-biasing circuit to compensate for the threshold voltage. A low-voltage digital circuit, subthreshold voltage regulator, and low-power level shifter were introduced for reducing the power consumption of the pre-biasing circuit and increasing the driving voltage for the switches at the same time. The circuit simulations revealed that the pre-biasing circuit was effective in a low RF input power region. However, the output voltage was degraded in a high power region. Then, we combined the pre-biased rectifier in parallel with a non-biased rectifier. Three types of rectifiers consisting of LC matching circuits, 3-stage rectifier cells, and biasing circuits were designed and fabricated using a 0.18-μm mixed signal/RF CMOS process with one poly and six metal layers. The fabricated pre-biased rectifier operated in a region of RF input power of less than -15 dBm, while the non-biased rectifier could not operate in this region. The parallel combination of pre-biased and non-biased rectifiers effectively solved the drawback of the pre-biased rectifier in a high RF input power region.

Keywords: rectifier, sensor network, 2.4 GHz, RF, low-power pulse generator, subthreshold CMOS

1. Introduction

Recently, wireless sensor networks (WSNs) and radio frequency identification (RFID) tags have attracted much attention towards the realization of a ubiquitous network society. A wireless sensor node consists of a sensor, analog-to-digital converter, digital signal processor, and wireless transceiver. Much work has been done for achieving small, low cost, and low power consumption sensor nodes. The power consumption of the node is one of the most crucial problems to be solved because individual node battery replacement is impractical due to deployment of many nodes and/or inaccessible nodes [1-3]. An ideal solution is to operate wireless sensor nodes with electric energy converted from solar, thermal, and vibration energy in the environment. In the meantime, however, such energy harvesting technology is limited to only specific applications. A realistic solution is a combination of a rechargeable battery and energy harvesting for extending the battery lifetime [4]. RF power feeding from base stations where the RF signal is converted to DC power with a rectifier is an attractive method [1, 2]. Schottky diodes have been used for achieving highly efficient rectifiers [5]. Since Schottky diodes cannot be fabricated using the standard CMOS process and the other circuits in a sensor node are fabricated using the CMOS process, a diode should be made by connecting the gate and drain of a MOS transistor. The most critical problem in the diode-connected MOS transistor is a drastic reduction in the conversion efficiency when the amplitude of the input RF signal is less than the threshold voltage V_{th} of the transistor. Several methods have been devised for solving this problem. Yao *et al*. used transistors with ultralow V_{th} in 0.35-μm CMOS process [6], while Le *et al*. reduced V_{th} by injecting the charge via Fowler-Nordheim tunneling [1]. However, these methods are not available in the standard CMOS process. V_{th} cancelling with self-biasing [2, 7, 8] and external biasing [9] simply and effectively increase the conversion efficiency. Despite those efforts, the minimum detectable RF input power of around -20 dBm is still high. A rectifier can also be used as an envelope detector in a wake-up receiver. However, the sensitivity of the detector [10] is quite low compared with other wake-up receivers [3].

In this paper, we propose a pre-biased rectifier to improve the minimum detectable RF input power based on the differential-drive CMOS rectifier [8]. A carrier frequency of 2.4 GHz is used here because a small antenna of 2 cm can be used in this frequency region [11].

2. Circuit configuration

As mentioned in the previous section, the DC output voltage degrades drastically when the peak voltage of the input RF signal is less than the threshold voltage V_{th} of the MOSFET. To solve this problem, we used a pre-biasing technique with the differential-drive CMOS rectifier proposed by Kotani *et al*. [8]. In principle, the pre-biasing circuit operates with the energy generated by the rectifier itself. In this paper, however, an external voltage source was used to drive the pre-biasing circuit for simplifying the proof of

the concept.

2.1 Basic rectifier cell

Figure 1(a) shows the basic cell of the differential-drive CMOS rectifier proposed by Kotani *et al.* [8]. The input node DC_{in} was grounded for operating the basic cell as a one-stage rectifier. When RF_+ was positive and RF_- was negative, the on-resistances of pMOS MP_1 and nMOS MN_2 were low while those of MP_2 and MN_1 were high. On the other hand, when RF_+ was negative and RF_- was positive, the on-resistances of MP_1 and MN_2 were high while those of MP_2 and MN_1 were low. As these two states were repeated, the potential of DC_{out} gradually increased. At the same time, the average potential of V_1 and V_2 were almost the same as half the potential of DC_{out}, which effectively compensated the V_{th} of the transistors. To improve the minimum detectable RF input power, we introduce a pre-biasing circuit into a modified version of the original rectifier. Figures 1(b) and 1(c) show the basic cell of our pre-biased rectifier and the pulse waveform driving the switches. For simplifying the biasing scheme, only nMOS's were used instead of the original CMOS configuration. At the start, the switches SW1 and SW1' were closed while SW2 and SW2' were open. In this period, the gate nodes of the transistors were charged. Rectifying started by turning off SW1 and SW1' and turning on SW2 and SW2'. The on-resistances of SW2 and SW2' should be low enough to lower the RF signal loss.

Note that the RF input signal was not rectified during the gate charging period. Therefore, the gate charging period should be as short as possible. In addition, the power consumption of the pulse generator for controlling the switches should be as low as possible.

2.2 Pulse generator

A low duty cycle, low power consumption, and high driving voltage for the switches were required for the pulse generator. The block diagram of the pulse generator is shown in Fig. 2. A driving voltage of 1.5 V was used to reduce the on-resistances of the switches, while low-voltage digital circuits were introduced to reduce the power consumption as well as the duty cycle of the pulse. A voltage regulator was used to generate the supply voltage V_{DDL} of 0.5 V for the digital circuits. A pulse train was generated with NAND operation of two outputs from two successive inverter stages in a 9-stage ring oscillator, as shown in Fig. 2. The level shifter increased the pulse amplitude from 0.5 V to 1.5 V.

Figure 3 shows the circuit diagram for the voltage regulator. The voltage V_{DDL} was kept the same as the gate voltage of M_1,V_{ref}, generated with a pMOS ladder circuit. To reduce the power consumption, a subthreshold op-amp was used [12]. In the op-amp, the gate of the current source M_2 was grounded, and the operating current was controlled by changing the gate width of M_2. The supply voltage V_{DDL} might deviate from the designed value due to V_{th} variations of the MOSFETs. Since precise control of the period

of the pulses was not needed, this deviation was not significant.

Figure 4 shows the circuit configuration of the level shifter used in this study. To simplify the circuit topology of the original level shifter proposed by Osaki *et al*. [13], the feedback path from the output to the logic error correction circuits and the current path for the fall-transition were eliminated. Although the delay for the fall transition was higher than that in the original level shifter, the simplified level shifter could be used in our pulse generator.

3. Design and fabrication

We designed and fabricated 3-stage pre-biased rectifiers in a 0.18-μm mixed signal/RF CMOS process with one poly and six metal layers. Figure 5 shows a circuit diagram of the entire rectifier. We used an Advanced Design System (ADS) circuit simulator with a process design kit (PDK) provided by the CMOS foundry. An *LC* matching circuit was designed to maximize the RF input amplitude supplied to the rectifier cells [2]. The S parameters for the long metal lines (pads to inductors and inductors to rectifier, see Fig. 8) in the LC matching circuit were calculated with an electromagnetic field simulator (ADS Momentum) and used in the circuit simulations. The other parasitic capacitances were not taken into account in the simulations. Figure 6 shows the simulation results for the output waveforms from the pulse generator and rectifier with a 1-MΩ resistive load, where the RF input power and bias voltage were -10 dBm and 0.4 V. After the pre-biasing when V_{pulse} was high, the output voltage of the rectifier, V_{out}, rapidly increased.

Figure7 shows the dependences of the rectified DC output voltage V_{out} on the RF input power for non-biased, pre-biased, and combined rectifiers. The output voltage for the non-biased rectifier drastically degraded below an input power of -15 dBm, while the pre-biased rectifier operated successfully. However, the output voltage of the pre-biased rectifier was lower than that of the non-biased rectifier for an input power higher than -10 dBm. This was caused by the backward leakage current. Hence, we combined the pre-biased and non-biased rectifiers in parallel connection. The combination effectively improved the performance of the pre-biased rectifier in the high input power region, as shown in Fig. 7. The output voltage of the combined rectifier was almost the same as that of the non-biased rectifier. Figure 8 shows a microphotograph of the combined rectifier with a size of 1.0 mm × 1.3 mm including probing pads.

4. Measurement results

The fabricated circuits were measured by on-wafer probing. Figure 9 shows the input return loss S_{11} for the combined rectifier measured with a vector network analyzer. The minimum S_{11} frequency for the fabricated rectifier shifted from the designed value to the lower value. The wave characteristics above 3 GHz were caused by insufficient calibration.

A continuous wave at 2.4 GHz from a microwave synthesizer was modulated at 1 kHz with a mixer and single-to-balance conversion was performed with a balun. The load resistance was fixed to 1 MΩ (the load in the oscilloscope used). The input and output waveforms for the combined rectifier with a pre-bias voltage V_{bias} of 0.4 V is shown in Fig. 10. Rectification from RF to DC was successfully achieved. The measured pulse train from the generator is shown in Fig.11. The pulse repetition frequency was 9 kHz, and the power consumption was 18.5 nW from the 1.5 V power supply V_{DDH}. The pulse generator operated with a pulse repletion frequency of 1.1 kHz and a power consumption of 1.8 nW under a V_{DDH} of 1.0 V. No degradation in the rectified DC voltage was observed when V_{DDH} varied from 1.5 to 1.0 V.

Figure 12 shows the dependences of the DC output voltages V_{out} on the RF input power P_{in} for non-biased, pre-biased, and combined rectifiers, where P_{in} was calculated from the waveform measured with the oscilloscope. The non-biased rectifier could not operate in the region where P_{in} was less than -15dBm. On the other hand, the pre-biased and combined rectifiers with pre-bias voltage V_{bias} of 0.4 V successfully operated in the power region. In addition, the output voltage of the combined rectifier exceeded that of the pre-biased rectifier in the region where P_{in} was higher than-12 dBm. These experimental results qualitatively matched the simulation results shown in Fig. 7. However, the measured DC output voltages were about half the designed voltages. The reasons for these results were suggested by the matching frequency shift shown in Fig. 9. The amplitude at the input node of the rectifier cells might decrease in the experiment due to the resonance frequency shift. The break even P_{in}, at which the rectified DC power equaled the power consumption in the pulse generator, was around -20 dBm. More stringent optimization of the circuit parameters will produce a higher output voltage and decrease the break even RF input power. The dependence of the DC output voltage on the pre-bias voltage V_{bias} for the pre-biased rectifier is shown in Fig. 13, where P_{in} was -18 dBm. A bias of around 0.4 V produced the highest output voltages for both pre-biased and combined rectifiers. This optimum bias was slightly lower than the V_{th} of nMOS in the 0.18-μm CMOS process. For a bias voltage higher than the optimum value, increased backward leakage current deteriorated the rectification efficiency. This bias voltage approximately matched the peak voltage of the input RF signal for the non-biased rectifier at which point the DC output voltage rapidly increased.

Table I compares the fabricated rectifier with those reported in the literature. The low output voltage for our rectifier was mainly caused by the small number of stages compared to other rectifiers. The output voltage can be increased by optimizing the number of stages. An improved rectifier will be useful for recharging the battery. A power management circuit will be required for controlling the rectifier and battery.

5. Conclusion

We developed a 2.4 GHz pre-biased rectifier to improve the minimum detectable RF input power. Three

types of rectifiers consisting of LC matching circuits, 3-stage rectifier cells, and biasing circuits were designed and fabricated using a 0.18-μm mixed signal/RF CMOS process with one poly and six metal layers. The fabricated pre-biased rectifier operated in the region where the RF input power was less than -15 dBm, while the non-biased rectifier could not operate in this region. The parallel combination of pre-biased and non-biased rectifiers effectively solved the drawback of the pre-biased rectifier in the high RF input power region. More stringent optimization of the circuit parameters, especially the LC matching circuit and the number of rectifier stages, will produce a higher output voltage. A pre-biased CMOS rectifier with self-biasing will be a challenge for future work.

Acknowledgments

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Figure captions

Fig. 1 **a** One-stage differential-drive CMOS rectifier [8], **b** one-stage pre-biased rectifier, and **c** waveform for controlling switches

Fig. 2 Block diagram of pulse generator

Fig. 3 Circuit diagram of regulator

Fig. 4 Circuit diagram of level shifter

Fig. 5 Circuit diagram of designed rectifier

Fig. 6 Simulated output waveforms of pulse generator and pre-biased rectifier

Fig. 7 Comparison of simulated DC output voltage versus RF input power characteristics for non-biased, pre-biased, and combined rectifiers

Fig. 8 Microphotograph of the combined rectifier

Fig. 9 Measured return loss S_{11} for pre-biased rectifier along with designed S_{11}

Fig. 10 Measured waveforms of input RF signal and DC output for combined rectifier

Fig. 11 Measured pulse train for controlling switches

Fig. 12 Comparison of measured DC output voltage versus RF input power characteristics for non-biased, pre-biased, and combined rectifiers

Fig. 13 Measured DC output voltages for pre-biased and combined rectifiers as function of pre-bias voltage

Table I Comparison of fabricated rectifier with those reported in literature

Reference	This work	G. Papotto *et al*. 2011 [2]	T. Le *et al*. 2008 [1]	T. Umeda *et al*. 2006 [9]	U. Karthaus *et al*. 2003 [5]	
CMOS technology	0.18 μm	90 nm	0.25 μm	0.3 μm	0.5 μm	
Additional requirements	Auxiliary battery	Deep n-well	Fowler-Nordheim tunneling	Auxiliary battery	Schottky diode	
Operating frequency	2.4 GHz	915 MHz	906 MHz	950 MHz	869 MHz	2.45 GHz
Number of rectifier stages	3	17	36	6		
Output voltage at minimum RF P_{in}	V_o= 0.04 V R_L= 1 MΩ P_{in}= –21.1 dBm	V_o= 1.2 V R_L= 1 MΩ P_{in}= –18.83 dBm	V_o= 0.36 V R_L= 1.32 MΩ P_{in}= –21 dBm	V_o= 1.5 V I_o = 400 nA P_{in}= –14 dBm	V_o= 1.5 V I_o = 950 nA P_{in}= –21.1 dBm	V_o= 1.5 V R_L= 1 MΩ P_{in}= –13.5 dBm
Settling time	0.1 ms R_L= 1 MΩ C_L= 13 pF P_{in}= –19 dBm	156 ms R_L= 1 MΩ C_L= 47 nF P_{in}= –18.77 dBm	6.01 s R_L= 5 MΩ C_L= 10 μF P_{in}= –18 dBm			

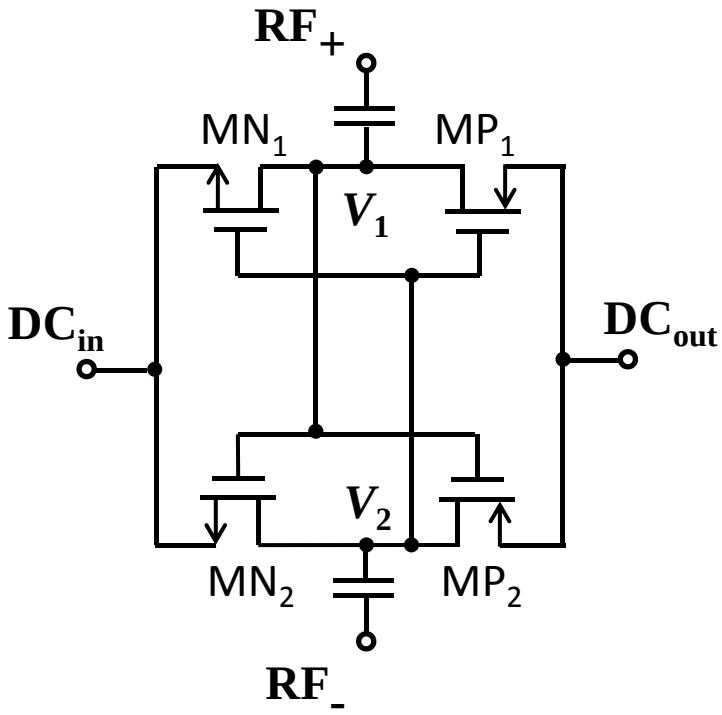

Fig. 1(a)

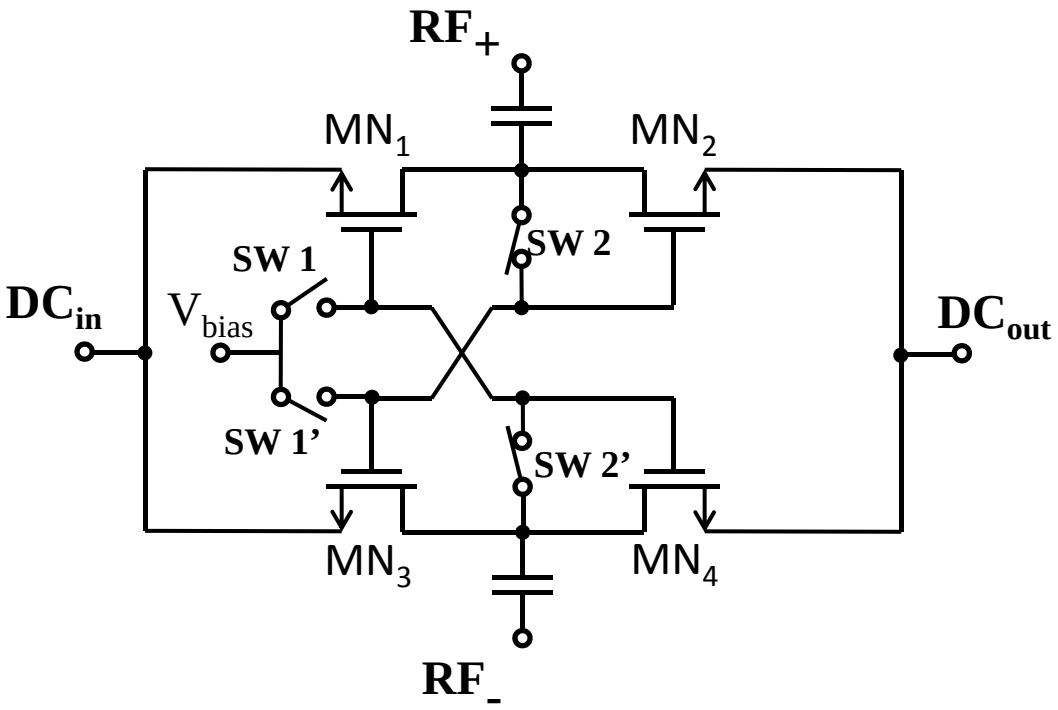

Fig. 1(b)

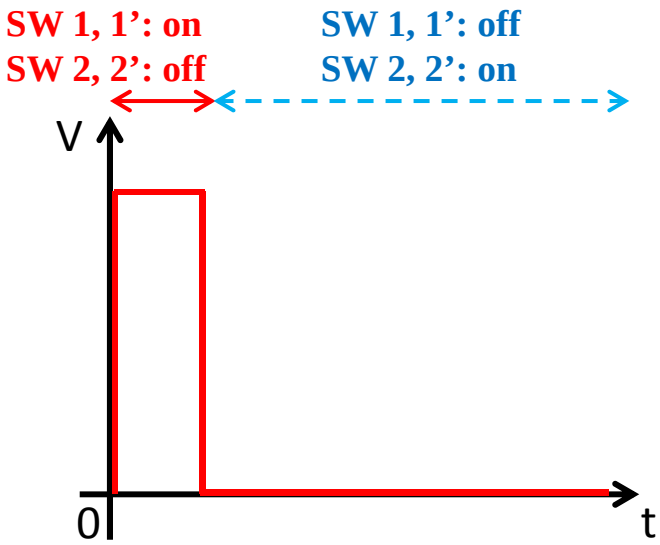

Fig. 1(c)

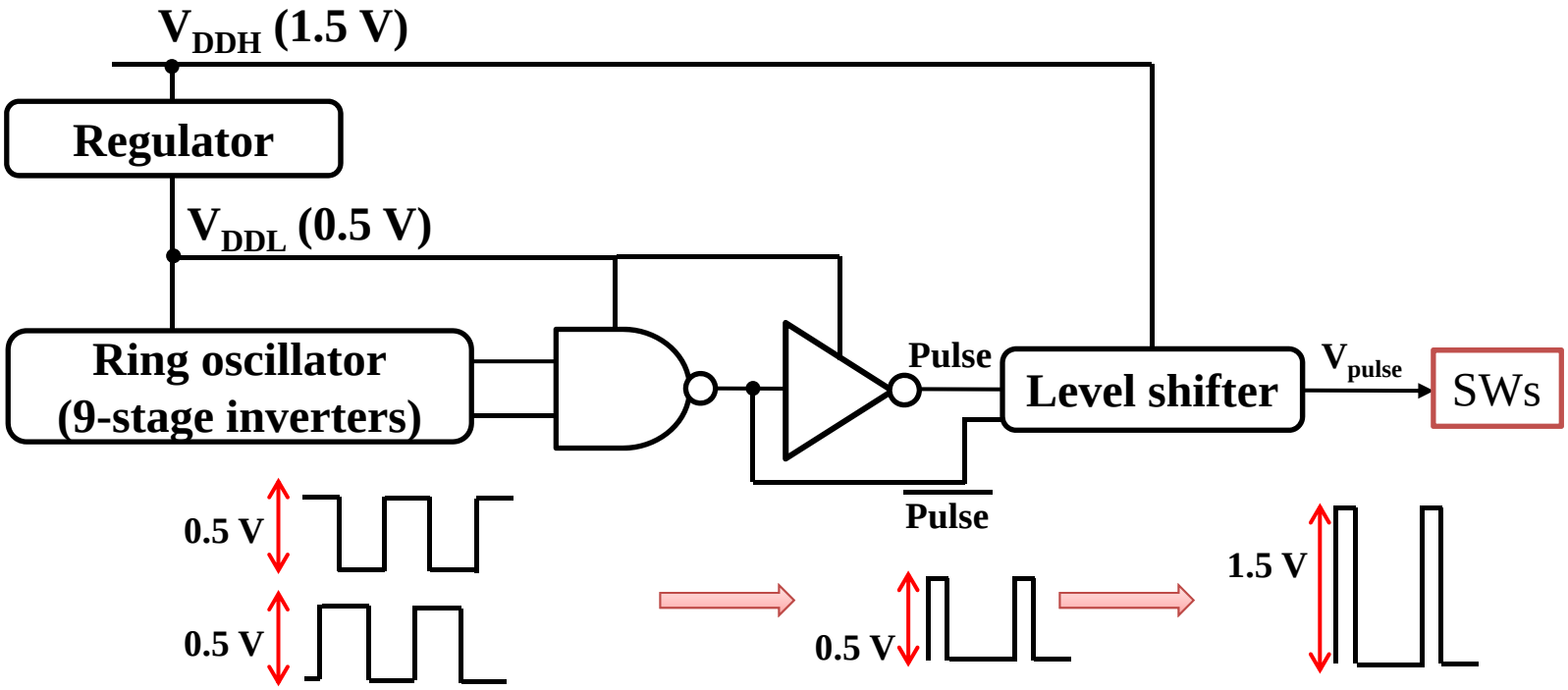
V_{DDH} (1.5 V)
Regulator
V_{DDL} (0.5 V)
Ring oscillator
(9-stage inverters)
Pulse
Level shifter
V_{pulse}
SWs
Pulse
0.5 V
0.5 V
0.5 V
1.5 V

Fig. 2

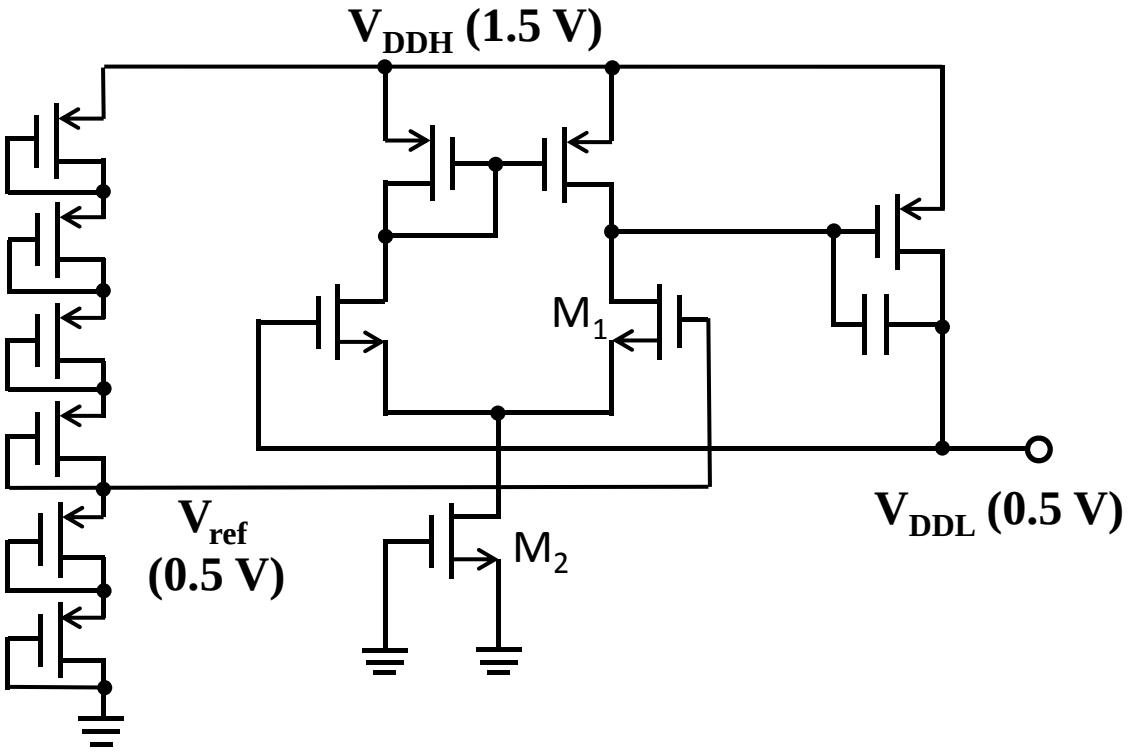

Fig. 3

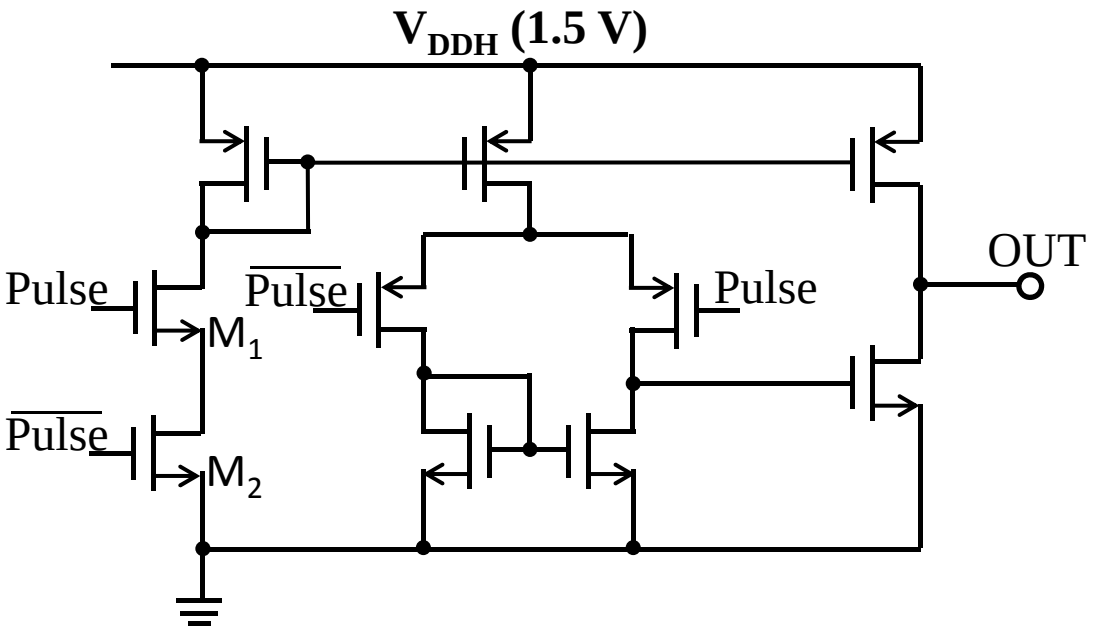
V_{DDH} (1.5 V)
OUT
Pulse
$\overline{\text{Pulse}}$
Pulse
M_1
$\overline{\text{Pulse}}$
M_2

Fig. 4

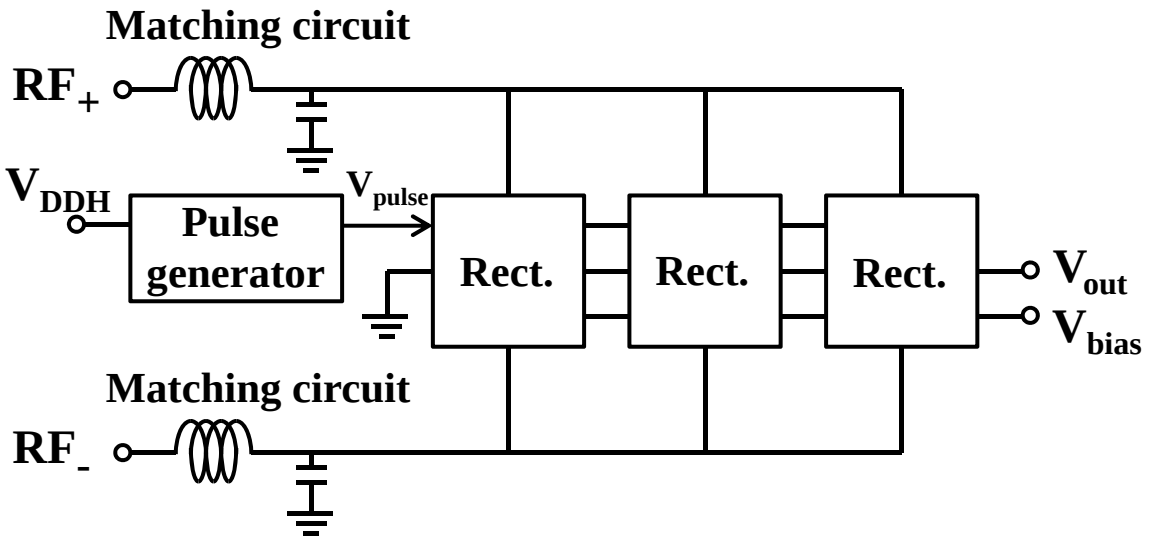
Matching circuit
RF+
VDDH
Pulse generator
Vpulse
Rect.
Rect.
Rect.
Vout
Vbias
Matching circuit
RF-

Fig. 5

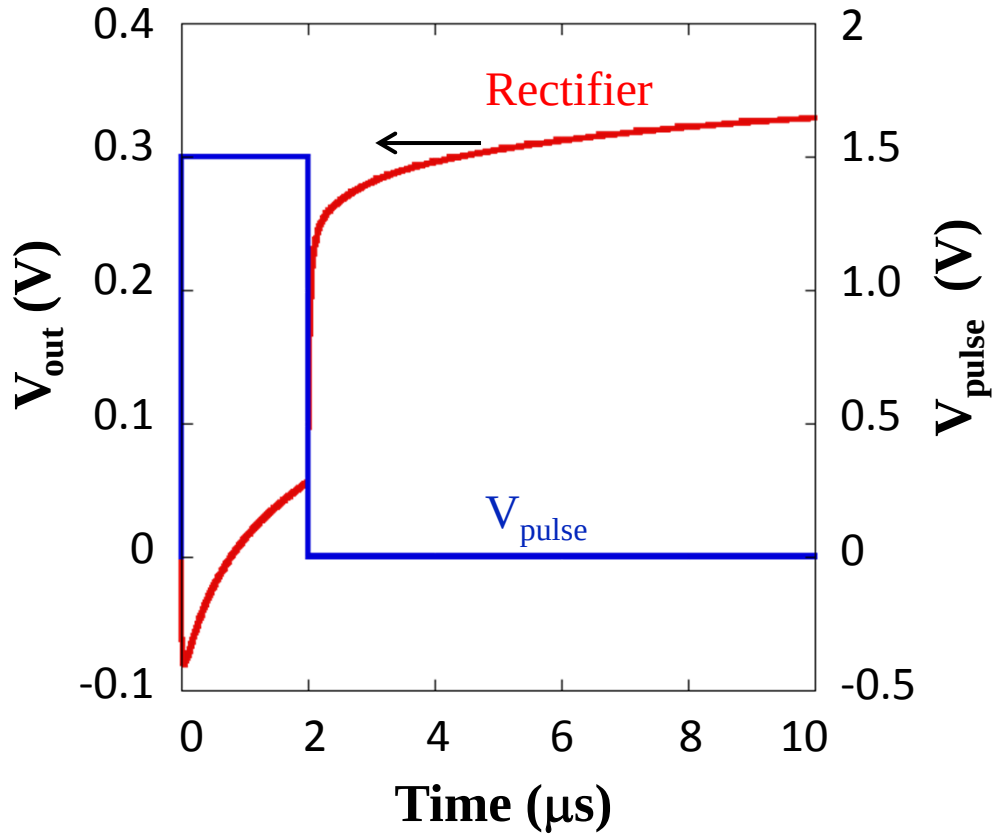
0.4
0.3
0.2
0.1
0
-0.1
2
1.5
1.0
0.5
0
-0.5
0
2
4
6
8
10
Rectifier
V_pulse
V_out (V)
V_pulse (V)
Time (μs)

Fig. 6

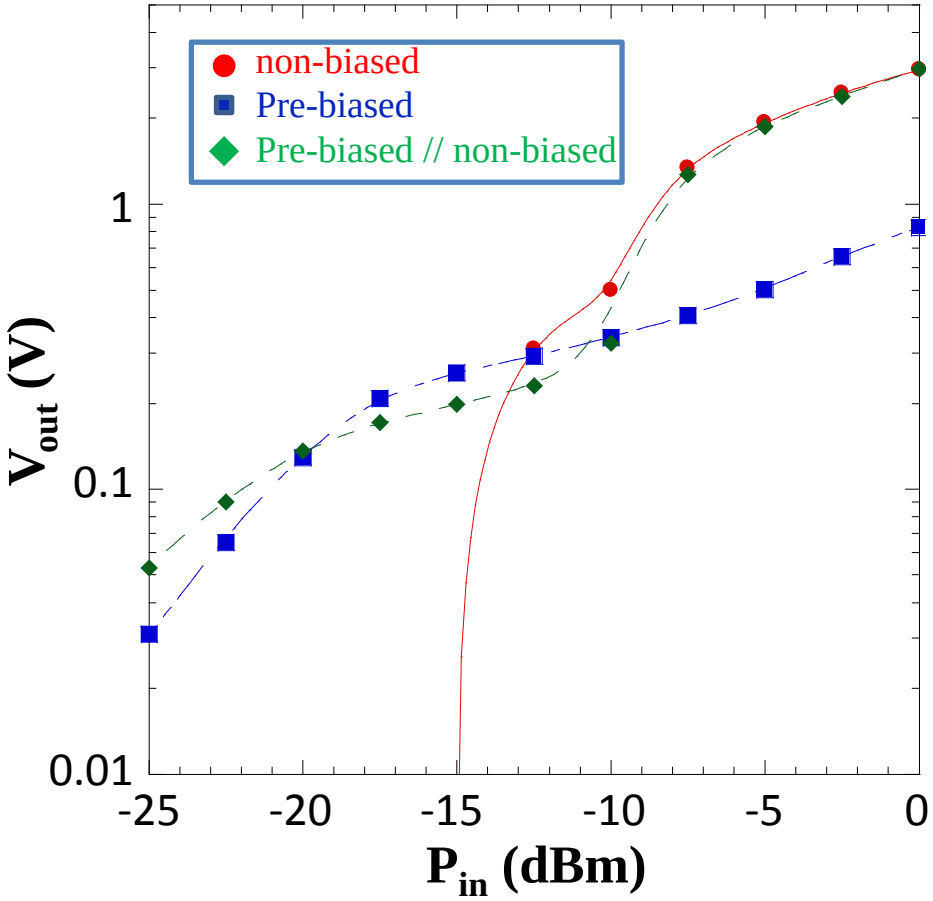
non-biased
Pre-biased
Pre-biased // non-biased
1
0.1
0.01
V_{out} (V)
-25
-20
-15
-10
-5
0
P_{in} (dBm)

Fig. 7

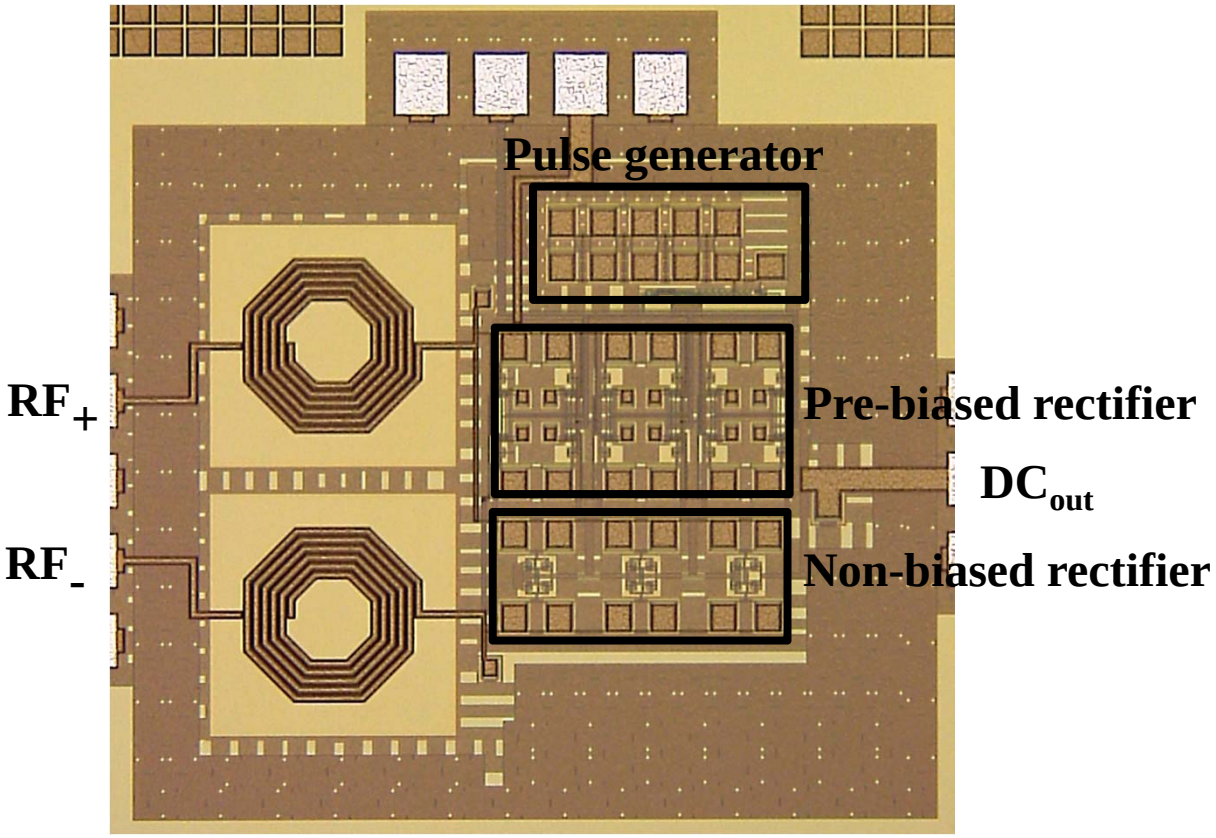
Pulse generator
RF+
Pre-biased rectifier
DCout
RF-
Non-biased rectifier

Fig. 8

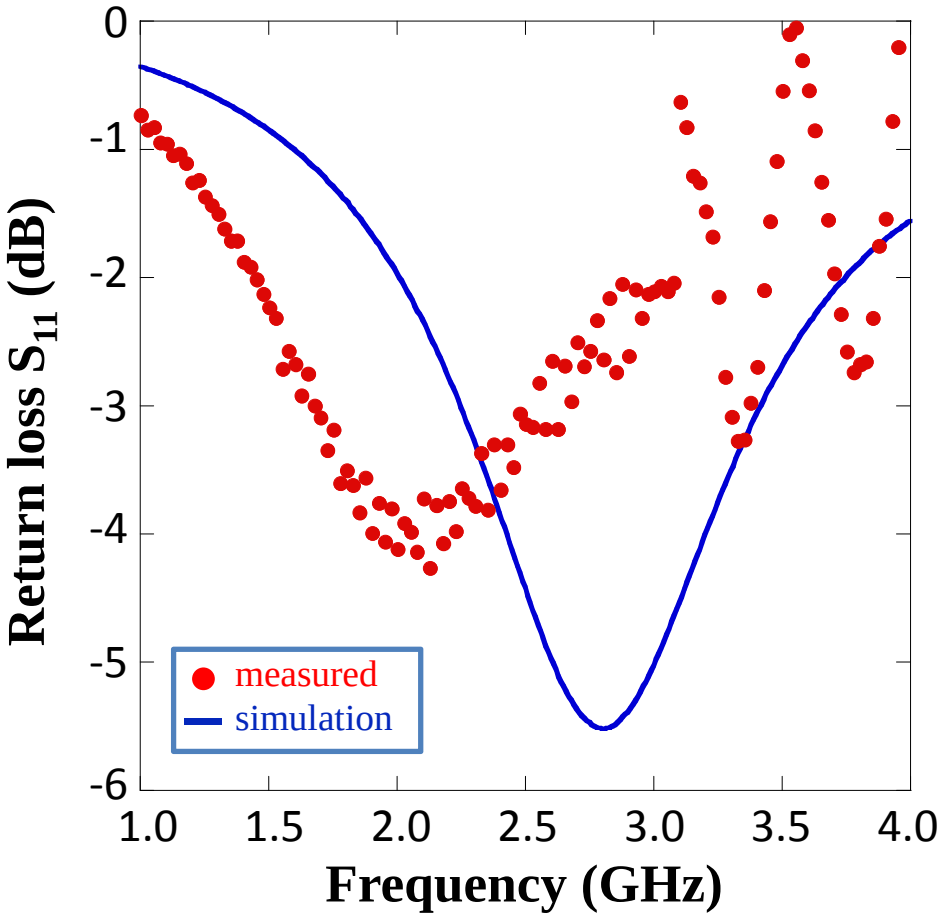
0
-1
-2
-3
-4
-5
-6
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Return loss S11 (dB)
Frequency (GHz)
measured
simulation

Fig. 9

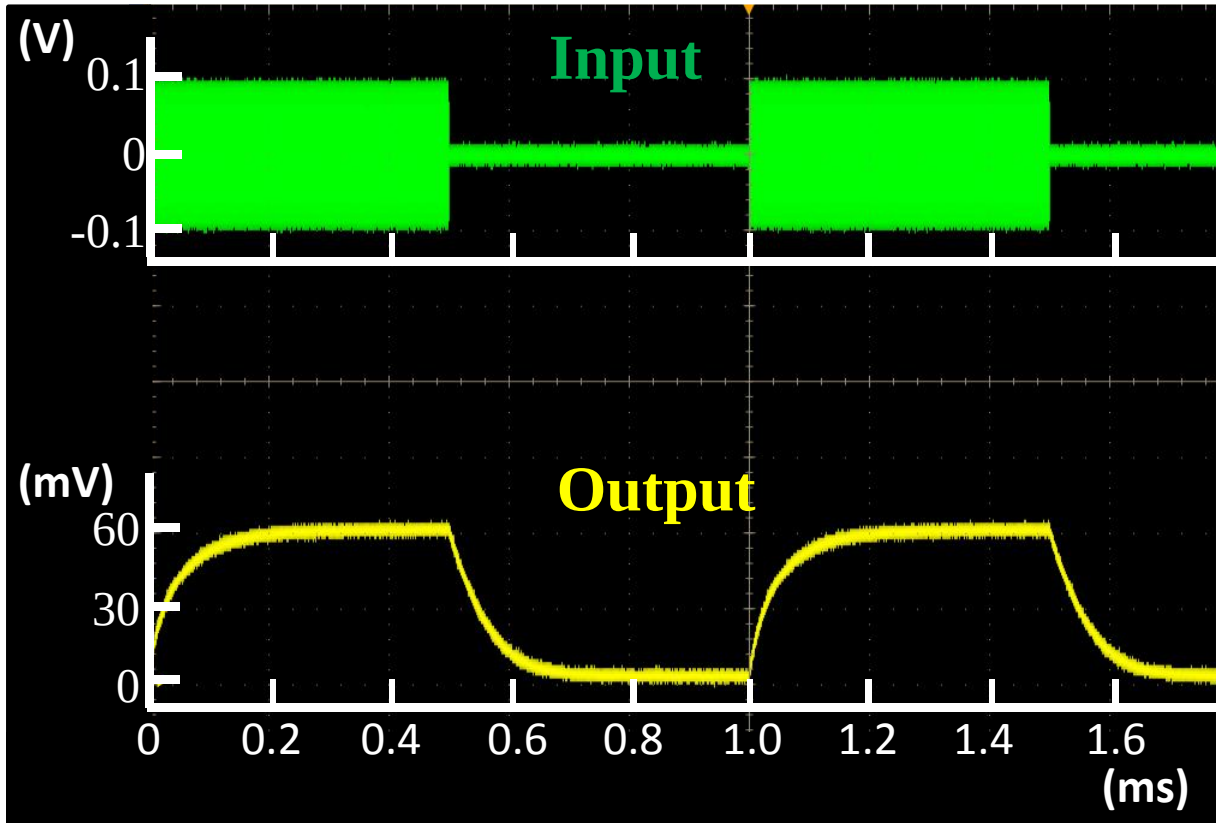

Fig. 10

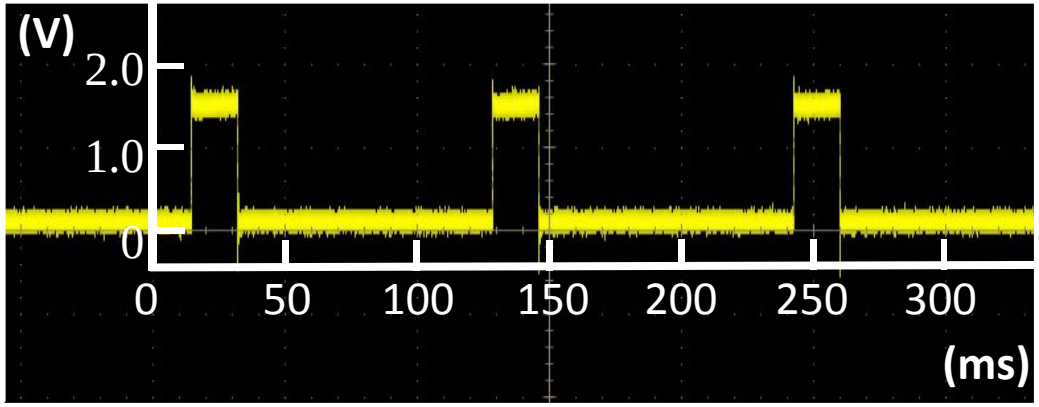

Fig. 11

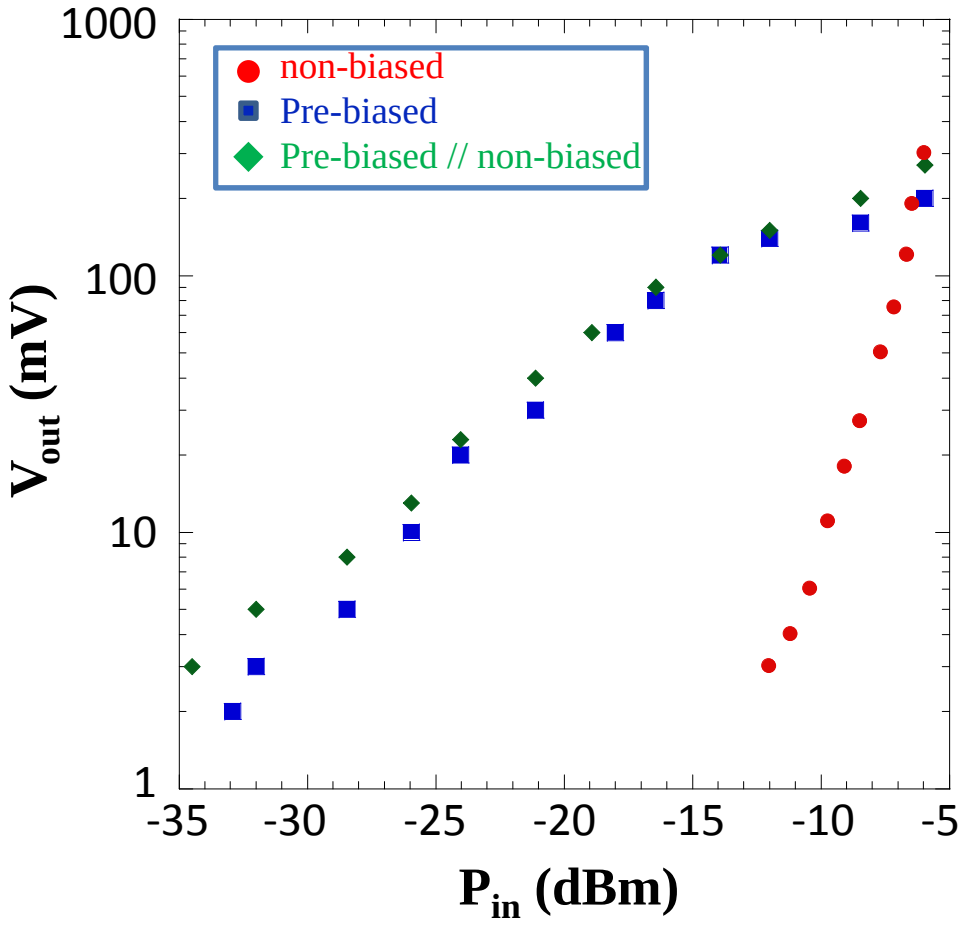
1000
100
10
1
non-biased
Pre-biased
Pre-biased // non-biased
V_{out} (mV)
-35
-30
-25
-20
-15
-10
-5
P_{in} (dBm)

Fig. 12

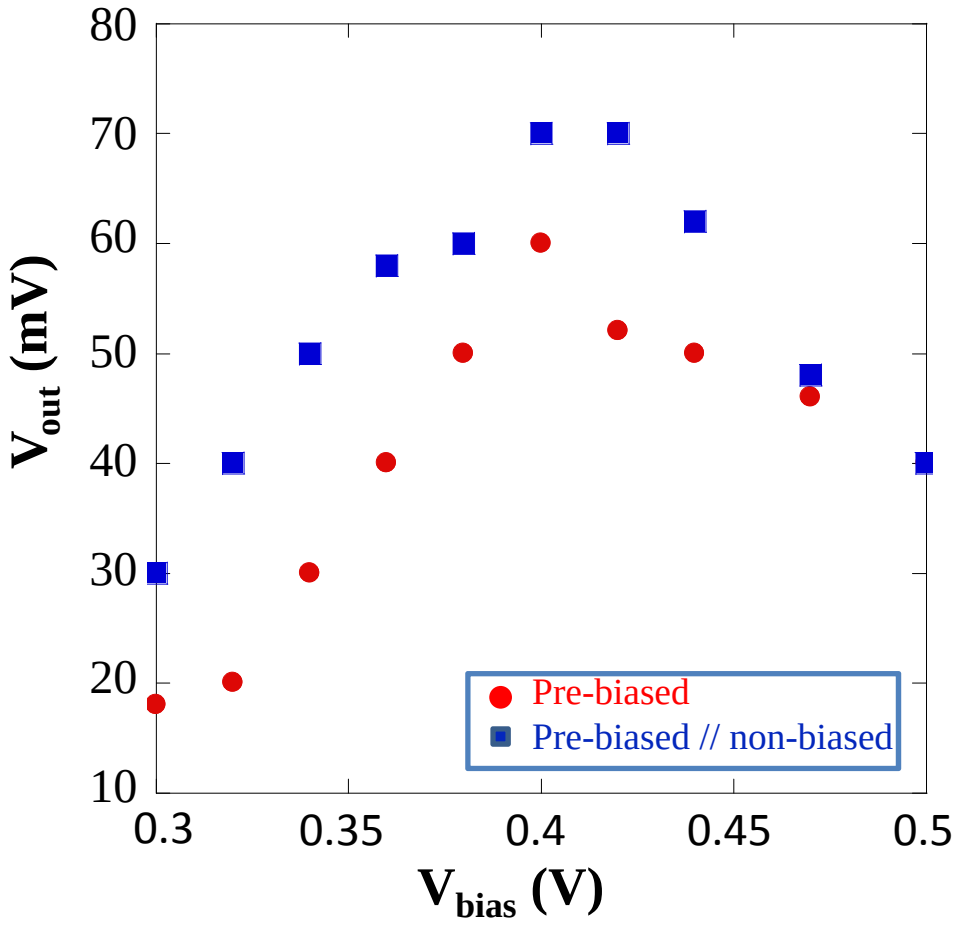
80
70
60
50
40
30
20
10
0.3
0.35
0.4
0.45
0.5
V_{out} (mV)
V_{bias} (V)
Pre-biased
Pre-biased // non-biased

Fig. 13