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博士論文

Bio-inspired Electronic Circuits and Stochastic Information Processing Systems exploiting Noise and Fluctuations
ゆらぎを利用する生物的な電子回路と確率的情報処理システムに関する研究

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Abstract

Current technological demands look for smaller, faster and more efficient systems. However, such demands are limited mainly by physical properties of devices (e.g. size of transistors, increase of electrical noise, etc.). At this point alternative solutions may have a response for such demands. The study of biological systems may offer a different perspective to fulfill such requirements. Biological structures have been optimized during millions of years of evolution resulting in power-efficient, fast and compact systems that are resilient against noisy and hostile environments. Although, no electrical system has been able to emulate any biological structure in their totality, neuromorphic systems have already proved to be efficient in many engineering applications.

This thesis is inspired specifically by how some biological structures use noise to improve determined tasks. The utilization of noise to enhance performance is a well-studied phenomenon and it is known as Stochastic Resonance (abbreviated as SR). Examples of SR in nature are found inside mechanoreceptors of some insects and fishes to detect weak signals from the environment, it is also observed in the human sensory system, as well as at molecular level to detect low-amplitude stimuli inside nervous system. And at system level, it is also involved in the evolution of human creativity, imagination and decision-making processes. At large-scale natural phenomena, SR has an effect in the ice age transitions.

The use of noise to improve certain tasks could seem counterintuitive from the electrical engineering point of view; however nature has given us many examples of the positive utilization of noise. Noise and fluctuations are inherently part of nature; and biological systems have already self-adapted to include external and internal fluctuations in their processing as a positive factor; in this sense, SR has been already exploited by biomedical engineers, just to mention some remarkable examples on the improvement of silicon cochlea, balance control systems and life-support ventilators, where the introduction of noise is a key factor for a more precise emulation of these artificial systems. Moreover, it has been also utilized in engineering systems such as electrical sensors to detect weak stimuli, signal amplification and noise-induced synchronization circuits.

In this thesis it is presented two main applications related with SR and its applications. The first case is based on the study on how electrical spikes are transmitted

along long axons inside the nervous systems. In this process, due to the variability of conductance among stages, the amplitude of electrical spikes may not be enough to excite next stage. However, it has been discovered that internal fluctuations inside node axons may enhance signal transmission. This idea could be mimicked by electrical systems to transmit signals efficiently in the presence of mismatches. Simulation results show that with the introduction of an optimal amount of noise, signal transmission is improved in the presence of mismatches.

The second part presents a novel application of the SR effect in the field of digital systems. Considering the problems that current devices are facing due to an increment of parameter variability (it may provoke malfunction of electrical chips) and demands for lowering their power, it is utilized noise to design logic gates with three main characteristics: low-power consumption, parameter-variability tolerance and a stable output regardless the introduction of noise. These gates were called stochastic resonance gates or simply SR gates. Simulations and experimental results show their effective performance on the recovery of logic functions in the presence of parameter variations of transistor (such as threshold voltage). However, due to their dependence on stochastic processes, their response presents an unpredictable delay. Therefore the most suitable application is found in the field of asynchronous circuits to design delay-insensitive circuits. Therefore the third part of this study is concentrated in the application of the SR gates to design asynchronous circuits. Synchronous circuit designs have been offering a robust solution for many years, however, considering the current challenges of VLSI circuits, asynchronous circuits may offer a better solution for designing faster, smaller and less power consuming circuits.

Finally, biological systems work inherently in noisy environments and during years of evolution they have self-adapt to these conditions, either by avoiding it or including it as a beneficial part. Towards the next generation of processors, to design more noise-resilient and efficient circuits, a positive collaboration of noise and fluctuations could be a necessary stage to achieve it.

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Chapter 1

Introduction

1.1 Background and motivation

With the continous miniaturization of conventional transistors, electrical chips have acquired smaller sizes with higher performance demands. However, as their physical dimensions have been shrunk, atomic dimensions have been reached (Fig. 1.1). At this point, many aspects of their performance are deteriorated [1–8].

Physical geometry patterns for lithography can not be printed reliably, resulting in severe degradation in device matching. It is predicted that in coming years, 14nm and 7nm technologies will be implemented with emerging devices; moreover, current oxide thickness is equivalent to 5 molecular layers of oxide, and by 2019 it is expected to be reduced by half. This gives as a results an increment on the leakage current due to the increase of oxide tunnel currents and decrease of threshold voltage. Leakage increment and gain decrement represent a challenge for designers, since they may seriously influence the functionality of the chip if the traditional designing methods are used. Moreover to fulfill the demands related with power reduction, supply and threshold voltage must be scaled also [9] (Fig. 1.2).

In the case of digital systems, new challenges are faced, such as energy-delay optimization, clock and power distribution. With demands for increasing performance, there is a dilemma between the necessity of an increment of power supply and the reduction of energy consumption.

In the case of analog systems, device matching became a key factor in the chip functionality, and more accurate models of devices are needed [11–13]. From the physical point of view there are many proposed solutions to integrate transistors at nanoscale to avoid problems such as the increment of tunneling current, de-

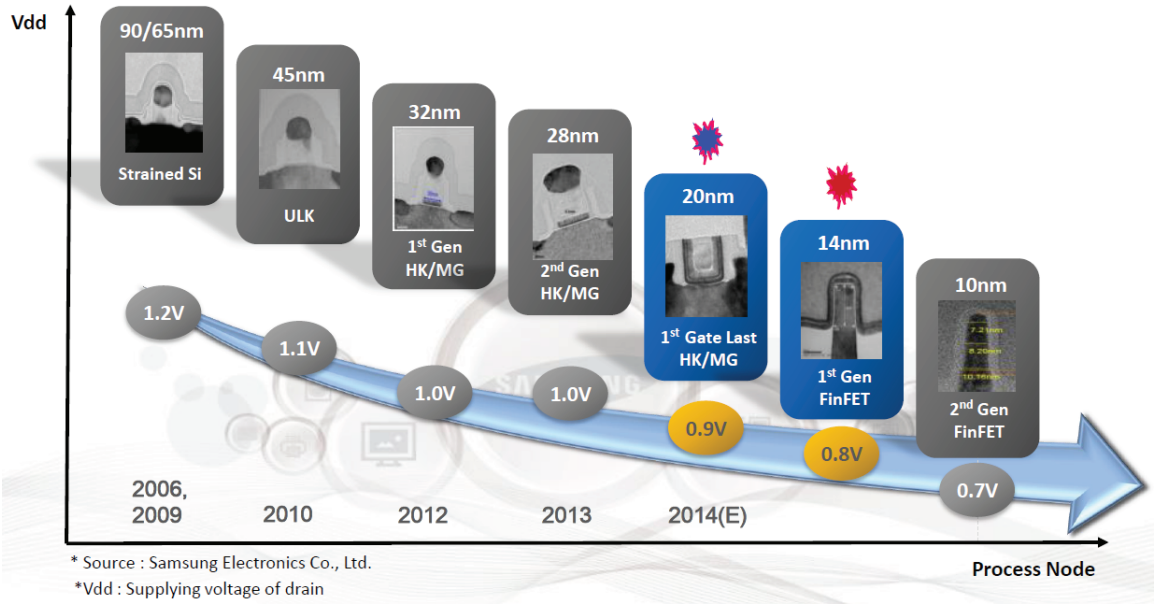


Figure 1.1: Roadmap of transistor miniaturization [10]

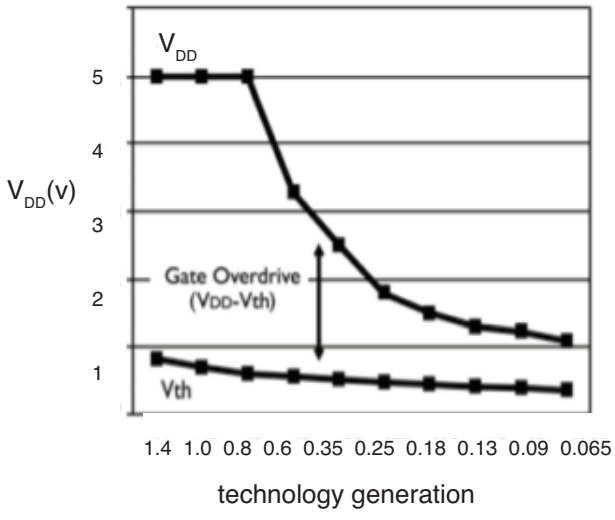


Figure 1.2: Trend of supply voltage and threshold voltage scaling.

creasing line delays and so on [14, 20]. Some of these solutions have already been integraed by using new materials in combination with the conventional CMOS technology.

There is also plenty of research done regarding promising devices that may substitute traditional MOS transistor and perform better at nanoscale sizes. Although the new 'holy grail' of electronics that could substitute MOS transistors definitively have not appeared yet, different alternatives have been explored, such as nanowire (NW) transistors [15], carbon nanotube field-effect transistors (CNTFETs) [16], graphene nano ribbon (GNR) transistor [17], single-electron transistors (SETs) [18], and quantum-dot cellular automata (QCA) [19], just to mention some examples.

From the design point of view, different strategies have been proposed as well, and these approaches are applied both to circuit and system levels [21]. Considering current state of nanoscale MOS transistors and emerging devices, demands for lowering power consumption and increasing robustness, in terms of parameter variabilities are presented in both cases, therefore our motivation is focused on studying different design strategies.

In this sense, many design strategies have been proposed out of traditional metdologies [22–24]. One of the most prominent areas is neuromorphic engineering. Nature designs have evolved during millions of years to produce compact, efficient and low-power consumption designs. Nature is inevitably surrounded by adverse environments, however nature designs seem to be resilient against this problem. How natural designs have accomplished to be successful into such a hostile environments? Many efforts have been made to answer this question. It is known that biological system are not deterministic systems but instead, they are the result of a combination of many factors (internal and external), that together produce complex systems governed by stochastic processes. It has been studied that fluctuations are responsible in many cases for assisting the realization of determined tasks, such as sensing and improving signal transmission in many biological structures. Therefore our motivations arise from the biological point of view.

The combination of nonlinear systems and the addition of weak periodic signals with additional noise is a well-studied phenomenon, known as Stochastic Resonance (SR). Among the applications of SR phenomena, electrical engineering is the key one. Although the use of noise to improve certain tasks is not part of the common sense knowledge among electrical engineers, it has been already demonstrated that noise-driven circuits can performer better in determined tasks.

This kind of circuits (as well as many new promising devices) are affected by the presence of delays that may provoke problems as clock skew and jitter in the case of synchronous circuits, that represents the key basis for most of current electrical chips; synchronous circuits are fast, robust and own a relatively easy design methodology. But as nano scales are reached, synchronization problems may arise. Therefore as a second motivation, the study of asynchronous circuits may be useful as an alternative to design delay-insensitive circuits.

1.2 Objectives and thesis organization

Following the motivations mentioned in previous paragraphs, the objectives of this thesis are based on the study on how noise is beneficial in some biological structures, and how these idea could be mapped in engineering to reduce power consumption and increase robustness against variabilities. Enclosed in this point, three main topics are explored:

1. Exploration on how biological structures, like nervous systems transmit spikes along long paths in the presence of conductance mismatches. Variations on conductances usually provoke spike transmission to be stopped. However, an interesting phenomenon occurs inside nodes, where the opening and closing channels generates fluctuations that actually help to improve spike propagation itself. Considering the problem of parameter variations, the addition of noise in an excitable system based in RLC circuits and their influence in electrical spike transmission is explored.

2. Design and implementation of transistor-based digital circuits based on Stochastic Resonance. With reduction of power supply and threshold voltages following integrated circuit miniaturization, designs are more sensitive to parameter variations. One key parameter for correct performance of circuits, is threshold voltage. To show how stochastic resonance could be beneficial, we proposed the design of digital logic gates based on threshold logic. These circuits must have the following characteristics:

- Transistor-based design: currently the main element of integrated circuits is the transistor; therefore these circuits could be easily implemented into chip.
- Mismatch-tolerant designs : one of the main purposes is the design of circuits that work properly independently of parameter variations, such as threshold voltage, therefore, there is an intentional standard deviation introduced to the nominal value of threshold voltages among transistors.
- Low-power consumption.
- Stable output regardless introduction of noise: In the case of bistable systems assisted by noise, although noise is fundamental to generate transitions correlated with a weak input signal, there are fluctuations present at the output due to the presence of noise. in this case we propose a configuration with a stable output.

3. According to previous subsection, nanoscale MOS transistors and emerging devices exhibit also delays as well. Systems governed by single clock, like in the case of synchronous circuits, may have synchronization problems; therefore the study of different alternative to design delay-insensitive circuits should be explored. Therefore, asynchronous circuits are proposed as a good candidate. Study of such systems an their implementation is conducted as follows:

   - Design of main elements to implement asynchronous circuits
   - Exploration of the most optimal protocols according to our necessities
   - Design and implementation of delay-insensitive, parameter-variation tolerant, low-power consumption circuits based on asynchronous design circuits as an application for noise-driven circuits.

Following the previous objectives, this thesis is outlined as follows:

Chapter 2 gives an introduction of the state of the art related with noise-driven phenomena in animal physiology, human perception system and brain. A brief description is provided along with examples suggesting that these biological structures have exploited noise through stochastic resonance phenomenon.

Moreover, it is analyzed the effect of stochastic resonance in bistable systems is analyzed from the mathematical point of view, and it is shown how noise assists transition between two stable states. Additionally, a brief descriptions of the different types of stochastic resonance are provided and it is explained how they have been applied in engineering.

Chapter 3 presents the state of the art of noise-assisted spike transmission is presented, it is known that internal noise, mainly generated by the random opening and closing of ion channels, is the responsible for enhancing the response of spike transmission in the presence of conductance variations. In a deterministic model, spike transmission would be impossible if low conductance values are presented; however, internal fluctuations assist spike transition. In this chapter, FitzHugh-Nagumo is electrically modeled and its characteristics are studied. Here, an specific case of noise-assisted spike transmission is studied, where amplitude of noise is proportional to the amplitude of the spikes. The benefits of noise are demonstrated through circuit simulation.

Chapter 4 is focused on the circuit design of novel logic gates driven by noise (called SR logic gates). Based on threshold logic, a hysteresis differential amplifier is utilized to design logic gates that have three main advantages: parameter variation tolerance (threshold voltage variations), low-power consumption and stable response even in the presence of noise. It is demonstrated that the beneficial role of noise is a key factor to recover logic functions under the presence of threshold voltage variations. Moreover, the presence of stochastic resonance phenomenon is demonstrated mathematically. Simulation and experimental results are presented to evaluate the performance of the SR logic gates.

Chapter 5 presents possible applications of SR gates may be found in the field of asynchronous circuit design. SR gates has a dependence on stochastic processes and therefore their response exhibits a random delay. In the case of synchronous circuits, a central clock governs synchronization among stages, when delays are presented, synchronization problems may arise. One possible solution is the exploration of asynchronous circuits that offer many advantages over synchronous circuits: delay-insensitive circuits, lower power consumption and increase of pro-

cessing speed; however this filed has nor been explored completely due to the lack of design and testing methodologies. Therefore this chapter offers a brief overview of basic theory of asynchronous circuits and concludes with the design of the basic elements of asynchronous circuits (based on the SR gates); it also includes design and circuit implementation of asynchronous pipelines (the backbone to design more complex asynchronous circuits) based on the SR logic gates. It is demonstrated through simulation and experimental results that delay-insensitive circuits based on the SR gates are achieved.

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Chapter 2

Biological-inspired noise-driven phenomena and computing

2.1 Noise in nature

In this chapter, a brief review of the influence of fluctuations in biological systems is explored. Further, a formal definition of noise-driven phenomena is presented and some examples are provided. Following sections represent the theoretical basis for this thesis.

2.1.1 Influence of noise on animal physiology

Nature inherently is a noisy environment, therefore many biological systems have learnt to adapt to such conditions. The first studies regarding how some biological structures use noise started with the study of the relationship between noise and and sensory neurons, since they are threshold systems that intrinsically generate noise [1]. There are other interesting studies, for example, the tail of a swimming predator, the crayfish possesses mechanoreceptors in its tail that are unable to detect weak signals without noise assistance [2]. In the same way, the sensory system of crickets can not detect weak signals coming from predators without assistance of environmental noise [3]. One of the latest experiments was conducted regarding the behavior of paddlefishes [4], that actually find its prey through emitted weak signals. It has been shown that, with the assistance of environmental noise, the paddlefish is able to find its prey faster rather than in the absence of noise (Fig. 2.1).

Previous examples show how noise-assisted tasks are exhibited at macrosclae

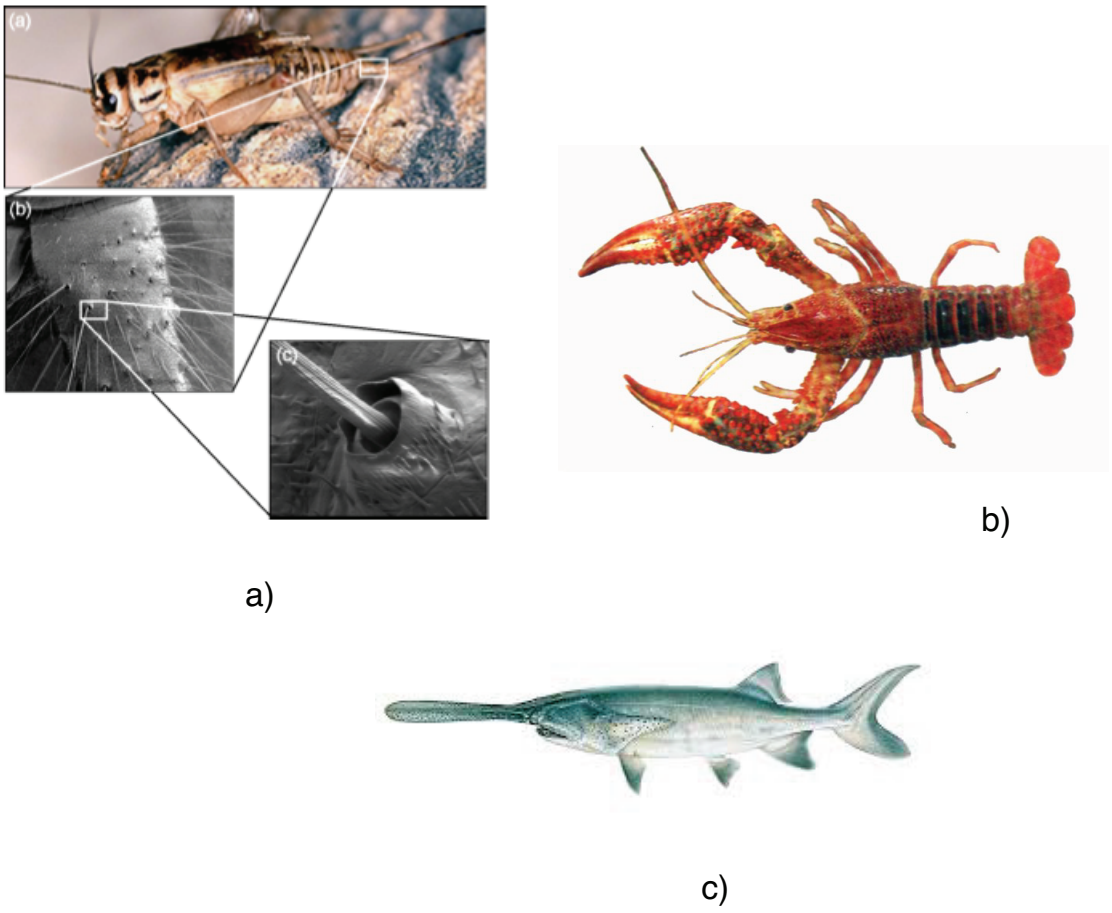


Figure 2.1: Examples of beneficial role of noise in animal kingdom: (a) cricket's hair, (b) crayfish and (c) paddlefish's sensory systems

biological systems. At cellular level SR effect has been also observed. It is speculated that SR effect has its origin in the ion channels of receptor cells membrane; it has been demonstrated through an artificial model that SR is exhibited [5]. The question that stills needs to be answered is whether SR is a phenomenon observed on a big scale level or it is also possible to be observed in a single ion channel. This result would have a great relevance, in fields as single-molecular devices.

2.1.2 Influence of noise on human perception

- Human vision
  An experiment was done consisting on a photo by adding noise with a

particular variance several times to create successive frames. This was done for different levels of noise variance, and a particularly optimal level was found for discerning the appearance of the image in the photo. Similar experiments also demonstrated an increased level of contrast sensitivity to sine wave gratings [6].

- Tactility
  Human subjects who undergo mechanical stimulation of a fingertip are able to detect a subthreshold impulse signal in the presence of a noisy mechanical vibration. The percentage of correct detections of the presence of the signal was maximized for a particular value of noise [7].

- Audition
  The auditory intensity detection thresholds of a number of human subjects were tested in the presence of noise. The subjects include four people with normal hearing, two with cochlear implants and one with an auditory brainstem implant [8]. The normal subjects were presented with two sound samples, one with a pure tone plus white noise and one with just white noise, and asked which one contained the pure tone. The level of noise which optimized the detection threshold in all four subjects was found to be between -15 and -20 dB relative to the pure tone, showing evidence of noise-assisted tasks in normal human hearing. A similar test in the subjects with cochlear implants only found improved detection thresholds for pure tones below 300 Hz, while improvements were found at frequencies greater than 60 Hz in the brainstem implant subject. The reason for the limited range of resonance effects are unknown. Additionally, the addition of noise to cochlear implant signals improved the threshold for frequency discrimination. In this work it is suggested that some type of white noise addition to cochlear implant signals could improve the utility of such devices.

2.1.3 Influence of noise on human brain

There are many studies related with noise in the brain, these studies are mainly divided at physiological and higher cognitive levels.

At cognitive level, it has been shown that the relatively random spiking times of neurons could represent a source of noise that is involved in the generation of a probabilistic behavior that can prevent deadlock and facilitate for example, to decision-making processes [9]. Moreover, stochastic neurodynamical effects are

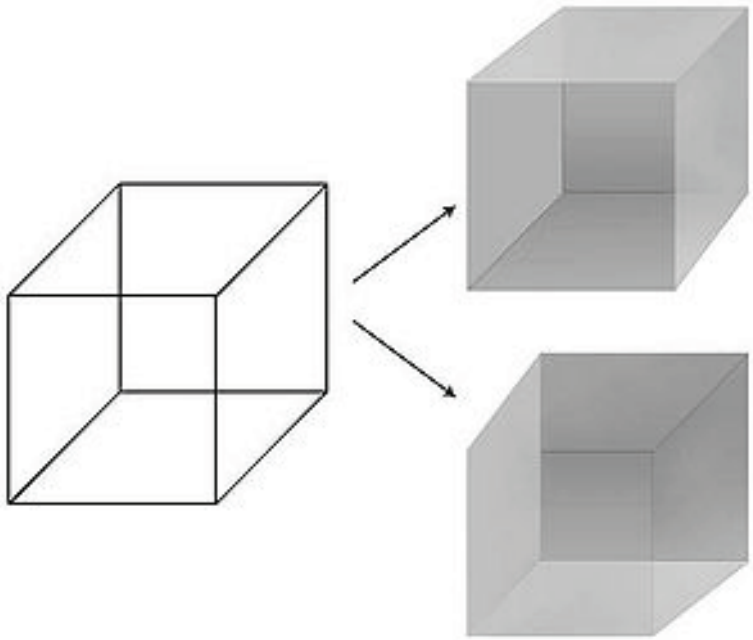


Figure 2.2: Necker cube, an example of a perceptual bistable process

important not only for decision-making processes, but also for memory recall, short-term memory, and attention.

Human brain does not work with deterministic computations, it is not a noiseless system but instead relies on stochastic dynamics. In the case of short term memory, spontaneous spikes can lead to a faster recovery of a memory. Another interesting case, is the perceptual decision-making, where perceptions can change spontaneously from one interpretation to another. A classical example is the Necker cube (Fig. 2.2), a perceptual bistable process, where two different states could be perceived. The hypothesis is that switching between multistable states is due to statical fluctuations on the network. This example provides an interesting demonstration on how noise can play a role for flipping from one attractor to another inside human brain. This experiment was already proved to be at [10], where an associative network with two stable states was trained so that both states have the same probability to be the perceived states; under the influence of a periodic weak force, SR effect is manifested.

There are another advantageous processes that arise due to the stochastic processes inside brain, just to mention some examples, creativity, where it has been speculated that without noise, the trajectory through a set of thoughts would tend to follow the same furrow each time, however under the influence of

random spiking, these trajectories would be different each time, facilitating the creative thinking. More examples are found inside unpredictable behaviors, that represents an advantage when, for example, a prey is escaping from a predator.

2.2 Stochastic resonance

In this section, a formal definition of noise-driven phenomenon is presented.

2.2.1 Definition

Stochastic resonance (SR) was first proposed to explain the periodic changes on glacial ages [11, 12]. It is known that climate processes are attained to several factors that generate variability. It was observed a periodicity of 10^5 years on ice ages and it was explained as a results of internal and external perturbations that affect earth climate and give rise to extreme climate changes. This phenomenon was called stochastic resonance and since then, there has been a great interest to study this phenomenon among physicists and mathematicians; therefore the definition of SR has been evolved during the last decades, but in general words it describes a phenomenon that involves the addition of an optimal amount of noise to a nonlinear system [13, 14], where its output quality is better than in the absence of noise, so it must be true that

$$performance(noise + nonlinear system) > performance(nonlinearity)$$

The classical graphical description of SR effect is depicted in Fig. 2.3, where the ball represents the state of a system trapped in a well of a double-well potential function; under the influence of a weak periodic signal, the ball would be trapped inside the well, however, under the influence of an external noise input, the ball could escape from one well to the other one. It has been shown that these escape events are not random, but there is correlation between the weak input signal and the escape rates. However, noise intensity should be tuned at its optimun, if the intensity of noise is increased, this correlation decreases; however too much noise could deteriorate the coherence of the output signal.

The term "stochastic resonance" was proposed because is involved with stochastic processes, and originally the graph signal-to-noise ratio was used as a performance measurement against noise intensity; the graph actually resembles the plot of frequency-dependent systems where there is a pick at a determined res-

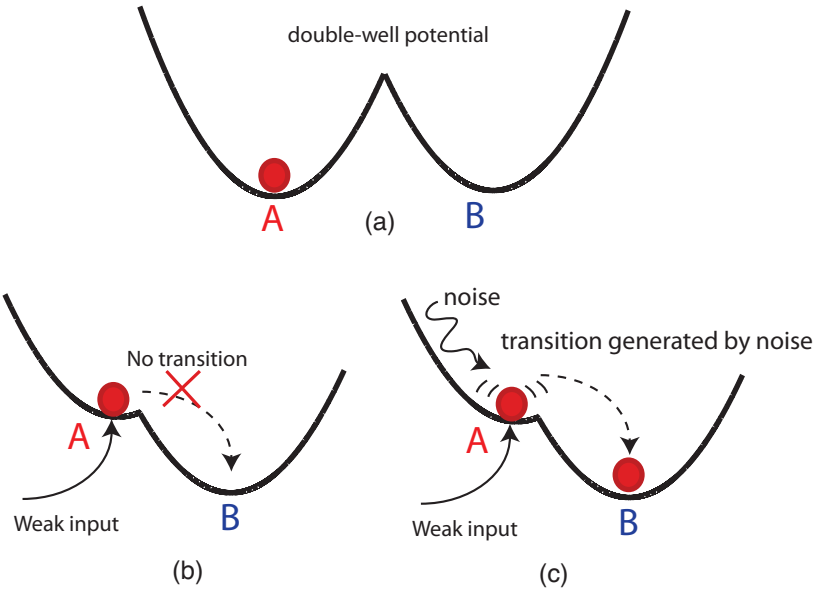


Figure 2.3: Particle in a double-well potential under the influence of noise: (a) system in equilibrium, (b) system under the influence of a weak-periodic external signal (no transition), and (c) noise-assisted transition

onant frequency, thus the term "resonance" was used to name this phenomenon erroneously.

Further SR gained attention among biologist since it was discovered that some biological structures (including human brain), utilizes internal and external fluctuations to improve determined tasks [15, 16].

2.2.2 Stochastic resonance in bistable systems

To understand the SR phenomenon, it is necessary to analyze it form the mathematical point of view. In the case of bistable systems, they posses an energy potential function with two minima (double-well potential function), which is represented in Fig. 2.3a. during equilibrium both wells have the same potential energy. However when an external force is introduced, the potential function of the wells is modified. If the external force is big enough, it may provoke a change on the current state. However, if this input has a low amplitude, it may not be enough to switch states (Fig. 2.3b); in this case, the introduction of a noisy input may assist these transitions (Fig. 2.3c).

Let's analyze a generic model of a overdamped motion of a Brownian particle in a bistable potential in the presence of noise and a periodic weak input, described

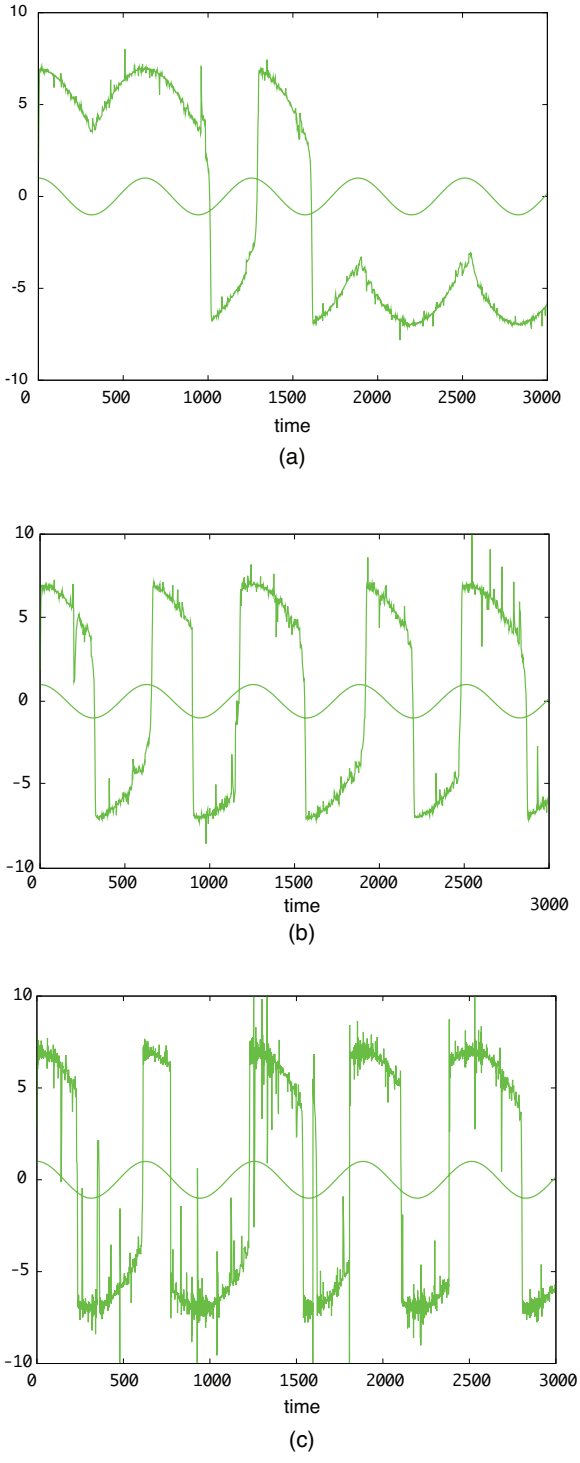


Figure 2.4: Noise-assisted transition in a double-well potential: (a) low intensity noise (b) optimal amount of noise (c) high amplitude noise

by:

$$x(t) = -V(x) + Acos\omega_s t + \xi(t) \tag{2.1}$$

where A represents the amplitude of the period input signal and $\xi(t)$ represents a zero-mean Gaussian white noise.

Here, the potential function is given by:

$$U(x) = -\frac{1}{2}x^2 + \frac{1}{4}x^4 \tag{2.2}$$

Where minimum points are found at $x = -1$, $x = 1$, and it has one saddle point at $x = 0$.

To show the SR effect, the previous system was simulated using the Euler-Maruyama method. Fig. 2.4a shows the periodic input signal in the absence of noise. Fig. 2.4b shows the same system under the presence of noise. With the introduction of a low amplitude intensity noise, it may no be enough to excite the systems, however under the presence of an optimal amount of noise, a periodic response is observed. However, higher amplitude noise may provoke the system to be unstable (Fig. 2.4c).

There are many methods to evaluate the presence of SR phenomenon, but the classical method is through the graph SNR, where an optimal performance is observed at a certain amount of noise (Fig. 2.5).

2.2.3 Stochastic resonance in non-dynamical systems

The simplest system that shows SR effect consists of a non-dynamical system with a threshold and a periodic weak signal as input [17]. Without noise this signal will never cross the threshold, however when noise is introduced a series of spike-like output signals are generated (Fig. 2.6).

2.2.4 Suprathreshold stochastic resonance

This is a special type of SR, and it happens where there is a set of excitable circuits sharing same input x [18]. These systems have the characteristic of having one threshold θ. In this case, independent white noise sources $\eta_N(t)$ are applied individually to each circuit, enhancing their response y (Fig. 2.7). Usually the performance measurement is given by the typical measurements of mutual information.

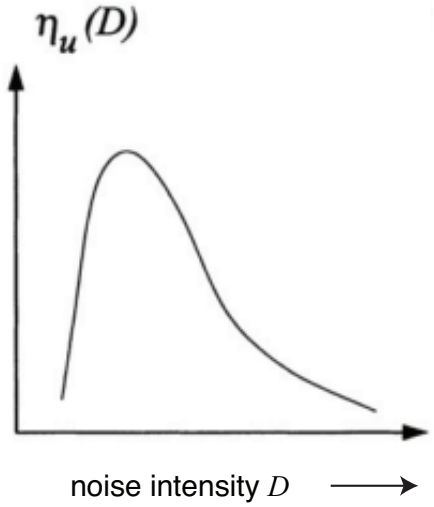


Figure 2.5: Characteristic curve Signal to Noise Ratio (SNR) exhibiting SR

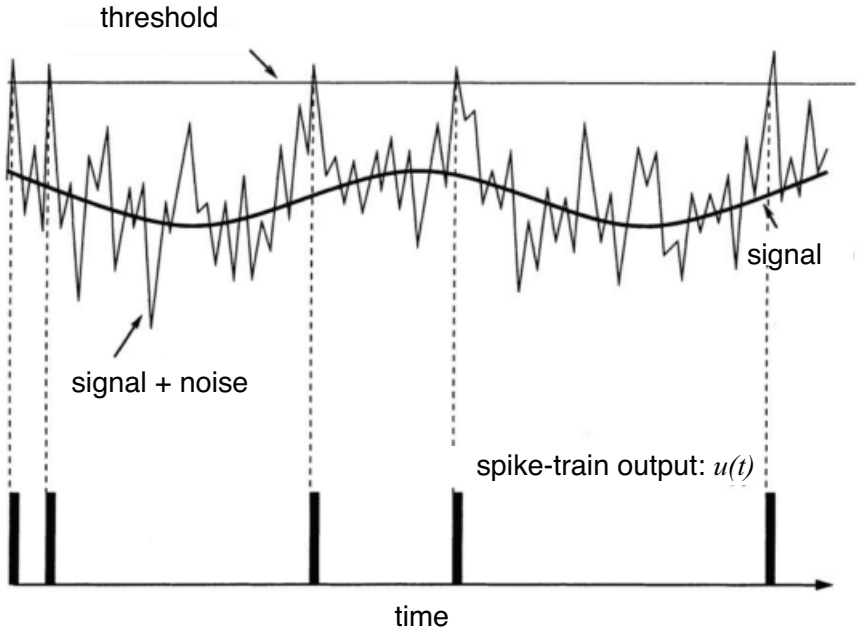


Figure 2.6: Non-dynamical SR

2.2.5 Applications of stochastic resonance

SR effect also gained attention in engineering field. In the case of electrical engineering, noise always has been considered as a signal with negative effects and

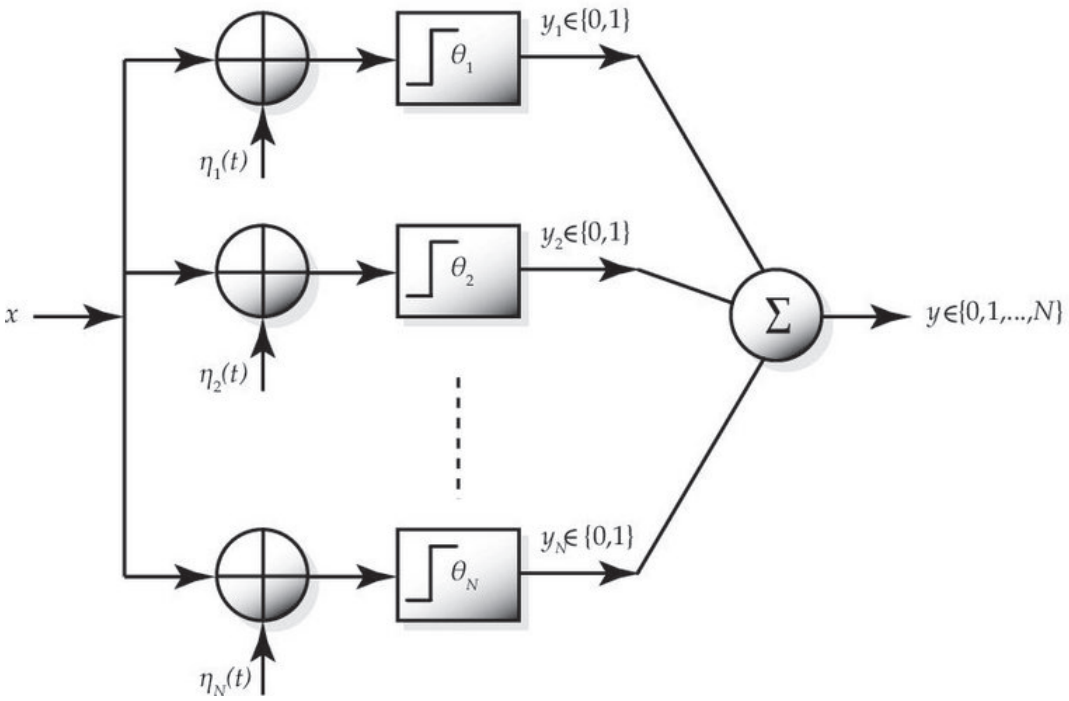


Figure 2.7: Suprathreshold SR system

thus the idea of a positive utilization of noise seems counterintuitive. However there have been a lot of studies related with SR effect and its applications in engineering. Just to mention the most remarkable applications in the field of biomedical engineering: Suprathreshold stochastic resonance was applied to the improvement of cochlear implants, the quality of these implants is still not optimal, and patients are still unable to distinguish sounds in noisy environments as well as distinguish musical instruments inside a pice of classical music. The idea here is that such artificial implants lack natural sensory hair cells that are used by human ear to encode sounds. These organelles posses inherent randomness, so the idea here is that with the introduction of artificial noise in artificial cochleas may help to improve hearing [19]. SR also found applications in the improvement of life-supported ventilators, where additional noise may be positive to emulate natural fluctuations in the respiratory system [20]. Moreover, SR effect has been used for improving the tactile sensation for patients having underthreshold tactile sensitivity [21]. Another application is found in the baroreflex, where a negative feedback is the responsible for controling blood pressure, by decreasing or increasing the heart rate; this compensation was found to be opti-

mized by the addition of noise to arterial blood pressure receptor [22]. Balance control in patients with diabetes or affected by a stroke, can be also optimized through the use of noise [23, 24].

Also, the phenomenon of SR has been also observed at bistable devices, such as tunnel diodes [25], optical systems, as in the case ring lasers [26]and magnetic systems [27]. Quantum phenomena also have been studied [28] and climate phenomenon and social-ill models [29, 30]. At electrical system level, SR has application in image filtering derived by the theory of non-dynamical SR; also it has been demonstrated to play a role on circuit synchronization, where the introduction of noise enhance synchronization on a network of oscillators [31]. Suprathreshold SR has applications in the design of analog to digital converters [32], as well as in the design of low-power digital accelerometers [33] and delta-sigma modulators [34]. At device level, SR has been observed at molecular devices [35].

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Chapter 3

Spike transmission assisted by noise

3.1 Biological background: spike transmission in nervous system

As an example of noise assisted tasks, we can find the improvement of the ability to detect weak signals in biological systems [1–5]. Several studies have demonstrated that the nervous system contains several sources of noise and research in this field has demonstrated that the nervous system has adopted these noise sources to improve its efficiency as it was reviewed in the previous chapter. Following this background, this chapter is based on the study of the technique used by myelinated axons to transmit spikes [6], based on the stochastic resonance (SR) effect. This is in order to emulate its dynamics to assist weak signal propagation in transmission lines with high values of internodal resistors. Correct information transmission is a key factor in active transmission lines [7]. An active transmission line in non-uniform medium is modeled as a chain of connected active compartments (Fig. 3.1), which are connected each other through resistive impedances (internodal resistances). The value of internodal resistances can fluctuate and sometimes acquire high values, provoking a loss of information. The influence of independent noise on improving spike transmission in nervous system, has been already investigated [8–13].

However, there is a characteristic that have not yet taken on account and it is the role of dynamic noise. Therefore, the main point of this section is to consider the dependence of noise on the membrane potential amplitude, where

a similar electrical model of a transmission line is found in myelinated axons. This characteristic allows a proper spike transmission, discriminating weak signals from parasitic fluctuations, that could generate a fake response. Inspired by this idea, we investigate how noise enhances the performance of spike transmission in serially-connected electrically circuits receiving subthreshold inputs.

Exploring how these biological structures are able to transmit information even in the presence of low conductances, may help to improve information transmission in electrical systems, having as a main point of this chapter, exploiting dynamical noise on spike transmission.

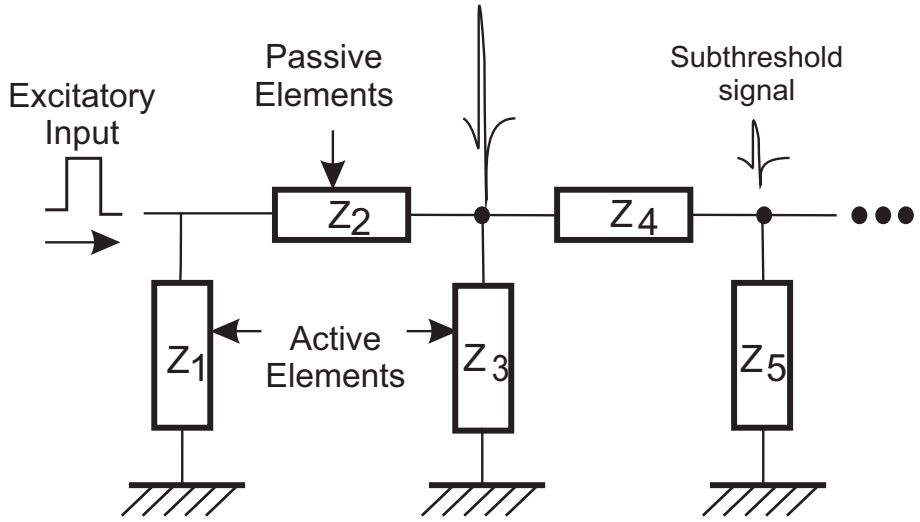


Figure 3.1: Basic model of transmission line in non-uniform medium.

The following section will review briefly the biological background of spike transmission as well as the theory of excitable models (used to emulate biological spike transmission).

3.2 Excitable models

Excitable systems are observed in a wide range of natural systems and they can be defined as monostable systems, where if the system is unperturbed, it will remain in the rest state, but once it is triggered by a strong perturbation, the system is moved to an excited state (or firing). In the nervous system, myelinated axons serve to transmit spikes in an excitable medium. Myelinated axons represent a very efficient biological technique to transmit spikes along large axons. This kind of axons are divided into segments separated each other through high-density ion

channel regions, known as the Ranvier nodes (Fig. 3.2), which actually can be modeled electrically as active components. On the other hand, low-density ion channel segments can be modeled as passive components. In that way, a myelinated axon is electrically represented as active elements connected each other through passive segments. A fact about myelinated axons is that the internodal resistances associated to the low density ion channel regions, are not the same for every segment (mainly due to variations on dimensions along the axon), so that in the same axon, we can find segments that possess a high resistivity, as well as segments with low resistivity. In the case of high resistivity segments, spike transmission is stopped. However, it has been demonstrated that although high resistance values exist, spike transmission is successful; so the question is how this biological design is able to transmit spikes successfully? The answer comes from the intrinsic noise generated by the opening and closing ion channels inside the Ranvier nodes. This uncorrelated noise, contributes with the improvement of spike transmission rate. Information transmission with noise assistance has been extensively studied in bistable systems and in electrical systems.

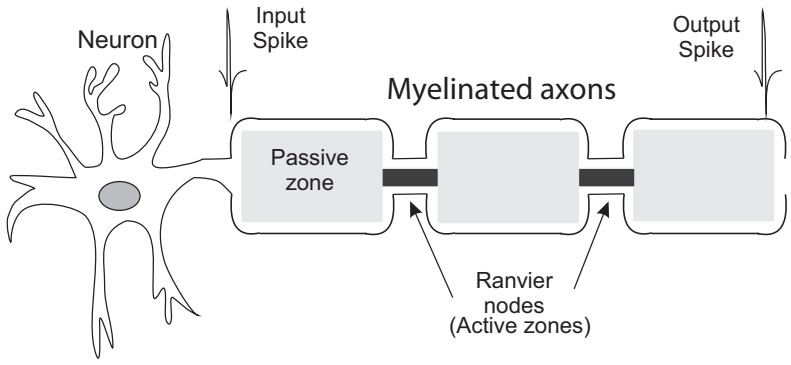


Figure 3.2: General scheme of myelinated axons.

However, previous works have considered noise sources as independent sources. In this chapter, it is introduced the effect of dynamical noise on system response. Experimental results from pyramidal neurons from rat neocortex, show the intrinsic noise has a non-linear dependence on membrane potential [14]. Steinmetz

et al., using the classical Hodgkin and Huxley model, predict that the standard deviation of voltage noise increases as the membrane potential is depolarized; the cause of this increment, is the increase of the probability that ion channels open [15]. We will further introduce the importance of including membrane potential dependent noise for correct spike transmission in our current model.

3.2.1 FitzHugh-Nagumo model

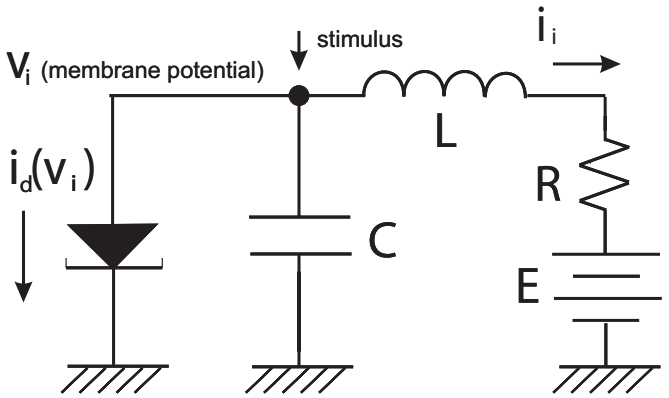


Figure 3.3: FitzHugh-Nagumo circuit.

It is employed an electrical circuit of the FitzHugh-Nagumo model operating in the excitable mode [16] to emulate myelinated axons. FitzHugh-Nagumo model has been widely used to emulate conductance-based neuron models as a simplification of Hodgkin-Huxley model, having cubic nullclines, where its dynamical behavior is represented by the following system of differential equations:

$$\frac{dV}{dt} = f(V) - W + I \tag{3.1}$$

$$\frac{dW}{dt} = a(bV - cW) \tag{3.2}$$

Where $f(V)$ is given by a cubic function of the form $V - V^3$. The nullclines of the FitzHugh-Nagumo model have a cubic and a linear form given by:

$$\frac{dV}{dt} = 0 \rightarrow \quad W = f(V) + i \quad \text{(V-nullcline)} \tag{3.3}$$

$$\frac{dW}{dt} = 0 \rightarrow \quad W = \left(\frac{b}{c}\right)V \quad \text{(W-nullcline)} \tag{3.4}$$

These nullclines can intersect in one, two or three points, resulting in one, two, or three equilibria, all of which may be unstable. There is an electrical circuit that possesses the same dynamic of the FitzHugh-Nagumo model and is shown in Fig. 3.3.

The dynamical equations governing the circuit from Fig. 3.3 are given as follows:

$$C\frac{dv}{dt} = i - i_d(v) \tag{3.5}$$

$$L\frac{di}{dt} = E - Ri - v \tag{3.6}$$

Where $i_d(v)$ represents the characteristic curve of a tunnel diode and could be described as a cubic function (Fig. 3.4) and v-nullcline and i-nullcline (Fig. 3.5) are given by:

$$\frac{dv}{dt} = 0 \rightarrow \quad i = i_d(v) \quad \text{(v-nullcline)}$$

$$\frac{di}{dt} = 0 \rightarrow \quad i = \frac{(E - v)}{R} \quad \text{(i-nullcline)}$$

Figure 3.6 depicts the v-nullcline and i-nullclines and their difference areas.

In order to demonstrate the previous model, simulations were performed using the following parameters: E=0.25V, L=10 μH, C=100pF, and $R = 0.2\Omega$, where under these parameters, the system will have a limit cycle around the fixed point (Fig. 3.7) [17], and the membrane potential behaves as a spike train (Fig. 3.8).

In order to establish a formal analysis for the fixed points of this system, the eigenvalues are obtained for a linear part of the v-nullcline. Then, we have the following matrix representation:

$$\begin{pmatrix} \frac{dv}{dt} \\ \\ \frac{di}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{g}{C} & \frac{1}{C} \\ \\ -\frac{1}{L} & -\frac{R}{L} \end{pmatrix} \begin{pmatrix} v \\ \\ i \end{pmatrix} + \begin{pmatrix} -\frac{q}{C} \\ \\ \frac{E}{L} \end{pmatrix} \tag{3.7}$$

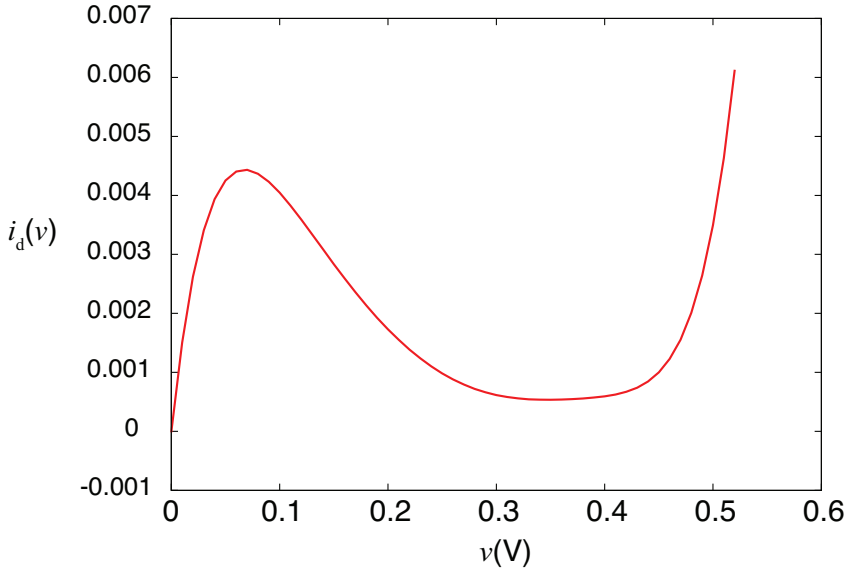


Figure 3.4: Plot of the i-v characteristic of the diode utilized to simulate the FitzHugh-Nagumo circuit, where clearly a cubic function is observed

where $i_d(v) = gv + q$ with $g = -10e^3$ and $q = 3.5e^3$; and the fixed points are given by $(v*, i*) = \left(\frac{E - qR}{Rg + 1}, \frac{q + gE}{Rg + 1}\right)$. If $V = v - v*$ and $I = i - i*$, therefore we have:

$$\begin{pmatrix} \frac{dV}{dt} \\ \\ \frac{dI}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{g}{C} & \frac{1}{C} \\ \\ -\frac{1}{L} & -\frac{R}{L} \end{pmatrix} \begin{pmatrix} V \\ \\ I \end{pmatrix} \tag{3.8}$$

Here the stability can be determined through the eigenvalues of the systems:

$$\begin{pmatrix} \frac{dV}{dt} \\ \\ \frac{dI}{dt} \end{pmatrix} = \begin{pmatrix} a & b \\ \\ c & d \end{pmatrix} \begin{pmatrix} x \\ \\ y \end{pmatrix}$$

,

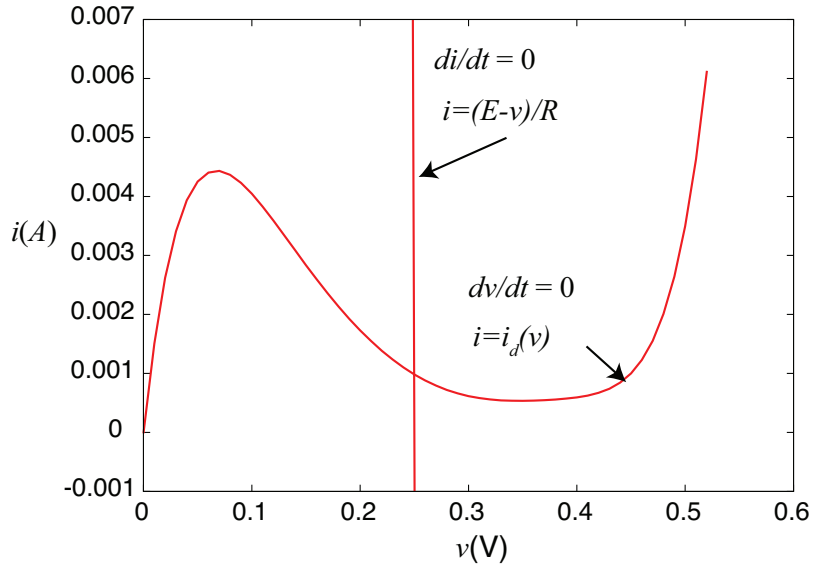


Figure 3.5: v-nullcline and i-nullcline for the circuit of Fig. 3.3

$$\begin{pmatrix} a-\lambda & b \\ c & d-\lambda \end{pmatrix}$$

The eigenvalues are given by $\lambda = \dfrac{(a+b) \pm \sqrt{(a+d)^2 - 4(ad-bc)}}{2}$. From the equation system 3.8, $a = -\dfrac{g}{C}$, $b = \dfrac{1}{C}$, $c = -\dfrac{1}{L}$, and $d = -\dfrac{R}{L}$. Therefore, the eigenvalues for our systems are given by:

$$2\lambda = -\left(\frac{g}{C} + \frac{R}{L}\right) \pm \sqrt{(\frac{g}{C} + \frac{R}{L})^2 - 4\frac{1+gR}{CL}} \tag{3.9}$$

If $\lambda > 0$, the response increases exponentially; if $\lambda < 0$ the system converge to a stable point; and if λ is complex, then the system is oscillatory. Therefore, to determine when the system is stable, λ should be negative. To obtain this result, it should be true that $-g > \sqrt{\dfrac{C}{L}}$. Evidently, $\sqrt{\dfrac{C}{L}}$ must be complex, which is impossible in terms of physical devices. However, if E is reduced to

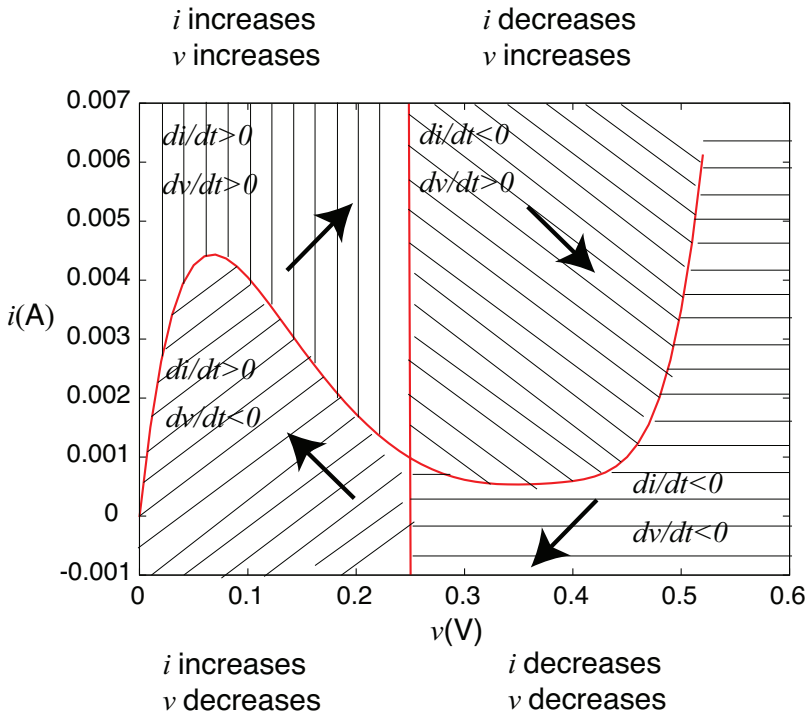


Figure 3.6: Four different areas are shown, according to the fixed point of v-nullcline and i-nullcline, where the direction of the vector field depends on the regions

0.05V, then the new linear region of v-nullcline has $g = 20e^{-}3$, with this value it is possible to have an stable fixed point, since the condition $\lambda < 0$ is true. Electrical simulation were performed, and it can be shown that parametric plot i versus v has a trajectory that converges to the sable fixed point (Fig. 3.9); also the temporal plot of membrane potential is shown in Fig. 3.10.

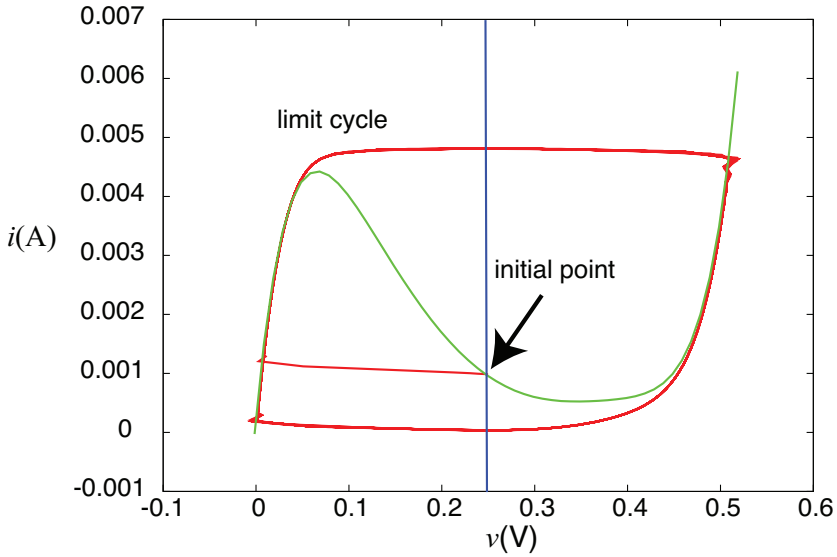


Figure 3.7: Parametric plot of i versus the membrane potential v, where clearly its trajectory is represented by a limit cycle, according to the circuit parameters

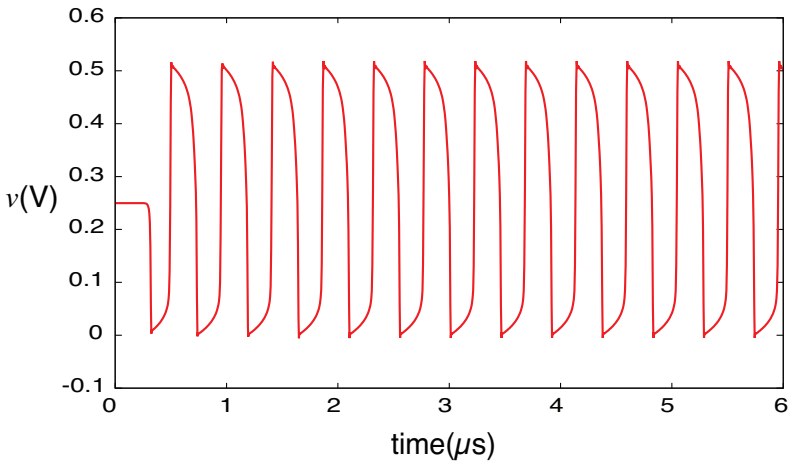


Figure 3.8: Spike-like membrane potential v

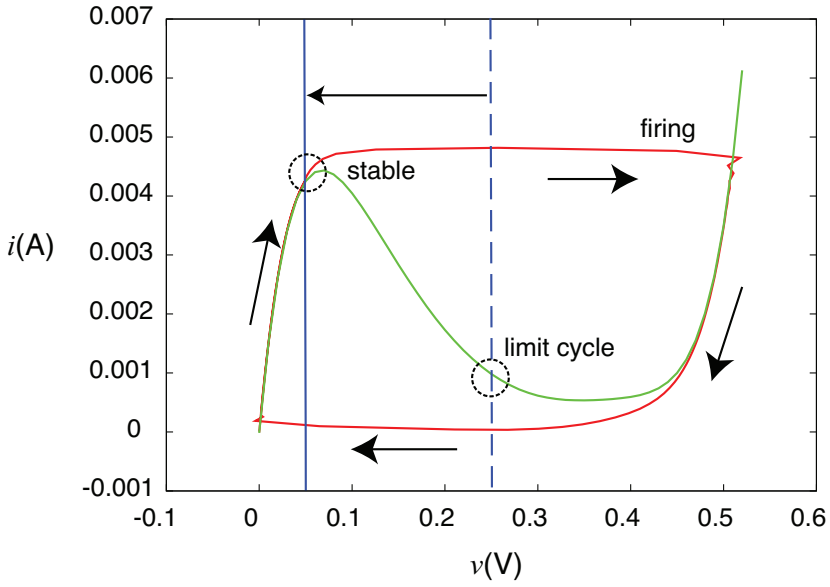


Figure 3.9: Parametric plot of i versus the membrane potential v, where the new fixed point is stable

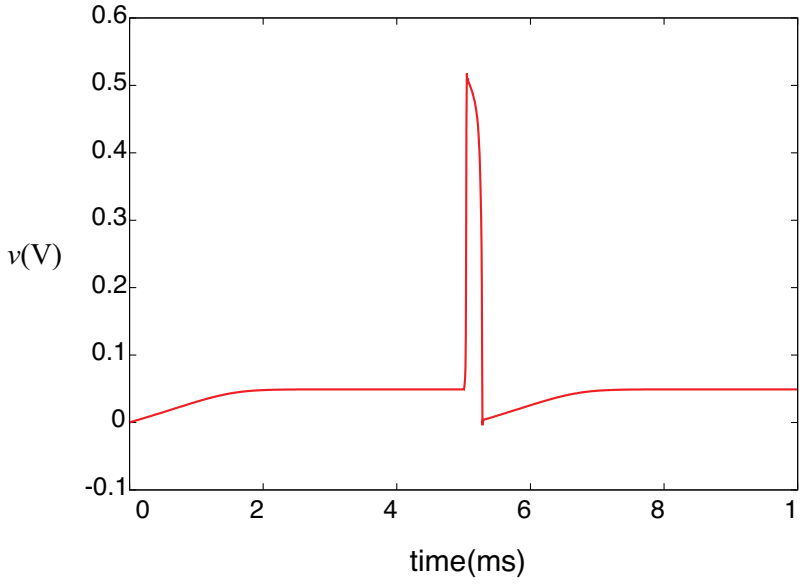


Figure 3.10: Spike-like membrane potential, after firing, the state returns to an stable state v

3.3 Noise-assisted spike transmission along excitable circuits

In this section, circuit design and electrical simulations are performed for noise-assisted spike transmission along a chain of excitable circuits (FitzHugh-Nagumo).

3.3.1 Circuit design

To emulate the noise effect in spike transmission, a current noise source in parallel with a tunnel diode was embedded (Fig. 3.11).

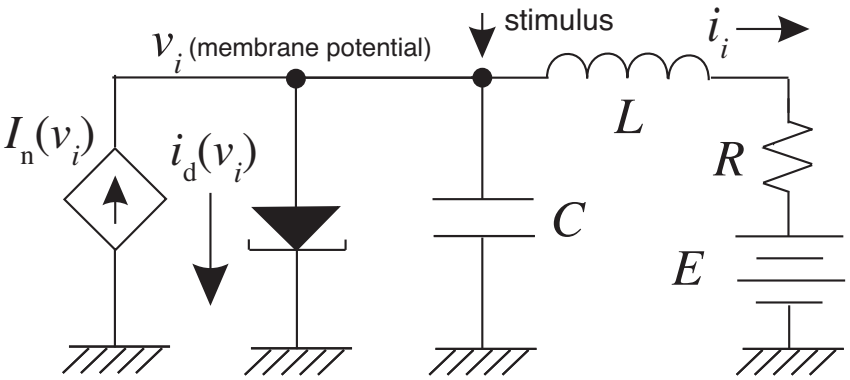


Figure 3.11: Noise-driven FitzHugh-Nagumo circuit.

On the other hand, if we consider a chain of electrical circuits, connected to each other by resistors R_c, the n-th circuit is described using the discrete FitzHugh-Nagumo equations as:

$$C\frac{dv_n(t)}{dt} = i_n(t) - i_{\mathrm{d,n}}(t) + \frac{v_{n-1}(t) + v_{n+1}(t) - 2v_n}{R_c} \tag{3.10}$$

$$L\frac{di_n(t)}{dt} = E - R \cdot i_n(t) - v(t) \tag{3.11}$$

where R_c represents the internodal resistance.

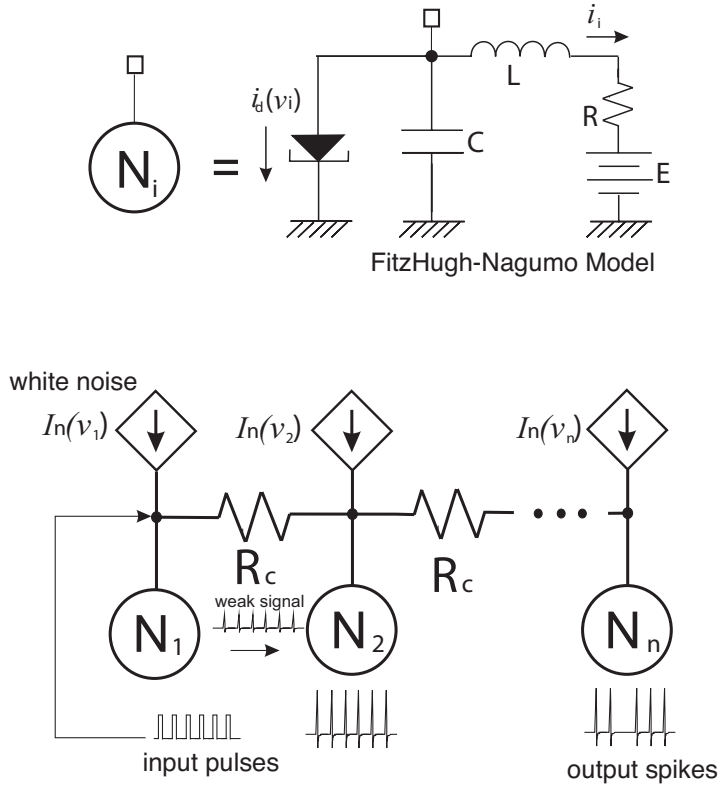


Figure 3.12: Block diagram of serially-connected circuits with noise-assisted spike propagation

The dynamics of the 1-D excitable medium (our virtual axon), where the excitable circuits were locally coupled, are represented by the continuous forms given by Eq. 3.12 and Eq. 3.13:

$$C\frac{\partial v(x)}{\partial t} = g\frac{\partial^2 v(x)}{\partial x^2} + i(x) - i_{\mathrm{d}}[v(x)] + I_{\mathrm{n}}[v(x)] \tag{3.12}$$

$$L\frac{\partial i(x)}{\partial t} = E - R \cdot i(x) - v(x) \tag{3.13}$$

where x represents the space, $i_d(\cdot)$ the i-v characteristics of the tunnel diode, $v(x)$ the membrane potential at x, E the resting potential, and $I_{\mathrm{n}}[v(x)]$ the $v(x)$-dependent dynamic noise current where the noise current is generated only when

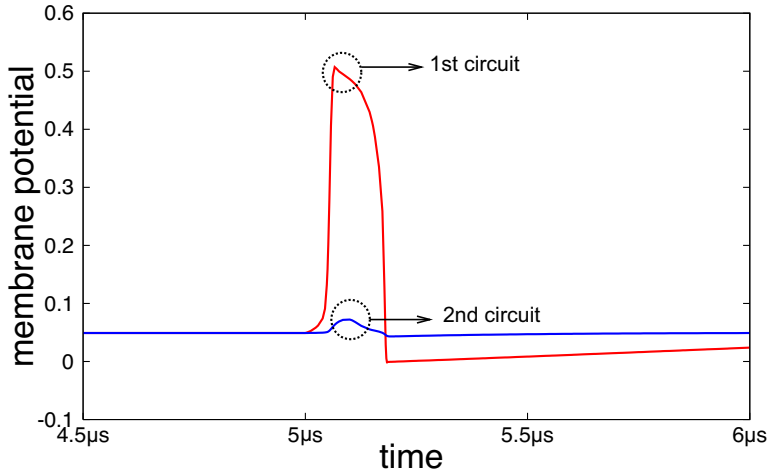
$v > E$.

This case represents the simplest one of membrane potential dependence. This choose ensures noise sources to be activated only in the presence of subthreshold inputs discriminating weak inputs from internal fluctuations. Therefore, the characteristics of $I_{\mathrm{n}}(\cdot)$ is crucial for successive spike transmission; *i.e.*, if noises were generated independently of v, excitable circuits that should not be depolarized (receiving no input) may be depolarized by the noise, whereas if noise were generated only when $v > E$, the circuits may be depolarized only when inputs (external stimuli or firing of the neighbors) are given, even if the input is below the threshold of the depolarization. This hypothesis is qualitatively consistent with experimental and simulation results shown in [14] and [15], where standard deviation of noise is increased as membrane is depolarized. Fig. 3.11, represents the classical FitzHugh-Nagumo electrical circuit, described by Eq. 3.5 and Eq. 3.6, while Fig. 3.12, represents the serially connected n circuits, with the membrane potential dependent noise sources, represented by Eq. 3.10 and 3.11.

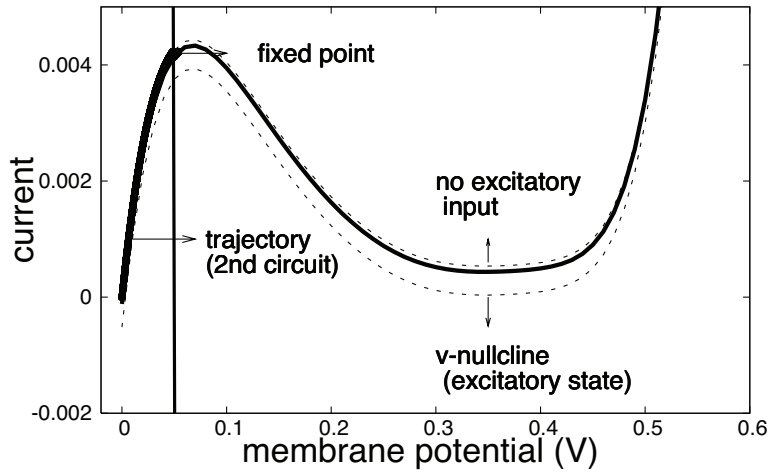
3.3.2 Simulations and results

SPICE simulations were conducted for this excitable system, with the following parameters: tunnel diode NEC 1S1760, $C = 0.1$ nF, $R = 0.2\ \Omega$, $L = 10\ \mu$H and $E = 50$ mV. Nine excitable circuits ($i = 1 \sim 9$) were locally connected by resistors R_{c} ($\sim g$), and the first circuit on the boundary was stimulated by an external current pulse (amplitude: 0.5 mA, width: 1 μs). When R_{c} is 1 kΩ, successive spike transmission was observed (from the first to the ninth circuit) without noise assistance, whereas spike transmission was randomly terminated when R_{c} was 1.5 kΩ also without noise assistance. As it can be observed in Fig. 3.13(a), postsynaptic potential is no generated, only a small perturbation in second circuit is observed. This phenomenon occurs as a result of the reduction of the input spike, due to the suprathreshold value of inernodal resistances, and therefore it is not possible to excite subsequent stages, remaining without any response. The corresponding phase portrait is shown in Fig. 3.13(b). The trajectory of the response of the second circuit, represents a non-excitatory response, such trajectory (solid thick line), starts from the resting state according to the initial conditions of the system, until converge to the fixed point generated by the intersection of the i and v-nullclines. The variation of the membrane potential is less than 0.1V and it does not represent a firing event. These figures, show clearly that spike transmission is stopped in the presence of suprathreshold values for

internodal resistors.



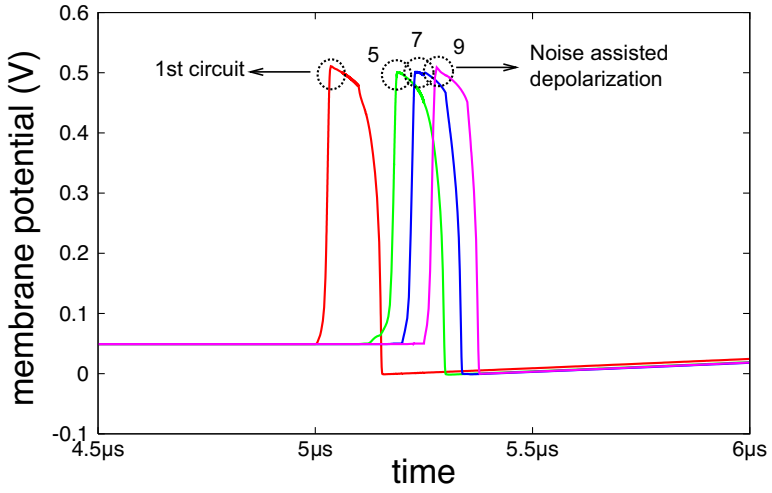
(a)



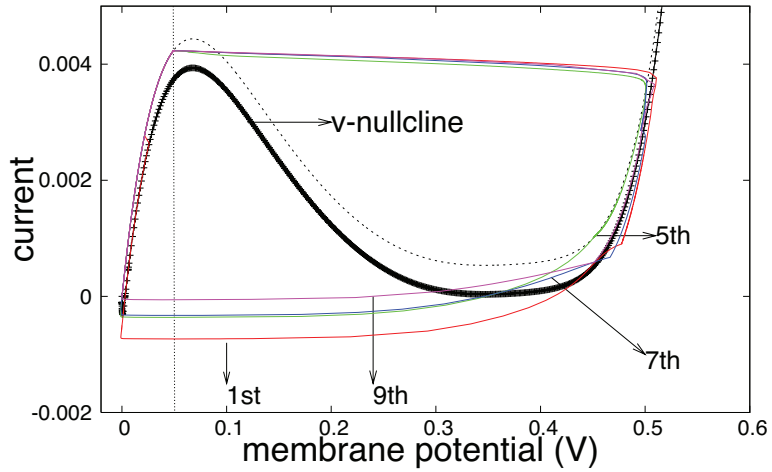
(b)

Figure 3.13: Spike-like potential at membrane potential at 1st and 2nd circuit without noise assistance (a) and its phase portrait (b).

On the other hand, when noise sources are introduced (white noise, with $\sigma = 0.45$ mA and $\mu = 0$), spike transmission is successful, Fig. 3.14(a) shows spike propagation for 1st, 5th, 7th and 9th circuit, showing that within the introduction of noise sources, spike propagation is achieved successfully. Fig. 3.14(b) shows the phase-portrait with the corresponding trajectories. Moreover, a more general view of spike transmission is necessary. Figure 3.15 shows simulation results for spike propagation along circuit 1, 3, 5 and 9, connected through suprathreshold values for internodal resistors, where a current pulse, as excitatory input dur-



(a)

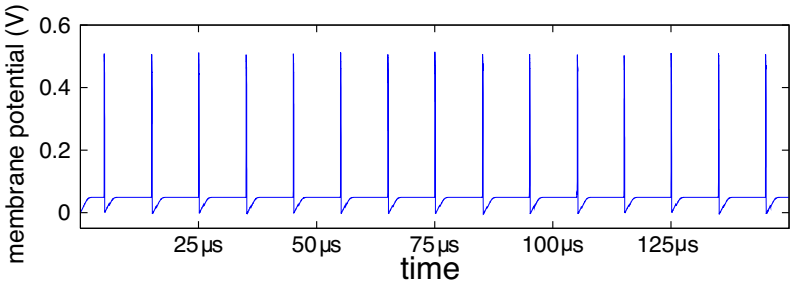


(b)

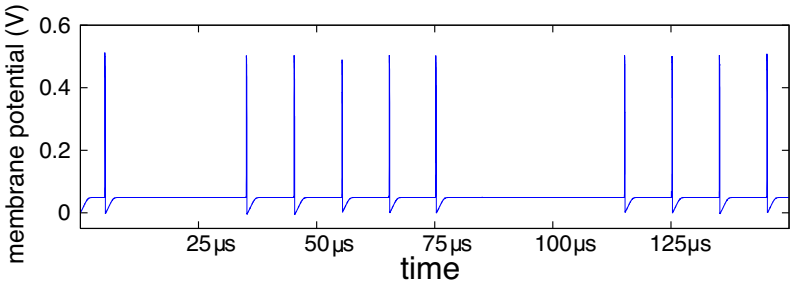
Figure 3.14: Spike-like potential at 1st, 5th, 7th and 9th circuit with noise assistance (a) and its phase portrait (b).

ing 150 μs, is applied. However, because of the stochastic nature of the noise sources, spike transmission is not successful in some cases, so we define the spike transmission rate as the percentage spikes transmitted to the last circuit.

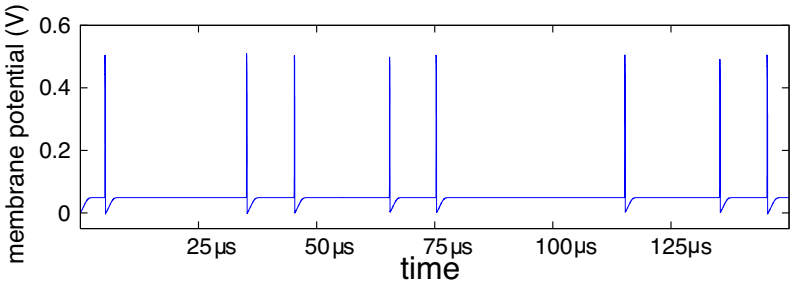
Also, it is necessary to explore how the standard deviation of noise affects the performance of spike transmission. Several simulations were run by using different values of standard deviation. Figure 3.16 shows transmission rate, for circuits 3,5,7 and 9. Monte Carlo simulations were run for 100 iterations for 21 different values of standard deviation, where the continuous lines represent the average between 10 Monte Carlo simulations. As it is observed, it is more probable



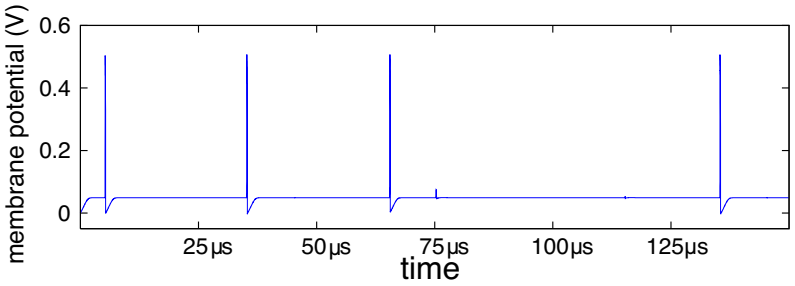
(a)



(b)



(c)



(d)

Figure 3.15: Generated spike train assisted by noise at (a) 1st circuit, (b) 5th circuit, (c) 7th circuit, and (d) 9th circuit

to generate a spike in the subsequents circuits as standard deviation of noise increases. If amplitude of noise input is independent from membrane potential, in this case, SR-like behavior could be observe; however in this particular case, noise is dependent on the membrane potential value, therefore, weak noise signals may not be able to assist weak inputs to excite subsequent stage; however as amplitude of noise signal increases, probabilities to generate a spike also increase. Moreover, we found that there is a specific value, where spike rate transmission stops increasing (around 0.8mA) and remains constant. However, even if SR-like behavior is not observed, the main advantage of the introduction of the dependent noise current source is that unwanted spikes are avoided. If noise amplitude is independent from the circuit parameters, then when noise amplitude is high enough, it can be rise to spike activity even in the absence of excitatory inputs.

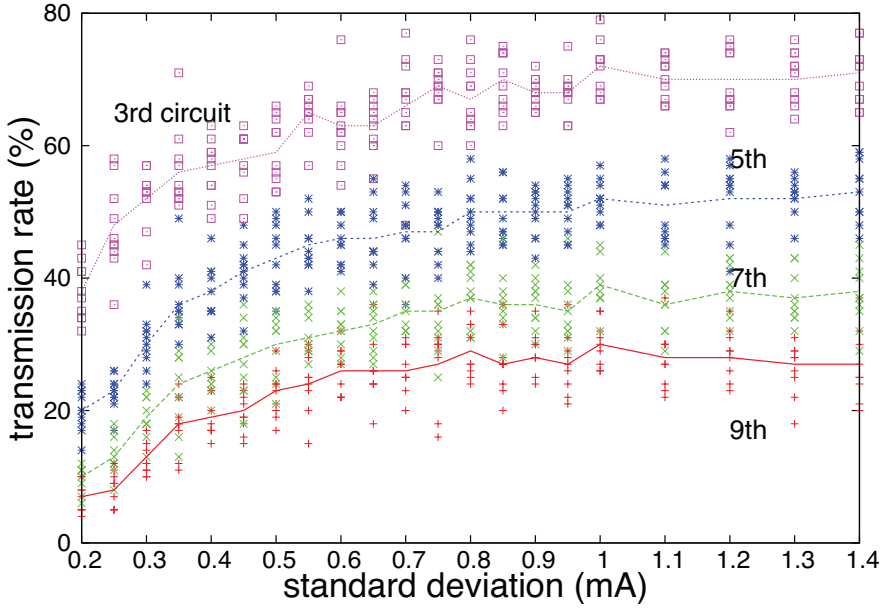


Figure 3.16: Percentage of successful spikes versus standard deviation of noise (mA).

3.3.3 Stochastic-resonance-like behavior from subthreshold and suprathreshold internodal resistances

So far, we have studied the impact of internal fluctuations to improve spike transmission rate along a transmission line, where internodal resistances have set to a specific value. This value must be large enough to induce a failure in spike transmission. So far, this value remains constant for all the iterations. In real physical systems, this value fluctuates, having different values for every resistance, so that, it is necessary to expand this study to a more realistic case, so we move our attention to the study of random fluctuations of internodal resistors. We choose zero resistance as mean value (ideal case), and we modify standard deviation. The first expectation was, as the standard deviation decreases, spike transmission rate must reach 100% so that, the graph of spike transmission rate vs standard deviation of internodal resistance, was expected to be represented by a decreasing function; however, simulation results using standard deviation values from 0.001kΩ to 5kΩ, demonstrated that there is an specific standard deviation value for internodal resistances where spike transmission reaches its maximum rate (Fig. 3.17).

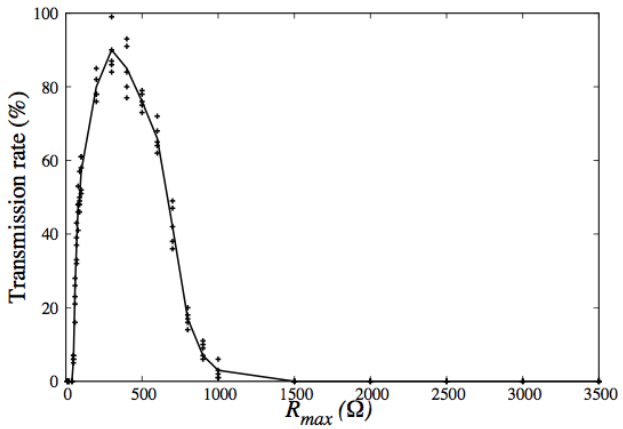


Figure 3.17: Percentage of successful spikes versus standard deviation of internodal resistor kΩ.

According to Fig. 3.17, a bell-shape curve describes the behavior of the system and only under a certain range of standard deviation for the internodal resistance, the best performance is achieved; so that, spike transmission rate can be depicted as a SR-like behavior, these simulations show very interesting results because the

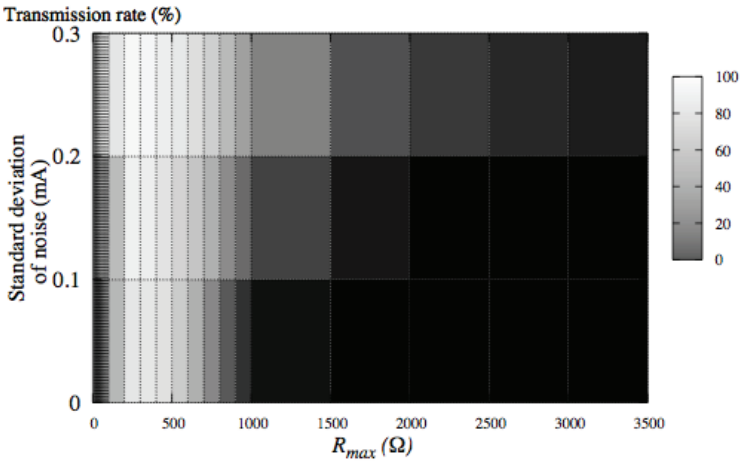


Figure 3.18: Spike transmission rate versus standard deviation of internodal resistor kΩ and standar deviation of noise (mA).

network exhibits a new kind of SR-like behavior. Simulation were run simultaneously for different values of the standard deviation of noise also, as it is shown in Fig. 3.18.

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Chapter 4

Noise-driven digital circuits

This chapter introduces the foundations for the design of noise-driven logic gates based on stochastic resonance (SR), as well as electrical and experimental results for their performance. The design of these gates is based on a hysteresis amplifier (implemented with an operation transconductance amplifier or OTA), therefore an introduction of the Schmitt-Trigger circuit is presented. Moreover, the design also includes Floating-Gate MOSFET's, thus a brief introduction also is presented. The following sections are devoted to the design and analysis of noise-driven logic gates, as well as the analysis of their performance.

4.1 Configuration of an operational amplifier with hysteresis

Figure 4.1 shows the operational amplifier configuration for a Schmitt-trigger circuit, a bistable circuit where the positive feedback is the responsible of generating hysteresis (Fig. 4.2) [1]. Here $x(t)$ represents the input, while R_1 and R_2 establish the levels $-V_0$ and $+V_0$; if the Schmitt-trigger is in the high state $+V_s$, the output voltage V_+ of the voltage divider is given by

$$V_+ = \frac{R_1}{R_1 + R_2}(-V_s) \tag{4.1}$$

The circuit will switch when $V_{in} = V_+$. So V_{in} must exceed above this voltage to get the output to switch. Once the circuit has switched to $-V_s$, the new threshold becomes:

$$V_- = \frac{R_1}{R_1 + R_2}(+V_s) \tag{4.2}$$

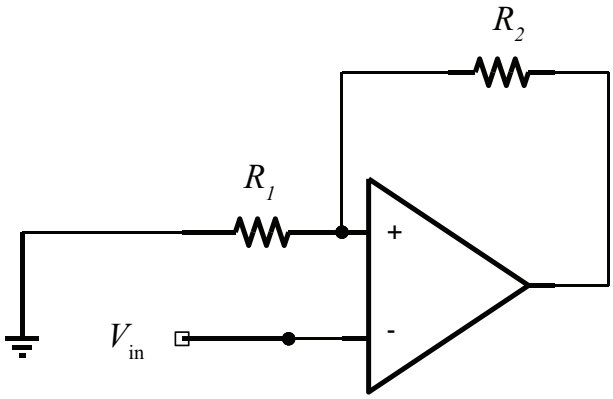


Figure 4.1: Schmitt-trigger operational amplifier configuration

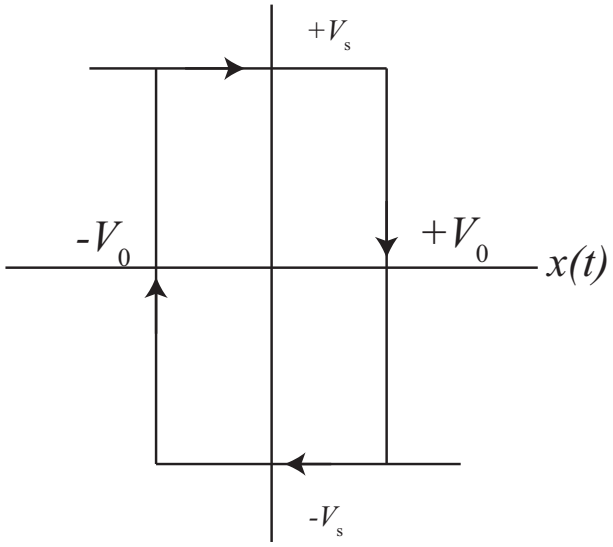


Figure 4.2: Typical hysteresis characteristic of a Schmitt-trigger circuit

One of the main applications of this configuration is the elimination of noise, since once the system achieves one of the two states, the new threshold, to return to the previous state, changes. Further, it is explained how this feature allows to have an stable output in noise-driven circuits.

4.2 Floating Gate MOSFET

The Floating Gate transistor is a field effect transistor, and it is composed of n number of inputs coupled capacitively to its gate. As its gate does not have any physical connection with any other part of the circuit, it is said that this node is floating and thus, this transistor is known as Floating Gate MOSFET or just

FGMOSFET [2]. Figure 4.3 shows the electrical diagram and of the Floating Gate MOSFET.

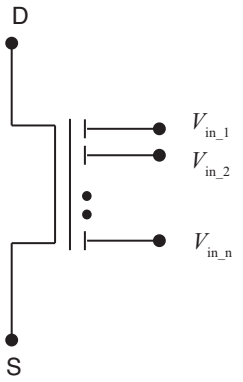


Figure 4.3: Symbol for the Floating Gate MOSFET

From the electrical diagram, it is easy to deduce an equation for the gate voltage, as follows:

$$V_{g1} = \frac{C_1}{C_{\mathrm{TOT}}} V_{\mathrm{in_1}} + \frac{C_2}{C_{\mathrm{TOT}}} V_{\mathrm{in_2}} + ... + \frac{C_n}{C_{\mathrm{TOT}}} V_{\mathrm{in_n}} \tag{4.3}$$

Where C_{i} is the capacitor at input, and C_{TOT} is the total capacitance, given by the sum of all input capacitances (considering parasitic capacitances small enough to be neglected). Therefore the equation for drain current of the FGMOSFET working in subthreshold would be given by:

$$I_D = I_0 exp\Big(\sum_{i=1}^{n} \frac{C_i}{C_{TOT}} \frac{V_i s}{n v_t} \Big) \tag{4.4}$$

Where I_0 is the subthreshold current factor, and v_t is the thermal voltage. In this approximation, parasitic capacitances and initial charge are neglected, although in reality, parasitic capacitance and trapped charge at the gate are important factors that can degraded the performance of the FGMOSFET. However, there are already several techniques to avoid this problem [4–7].

4.3 Design of stochastic-resonance logic gates

A novel application of the SR effect in nonlinear systems is in the field of digital circuit design, where a certain range of noise serves to change the state in a bistable system; each state represents a logic state, and therefore the basic logic operations can be implemented by electrically modeling a double-well potential function with an additive Gaussian noise [8, 9]. Further, the precise values for the bias are necessary to set the logical operation, and this requires additional bias sources. Moreover, the implementation of this system is quite complex because it requires the use of several operational amplifiers and additional bias circuits, which is expensive in terms of VLSI.

This section shows a novel configuration that utilizes the cooperative role of noise in nonlinear systems. The concept involves electrical systems that exhibit hysteresis characteristic. This can be achieved easily by using an operational transconductance amplifier with positive feedback. As in the case of the Schmitt-trigger circuit, the presence of two thresholds prevents the activation of the output in the presence of large noise fluctuations. However, the main limitation is the timing of the SR gates, as it will be discussed later. The delay time of the SR gate response is limited by the stochastic process; therefore, synchronization is the main limitation for the effective performance of high-complexity synchronous circuit configurations. However, a suitable alternative is the implementation of asynchronous circuits with the current SR gates, considering the lack of a common clock. This characteristic allows for more reliable designs of the elements in the presence of delays, as in the case of SR gate.

4.3.1 Circuit design

Our idea is based on the utilization of noise to build logic gates. The main design is based on electrical systems with hysteresis characteristics, where the input is represented as a weighted sum of logic inputs (Fig. 4.4a, rightmost subfigure). Traditionally, noise assistance has been used to improve subthreshold-signal detection in systems with one threshold, here the red dot represents the subthreshold signal (Fig. 4.4a, center-left subfigure); subthreshold signals can be driven by noise to higher values than the threshold θ (gray dot, at center-right subfigure). However, one evident problem is that a high-amplitude peak in the noise signal can trigger an unnecessary response (rightmost subfigure). Generally, this response has hazards.

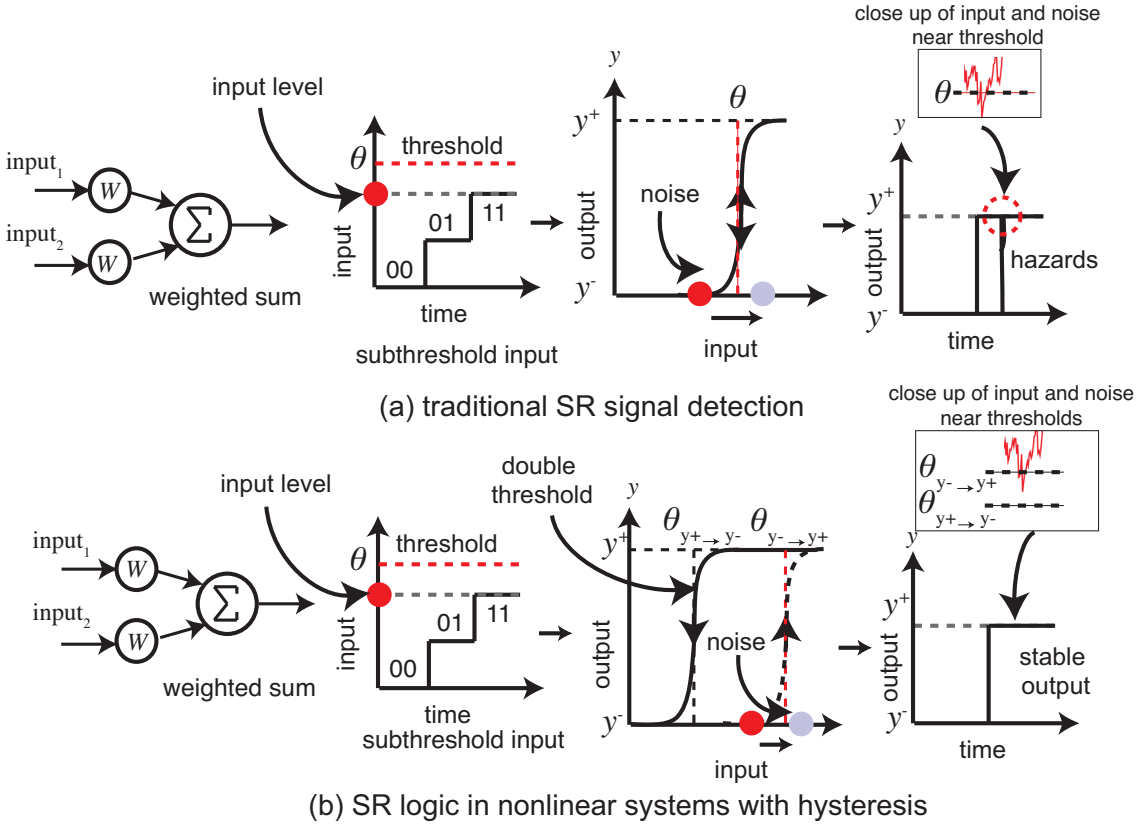


Figure 4.4: Noise assistance in nonlinear systems with one threshold (a), noise assistance in nonlinear systems exhibiting hysteresis (b).

Figure 4.4b represents our approach, utilizing nonlinear systems with two thresholds: $\theta_{y^+ \to y^-}$ and $\theta_{y^- \to y^+}$ (center-left subfigure). The first one is defined as the necessary threshold to change from the positive state y^+ to the negative state y^- and the second one, represents the necessary threshold to change from y^- to y^+. Due to this hysteresis characteristic, the output will be stable (rightmost subfigure).

Figure 4.5 shows a subthreshold operational transconductance amplifier (OTA), where V_{g1} and V_{g2} denote the input gate voltages, and V_{out} and $\overline{V_{out}}$ are the outputs. $\overline{V_{out}}$ is obtained by adding two current mirrors to invert the output. This is carried out in order to maintain a high-impedance node as in the non-inverted output V_{out} [10, 11].

The generic symbol of the four-terminal OTA is shown in Fig.4.6. Figure 4.7 shows the electrical connections of the generic SR gate for implementing the four basic logic operations. The inputs are capacitively coupled, where the values of

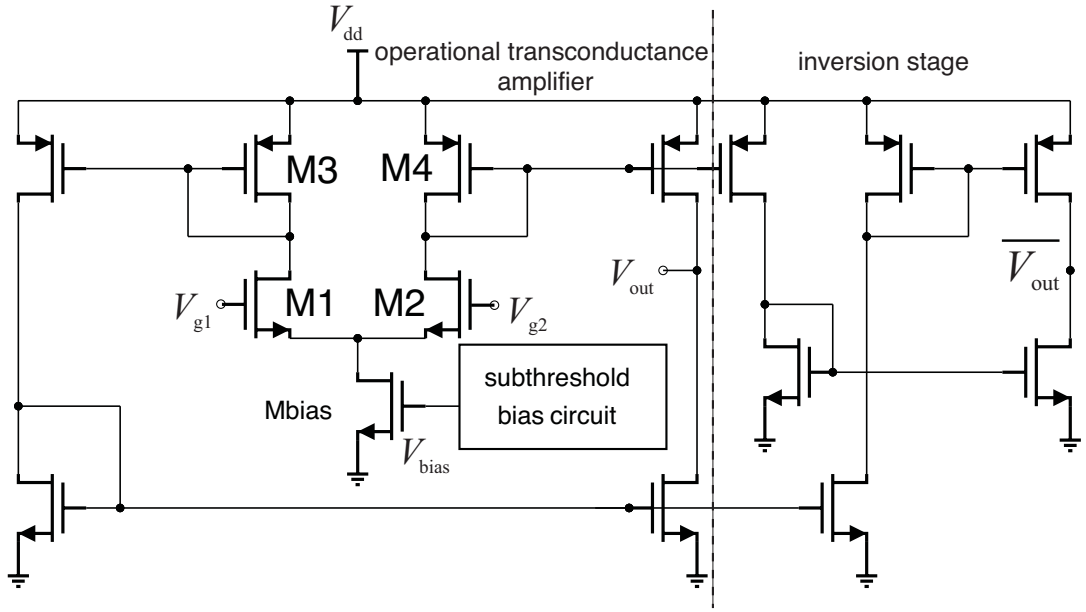


Figure 4.5: CMOS design of the subthreshold operational transconductance amplifier (OTA).

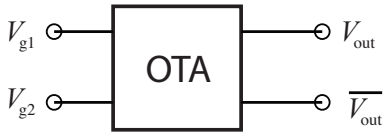


Figure 4.6: Generic symbol of an OTA.

V_{g1} and V_{g2} are the weighted sum of the input capacitors. This weighted sum is easily implemented with a floating-gate MOSFET (FGMOSFET) owing to its inherent property that generates a floating-gate potential equal to the weighted sum of its inputs. Here, parting from the equations of the FGMOSFET , in the case of Fig. 4.7, the equations for the gate voltages V_{g1} and V_{g2} are given by Eq. 4.5 and Eq. 4.6 respectively:

$$V_{g1} = \frac{C_1}{C_{\mathrm{TOT}}} V_{\mathrm{in1}} + \frac{C_2}{C_{\mathrm{TOT}}} V_{\mathrm{in2}} + \frac{C_3}{C_{\mathrm{TOT}}} V_{\mathrm{bias1}} \tag{4.5}$$

$$V_{g2} = \frac{C_4}{C_{\mathrm{TOT}}} V_{\mathrm{bias2}} + \frac{C_5}{C_{\mathrm{TOT}}} V_{\mathrm{noise}} + \frac{C_6}{C_{\mathrm{TOT}}} V_{\mathrm{out}} \tag{4.6}$$

Where C_{i} is the capacitor at input, and C_{TOT} is the total capacitance, given

by the sum of all input capacitances (considering parasitic capacitances small enough to be neglected). Here, V_{bias1} and V_{bias2} serve as selectors for the logic operations. To generate logic operations, we used the concept of threshold logic. If we consider a two input FGMOSFET, where input capacitors are equal, then each input is multiplied by a factor of 0.5. If each input is mapped as a logic input, then the input combinations will be represented as a weighted sum. If there is at least a logic one , the weighted sum will be half of the total, if both inputs are logic one, then the weighted sum will be at its maximum value. Table 4.1 lists the combinations of V_{bias1} and V_{bias2} to set either the NOR or NAND operation with V_{out} as the output. By selecting $\overline{V_{\text{out}}}$ as the output, both the OR and AND operations can be performed.

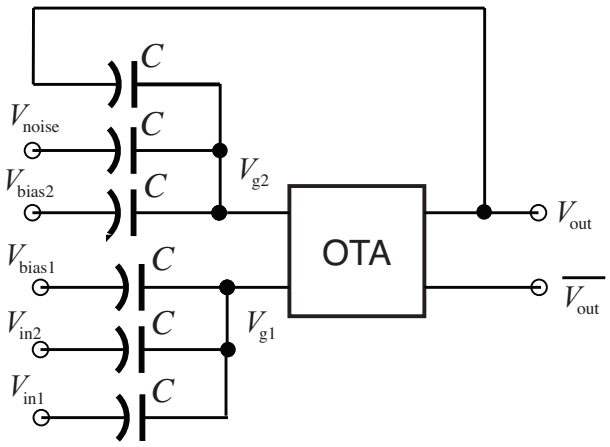


Figure 4.7: Construction of the proposed SR gate configuration for the basic logic operations. The configuration depends on the values of V_{bias1} and V_{bias2}.

Table 4.1: Selection of the logic operations according to V_{bias1} and V_{bias2} as well as V_{out} and $\overline{V_{\text{out}}}$

V_{bias1}	V_{bias2}	$\overline{V_{\text{out}}}$	V_{out}
V_{dd}	0 V	OR	NOR
V_{dd}	V_{dd}	AND	NAND

4.3.2 Mathematical model of stochastic-resonance logic gates

On the other hand, in order to confirm the operation of the SR gates, we show a suitable mathematical model for the SR logic gates based on the work of McNamara *et al.* [12]. For simplicity, we omitted the bias sources V_{bias1} and V_{bias2} in the analysis, since they serve only as threshold modifiers. Considering normalizing values of +1 and -1, for high logic and low logic respectively, the normalized output of the OTA can be given by:

$$y = sgn(z) = \begin{cases} +1, \text{ if } z > 0 \\ -1, \text{ if } z < 0 \end{cases} \tag{4.7}$$

In this analysis, we consider a periodic signal as input, where $V_{\text{g1}} = V_{\text{in}} = V_{\text{s}} \cos \omega_{\text{s}} t$ and $V_{rmg2} = V_{\text{out}} + V_{\text{noise}}$, where V_{dd} is the power supply. If we define normalization coefficients as $\varepsilon = V_{\text{in}}/V_{\text{dd}}$ and $\sigma' = V_{\text{noise}}/\gamma V_{\text{dd}}$, then Eq. 4.7 can be expressed as:

$$y = \text{sgn}(\frac{\gamma}{2}(y+1) + \sigma'\xi(t) - \varepsilon \cos \omega_{\text{s}} t) \tag{4.8}$$

Where $\sigma(t)$ represents white noise. In this system, a double threshold is generated due to the positive feedback of the OTA configuration. If $y = +1$, then $\varepsilon > \gamma$ is necessary to change state, therefore the threshold to change from positive to negative state is $\theta_{y^+ \to y^-} = \gamma$. On the other hand , if $y = -1$, then $\varepsilon < 0$ is required to change y to the positive state, and the new threshold is given by $\theta_{y^- \to y+} = 0$.

A realistic approximation to avoid infinite power is proposed by considering colored noise, where τ_{c} is the correlation time, where the switching time is short compared with τ_{c}. Therefore an approximate dynamical model of the OTA is given by:

$$\dot{y} = -\beta\{y - \tanh[A(\frac{\gamma}{2}(y+1) + x - \varepsilon \cos \omega_{\text{s}} t)]\} \tag{4.9}$$

$$\dot{x} = -kx + \sigma\xi(t) \tag{4.10}$$

Where noise is modeled as an Ornstein-Uhlenbeck process, where $k = \tau_c^{-1}$, and $\sigma = \sqrt{2k}\sigma'$. When β and $A \to \infty$, the behavior is approximated to an ideal operational amplifier with positive feedback. The system has two stables states

at y^+ and y^- in the range of $\varepsilon\cos\omega_s t - \gamma < x < \varepsilon\cos\omega_s t$. As we are interested on demonstrating the beneficial utilization of noise, equations for transition rate are presented. Let us define $x^- = \varepsilon\cos\omega_s t - \gamma$ and $x^+ = \varepsilon\cos\omega_s t$. Where a transition from y^- to y^+ is given when $x > x^-$ and a transition from y^+ to y^- is given when $x < x^+$. The transition rate W_t can be obtained then from the reciprocal of the mean time T of the transition from x^- to x^+. Defining $u = x\sqrt{k}/\sigma$, $u^- = x^-\sqrt{k}/\sigma$, and $u^+ = x^+\sqrt{k}/\sigma$, we have:

$$W_t^{-1}(x^- \rightarrow x^+) = \frac{2\sqrt{\pi}}{k}\int_{u^-}^{u^+} e^{u^2}\phi(u)du \tag{4.11}$$

where:

$$\phi(u) = \frac{1}{\sqrt{\pi}}\int_{\infty}^{u} e^{u^2}du \tag{4.12}$$

Executing numerical integrations, Eq. 4.11 and 4.12 were solved. The parameters for numerical simulations were set to $\varepsilon = 0.7$, $\gamma = 0.75$, and $\sigma' = 0.038$. A qualitatively behavior was confirmed, as the amplitude of the normalized standard deviation of noise is increased, the transition rate is increased exponentially (Fig. 4.8).

An equation for the potential function can be obtained by integrating Eq. 4.8, and it is given by the following equation:

$$U(y,t) = \beta\{\frac{1}{2}y^2 - \frac{2}{\gamma A}\ln\cosh[A\frac{\gamma}{2}(y-1) + x - \varepsilon\cos\omega_s t + \alpha]\} \tag{4.13}$$

Here, α is the normalized value of the bias voltage V_{bias}, and we define it as $\alpha = V_{bias}/\gamma V_{dd}$. Figure 4.9 shows the numerical simulations for the double-well potential, where α modifies the double-well potential shape to generate logic operations. Figure 4.9a represents NAND operation, with a subthreshold input ε (red line) and output y (blue line), where $\gamma = 0.682$, $\alpha = 0.142$, and $\beta = 5x10^{-4}$. Figure 4.9b represents the double-well potential obtained from Eq. 4.13, when ε is near the threshold $\theta_{y^+\rightarrow y^-}$, the transition probability increases. Figure 4.9c represents the opposite case for $\theta_{y^-\rightarrow y^+}$. To generate NOR operation, $\alpha = -0.77$ (Fig. 4.9d). Figure 4.9e and 4.9f are the double-well potential for the cases of ε near $\theta_{y^+\rightarrow y^-}$ and $\theta_{y^-\rightarrow y^+}$ respectively.

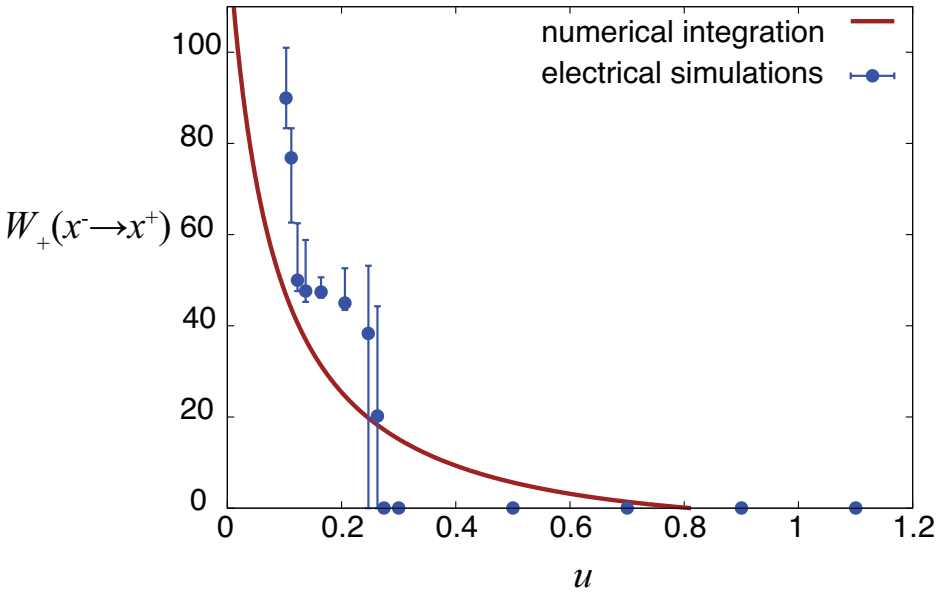
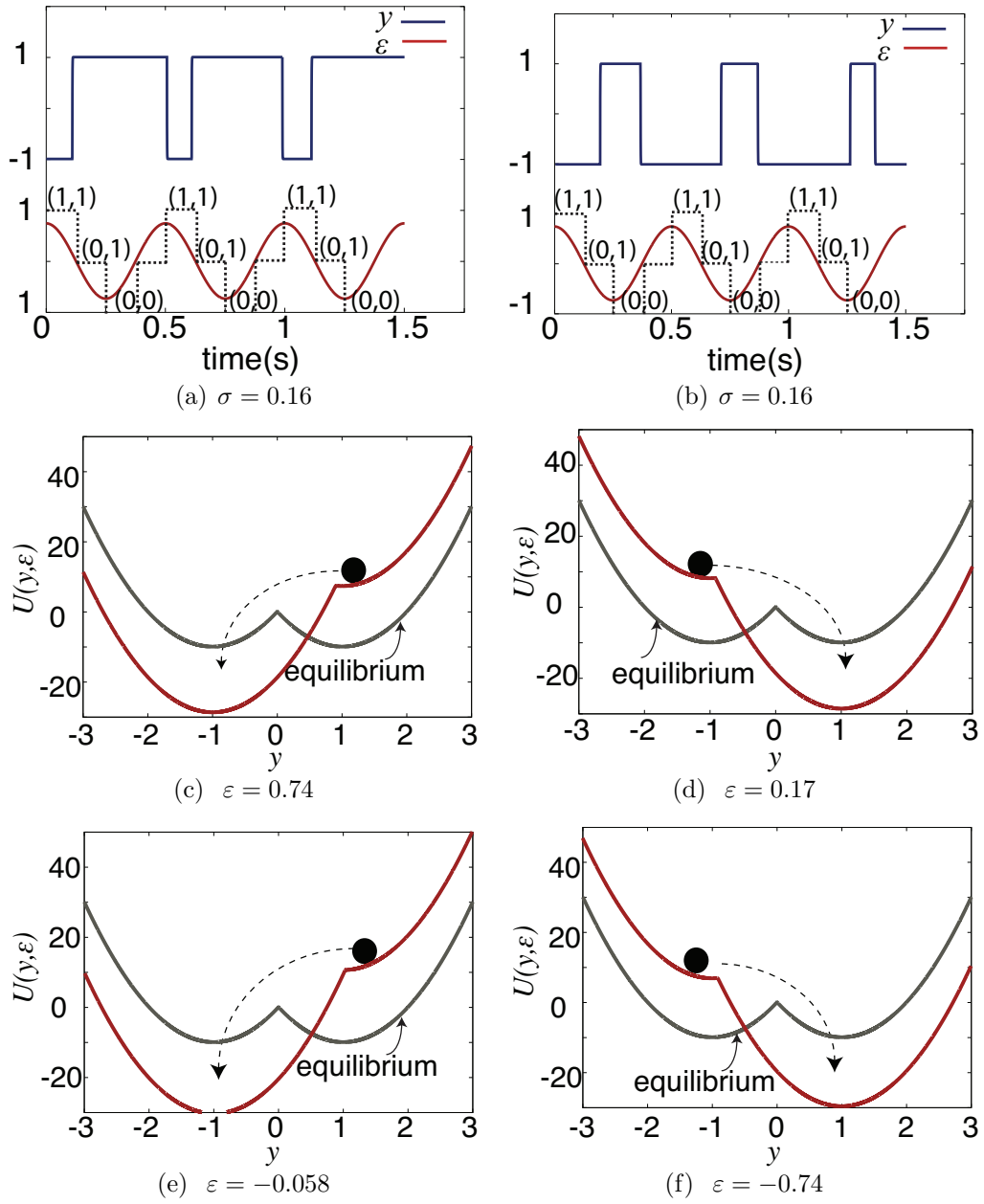


Figure 4.8: Transition rate $W_+(x^- \rightarrow x^+)$



(a) $\sigma = 0.16$ (b) $\sigma = 0.16$

(c) $\varepsilon = 0.74$ (d) $\varepsilon = 0.17$

(e) $\varepsilon = -0.058$ (f) $\varepsilon = -0.74$

Figure 4.9: Setting logic operations depending on the bias value α: (a) NAND operation, and (b) NOR operation; (c) and (d) are the double-well potential function for NAND operation; (e) and (f) are the double-well potential function for NOR operation.

4.4 Simulation results

This section is divided into two subsections: the first one discusses the simulations of the performance of the SR gates as well as the experimental results, and the second one details the results regarding the timing analysis of the SR gates.

4.4.1 Performance of the stochastic-resonance logic gates

The circuit simulations are carried out by using a SPICE program using 0.18-μm CMOS technology. The power supply is set to 0.35 V. This value corresponds to the minimum power supply for which the error rate of the SR gates is zero, considering a variation in V_{th} of M2 of 0.1 V, where V_{th} represents the transistor threshold voltage. All transistors operate in the subthreshold region. Gaussian noise is introduced in V_{noise} with a mean value of zero, a standard deviation $\sigma_{V_{\text{noise}}}$ of 18 mV, and an offset voltage of V_{dd}. This value was obtained through electrical simulations and corresponds to the value of the standard deviation of noise for which a circuit error rate of zero is achieved.

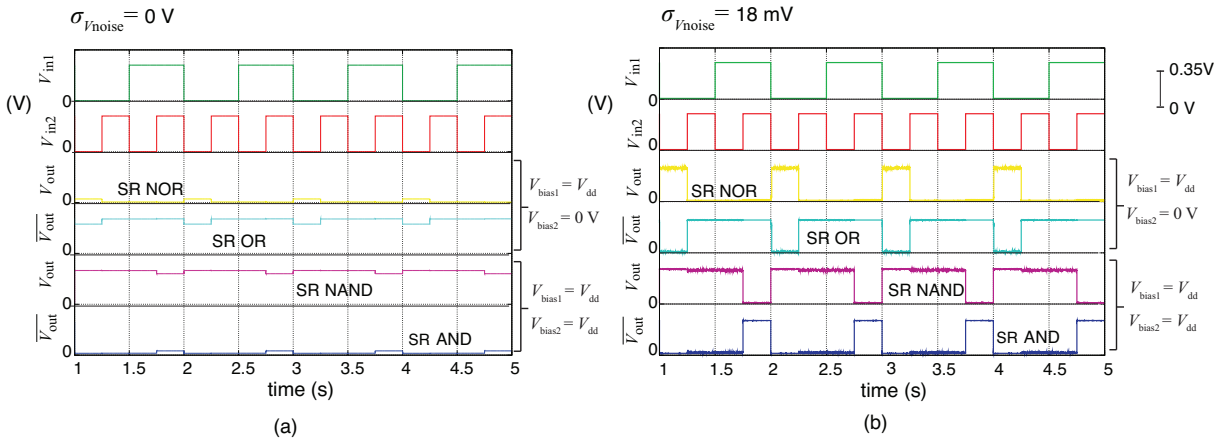


Figure 4.10: Simulation results of an SR gate for NOR, OR, NAND and AND operations. (a) without noise, the logic operations are not generated. (b) with an optimal amount of noise, the logic operations are generated correctly

The SR effect is observed during the simulations. For $\sigma_{V_{\text{noise}}} = 0$ V, the inputs do not exceed the threshold, and there is no response (Fig. 4.10a). Figure 4.10b shows the simulation results of the SR gates of the four basic logic gates when $\sigma_{V_{\text{noise}}} = 18$ mV. These responses are consistent with the true table of each logic gate, demonstrating that the application of noise helps to recover the logic operations in the presence of mismatches. It is also observed that the outputs exhibit

low amplitude fluctuations that can be explained as a result of the direct application of noise to one of the floating gate inputs of the operational transconductance amplifier.

Moreover, two basic simulations were performed: the first one shows a SPICE simulation of the power consumption P versus the power supply V_{dd} and the standard deviation of V_{th} ($\sigma_{V_{\mathrm{th}}}$) (Fig. 4.11). This simulation was obtained by calculating the average current of V_{dd} using the control commands of the SPICE simulator. This graph shows that the average power performance is on the order of picowatts , which makes the SR logic gates suitable for low-power applications.

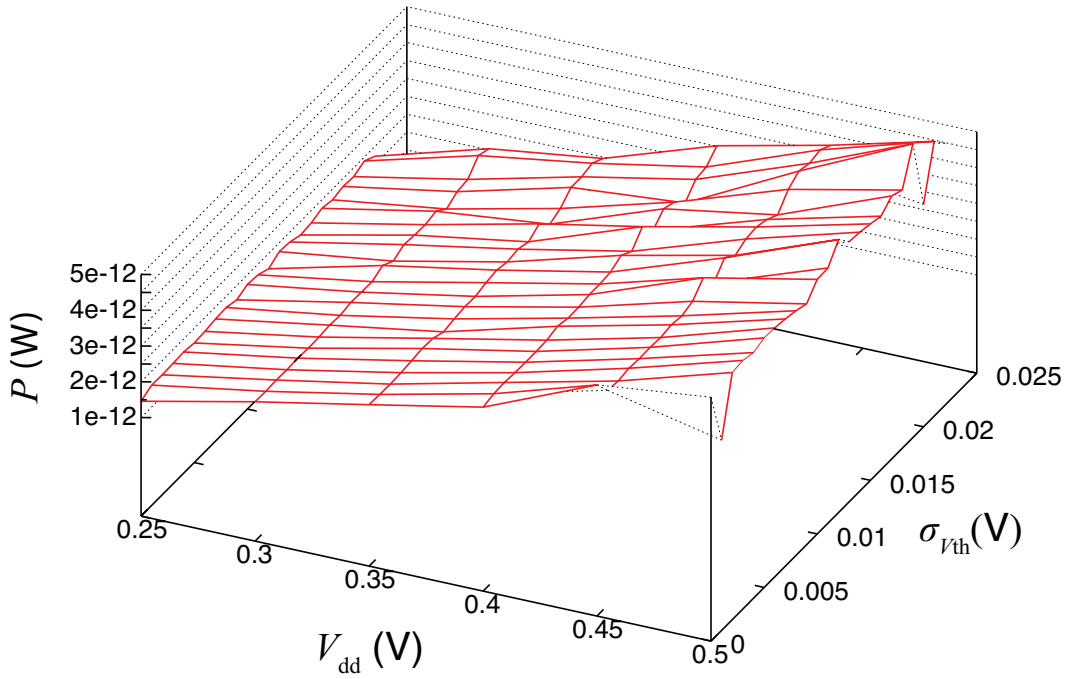


Figure 4.11: Power consumption P versus the power supply V_{dd} and the standard deviation of V_{th}

Electrical simulations were also performed to compare the power consumption of a conventional transistor-based NAND gate and our approach. Figure 4.12 shows that in the region where logic function is achieved correctly, the power consumption of the SR gates is lower, in the order of picowatts.

However, one implication of working with low power consumption is the increase in the sensitivity to variations in the threshold voltage, particularly in differential-pair configurations, where precise matching is required between the transistors. However, in this particular case, noise actually improves the perfor-

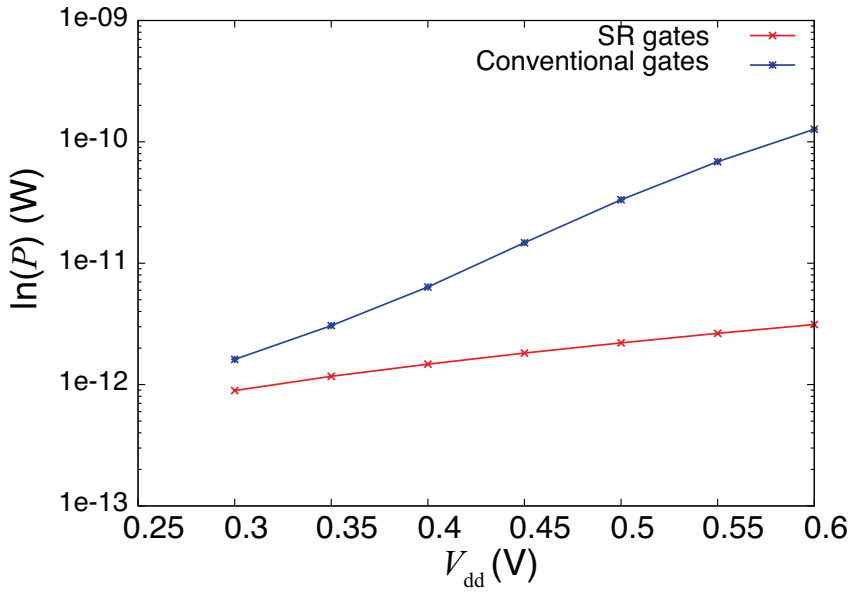


Figure 4.12: Power consumption of a conventional NAND gate and a SR NAND gate

mance regarding fluctuations in the threshold voltage, as shown in Fig. 4.13. This simulation consists of a phase diagram of the error rate versus two variables: $V_{\rm dd}$ and $\sigma_{V_{\rm th}}$. Here, intra-die variations are considered instead of the worst-case threshold-voltage variation. Monte Carlo simulations were carried out for ten values of $\sigma_{V_{\rm th}}$. Each one was set to six different values of $V_{\rm dd}$. The phase diagram shows the region where the error rate corresponds to 0%. The error rate greater than 0% is outside of this region.

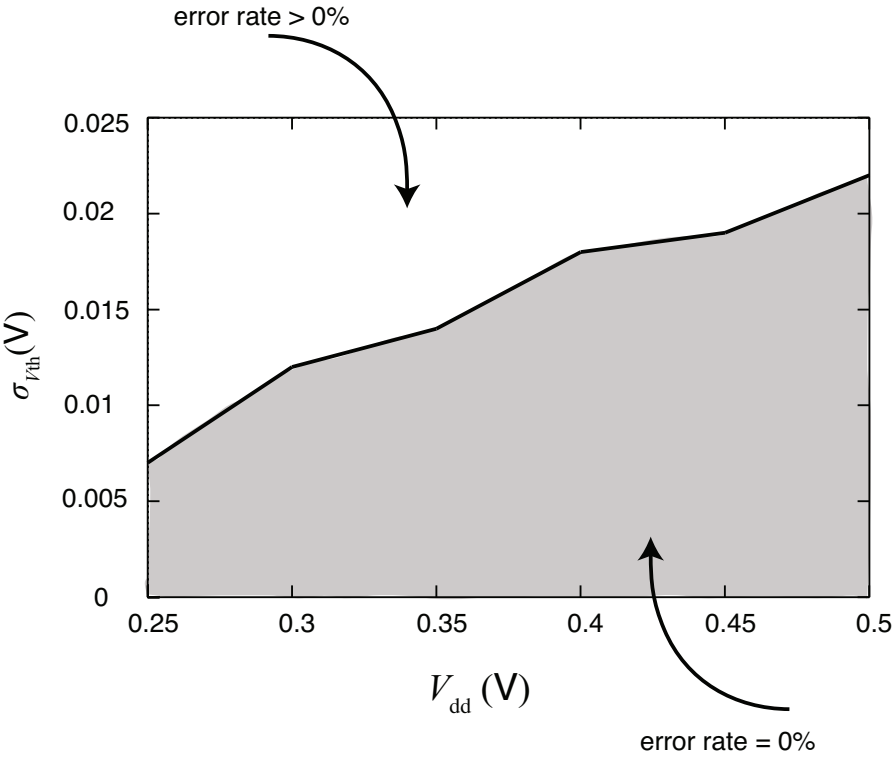


Figure 4.13: Phase diagram of the SR NAND gate error rate versus $V_{\rm dd}$ and $\sigma_{V_{\rm th}}$

4.4.2 Experimental results: stochastic-resonance logic gates based on an operational amplifier

Moreover, experimental results were performed by implementing a macrosystem for the SR NAND gate (Fig. 4.14). An operational amplifier OP284 was connected with positive feedback to generate the hysteresis characteristic.

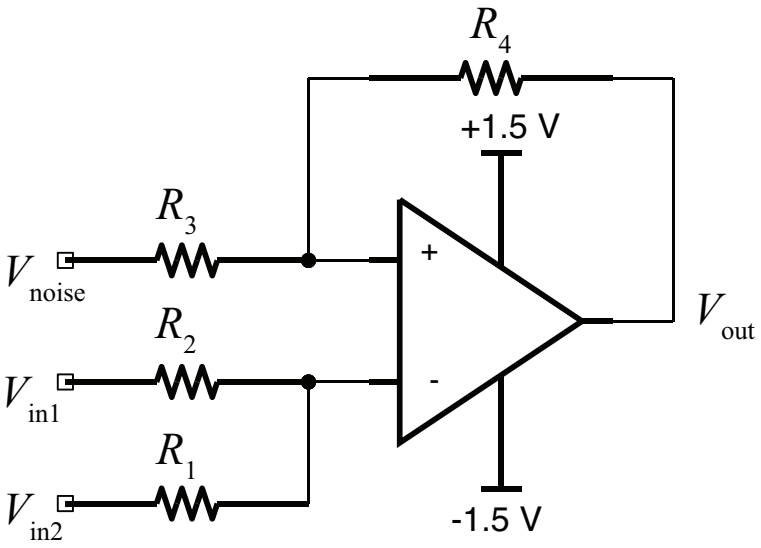


Figure 4.14: OP284 with a positive feedback configuration.

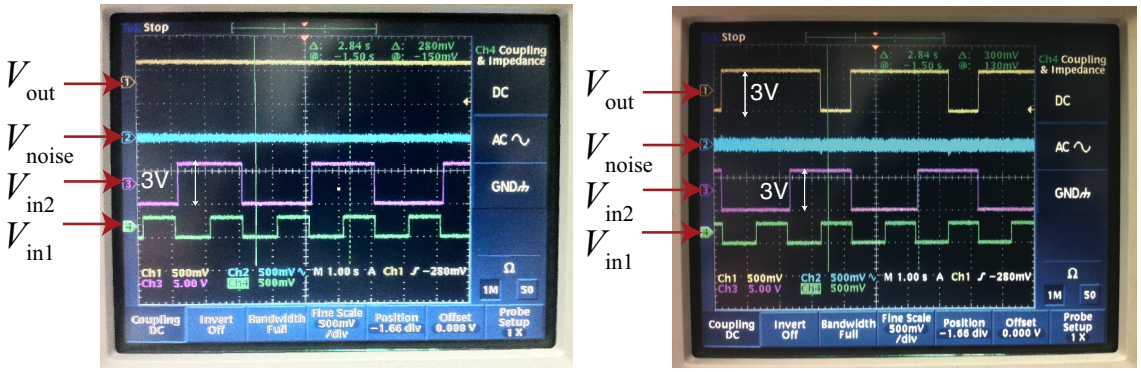


Figure 4.15: Experimental results of the SR gates: (a) low amplitude of noise, not enough to detect the signal, and (b) shows the minimum standard deviation to effectively detect the signal.

The supply voltage was set to +1.5 V and -1.5 V. In the case of floating-gate

technology, the gate potential is isolated electrically from the rest of the circuit. However, it is not possible to completely isolate the input of the operational amplifier. The digital inputs were connected through two resistors to emulate the weighted sum of the inputs of the FGMOSFET at the negative input of the operational amplifier. To indirectly emulate fluctuations in threshold voltage, one of the digital inputs (V_{in1}) was set to $V_{\text{pp}} = 1.5$ V, where is defined as the amplitude of the pulse, from -0.75 V to +0.75V; while V_{in2} remained at $V_{\text{pp}} = 3$ V. Noise was provided by the white noise source of an electrical waveform generator HIOKI 7075. First, no response is present without noise, but the circuit correctly generates the output of the SR NAND gate as the standard deviation of noise increases, as shown in Fig. 4.15.

4.4.3 Delay time of the stochastic-resonance logic gates

Owing to the stochastic nature of the SR logic, the response of the gates exhibits an unpredictable delay time. Figure 4.16 shows the frequency of the delay time t_{d} for intervals corresponding to 5 ms from 0 ms to 115 ms. These results correspond to the response of the SR NAND gate, where the time difference t_{d} between the input toggles and the output toggles was obtained.

Figure 4.16 shows that $t_{\text{d}} = 25$ ms is more likely to occur. The presence of t_{d} is critical for high-complexity synchronous digital circuits, where precise synchronization among digital blocks is required. Considering these results, the proper applications of the SR gates are in asynchronous circuit design.

However, there is a delay time associated with the response of the SR gates. This characteristic directs the applications of SR logic gates to the field of asynchronous circuit design rather than synchronous circuit design, where precise synchronization is required. In this framework, we proposed the basis for asynchronous circuit design based on the SR logic gates in the following chapter. As the previous statistical simulation shows, this delay time has a mean value. Although this result may direct asynchronous circuit design on the basis of the worst-case approach for the delay time, it also requires a precise timing analysis, not only for a single logic gate, but for the entire circuit. This approach also requires the implementation of delay elements to synchronize control signals with data. A second approach assumes the design of delay-insensitive asynchronous circuits. These circuits are correct by design, and it is not necessary to add delay

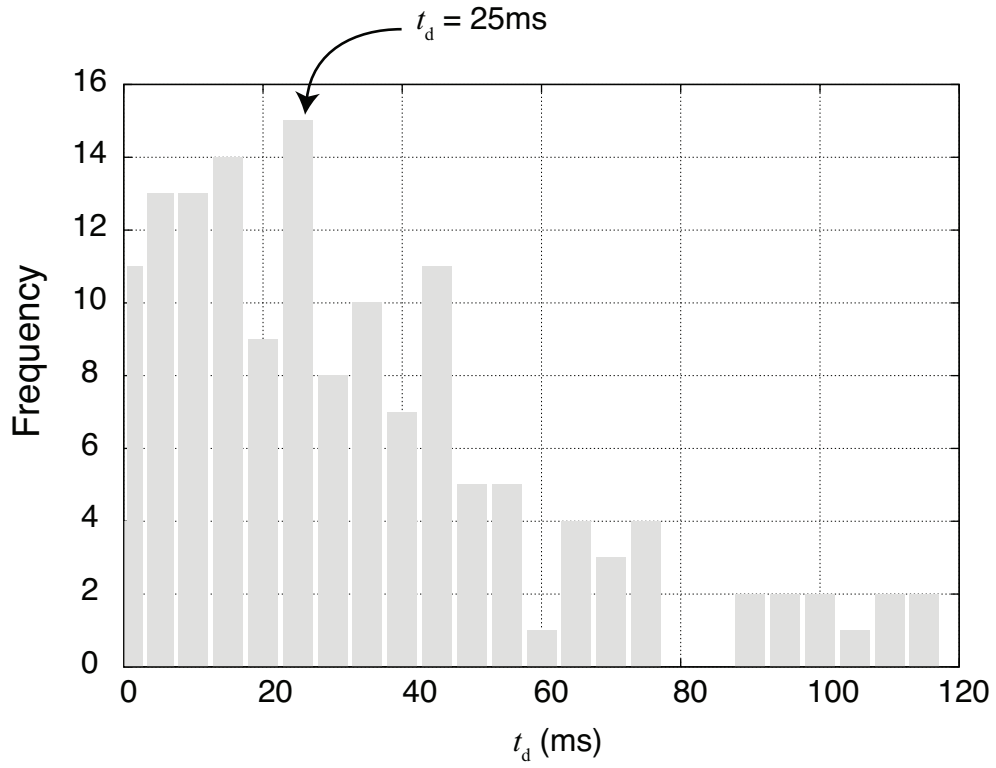


Figure 4.16: Histogram for the delay time t_d of the response of the SR NAND gate

elements. This approach is the most suitable model for implementing our current work. The first step is to propose a configuration for one of the basic blocks of delay-insensitive asynchronous circuit design : the C-element. This element plays a key role in controlling the synchronization of several inputs arriving at different times owing to delays in their response. Next chapter includes the design of asynchronous logic circuits using the proposed SR logic gates in combination with the C-element.

The SR effect has been demonstrated to be an effective technique to detect weak stimuli in nonlinear systems. The main contribution of this section is the use the hysteresis characteristic in a differential-pair configuration to avoid spontaneous hazards and high-amplitude oscillations. Owing to the fact that all transistors operate in the subthreshold regime, the circuit achieves low power consumption. According to the electrical simulations, power consumption is on

the order of picowatts. In addition, the introduction of noise actually reduces the mismatch effect, which is more evident in subthreshold systems. The circuit simulations have demonstrated the effectiveness of using noise in the proposed configuration to build logical circuits. However, one of the limitations of these noise-driven logic gates is the timing response. Owing to the stochastic nature of this circuit, there is an unpredictable delay time. This drawback is critical for the correct performance of synchronous digital circuits, where precise synchronization among gates is required. In this regard, the most suitable application for these SR gates is asynchronous logic design. In the next chapter, we will study the design of high-level asynchronous circuit designs based on the SR logic.

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Chapter 5

Applications of stochastic resonance logic gates: Asynchronous circuits

5.1 Definition of asynchronous circuits

There is an easy example to explain the definition of asynchronous circuits [1]. Let's consider a winery in charge of producing wine bottles (Fig. 5.1); these bottles should be delivered one by one to the shop. In this example, the shop is in charge of supplying wine to the patron. However, there are some basic rules that must be followed. First, as soon as the shop is ready to receive a new bottle of wine, the winery should send it. If the bottle arrives before the patron picks a bottle up, then the bottle won't be received by the shop. To have a successful delivery, it is necessary then to have an efficient way to communicate, and to notify, for example when the shop is ready to receive a bottle of wine. Then, anytime the shop send a requirement to the winery, a new bottle will be delivered. A similar communication happens between the shop and the patron.

In a synchronous communication, the bottle would be delivered at discrete times, regardless the availability of the shop to receive the bottle of wine. If there are some delays in the delivery between the patron and the shop, then the bottles won't be correctly delivered. On the other hand, if bottles are produced faster, in order to deliver the next bottle, all stages must wait for the clock signal to deliver the next one, reducing the speed of tasks; here synchronous circuits rely their synchronization on a central clock Fig. 5.2.



Figure 5.1: Analogy of asynchronous circuits with a winery-shop-patron example

However, an asynchronous circuit behaves as the analogy with the winery-shop-patron problem, where instead of relying on a central clock to control timing, it relies on handshake protocols. These handshake protocols are based in control signals for communication among processes; requirement (req) and acknowledgment (ack) signal. These signals indicate when new data are required (indicated by a change of state of req signal) to perform a certain task and when the current task is accomplished (indicated by a change of state of the ack signal). Execution of instructions among stages relies on the exchange of these signals .

Therefore even in the presence of delays, information will be transmitted properly. So we can take this advantage to design delay-insensitive circuits. Moreover, there are another advantages over their synchronous counterparts. One of the main sources of power consumption in synchronous circuits comes form the clock, therefore, by eliminating clock, power consumption could be reduced considerably; the other advantage comes from timing. In the case of synchronous circuits, speed is limited by the frequency of the central clock, however here speed is limited by the own speed of the circuit, therefore circuit could work at higher speeds [2–4]. Next points enlist some advantages of asynchronous circuits:

- There is no clock skew: by definition is the difference on time between the arriving of clock signal to the different parts of the circuit. Considering that asynchronous circuits do not depend on the correct distribution of clock signals, clock skew is not present in asynchronous circuits.

- Lower power: synchronous circuits posses precharge and discharge of some

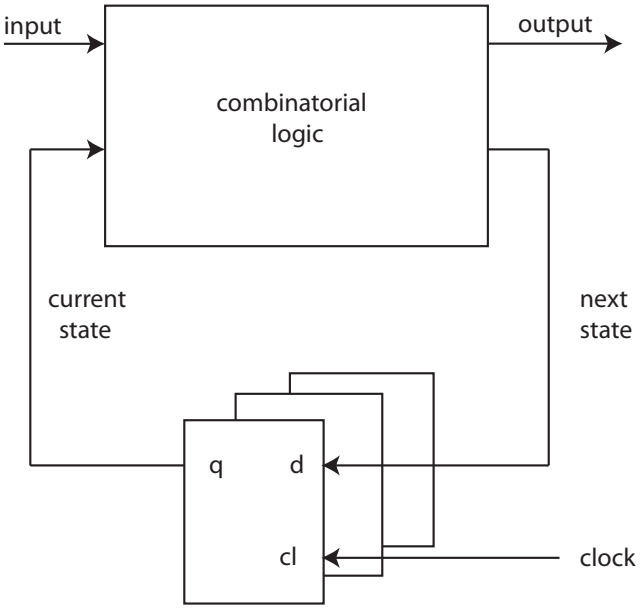


Figure 5.2: Synchronous circuit general scheme

stages that are not in use, consuming unnecessary power. In the case of asynchronous circuits, they generally have transitions only in areas involve with current computations.

- Average-case instead of worst-case performance
- Easing global timing issues: In the case of synchronous circuits, the timing depends on the slowest path.
- Better adaptation to physical properties: asynchronous circuits can detect when a computation has been done and run as soon as physical properties allow (variations in fabrication process, temperature, low-power supply).

In spite of all these advantages, still synchronous circuits are dominant in IC market. The reason is because asynchronous circuits also posses some disadvantages, such as a difficult design methodology. To design synchronous circuits, methodologies are already established, if clock frequency is reduced, problems

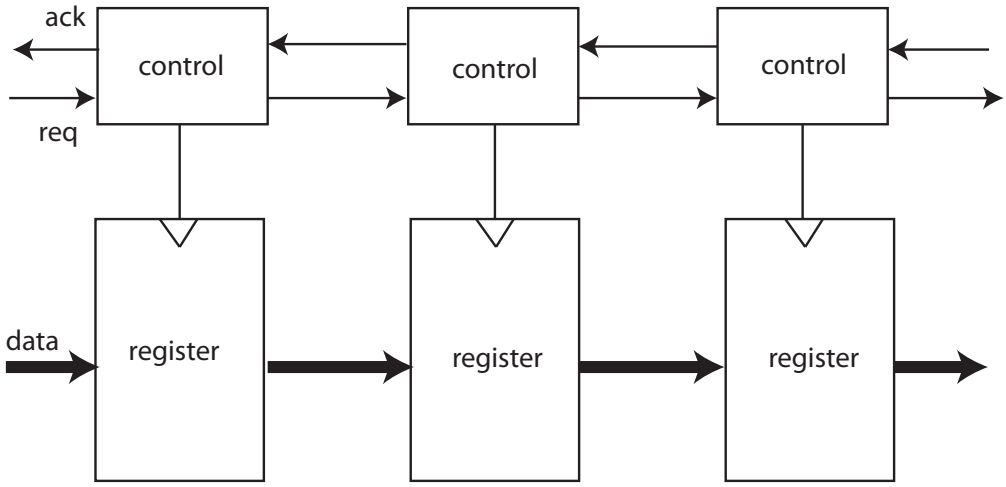


Figure 5.3: Asynchronous circuit general scheme

such as hazards and delay are removed automatically. In the case of asynchronous circuits, a deeper analysis is necessary, paying attention in the dynamics of each state. For complex designs, these analysis can be very difficult and time consuming, moreover there is a lack of available CAD tools to design asynchronous circuits. Testing and verification are yet too complex to handle adequately for asynchronous circuits.

To introduce the theory of asynchronous circuits, it is necessary to present the basic concepts. There are many data encodings, communication protocols and types of designs that can be used depending on the purpose. Next subsection will explore briefly the theory of the different kinds of asynchronous circuits.

5.2 Basic concepts

In this section, a brief introduction of asynchronous circuit design is reviewed in order to design asynchronous pipelines (backbones of asynchronous circuits) based on the stochastic-logic gates SR logic gates.

5.2.1 Delay models

The delay models dictates the assumption made about delays in the gates and wires during the design process. Basically there are four delay models, Delay-insensitive design (DI), quasi-delay-insensitive design (QDI), speed independent design (SI) and bounded-delay designs. DI designs consider unbounded delays, and they are the most robust of all delay models, however at gate level, it has already showed that DI design are not practical. This gives rise to the study of QDI designs, where gates and wires can have arbitrary delays, except in the case of wire folks (*iscochronic*); if this condition is true, QDI designs are robust as DI designs, and allow DI designs are gate level; because of this reason, a QDI design is chosen in this study. The last two models, Speed Independent (SI) design consider wire delays to be negligible and bounded-delay designs consider the maximum and minimum bounded delays of all gates (this model is the least robust in the presence of unknown delays).

5.2.2 Data encoding

Data encoding in asynchronous circuits is basically divided into two groups: "bundle data" and "dual-rail data" [5]. The first one (Fig. 5.4) uses only one channel to communicate between stages, therefore extra channels are necessary to send the control signals. Data and control signals must arrive at the same time; therefore it is also necessary extra circuitry to interpret control signals; moreover both, data and control signals must arrive on time, otherwise synchronization problems may arise. Delays are compensated through the use of delay elements (such as inverters, that are area and power consuming elements).

The second one is the dual-rail protocol. In this protocol data is encoded into two channels, this means that one bit is mapped into a two bit representation. Dual-rail data encoding refers to converting one bit to two-bit encoding (Fig. 5.5), where valid data are given by {0, 1} and {1, 0} which represents 0 and 1 logic respectively. {0, 0} is a spacer between valid data and {1, 1} is not used (Fig.5.6). Another advantage of the dual-rail data encoding is that it contains the *req* signal implicit in the data (where {0, 1} or {1, 0} represents a *req* signal equal to one); therefore, an additional channel for *req* signal is not necessary, neither synchronization problems may arise.

This type of protocol is actually more robust in terms of delay tolerance but the number of channels also increased with the number of bits. However it may

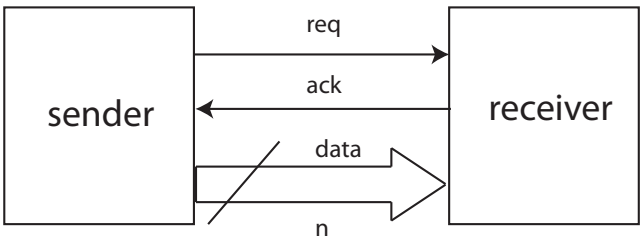


Figure 5.4: Bundle data encoding

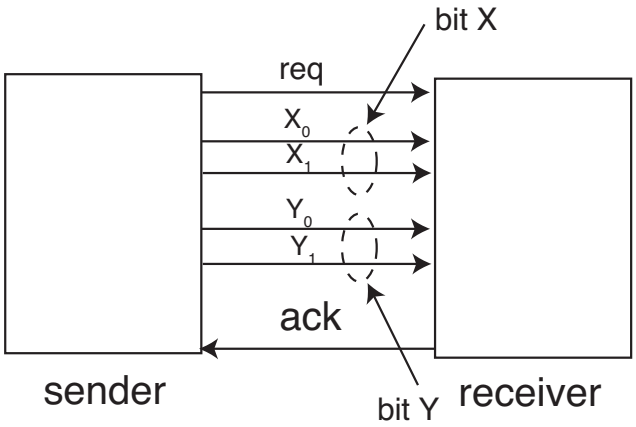


Figure 5.5: Dual-rail data encoding

allow the design of delay-insensitive circuits following determined strategies, thus it is chosen for this study.

	Codeword
Data 0	{0, 1}
Data 1	{1, 0}
Spacer	{0, 0}
Not used	{1, 1}

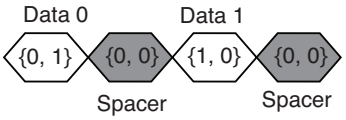


Figure 5.6: Dual-rail data representation

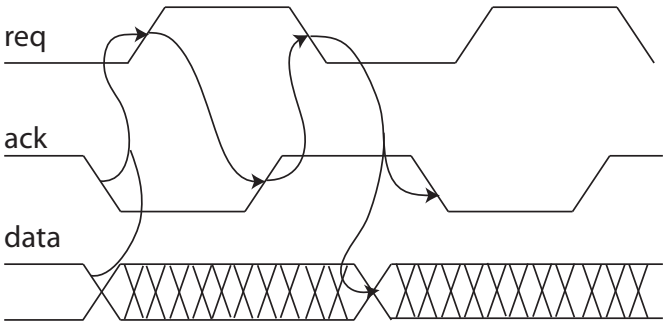


Figure 5.7: Four-phase protocol

5.2.3 Communication protocols

Dual-rail data encoding requires a four-phase protocol for data transmission (Fig. 5.7). The four-phase protocol resets the signals *req* and *ack* when the current task has been completed, in contrast with the two-phase protocol (Fig. 5.8), where a reset it is not necessary. To implement dual-rail encoding, data are necessary to design dual-rail logic gates based on their single-rail counterparts.

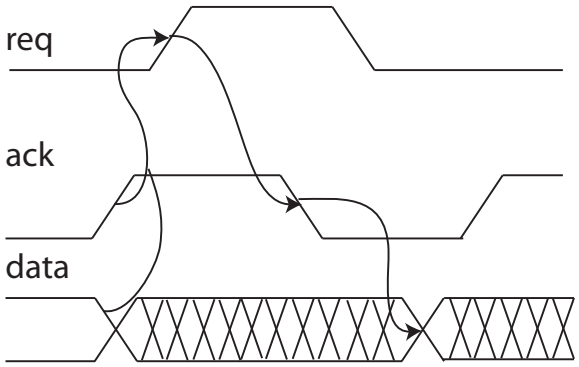


Figure 5.8: Two-phase protocol

5.3 Dual-rail gates based on stochastic-resonance logic gates

In this section, simulation results are presented for a AND/NAND logic gate based on SR gates. Simulations were performed in SPICE for a 0.18-μm CMOS technology.

5.3.1 Circuit design

Figure 5.9 shows the implementation of a dual-rail AND/NAND logic gate based on SR gates. Here the inputs have a two-bit representation, and NOT operation can be easily performed by inverting the outputs, thus, the same configuration can be used to implement AND or NAND operation, depending on the position of the output bits O_0 and O_1.

5.3.2 Simulation results

Here we show electrical simulations of the dual-rail NAND/AND gate (Fig. 5.10), where the power supply was set to $V_{\rm dd} = 0.35$ V and the standard deviation of noise to $\sigma_{V_{\rm noise}} = 0.27$ mV. Figure 5.10 shows the simulation results, where two cases are present: without noise and with noise. In the first case, owing to the

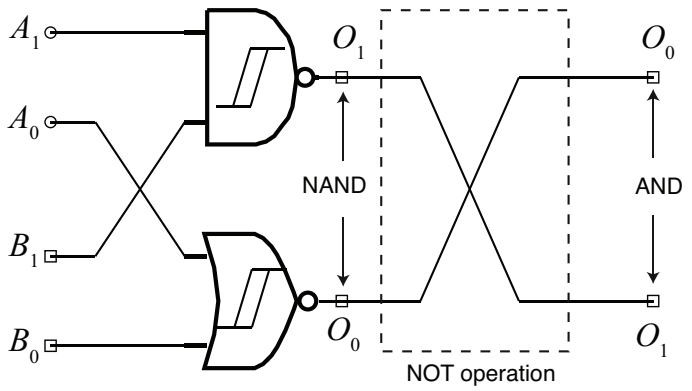


Figure 5.9: Dual-rail SR AND/NAND gate

presence of mismatches, the logic functions are not generated. In the second case, when noise is applied, the logic functions are recovered, demonstrating the beneficial effect of noise.

5.4 Asynchronous logic components with hysteresis

Table 5.1: C-element state table with input voltages mapped as logic inputs

V_{in1}	V_{in2}	Y
0	0	0
0	1	Y^{-1}
1	0	Y^{-1}
1	1	1

As we mentioned previously, we proposed a suitable application in the field of asynchronous circuit design for the SR logic gates owing to the timing limitations. In the case of asynchronous circuit design, the performance of a circuit does not rely on a central clock but on handshaking protocols. Although there is not an established methodology for designing asynchronous logic, there are some basic

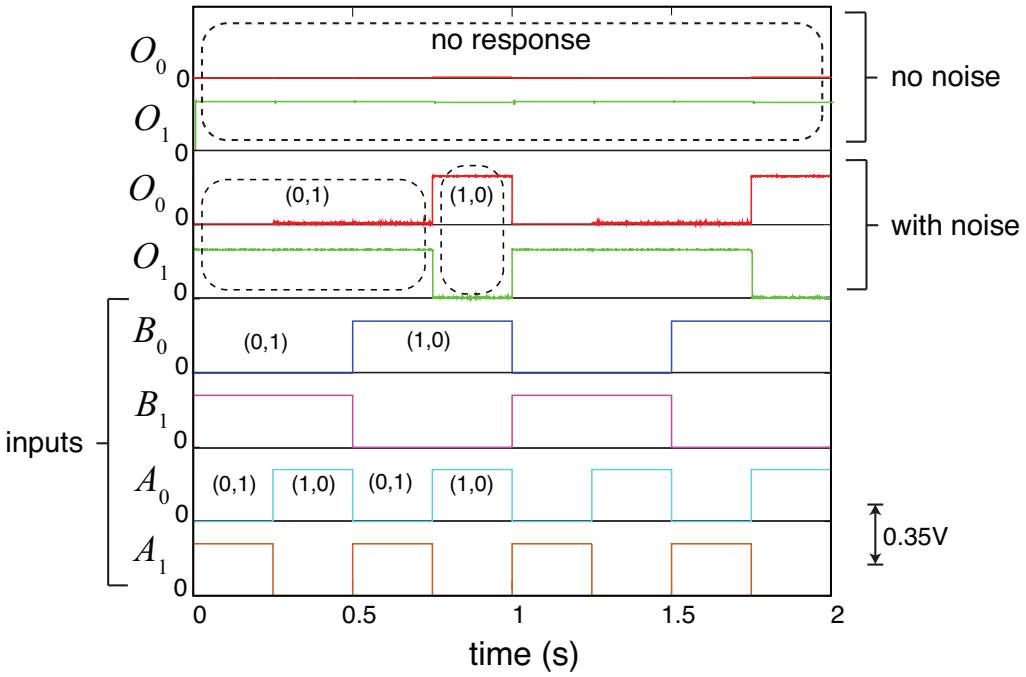


Figure 5.10: SPICE simulations for the dual-rail SR AND/NAND gate (case with noise)

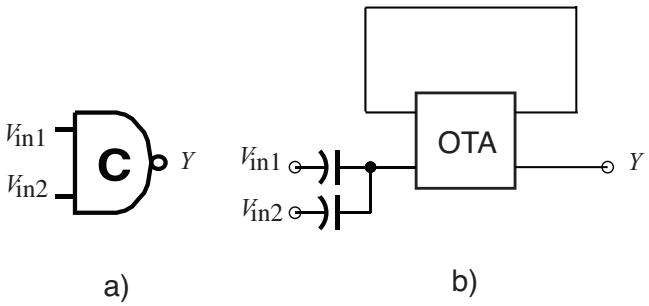


Figure 5.11: Electrical symbol for the C-element (b), and implementation of the C-element using an OTA (b).

digital circuits that are different from those in synchronous logic. Therefore, there are some necessary configurations required to implement certain functions of the asynchronous logic in addition to the basic logic gates, as in the case of the C-

element, which is one of the main elements in asynchronous circuit design. The C-element is a hysteresis element that verifies the state of current inputs, and its electrical symbol is shown in Fig. 5.11a. The output will change either to 1 or 0 when both inputs are set to 1 or 0 respectively, however, when inputs are different, previous state will be kept (Table 5.1). This property is really important at the moment to verify the current state of input data.

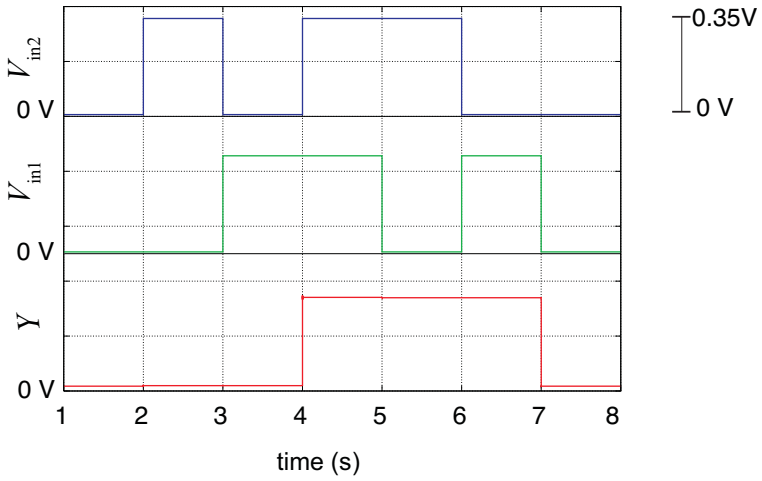


Figure 5.12: Simulation results for the C-element.

This configuration can be implemented as shown in Fig. 5.11b using the same OTA configuration. In this case, the feedback allows the previous state to be stored until both the inputs attain the same value. The simulation results are shown in Fig. 5.12 for a power supply of 0.35 V.

5.5 Asynchronous pipelines

The main purpose of this section is to present a brief introduction of asynchronous pipelining. Pipelining represents one of the foundations for high-performance asynchronous digital systems design [6]. For asynchronous circuits, a protocol for interaction between stages is necessary, as well the type of data encoding and storage elements [7–11]. Additionally, an explicit distributed control structure must be designed. All these elements constitutes the skeleton for coordinating the blocks of pipelined asynchronous circuits.

The advantages of pipelined asynchronous systems over their synchronous counterparts could be enlisted as follows:

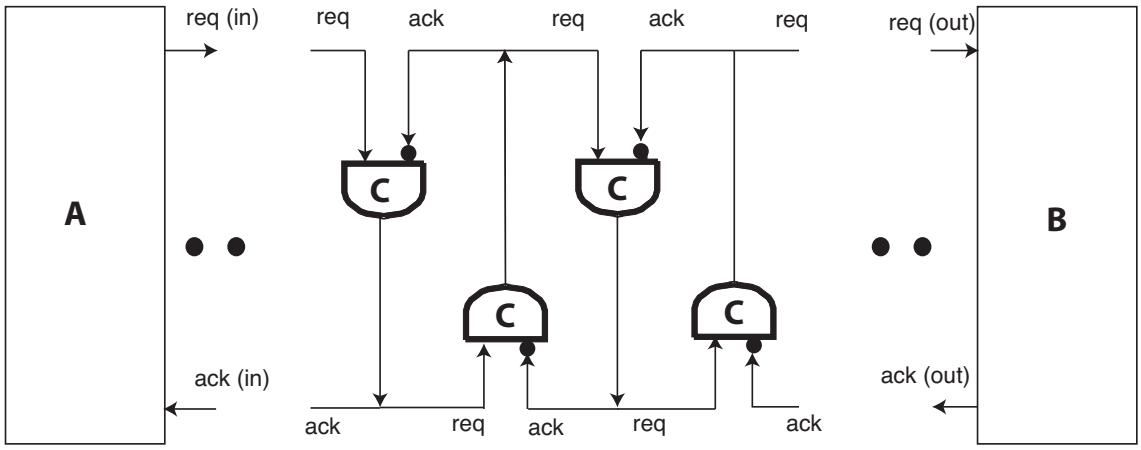


Figure 5.13: Muller pipeline

- Dynamic power that naturally adapts to the actual traffic.

- Flexibility to handle variable input and output rates and delay stages.

- Ability to support dynamic voltage and frequency scaling as interface.

- Ability to serve as an interface to connect unrelated synchronous clock domains.

Some future applications are found in the field of nanotechnology, where new devices, such as carbon nanotubes are looking towards asynchronous pipelines as organization structures due to its ability to deal with timing irregularities.

Basically, asynchronous pipelines have three components: data (i.e. channels and logic blocks), control, and latches. Figure 5.13 shows one of the traditional asynchronous pipeline configurations. In this circuit, data transmission relies on the control signals *req* and *ack*

5.6 Asynchronous pipelines based on stochastic-resonance logic gates

As it was reviewed previously, in delay-insensitive design it is assumed that the delays of the gates and wires is unbounded and thus the circuit will work correctly for any arbitrary set of time-varying gate and wire delays. This is the most conservative and robust model, but it has been shown that it is not very practical because very few DI circuits exist. Therefore the notion of quasi-delay circuits have been developed. These circuits work correctly regardless of the values of the delays in the gates and wires, except for those associated with wire forks. If this forks are physically localized to a small region, QDI circuit can be practically as robust as DI circuits. Therefore, this section presents an example of a QDI template pipeline: the Weak-Conditioned Half Buffer pipeline or WCHB pipeline.

5.6.1 Circuit design

Figure 5.14 shows the block diagram of a WCHB pipeline, and the implementation based on SR gates is shown in Fig. 5.15 for a three-stage WCHB pipeline. This pipeline is based on a dual-rail encoding, where $L_{0,0}$ and $L_{0,1}$ are the dual-rail input data. The C-element will evaluate when the next stage is ready to receive new data ($L_{ack,n}$ =1), and the SR NAND gate will evaluate when data has been received. Next subsection will show the simulation results for this configuration.

5.6.2 Simulation results

Data transmission is shown in Fig. 5.16 for a three-stage WCHB asynchronous pipeline based on the SR gates (under the presence of intentional mismatch among transistors). Here, data transmission is achieved successfully under the presence of noise. The signals at the bottom of the figure represent input data, in which every time data have been passed to the next stage (*ack* signal = 1), is generated new data, alternating between {0, 1} and {1, 0} (0 and 1) with the reset (spacer) between valid data. The red lines represent data of channel 0 ($L_{\mathrm{n},0}$), and the blue ones represent data of channel 1 ($L_{\mathrm{n},1}$). Note that data transmission is accomplished regardless different values of delays among stages.

Figure 5.17 shows in greater detail the control signals *ack* and *req* that help accomplish data transmission between stages 1 and 2.

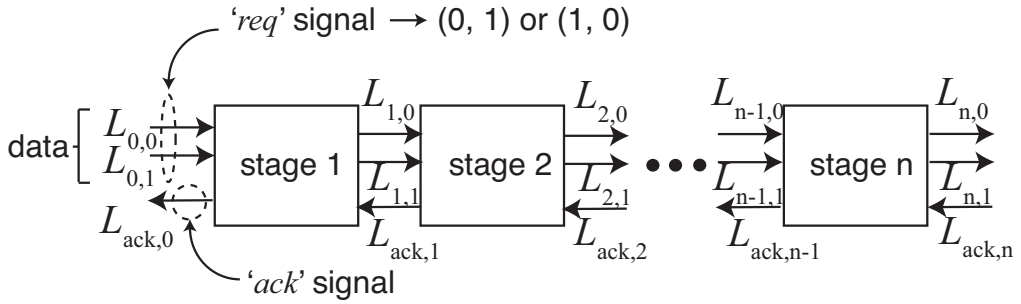


Figure 5.14: WCHB pipeline diagram block

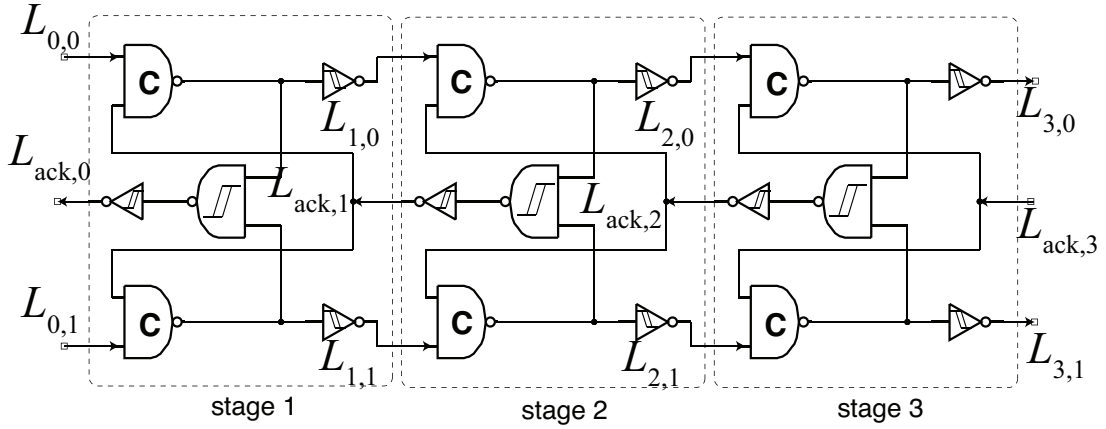


Figure 5.15: Three-stage WCHB asynchronous pipeline

Moreover, the general performance of the three-stage WCHB pipeline is described in greater detail in terms of the power consumption and error rate. Figure 5.18 shows the simulation results of the power consumption (P) versus standard deviation of noise ($\sigma_{V_{\text{noise}}}$), where a linear relationship between the parameters is observed. The power consumption is 105 pA for our current setting ($V_{\text{dd}} =$ 0.35 V), demonstrating that the pipeline is consuming low power. Additional simulations were performed for the error rate (%) versus ($\sigma_{V_{\text{noise}}}$), where a zero tolerance is demonstrated for a $\sigma_{V_{\text{noise}}}$ value less than 0.25 V(Fig. 5.19).

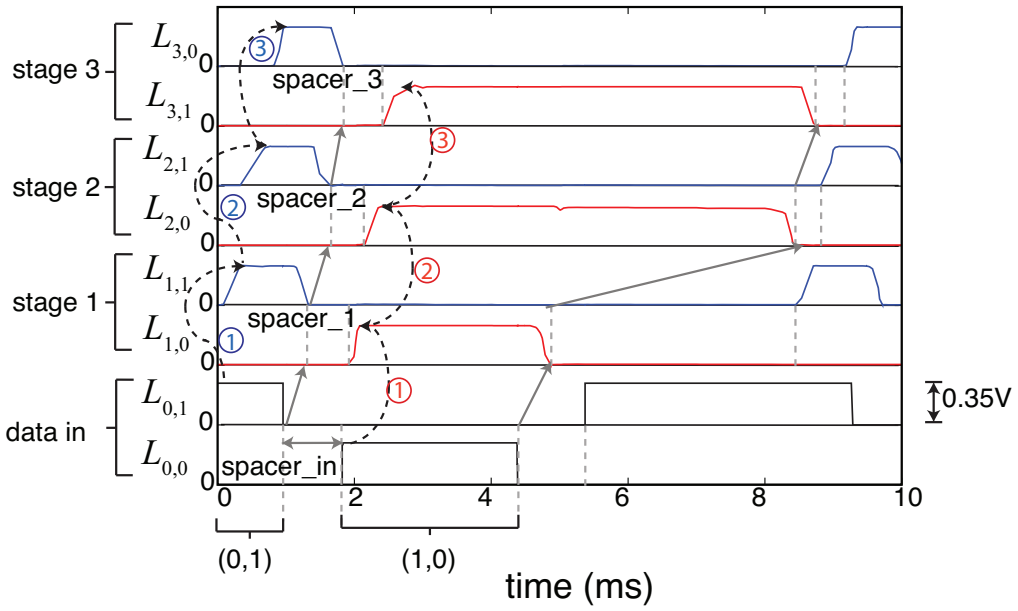


Figure 5.16: SPICE simulations for the WCHB asynchronous pipeline based on SR logic gates (case with noise)

5.7 Implementation of asynchronous pipelines based on stochastic-resonance gates utilizing an operational amplifier

In order to confirm the physical performance of the WCHB pipeline, this section shows the circuit design of the WCHB pipeline based on a Operational amplifier OP284.

5.7.1 Circuit design

In addition to the simulations, a three-stage WCHB pipeline was built using an operational amplifier OP284 connected with a positive feedback to generate a hysteresis characteristic. SR logic gates were built using the configuration shown in Fig. 5.20, where electrical parameters are the same as those used in subsection

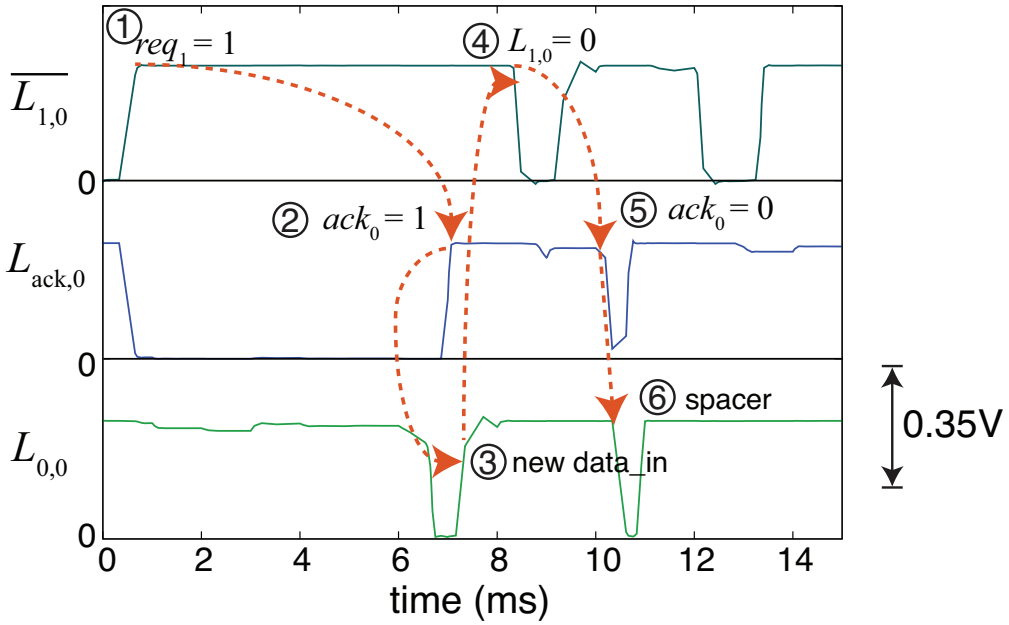


Figure 5.17: Control signals between stages 1 and 2 of the WCHB asynchronous pipeline

4.4.2.

5.7.2 Experimental results

Note that the circuit used for experimental results does not correspond to the practical implementation of the circuit for SR logic gates of Fig. 5.15, but it is used to demonstrate how the noise can be utilized in nonlinear circuits to recover logic functions in the presence of mismatches. Therefore, parameters such as power consumption and delay time vary from those of simulation results. Figure 5.21 shows the experimental results of data transmission between the three stages, and it is seen that data are transmitted independently of the presence of delays. Figure 5.22 shows the control signals between stages 1 and 2. The implementation of this circuit is shown in Fig. 5.23.

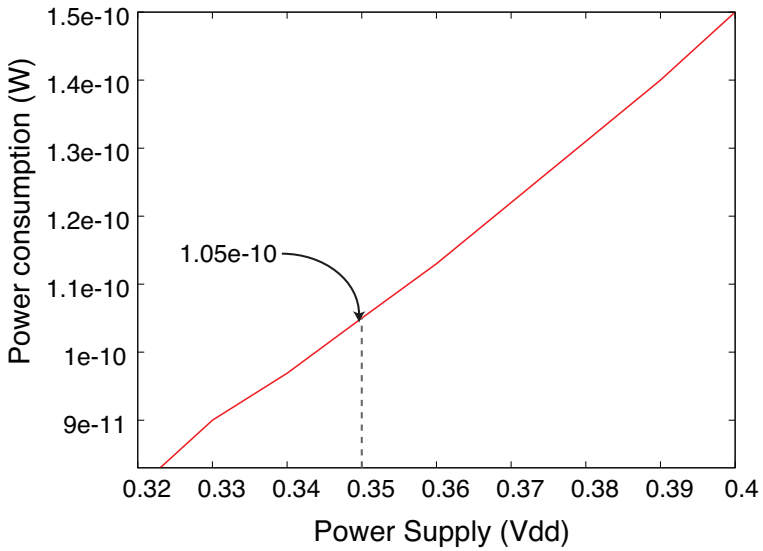


Figure 5.18: Power consumption of the three stage WCHB asynchronous pipeline

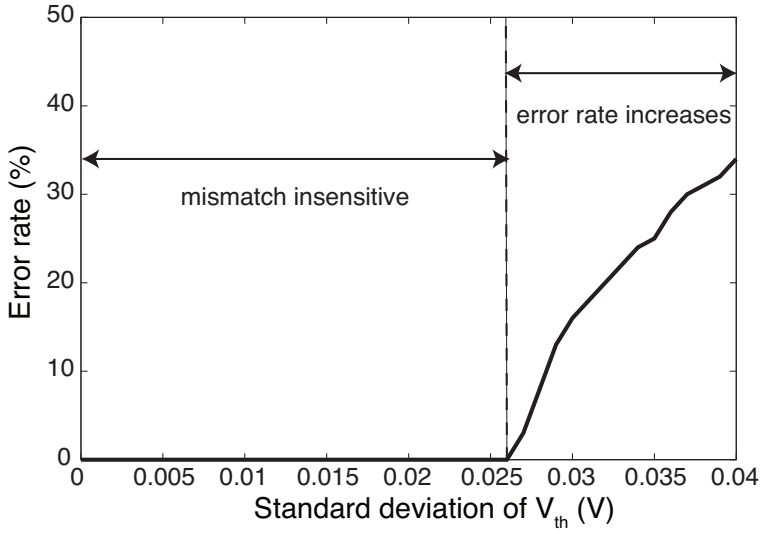


Figure 5.19: Error rate versus $\sigma_{V_{\mathrm{th}}}$ (V)

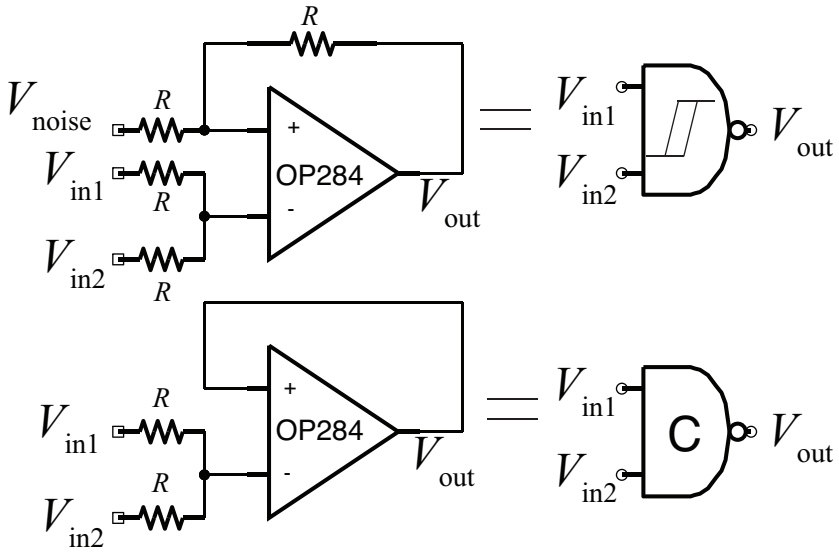


Figure 5.20: OP284 configuration to implement the SR NAND gate and the C-element

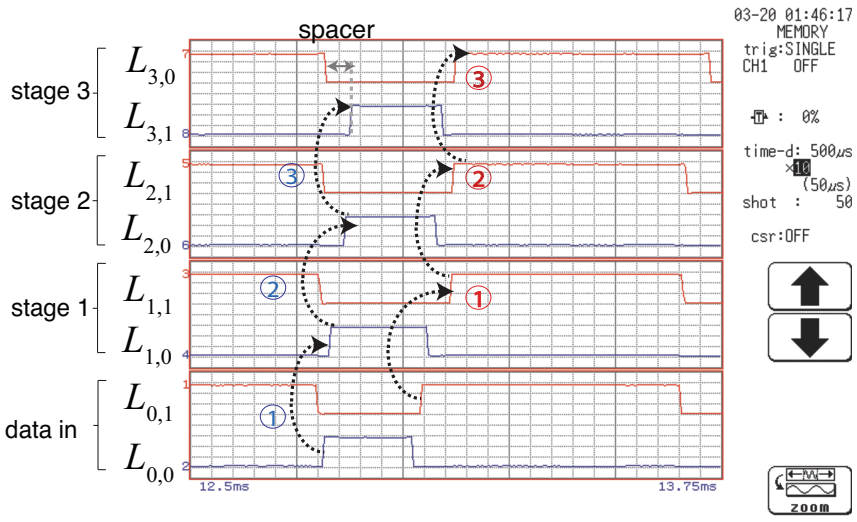


Figure 5.21: Experimental results for the three-stage WCHB asynchronous pipeline (data transmission), obtained from a Memory Hicorder HIOKI 8826

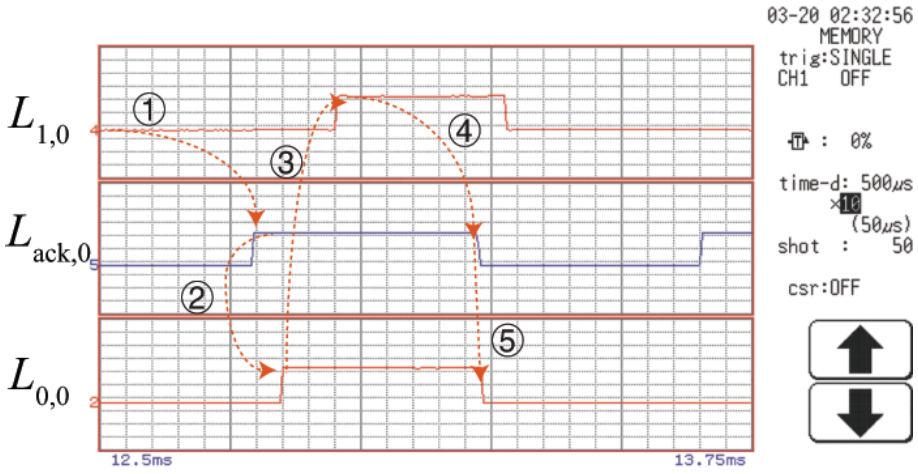


Figure 5.22: Experimental results for the three-stage WCHB asynchronous pipeline (acknowledge signal between two stages)

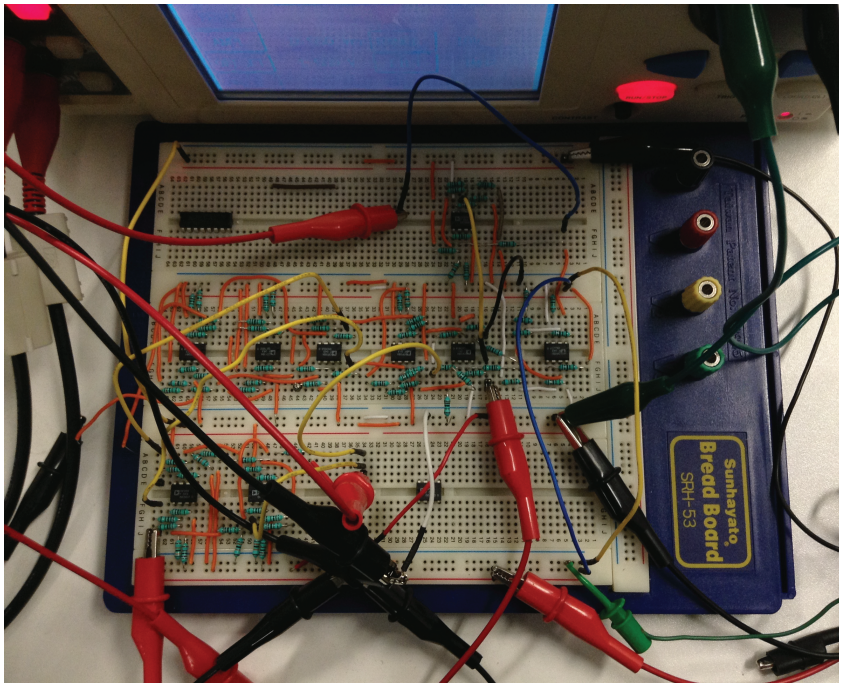


Figure 5.23: Breadboard implementation of the three-stage WCHB asynchronous pipeline based on OP284

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Chapter 6

Conclusions

Noise-driven circuits have an inspiration in biological systems and how they are resilient against noisy environments. Based on several studies in the field of biology and neuroscience, it was found that noise plays a beneficial role from cellular to cognitive levels in a wide variety of species, including humans. In chapter 2, a recompilation of several of these examples was revised. Although a big debate has emerged in the scientific community regarding the true existence of stochastic resonance effect, many experimental and theoretical works in the field of physics, mathematics, biology, engineering, etc., suggest the existence of this phenomenon.

Among many applications in engineering, stochastic resonance may be applied in the field of nanoscale devices. The presence of parameter fluctuations in nanoscale transistors and emerging devices is unavoidable, therefore designers must look into new alternatives to overcome those problems. In my opinion, studying how biological structures have evolved during millions years to perform certain tasks, may provide a hint on how to create noise and parameter-variation tolerant designs. These systems have already provided some remarkable applications in the field of electrical engineering. Therefore, this thesis was dedicated to the study of noise-driven phenomena and their applications for electrical circuits. The main points of this theses are summarized as follows:

- The first application of this work consisted in the study on how dynamical noise can assist electrical spike transmission. Simulation results proved that the introduction of noise was a key factor for the correct transmission of spikes in the prescience of parameter variations.

- The second application presents the basis of a new kind of logic gates.

These gates are based on a noise-driven design and presents the following characteristics:

  - Tolerance to parameter fluctuations
  - Low-power consumption
  - Stable output independently of the introduction of noise

  Although the circuit configuration is based on transistors (operational amplifier configuration), this idea can be further mapped into emerging devices.

- The third part of this work is devoted to solve the timing issues of SR gates. Different techniques may provide a solution for this problem,as in the case of asynchronous circuit designs. Asynchronous circuit design represents a solution to design delay-insensitive circuits and they have been already been applied to solve timing problems at device level, such as in the case of nanotubes devices. Therefore, in this study also is explored the theory of asynchronous circuit design to solve the problem of unpredictable delays due to the dependance of SR gates in stochastic processes. Results are summarized as follows:

  - Delay-insensitive circuits based on SR gates were designed and implemented based on asynchronous circuit theory
  - The speed of the circuit will depend in the time of delays
  - In terms of speed, SR gates should be applied in systems where speed is not an issue, but lower consumption and fluctuation-tolerant designs are required

Further, the utilization of noise-driven designs as an alternative to design more robust circuits could represent a solution to the current demands in IC design industry. Although, noise-driven systems may not represent the ultimate solution for all problems related with device miniaturization, they could provide an alternative tool to be considered together with the development of new design strategies; after all the most efficient designs in nature have adopted external and internal fluctuations as a beneficial part to achieve robustness and low-power consumption in some cases.

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List of publications

1. Papers published in academic peer reviewed journals

1. Gonzalez-Carabarin L., Asai T., and Motomura M., "Application of nonlinear systems for designing low-power logic gates based on stochastic resonance," *Nonlinear Theory and Its Applications*, vol. 5, no. 4, pp. 445-455, 2014.

2. Gonzalez-Carabarin L., Asai T., and Motomura M., "Low-power asynchronous digital pipeline based on mismatch-tolerant logic gates," *IEICE Electronics Express*, vol. 11, no. 15, pp. 20140632/1-9, 2014.

3. Gonzalez-Carabarin L., Asai T., and Motomura M., "Impact of noise on spike transmission through serially-connected electrical FitzHugh-Nagumo circuits with subthreshold and suprathreshold interconductances," *Journal of Signal Processing*, vol. 16, no. 6, pp. 503-509, 2012.

2. Invited Talk

1. Gonzalez-Carabarin L. and Asai T., "Asynchronous digital circuits based on stochastic resonance for coarse-grained/low-voltage devices," *CMOS Emerging Technologies Research 2014 Symposium*, MINATEC, Grenoble, France (Jul. 7-8, 2014).

3. International Conference Proceedings

1. Gonzalez-Carabarin L., Asai T., and Motomura M., "Dual-rail asynchronous pipeline based on stochastic resonance logic gates," *Proceedings of the 2014*

International Symposium on Nonlinear Theory and its Applications, pp. 85-88, Cinema of Bourbaki Panorama, Luzern, Switzerland (Sep. 14-18, 2014).

2. Gonzalez-Carabarin L., Asai T., and Motomura M., "Asynchronous digital circuit design using noise-driven stochastic gates," *2013 International Symposium on Nonlinear Theory and its Applications*, Santa Fe Community Convention Center, Santa Fe, U.S.A. (Sep. 8-12, 2013).

3. Gonzalez-Carabarin L., Asai T., and Motomura M., "Towards asynchronous digital circuit design based on stochastic resonance," *The 1st International Conference on Nanoenergy*, Hotel Gio, Perugia, Italy (Jul. 10-13, 2013).

4. Gonzalez-Carabarin L., Asai T., and Motomura M., "Spike propagation in excitable systems enhanced by membrane-potential-dependent noise," *The 2012 International Symposium on Nonlinear Theory and its Applications*, Gran Melia Victoria, Majorca, Spain (Oct. 22-26, 2012).

5. Gonzalez-Carabarin L., Asai T., and Motomura M., "Spike transmission in locally coupled excitable circuits enhanced by membrane-potential-dependent noise," *Asia Conference on Nanoscience and Nanotechnology 2012*, Crowne Plaza Lijiang Ancient Town, Yunnan, China (Sep. 7-10, 2012).

6. Gonzalez-Carabarin L., Asai T., and Motomura M., "Noise impact on spike transmission through serially-connected electrical FitzHugh-Nagumo model with subthreshold and suprathreshold interconductances," *The 16th International Conference On Cognitive and Neural Systems*, Boston University, Boston, U.S.A. (May 30-Jun. 1, 2012).

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4. Awards

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5. Domestic Conference Proceedings

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2. Gonzalez-Carabarin L., 浅井 哲也, 本村 真人, "Mismatch-tolerant stochastic logic gates and their application to low-power asynchronous VLSI circuits," *LSI* とシステムのワークショップ, P27, 北九州国際会議場 (北九州市), 2014 年 5 月 26-28 日.

3. Gonzalez-Carabarin L., 浅井 哲也, 本村 真人, "Stochastic Circuit Design for Molecular Architectonics," 第 *4* 回分子アーキテクトニクス研究会, 東京大学山上会館 (東京), 2014 年 3 月 11-12 日.

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