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GROWTH AND SPIN TRANSPORT IN INAs NANOWIRES

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To my family

Abstract

In recent years, InAs nanowire has been revealed to be a 1-dimensional nanostructure with outstanding promise for device applications because of its high electron mobility and strong quantum confinement effects. In this thesis, InAs nanowires have been proposed as fine spin transport channels for spintronics device applications, particularly, the Datta-Das spin field effect transistor. The growth processes, based on vapor-liquid-solid techniques using molecule beam epitaxy system, have been developed. With these growth processes, InAs nanowires and InAs/InP core/shell nanowires have been grown. In addition, the electrical transport properties, particularly, the spin transport properties have been investigated. Reduced spin relaxation and enhanced transport properties in our core/shell nanowires have been confirmed. Furthermore, we have demonstrated the growth of $\langle 110 \rangle$ -oriented InAs nanowire with a palladium catalyst. Compared with other $\langle 111 \rangle$ -oriented InAs nanowires our $\langle 110 \rangle$ InAs nanowire shows an outstanding transport property. We attribute this transport superiority to the stable zinc-blende crystal structure with no wurtzite stack defects. Finally, with a single nanowire Hall-bar device, the electrical transport properties of $\langle 110 \rangle$ InAs nanowires have been investigated.

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Sapporo

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Chapter 1

Introduction

The field effect transistor (FET) is the basic logical cell for modern integrated circuit. The FET controls the flow of electrons (or holes) from the source to drain by voltage applied across the gate and source terminals. However, the scaling technology, which is supporting the development of FET, is facing the physical limitation. The researches of logical device based on new operation mechanisms theory are essential. Among numerous device proposals, the spin field effect transistor (Spin-FET) proposed by Datta and Das [1] has attracted a lot of attention. As the logic of Datta-Das Spin-FET is depend on the orientation of electron spin, the energy cost could be lowered substantially compared with the classical FET. Furthermore, the manipulation of electron spin would provide a lot of possibilities for quantum computing. Meanwhile, the successful operations of the Spin-FET require an effective semiconductor channel which is able to provide sufficient capacities for transport and manipulation of electron spin. In recent years, indium arsenide (InAs) nanowire becomes a platform for quantum information processing as a low dimension material. In this thesis, we propose to apply InAs nanowire to Spin-FET structure as a electron spin channel, and further investigate the growth methods and feasibility for spin manipulation and transportation.

1.1 Datta-Das Spin FET

The FET is the basic logical cell for modern integrated circuit. The FET, similar to a water faucet owning three terminals, controls the flow of electrons (or holes) from the source to drain by voltage applied across the gate and source terminals, shown in Fig. 1.1a. The development of FET depending on the scaling process technology improved successfully following Moore's Law [2]. Until recent years, however, it is more difficult to drive Moore's law down to 20 nm because the process technologies are facing the physical limitations. And the limitation of sub-threshold swing [3] is 60mV/dec at room temperature (300K). Meanwhile, the spintronics, where it is not the electron charge but the electron spin that carries information, offers opportunities for a new generation of electronic devices including logical computing devices.

Among numerous spintronics device proposals, the spin field effect transistor (Spin-FET) proposed by Datta and Das has attracted a lot of attention, shown in Fig.1.1b [1]. According to this idea, electron spins, which are injected from a ferromagnetic (FM) source terminal into a semiconductor channel, controllably undergo precession during their passage from source to drain by means of the spin-orbit interaction. The orientation of electron spin at the end of channel can be sensed by the ferromagnetic drain terminal. The successful operation of the Spin-FET requires an effective semiconductor channel that is able to provide sufficient capacities for transport and manipulation of electron spin. For electron manipulation by gate voltages, the channel material with strong spin-orbit interactions is essential.

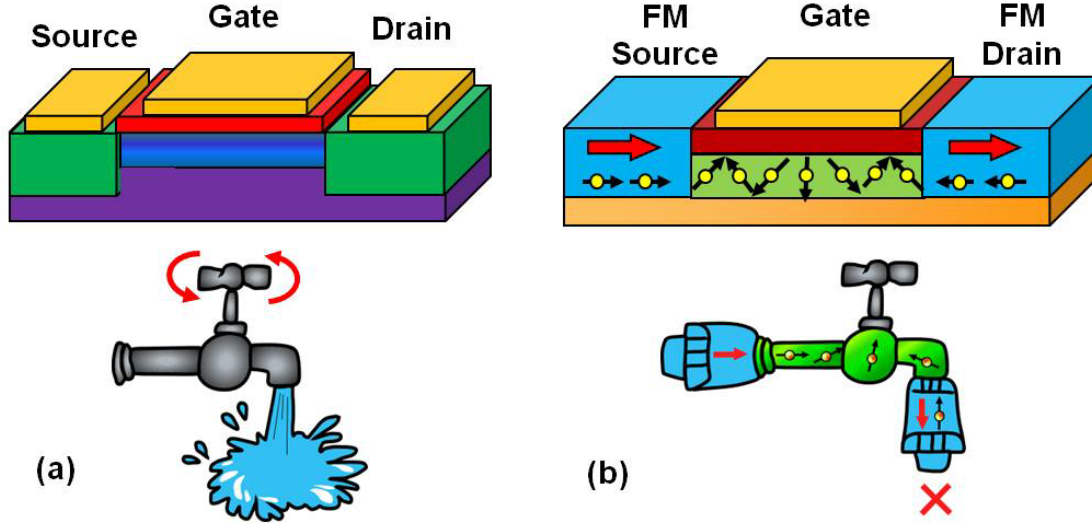


Figure 1.1: Schematic of FET and Spin-FET. (a): Classic FET similar to a water faucet owning three terminals, using electron flow to carry information. (b): A Spin-FET owning spin filter drain and source terminals and using electron spin to carry information.

1.2 Spin Orbit Interactions

In solids such as semiconductor materials, the velocity of moving electrons is so high that any net electric field seen by the moving electron is a momentum dependent effective magnetic field. The Hamiltonian including spin-orbit interaction is

$$H = \left[\frac{p^2}{2m} + V + \frac{\hbar}{4m^2c^2} (\nabla V \times p) \cdot \sigma \right], \quad (1.1)$$

where p is the momentum of electrons, V is the electrostatic potential, σ is the vector of Pauli matrices. The electrostatic potential V can be caused by bulk inversion asymmetry (BIA) in the semiconductor material, known as Dresselhaus spin-orbit interaction [3]. In III-V and II-VI semiconductors, such as GaAs, InAs, and InSb, there is an underlying inversion asymmetry between different atoms. Similarly, the electrostatic potential can be driven by any other nonuniform charge densities, which can exist in a heterostructure or be built by an external gate voltage. This is

known as structure inversion asymmetry (SIA) or Rashba spin-orbit interaction [4]. These two kinds of spin-orbit interaction are most to be explored in the spintronics fields for electron spin manipulations.

In the proposal of Datta-Das Spin-FET, Rashba spin-orbit interaction is used to perform controlled rotations of electron spins passing through a 2-dimensional semiconductor channel. The Rashba spin orbit interaction is due to the inversion asymmetry of the confining potential, which can be modulated by the external gate voltage. As shown in Eq. 1.2, the β is tunable in strength by the external gate voltage. One can use this property to control electron spin by electric field instead of magnetic field or light, which is important for nanoscale device performance and real application in the future.

$$H_R = \frac{\alpha}{\hbar}(p_x\sigma^y - p_y\sigma^x) \quad (1.2)$$

Similarly, in the 2-dimensional system, Dresselhaus spin-orbit interaction can be described as Eq.1.3.

$$H_D = \frac{\beta}{\hbar}(p_x\sigma^x - p_y\sigma^y) \quad (1.3)$$

In this study, we focus on these two most important spin orbit interactions for Datta-Das Spin-FET, and, the Hamiltonian of spin orbit interaction can be written as Eq.1.4.

$$H_{S.O.} = \frac{\alpha}{\hbar}(p_x\sigma^y - p_y\sigma^x) + \frac{\beta}{\hbar}(p_x\sigma^x - p_y\sigma^y) \quad (1.4)$$

1.3 Semiconductor Spin Transport Channel

As discussed above, a semiconductor channel owning spin transport and manipulation properties is the essential part of the Datta-Das Spin-FET. In this semiconductor channel, the electron spin encoded information should be conserved

for relatively long time, which should be comparable to the electron spin transport time from the source to the drain terminal. And this transport of the spin information corresponds to a nonequilibrium state of electron spins. However, there are four major physical spin relaxation mechanisms responsible for spin equilibrium in nonmagnetic electronic systems: Elliott-Yafet (EY) [5], D'yakonov-Perel' (DP) [6], Bir-Aronov-Pikus (BAP) [7], and hyperfine interaction processes. [8] Therefore, the keys to achieve the operation of the Datta-Das Spin-FET are the suppressions and the utilizations of these spin relaxation mechanisms in the semiconductor channel.

The EY mechanism causes spin relaxation in the case of ion scattering, which should be suppressed in the spintronics devices. Every time the electron scatters to a new state, during the collision, there is a chance to couple a different spin from the ion impurity. However, the DP mechanism is the spin relaxation process due to the spin orbit interactions, which could be promisingly utilized for the spintronics applications. For a moving electron spin, the relaxation is caused by the precession due to the internal effective magnetic fields, thus, the effective magnetic field is also proposed for electron spin manipulations. In addition, Rashba spin orbit interaction can provide a prospective method for the technological application as one can use an external gate voltage to control the rotation of electron spins. As shown in Fig. 1.2a, the effective magnetic field caused by Rashba spin orbit interaction is a momentum dependent field, implying that the scattering during spin transport strongly influences the electron spin orientation. [9] For this reason, the operation of Datta-Das Spin-FET is limited in the regime of ballistic transport where the momentum of electron does not change. [10]

Furthermore, at room temperature, electron spin relaxations due to the DP mechanism are the most dominant. And it has been demonstrated that when the Rashba and Dresselhaus spin orbit interactions linear-in- k terms have equal strength, the relaxation of spin orientation in one of the $\langle 110 \rangle$ axes is totally

suppressed.[11, 12] As shown in Eq.1.4, when the Rashba and Dresselhaus spin orbit interactions have equal strength ($\alpha = \beta$), for electron moving in the direction of $\langle 110 \rangle$ axes ($k_x = k_y$), the electron spin will be momentum independent. This will provide a possibility for the robust Spin-FET even in the regime of diffusion transport.

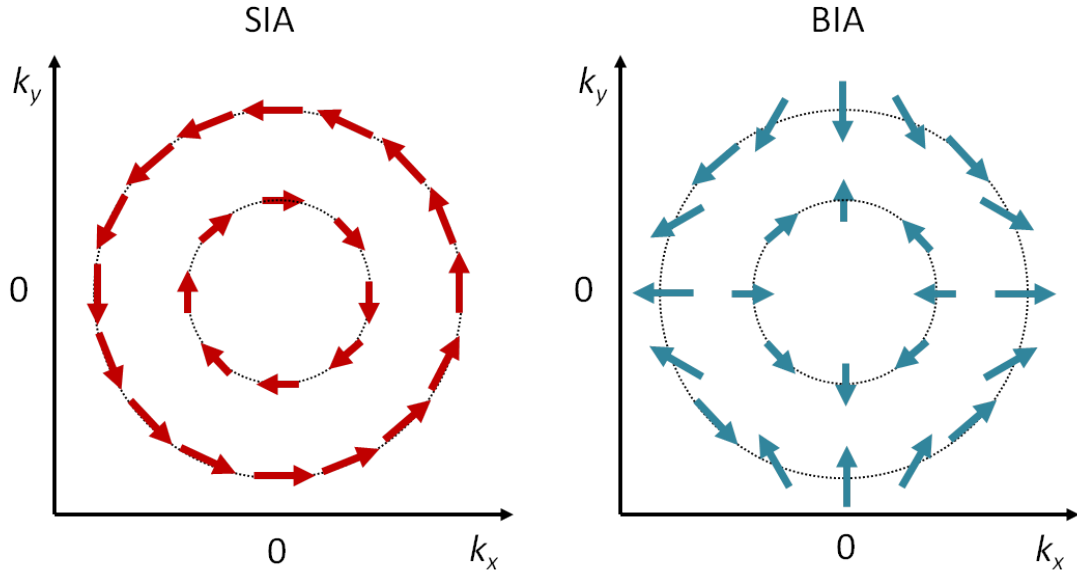


Figure 1.2: The effective magnetic fields of (a) structure inversion asymmetry, and (b) bulk inversion asymmetry in 2-dimensional system.

1.4 InAs Nanowire: A New Proposal for Spin FET

Quantum wire is an attractive nanoscale structure for quantum devices. As electrons could be quantum-confined laterally in this structure, a lot of interesting quantum effects or transport properties can be investigated. To fabricate the nanoscale structure, a general technique is the lithography and etching processes [16]. However, the etching processes always lead to significant surface damage, which introduce the surface roughness and surface states. Nanoscale structure, particularly, quantum wires with very large surface-volume-ratio are very sensitive to the surface roughness and surface states. In recent years, semiconductor

nanowires are fabricated by the bottom-up growth techniques. As this growth process is self-organized without the aids of *ex situ* techniques, semiconductor nanowires grown with bottom-up techniques, representing a unique quasi-one-dimensional (1D) system, have stimulated the experimental investigation of physical phenomena and quantum devices [17][18][19]. In particular, indium arsenide (InAs) nanowire is reported as a 1D nanostructure with outstanding promise for device applications because of its high electron mobility and strong quantum confinement effects [20][21][22]. In this thesis, we propose that InAs nanowire is a promising spin transport semiconductor channel candidate for the spintronics devices, particularly, the Datta-Das Spin-FET based on the three primary reasons following.

First, as discussed Section 1.3, the spin relaxation due to the scattering is essential for the information loss during the transport in the channel. According to predictions of reduced spin relaxation in the 1D systems [12], the InAs nanowire should be able to provide a big advantage by suppressing the relaxation of spin coherence along the channel. Besides, in the case of a strong 1D confinement channel, the momentum scatterings in the directions except for the electron propagation direction are probably suppressed. It is extremely advantageous for the utilization of Rashba and Dresselhaus spin orbit interactions, whose effective magnetic field is dependent on the momentum of the electron propagation direction.

Secondly, since the strong Rashba spin orbit interaction can provide an effective electron spin manipulation, the large spin orbit interaction of electrons in InAs makes it ideally suited for the applications of spin devices. In the proposal of Datta-Das Spin-FET, logical information is carried by electron spin as the orientation. Because the spin precession angle or the spin rotation rate is dependent on the strength of the effective magnetic field, a strong spin orbit interaction is essential for a high On-Off switch device. As discussed in Section 1.3, the strength of Rashba spin orbit interaction is dependent on structure inversion asymmetry,

which can be enhanced by a heterostructure design or an external gate voltage as well. The strength of Rashba coefficient α can be expressed as:

$$\alpha = \frac{g\mu_B E_0}{2m_e c^2}, \quad (1.5)$$

where g is the g-factor of electron, μ_B is the Bohr magneton, E_0 is the static electrical field, m is the mass of electron, and c is the velocity of light. The band structure at 300 K of bulk InAs is shown in Fig.1.3. [13] The narrow band gap of around 0.35 eV and the effective mass for conduction electrons near the bottom of the Γ valley is $m_e \sim 0.023 m_0$. This very small effective mass is one of most attractive properties of InAs for quantum device applications. In this thesis, the narrow band gap and the small effective mass of electron can provide a relative large Rashba spin orbit interaction according to Eq.1.5. In 2-dimension system, InAs-based heterostructure whose Rashba effect can be made anomalously large by band-gap engineering, [14] thus, InAs is a well known promising candidate channel material of spintronics devices, particularly the Datta-Das Spin-FET [10][15].

Thirdly, owing to the relaxed lattice matching requirements of nanowire growth compared with the heteroepitaxy film (2D) growth, facilitating the freedom to combine materials with different lattice constant. Nanowire structure provides more possibilities and potentials for band gap engineering, so that, the strength of spin orbit interactions, particularly, Rashba spin orbit interaction can be modulated more effectively. Therefore, in this thesis, we propose InAs nanowire for use as the electron spin transport channel for applications to spintronics devices, particularly the Datta-Das Spin-FET. We expected that InAs nanowire might be applied to spintronics devices as an efficient 1D spin transport channel, therefore, investigating growth and transport properties is desirable for spintronics applications.

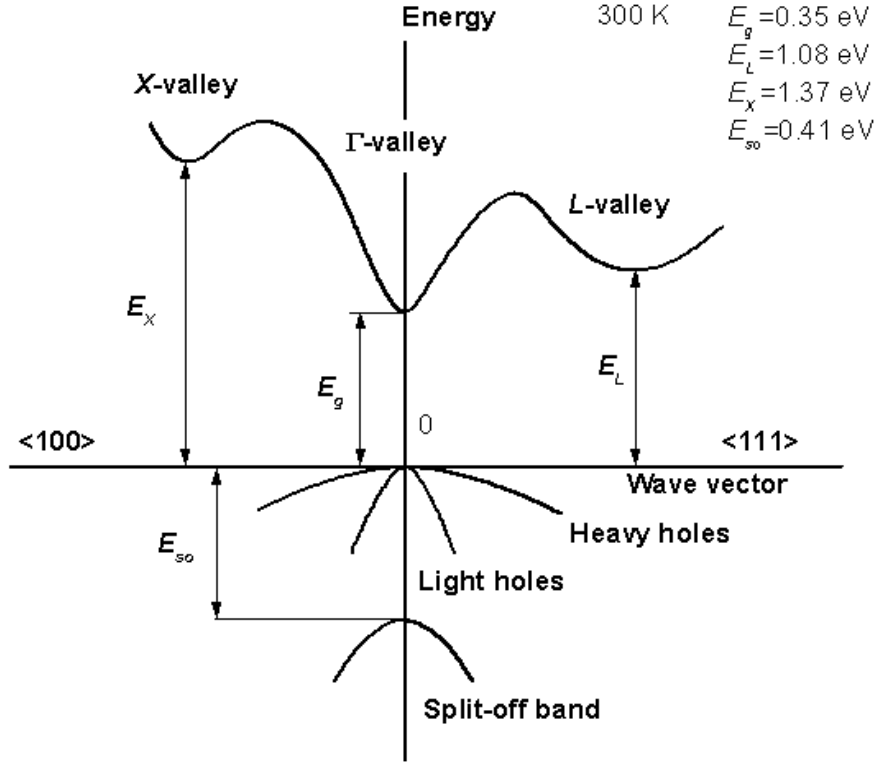


Figure 1.3: The band structure of bulk InAs at 300K [13]. The narrow band gap is the most attractive property for the applications of spintronics.

1.5 Thesis Composition

The thesis presents the proposal of InAs nanowire spin transport channel and a series of experiments, including the growth and electrical characterizations of InAs nanowires for spintronics devices, particularly, the Datta-Das spin FET.

First, the growth processes of InAs nanowires based on vapor-liquid-solid techniques using molecular beam epitaxy system are briefly overviewed in chapter 2. With these processes, the growth of common InAs nanowires with <111> orientation have been developed. Furthermore, the nanowire of core/shell structure has been expected that would provide more promising electron spin transport properties, therefore, the InAs/InP core/shell nanowires have been grown with similar processes.

Consequently, the transport properties of the common nanowire and core/shell

nanowire have been investigated and compared in chapter 3. The spin relaxation length which is an important parameter of spin transport has been also evaluated with magneto-conductance observations. As one of conclusions of this thesis, compared with the common InAs nanowire, the core/shell structure InAs nanowires are more suitable for the applications of spin transport devices.

In chapter 4, InAs nanowire with $\langle 110 \rangle$ growth orientations are proposed as a more effective spin transport channel for the Datta-Das spin FETs. According to the demonstrations that the relaxation of spin orientation in one of the $\langle 110 \rangle$ axes could be totally suppressed. The $\langle 110 \rangle$ -oriented InAs nanowires are successfully grown by using MBE system for the first time, and the growth processes are introduced specifically. In addition, compared with the $\langle 111 \rangle$ -oriented InAs nanowires, several distinguishing features are found in the $\langle 110 \rangle$ -oriented nanowire, including the absence of ZB/WZ stack defects. Furthermore, based on the observations of the crystalline structure and morphology of the $\langle 110 \rangle$ -oriented InAs nanowires, the growth of InAs nanowire is investigated more specifically.

In chapter 5, similarly, the transport properties of the $\langle 110 \rangle$ -oriented InAs nanowires are investigated with field-effect mobility measurements. By comparing with the $\langle 111 \rangle$ -oriented discussed in chapter 3, it is found that the $\langle 110 \rangle$ -oriented InAs nanowire owns advantage transport properties due to the absence of the ZB/WZ stack defects. And this feature should be significant for the electron spin transport. Thus, the transport properties of $\langle 110 \rangle$ -oriented InAs nanowire are investigated more precisely with a single nanowire Hall device, and an effective fabrication process is introduced as well. Eventually, the scattering mechanism and carrier behavior are investigated based on the Hall measurement at different temperatures. In addition, some primary results of the spin injection measurements are discussed as well.

Finally, this thesis is concluded in chapter 6.

Bibliography

- [1] S. Datta and B. Das, Appl. Phys. Lett. 56, 665 (1990).
- [2] G. Moore, Electronics Magazine. p. 4. Retrieved 2006.
- [3] G. Dresselhaus, Phys. Rev. 100, 580 - 586 (1955).
- [4] Y. A. Bychkov and E. I. Rashba, J. Phys. C 17, 6039 (1984).
- [5] Y. Yafet, Phys. Rev. 85, 478 (1952); R. J. Elliot, Phys. Rev. 96, 266 (1954).
- [6] M. I. D'yakonov and V. I. Perel', Zh. Eksp. Teor. Fiz. 60, 1954 (1971). [Sov. Phys. JEPT 33, 1053 (1971)].
- [7] G. L. Bir, A. G. Aronov, and G. E. Pikus, Zh. Eksp. Teor. Fiz. 69, 1382 (1975) [Sov. Phys. JETP 42, 705 (1975)].
- [8] I. Zutic, J. Fabian, and S. Das Sarma, Rev. Mod. Phys. 76, April (2004).
- [9] R. Winler, Phys. Rev. B 69, 045317 (2004).
- [10] H. C. Koo, J. H. Kwon, J. Eom, J. Chang, S.H. Han, and M. Johnson, Science. 325, 1515 (2009).
- [11] M. Ohno and K. Yoh, Phys. Rev. B 75, 241308 (2007).
- [12] J. Schliemann, J. C. Egues, and D. Loss, Phys. Rev. Lett. 90, 146801 (2003).
- [13] <http://www.ioffe.rssi.ru/SVA/NSM/Semicond/InAs/Figs/721.gif>
- [14] T. Matsuda and K. Yoh, Physica E 42, 979 - 983 (2010).
- [15] T. Ishikura, L.-K. Liefeth, Z. Cui, K. Konishi, K. Yoh, and T. Uemura, Appl. Phys. Express 7, 073001 (2014).
- [16] M.A. Reed, J.N. Randall, R.J. Aggarwal, R.J. Matyi, T.M. Moore, A.E. Wetsel, Phys. Rev. Lett. 60, 535 (1988).
- [17] A. Das, Y. Ronen, Y. Most, Y. Oreg, M. Heiblum, and H. Shtrikman, Nature Physics. 8, 887-895 (2012).
- [18] S. Heedt, C. Morgan, K. Weis, D. E. Bürgler, R. Calarco, H. Hardtdegen, D. Grützmacher, and Th. Schäpers, Nano. Lett. 12, 4437 - 4443 (2012).
- [19] J. Tarun, S. Huang, Y. Fukuma, H. Idzuchi, Y. Otani, N. Fukata, K. Ishibashi,

and S. Oda, Appl. Phys. Express 5, 045001 (2012).

[20] S. Chuang, Q. Gao, R. Kapadia, AC. Ford, J. Guo, and A. Javey, Nano Lett. 13, 555–558 (2013).

[21] S. A. Dayeh and D. Wang, Small. 2, 326 - 332 (2007).

[22] T. Bryllert, L-E. Wernersson, T. Lowgre, and L. Samuelson, Nanotechnology. 17, 227 - 230 (2006).

Chapter 2

Growth of InAs Nanowire

InAs nanowire is the platform of this thesis. InAs nanowire not only provides the useful electronic properties of InAs, but also is very useful for studying the quantum effects such as electron spin transport as a 1D nanoscale structure. In this chapter, based on the growth of $\langle 111 \rangle$ -oriented InAs nanowires, vapor-liquid-solid (VLS) technique, which is a self-organized growth process for InAs nanowire fabrication, is discussed. We review various growth methods of InAs nanowire particularly the VLS technique in molecular beam epitaxy (MBE) system. A core/shell structure of $\langle 111 \rangle$ -oriented InAs/InP nanowire is discussed as well, which is expected as a promising structure for electron spin transport.

2.1 Introduction

As discussed in Section 1.4, the formations of formal semiconductor nanoscale structures such as nanowires are the lithography and etching processes, which include a lot of defects and impurities. For the nanoscale device in the range of sub-100 nm, the surface roughness and the impurities critically affect the transport properties and quantum effects investigations. Regarding these reasons, many approaches have been studied, including the vapor-liquid-solid (VLS) mechanism

[1][2], the vapor-solid-solid (VSS) mechanism [3]. Among these self-organized growth methods, the VLS mechanism is most widely applied in growth of elemental semiconductor nanowires [2], III-V semiconductors [4–7], II-VI semiconductors [8][9]. And owing to its simplicity and versatility, the VLS mechanism is successfully used in many semiconductor systems and techniques such as metal-organic vapor phase epitaxy (MOVPE) [7][10], chemical vapor deposition (CVD) [11][12], thermal evaporation, molecular beam epitaxy (MBE) [5][6], chemical beam epitaxy [13]. In this thesis, <111>-oriented InAs nanowire is grown using a MBE system by VLS mechanism. Furthermore, nanowires with different crystal structures (zinc-blende structure and wurtzite structure) and different crystal orientations can be grown in particular growth conditions, the growth conditions of nanowires for spintronics are investigated.

2.2 VLS Growth Process

The principle of VLS InAs nanowire grown by MBE is schematically shown in Fig.2.1. (a) The Au particles used as catalyst metal particles can be formed by a thermal process of a thin Au film, or can be pin coated on the substrate in the case of using Au colloid. Correspondingly, the size and density of the Au particles decide the diameter and density of nanowires. (b) After a thermal treatment in the growth system, the deposited Au particles alloyed with the In atoms of the InAs substrate, before that the preparation of the substrate surface is critical for growing high-quality nanowires. Owing to the melting temperature of the Au-In alloy at the eutectic point is much lower than that of Au, liquid Au-In alloy droplets are formed. (c) At the growth temperature, the In and As sources are opened and atoms of In and As are evaporated. The Au-In droplets can keep absorbing the In and As vapor of atoms resulting in a supersaturated state. (d) Since the melting point of InAs is higher than the nanowire growth temperature, at the interface between

supersaturated droplets and the substrate, In and As atoms precipitate from the droplets and bond at the liquid-solid interface, and the liquid droplets rises from the InAs substrate surface. (e) The absorption, precipitation and crystallization processes continuously carry out until the end of vapor sources supplement. Finally, InAs nanowires are grown by the VLS technique.

As discussed in Sec.2.1, the VLS methods can be applied for growth a variety of 1D nanowires. And the details of nanowire growth such as diameter control, vertical growth and heterostructure growth will be briefly discussed in the Sec.2.4 and Sec.2.5.

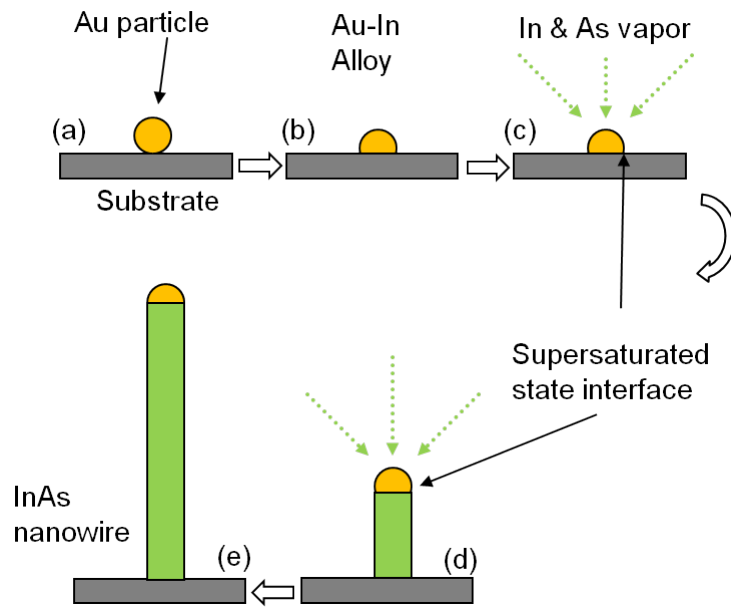


Figure 2.1: The schematic of VLS growth of InAs nanowire. (a): Au colloid used as catalyst metal particles is pin-coated on the substrate wafer. (b): After the thermal processes in the MBE growth chamber, the Au particles and the In of the substrate wafer formed liquid alloyed droplets. (c): The Au-In alloy droplet is irradiated by In and As source beam, and keep absorbing the atom of In and As. (d): At the interface of between the droplet and the substrate, the supersaturated In and As source precipitate and crystallize at this interface. The droplet arises from the substrate. (e): Finally, after the circulation of the absorption-supersaturation-precipitation processes, nanowire structure is grown.

2.3 MBE System

Since the InAs nanowires in this thesis are grown by Molecular beam epitaxy (MBE) system shown in Fig.2.2, in this section, the structure and operation theory are introduced briefly. MBE, which was invented in the late 1960s [14], is used in the manufacture of semiconductor devices.

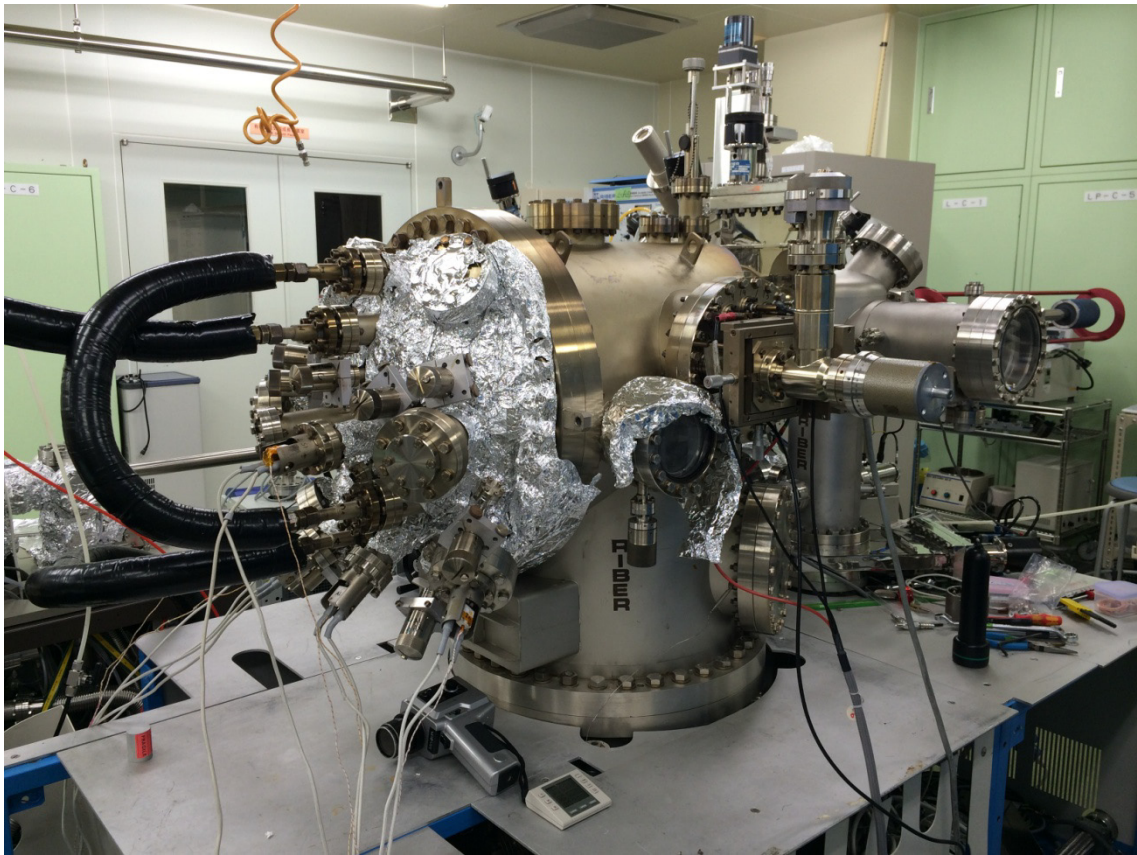


Figure 2.2: Picture of MBE for nanowire growth of this thesis. The MBE is rebuilt based on a Riber MBE. The equipment MBE system provides an ideal clean semiconductor growth environment in high vacuum or ultra-high vacuum (10^{-9} Torr).

MBE system provides an ideal clean semiconductor growth environment in high vacuum or ultra-high vacuum (10^{-8} Pa). Since the mean free path of the source molecules under vacuum conditions of 10^{-5} Torr is about 0.2 m, the elemental atom

beam will not react or crystallize until they reach the substrate wafer. In solid-source MBE, elements sources such as In and As, are heated in separate effusion cells with until they begin to sublime. The sublimed source atoms or molecules from the effusion cells behave like a beam aiming directly at the substrate shown in Fig.2.3. Then the source atom beams condense on the substrate wafer and single crystal InAs is formed. Since the shutters in front of the effusion cells can be controlled, the thickness of each layer, the doping states and heterostructures can be well controlled. The growth, surface structures and contamination can be monitored *in situ* by reflection high-energy electron diffraction techniques (RHEED) and quadrupole mass spectrometer (QMASS).

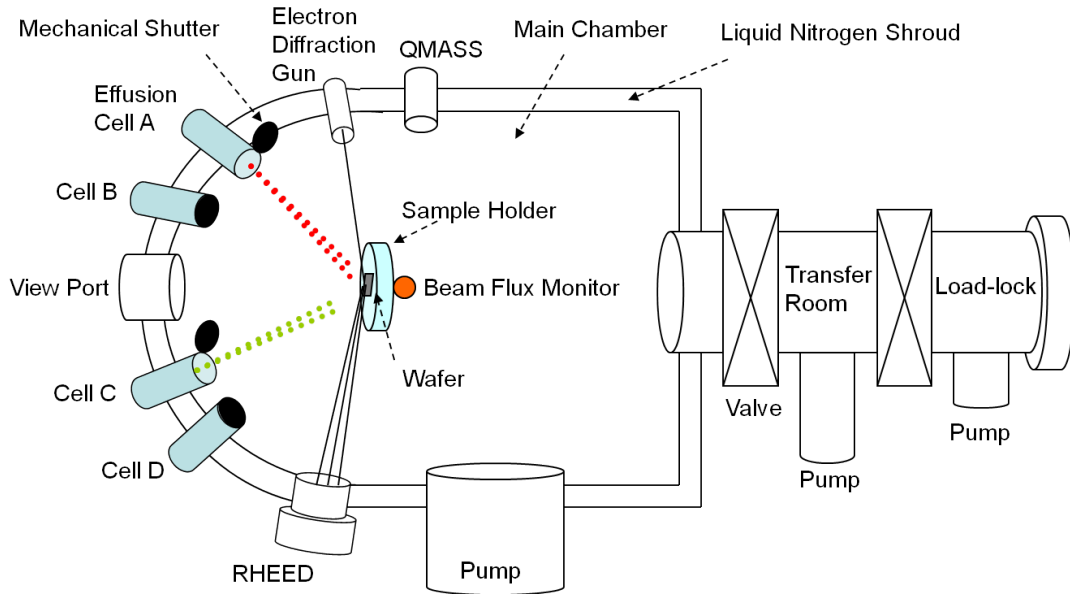


Figure 2.3: Schematic of MBE. The rebuilt Riber MBE owes one load-lock, two transfer room, and one main chamber. Five solid sources are set, including In, As, Si, Ga and Al.

Recently, MBE systems have been widely used for both compound semiconductor nanowire [5][6] and elemental Si nanowire [15] based on VLS

mechanism. Combined with the VLS, these techniques are able to grow semiconductor nanowires with high crystalline quality and even provide the growth of 1D heterostructures with clean interfaces [16]. Specifically, for nanowire growth, MBE has several advantages over other synthesis techniques: (1) the ultra-high vacuum can reduce contamination/oxidation and increase the quantities of crystal structure; (2) the growth can be monitored *in situ*; (3) since all growth parameters can be adjusted precisely and separately, the intrinsic nanowire growth phenomena can be studied individually, different nanowire with different structure such as heterostructure can be grown; (4) the absence of carrier gases not only result in the high purity of nanowire growth, but also simplify the nanowire growth process, since no molecules or precursors need to decompose from the carrier gases. A disadvantage of MBE systems is that the ultra high vacuum chambers are very expensive to set up and maintain.

2.4 <111>-oriented InAs Nanowire Growth

2.4.1 <111>-oriented InAs Nanowire

Since the most common crystalline structure for nanowires growth in MBE by VLS techniques are <111>-oriented with {110} side facets, first, <111>-oriented nanowires were grown. There have been general theoretical models explaining the parameters and the growth mechanism behind the Au-assisted nanowire growth [17, 18]. The morphology and crystal quality are the most important factors affecting the InAs nanowires and their device properties. Besides these two properties, the InAs nanowires applied for spintronics devices, particularly the Spin-FET, should have sufficient length and uniformity to make the fabrication and characterization of devices conveniently. For these purpose, the growth processes and the growth conditions are investigated in order to obtain the nanowires suitable for this thesis.

Among the various parameters influencing the growth of nanowires, individual group III and V flux rates play a distinct role. The growth rate, diameter, shape and length of nanowire are affected by the diffusion kinetics which is decided by the III and V flux. Furthermore, as discussed in Sec.2.2, in the VLS growth processes of MBE, the metal catalyst such as Au particle is not expected to help the decomposition of the precursor species such as the sources gas. Owing to the source atoms (adatom) absorption, the crystal can grow faster at the catalyst/substrate interface than on the remaining surface then form the nanowire structure. During the growth, besides the adatoms which directly arrive the catalyst droplet, a major contribution to this adatoms comes from the incoming flux intercepted by the sidewalls of nanowires [19, 20]. Therefore, the diffusion length of the adatoms on the sidewalls of the nanowire becomes important for morphology of nanowires, particularly the length at which diameter tapering starts. In the case of longer diffusion length, the supplement of the adatom to the alloyed droplet on the top of the nanowire is sufficient, which leads rod like structure. On the other hand, if the diffusion length is not long enough to make sufficient adatom supplement to the droplet, the nanowire growth tends to the radial growth and tapered morphology. The diffusion length of the adatoms on the sidewalls of nanowire is decided by the parameters such as the growth temperature and the individual III and V source flux. For the InAs nanowire growth, the species of solid As source such as As_2 and As_4 are impact the diffusion length [19]. As_4 is more efficient to obtain longer diffusion length which leads rod like structure nanowire growth, therefore, As_4 is used as the solid As source as length and uniformity are necessary for the fabrication devices. On the other hand, As_2 leads the growth of radial shape nanowire structure, which is more efficient for core-shell structure nanowire growth. And this structure of nanowire is importance for the application of spin device which will be discussed in Sec. 5.4.

For these reasons, in the next section, a growth process of <111>-oriented InAs nanowire in Au assisted MBE based on the investigation of III and V flux and growth temperature investigation will be discussed, in order to obtain suitable uniformity and relatively long length.

2.4.2 Experimental Procedure

This section includes the preparation of MBE growth substrate wafer and the MBE growth processes.

First, the following is the preparation of the growth substrate wafer.

1. Cleaning: Cleaved epi-ready (111)-oriented InAs wafer is processed ultrasonic cleaning in organic solvent with weakest power. The organic solvents used are acetone, ethanol and isopropyl alcohol. The processing time is about 3 minutes respectively. To remove the surface native oxide layer of InAs wafer, a brief etching around 30-sec with $\text{NH}_4 : \text{H}_2\text{O} = 1 : 10$ is preferred, following with a 1-min DI water rinsing.
2. Au-nanoparticles dispersion: Au-nanoparticles in the colloidal form are dispersed on the InAs surface by the spin-coating technique. Spin coating should be not carried out until the temperature of Au colloid returned to room temperature as the Au colloid should always be stored in the refrigerator. A 500-rpm/5-sec and 3000-rpm/30-sec spin coating process provides reasonable density of Au particles. Then the substrate wafer is baked in 110 °C for 10-min.
3. After the preparation of the growth substrate wafer, the substrate wafer is set onto the MBE growth holder with melted In.

After the preparation of growth substrate wafer, the growth process is carried out as following steps.

1. A pre-bake at 250 °C is carried out to remove water and other contaminant during transfer, before the growth substrate sample is transferred to MBE growth chamber.
2. Au-semiconductor alloying was carried out at 450 °C in As-atmosphere for 5-min in As-atmosphere.
3. Return the substrate temperature from the annealing temperature of 450 °C to the growth temperature of 420 °C.
4. Open the shutter of In source to start the growth, and the growth process is carried out for 1-hour to get enough length of nanowire. The flux of As is around 1.2×10^{-5} Torr and the flux of In is around 6×10^{-7} Torr, which leads the V/III ratio is around 20.

2.4.3 Growth Parameters and Results

With the growth processes of Sec. 2.4.2, <111>-oriented InAs nanowires are grown at different conditions of In and As source flux. The typical as grown sample is observed and investigated by scanning electron microscope (SEM), and the cross-sectional SEM image is shown in Fig.2.4, showing the length of nanowire is around 10 ~ 14 μm with growth time of 1-hour. The nanowires are perpendicular to the (111)-oriented InAs substrate indicating the grown nanowires are <111>-oriented. The relative long length owes to the high growth rate of ~ 3.8 nm/s as reported in ref.5. Moreover, this high growth rate also results in numerous advantages like less tapering. From Fig.2.4c, a reasonable density of the grown nanowire sample is shown. Since our target is to investigate the transport property of a single nanowire by electrical measurements, a proper density is conducive to

fabricate nanowire device whose processes will be introduced in detail in Ch. 3 and Ch.5.

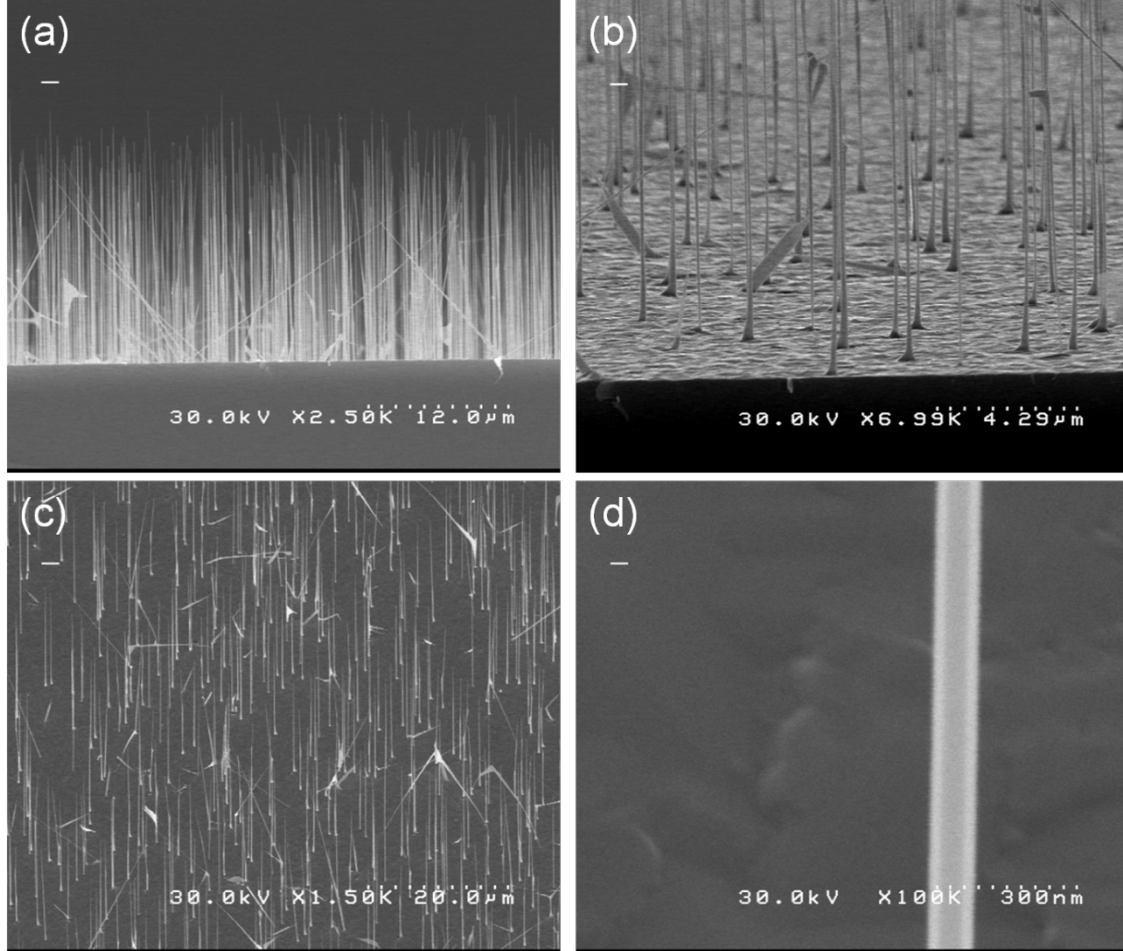


Figure 2.4: SEM images of <111>-oriented InAs nanowires grown on (111)-oriented InAs substrate with growth conditions: In flux $\sim 0.9 \times 10^{-6}$ Torr and As flux $\sim 1.2 \times 10^{-5}$ Torr. (a): A cross-sectional image of the grown nanowires, indicating the length of nanowires is around $10 \sim 14 \mu\text{m}$. (b): A 45-degree tilted view of the grown nanowires, showing the grown nanowire are perpendicular to the growth substrate. (c): A 45-degree tilted view, showing a reasonable density of nanowires on the growth substrate. (d): SEM image of a single InAs nanowire, the diameter of this nanowire is around 90 nm.

For the same purpose of convenient device fabrications, the <111>-oriented InAs nanowires should be grown with the conditions that can provide reasonable

diameter of 30 ~ 300 nm and length of 5 ~ 15 μm . Therefore, In flux dependency and As flux dependency are confirmed, which are concluded in Fig. 2.7. It should be mentioned that the identical growth conditions dependency of the previous research [5] has not been attained, which could be explained by condition variations of MBE system. Nevertheless, <111>-oriented InAs nanowire suitable for electrical device fabrications are obtained.

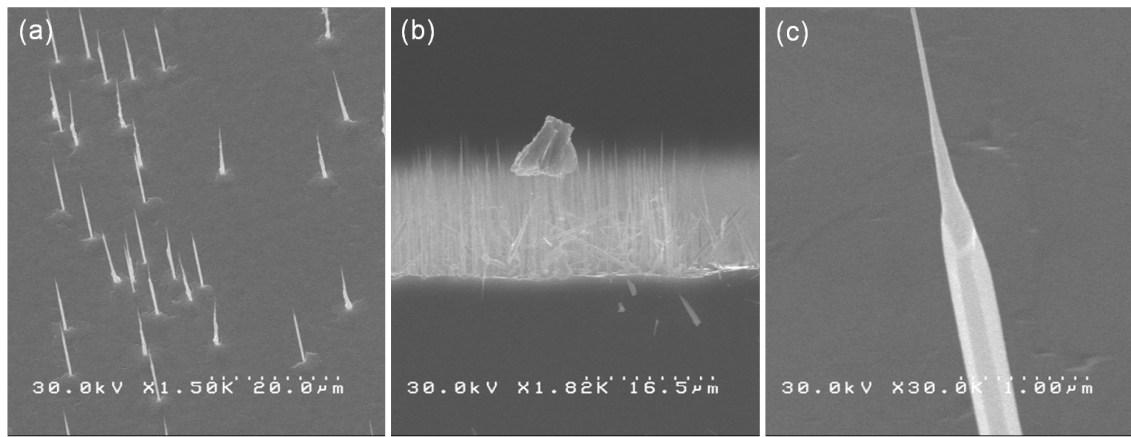


Figure 2.5: SEM images of <111>-oriented InAs nanowires grown with growth conditions: In flux $\sim 1.4 \times 10^{-6}$ Torr and As flux $\sim 1.2 \times 10^{-5}$ Torr. (a) A 45-degree tilted view. (b) A cross-sectional view. (c) SEM image of a single InAs nanowire, the diameter of this nanowire is around ~ 300 nm.

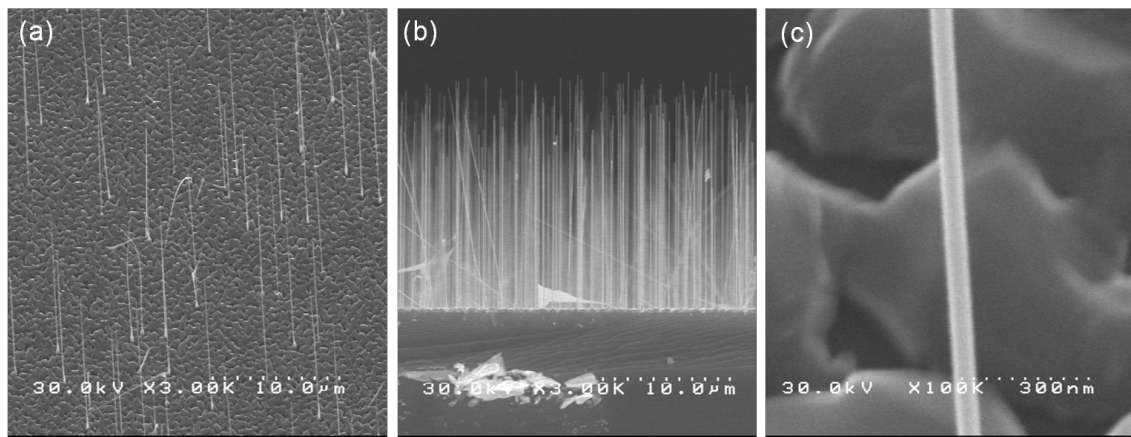


Figure 2.6: SEM images of <111>-oriented InAs nanowires grown with growth conditions: In flux $\sim 1.4 \times 10^{-6}$ Torr and As flux $\sim 1.2 \times 10^{-5}$ Torr. (a) A 45-degree tilted view. (b) A

cross-sectional view. (c) SEM image of a single InAs nanowire, the diameter of this nanowire is around ~ 300 nm.

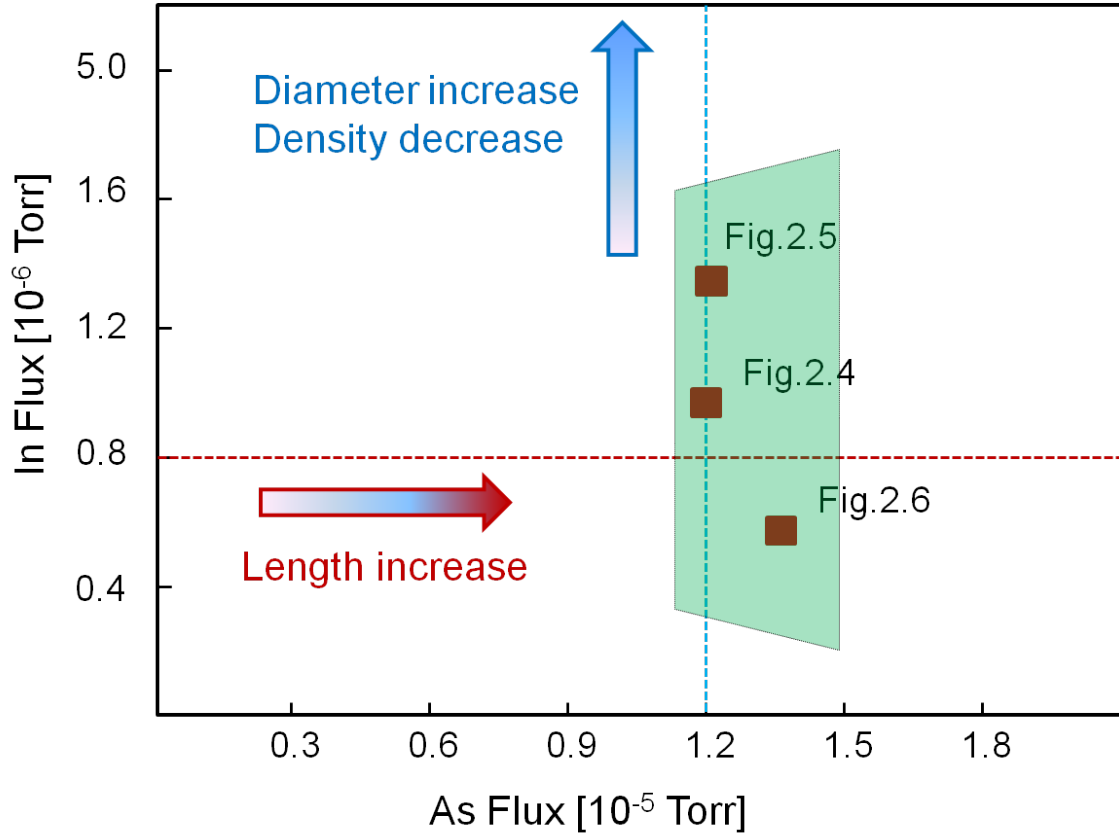


Figure 2.7: Conclusion of the In flux and As flux dependence of <111>-oriented InAs nanowires. The growth points, whose SEM images have been depicted above, are shown on positions of their growth conditions. The tendency of radial growth, density, and high growth rate are denoted by the arrow signs. Growth conditions in the shadow area are utilized for the nanowires for the device fabrications.

Based on the SEM observations above, we can discuss the morphology more specifically. With the growth conditions in the shadow area of Fig.2.7, <111>-oriented InAs nanowires with different diameters can be grown. Regardless of the diameter, the grown nanowires show fine rod-like without tapering morphology. It is could be explained by the high growth rate of our nanowires, due

to a relatively long diffusion length of In species. Since the growth temperature, which is an effective parameter of the radial growth, is fixed in the thesis, the variations of diameter and length of the nanowires are mainly attributed to the variations in In and As fluxes. And the uniformity of the nanowires are acceptable, because the dispersion of the Au nanoparticles are relative uniform, which dispersed by spin coating process. This uniformity of the Au nanoparticles dispersion ensures that the same amount of In species are collected. In addition, the diameter of the nanowire should be dependent on the size of the nanoparticles as well.

2.5 InAs/InP Core/Shell Nanowire

InAs nanowire is expected as a decent electron spin transport channel material due to its high electron mobility and strong spin orbit interactions. Based on these merits of the common InAs nanowire, a core/shell structure of nanowire could provide more interesting properties for the quantum devices particularly spin transport devices [21, 22]. As depicted in Fig.2.8, in case of InAs/InP, core/shell nanowire is a radial heterostructure with a common InAs nanowire core and a InP shell.

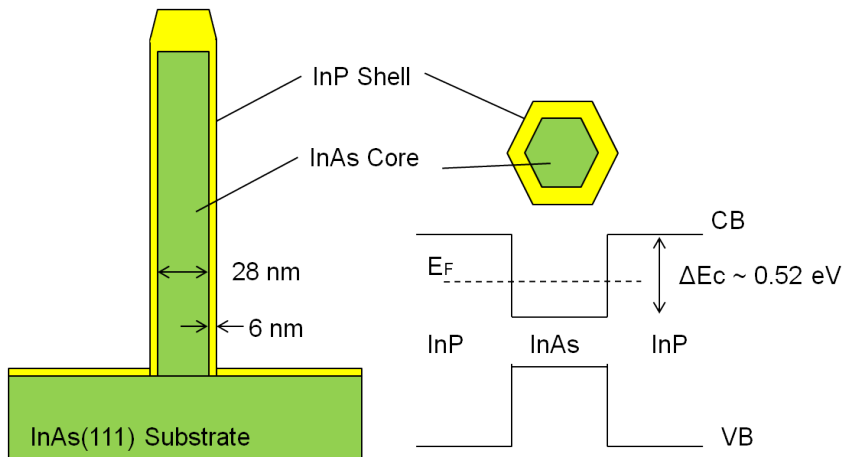


Figure 2.8: The schematic of InAs/InP core/shell nanowire.

This structure with protection on the surface of InAs nanowire can provide enhanced transport properties since the shell reduces the surface scattering. Furthermore, the conduction band offset of ~ 0.52 eV provides quantum-confined electrons, which is attractive for the enhancement of the transport properties as well. In the thesis, to identify the superiority of the core/shell structure, <111>-oriented InAs/InP core nanowires were grown by the VLS process in a Riber MBE system using Au-colloid solution on InAs (111) substrate. The growth processes can be briefly described as following. After the common InAs nanowire was grown, InP shell growth was performed by a 2-min growth of InP shell 2-dimensional growth. The InAs/InP nanowire has a length of $2\ \mu\text{m}$ and a diameter of $40\ \text{nm}$. Since the lattice mismatch of 3 % between InAs and InP is relatively large, after the 2-dimensional growth for the InP shell, bending nanowire can be observed. The structure and the morphology of this core/shell nanowire are confirmed by SEM and transmission electron microscope (TEM), the results are depicted as Fig.2.9.

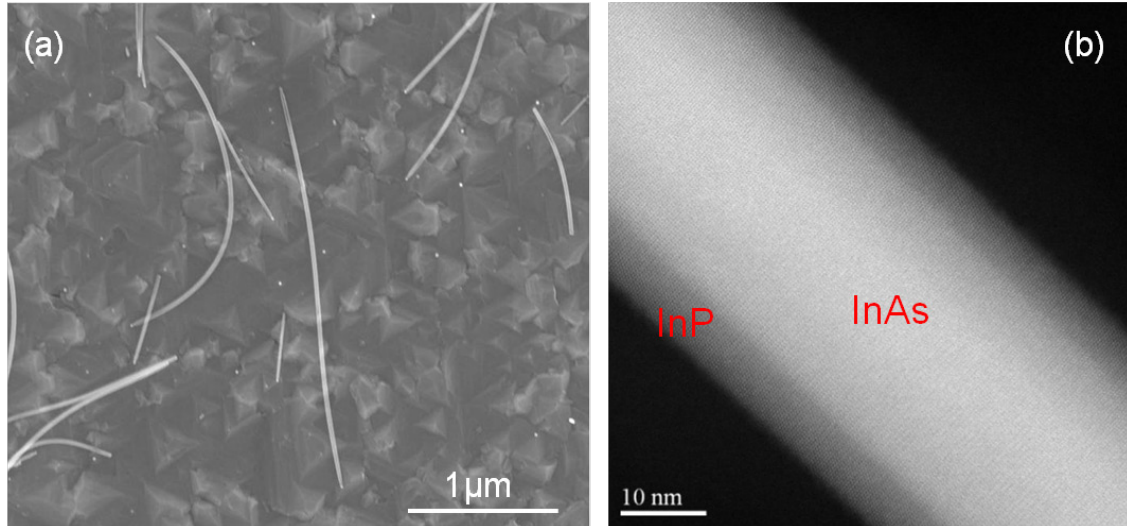


Figure 2.9: SEM and TEM images of <111>-oriented InAs/InP core/shell nanowires grown on (111)-oriented InAs substrate. (a): SEM image of the nanowires show these nanowires are around $\sim 2\ \mu\text{m}$ long with diameter of around $\sim 40\ \text{nm}$. (b): TEM image shows the InP shell is around $\sim 6\ \text{nm}$ and the InAs core is around $\sim 28\ \text{nm}$.

Bibliography

- [1] R.S. Wagner, W.C. Ellis, Appl. Phys. Lett. 4. 89 (1964).
- [2] E.I. Givargizov, J. Cryst. Growth 31. 20 (1975).
- [3] S.A. Dayeh, E.T. Yu, D. Wang, J. Phys. Chem. C 111. 13331 (2007).
- [4] K. Hiruma, M. Yazawa, T. Katsuyama, K. Ogawa, K. Haraguchi, M. Koguchi, H. Kakibayashi, J. Appl. Phys. 77. 447 (1995).
- [5] J. B. Babu, K. Yoh. J. Cryst. Growth 322. 10 (2011).
- [6] R Perumal, Z. Cui, P. Gille, J-C. Harmand, and K, Yoh. Semicond. Sci. Technol. 29. 115005 (2014).
- [7] K. Tomioka, J. Motohisa, S. Hara, and T. Fukui, Nano. Lett. 8. 10 (2008).
- [8] M. Lopez-Lopez, A. Guillen-Cervantes, Z. Rivera-Alearez, I. Hernandez-Calderon, J. Cryst. Growth 193. 528 (1998).
- [9] M. H. Huang, Y. Wu, H. Feick, N. Tran, E. Weber, and P. Yang, Adv. Mater. 13, 2 (2001).
- [10] K. Kumakura, K. Nakakoshi, M. Kishida, J. Motohisa, T. Fukui, H. Hasegawa, J. Cryst. Growth 145. 308 (1975).
- [11] A.M. Morales, C.M. Lieber, Science 279. 208 (1998).
- [12] Z.W. Pen, Z.R. Dai, Z.L. Wang, Science 291. 1947 (2001).
- [13] M.T. Bjork, B.J. Ohlsson, T. Sass, A.I. Persson, C. Thelander, M.H. Magnusson, K. Deppert, L.R. Wallenberg, L. Samuelson, Appl. Phys. Lett. 80. 1058 (2002).
- [14] A. Y. Cho, J. R. Arthur, Solid State Chem. 10. 157. (1975).
- [15] L. Schubert, P. Werner, N.D. Zakharov, G. Gerth, F.M. Kolb, L. Long, U. Gosele, T. Y. Tan, Appl. Phys. Lett. 84. 4968 (2004).
- [16] B. J. Ohlsson, M. T. Bjork, A. I Persson, C. Thelander, L. R. Wallenberg, M. H. Magnusson, K. Deppert, and L. Samuelson. Physica E, 13. 1126 (2002).
- [17] M.C. Plante, R.R. LaPierre, J. Appl. Phys. 105. 114304 (2009).
- [18] M. Tchernycheva, L. Travers, G. Patriarche, F. Glas, J.-C. Harmand, G.E. Cirlin,

V.G. Dubrovskii, J. Appl. Phys. 102. 094313 (2007).

[19] C. Sartel, D.L. Dheeraj, F. Jabeen, J.-C. Harmand, J. Cryst. Growth 312. 2073 (2010).

[20] J.-C. Harmand, G. Patriarche, N. Pere-Laperne, M.-N. Met-Combes, L. Travers, F. Glas, Appl. Phys. Lett. 87. 203101 (2005).

Chapter 3

Transport Properties of InAs/InP Core/Shell Nanowire

In this chapter, the transport properties of the nanowires and the superiority of the InAs/InP core/shell structure nanowires are confirmed. The fabrications and characterizations of the single nanowire transistor structure are discussed. Based on the transistor structure, the field-effect mobility of a single nanowire was investigated for the common $\langle 111 \rangle$ -oriented InAs nanowire and $\langle 111 \rangle$ -oriented InAs/InP core/shell nanowire respectively, which are both grown by VLS mechanism using MBE system. The field-effect mobility of the core shell nanowire was $\sim 4,600 \text{ cm}^2/\text{Vs}$ at room temperature, which is approximate 6-fold increase comparing to the simple InAs nanowire. Estimated field-effect mobility at $V_{ds} = 0.1 \text{ V}$ increased from $\sim 4,600 \text{ cm}^2/\text{Vs}$ at RT to $\sim 5,600 \text{ cm}^2/\text{Vs}$ at low temperature. A gate voltage dependent crossover from weak localization to weak anti-localization was observed. We extracted the spin relaxation length and coherence length using a quasi-one-dimensional model of the conductance, which are larger than the previous reports. The spin relaxation mechanism in the InAs nanowires are discussed as well.

3.1 Introduction

As discussed in Sec.1.1, the rapid progress in VLS nanowire growth by MBE has stimulated the experimental investigations of 1D quantum devices since the length, diameter, growth rate and density of the nanowire can be controlled by the effect of growth temperature, source flux ratio and substrate orientation. The growth of $\langle 111 \rangle$ -oriented InAs nanowire was described in last chapter, meanwhile the common $\langle 111 \rangle$ -oriented InAs nanowire and the $\langle 111 \rangle$ -oriented InAs/InP core/shell nanowire are obtained. In order to apply the nanowires to the electronic device particularly spin transport device, the transport properties of a single nanowire should be investigated. And the primary interesting is to confirm the superiority of the InAs/InP core/shell structure nanowire in electron and spin transport. For the investigation of carrier mobility, the field effect transistor (FET) structure is widely used [1, 2], so that, this method is also applied in our nanowire for both common nanowires and core/shell nanowires. Therefore, the comparison of the effective mobility between the common nanowire and the core/shell nanowire is able to provide the working direction of nanowire growth, from the aspect of nanowire structure. Specifically, the transport superiority of the core/shell structure is able to be attained by the characterization of the FET structure which is expected based on the band structure.

First, the fabrications of the FET structure based on a single nanowire are discussed. Particularly, since the contact resistance of the nanowire and the metal terminals are the key point of the device fabrication, the pre-etching processes of the nanowire prior to the formation of metal contact are summarized. In order to attain the identical FET structure based on the common $\langle 111 \rangle$ nanowire and the core/shell nanowires respectively, different fabrication processes are designed for each nanowire. Using the same FET structure device of both nanowires, the transport properties such as effective mobility are investigated, meanwhile, the

transport properties are compared at different temperatures. Enhanced transport properties and robustness of InAs/InP core shell nanowire are confirmed.

Second, our studies also aim at confirming 1-dimension transport properties and spin precession behaviors of core shell nanowires, thus magneto-conductance properties such as weak localization (WL) and weak anti-localization (WAL) of the same structure transistor devices were observed at low temperature, since spin relaxation can be probed via magneto-conductance measurements. In disordered conductors at low temperatures, constructive interference of pairs of backscattered, time reversed paths results in a negative WL correction to the conductivity [3]. In the presence of spin relaxation, the interference can be destructive, yielding a positive conductivity correction known as weak WAL [4, 5]. The conductivity correction disappears when a magnetic field sufficient to dephase time-reversed paths is applied. The magneto-conductivity correction depends on the length scales over which phase- and spin information is preserved. Recently, in order to understand the spin-orbit interaction and relaxation mechanisms, magnetotransport measurements have been done on the common InAs nanowires [6-8]. The gate voltage dependence WL-WAL crossover was investigated using a quasi-one-dimensional model. The extracted spin relaxation length (~ 290 nm) is longer than previous report [6-8] which indicates reduced spin relaxation in our core shell nanowires.

3.2 Fabrications of FET Structure Nanowire Device

3.2.1 Fabrication Processes

For the common $\langle 111 \rangle$ -oriented InAs nanowires growth, the processes discussed in Sec.2.4 were utilized, which provides the nanowire with a length of ~ 10 μm and a diameter of ~ 40 nm. Similarly, the InAs nanowires were grown by the VLS process

in a Riber MBE system using Au-colloid seed solution on InAs (111) substrate which also was discussed in Sec.2.5. After the InAs nanowire was grown, InP shell growth was performed for 2-min followed by a Si- δ layer and 2-min growth of InP shell. The InAs/InP nanowire has a length of $\sim 2\ \mu\text{m}$ and a diameter of $\sim 40\ \text{nm}$, while the InP shell has a thickness of 6 nm which was confirmed by a TEM.

For the characterization devices fabrications, the detail processes are described as following.

1. Address substrate fabrications:

To investigate the properties of a single nanowire, the nanowires should be detached from the grown substrate and transferred to another substrate with address marks. Dice the substrate wafer, which is a highly doped p-t type Si substrate with a 100 nm (or 300 nm) thick SiO_2 layer, into $8\ \text{mm} \times 8\ \text{mm}$ pieces. After the typical organic cleaning, spin-coat the primer and ZEP520 with $500\ \text{rpm} \times 3\ \text{sec}$ and $5000\ \text{rpm} \times 30\ \text{sec}$. For the hard baking in the oven, two steps of $170\ ^\circ\text{C} \times 2\ \text{min}$ and $90\ ^\circ\text{C} \times 5\ \text{min}$ are applied. Since the address mark patterns are relatively large (minimum size is $1\ \mu\text{m}$), electron beam (EB) lithography is carried out with $\sim 5\ \text{nA}$, a test drawing is preferred. After the EB lithography, develop the sample with Xylene for 45 sec following a rinse with isopropyl alcohol (IPA) for 45 sec. The patterns should properly developed with a sufficient dose and this recipe, however, the develop time and rinse time can be increased to 60 sec in case the pattern is not well developed. Then, the developed sample is baked in the oven with $110\ ^\circ\text{C} \times 10\ \text{min}$ for hard baking. For the address mark formation, 50 nm of Ti and 150 nm of Au are deposited with ANELVA electron beam evaporator at a pressure of $\sim 5.0 \times 10^{-6}\ \text{Torr}$. With the ZDMAC solution, the Ti/Au metal layers are lift-off. After soaking in the solution for 3 hours at least, a briefly ultra-sonic process can be applied here. Finally, the lift-off samples are rinsed in IPA for 1 min following a baking

process with oven for 10 min. The layout of the address substrate is shown in the Fig.3.1a, alignment marks are designed on the four edges of the $3400\text{ }\mu\text{m} \times 3400\text{ }\mu\text{m}$ address area. The position of transferred nanowires are defined with the cross marks shown in Fig.3.1b.

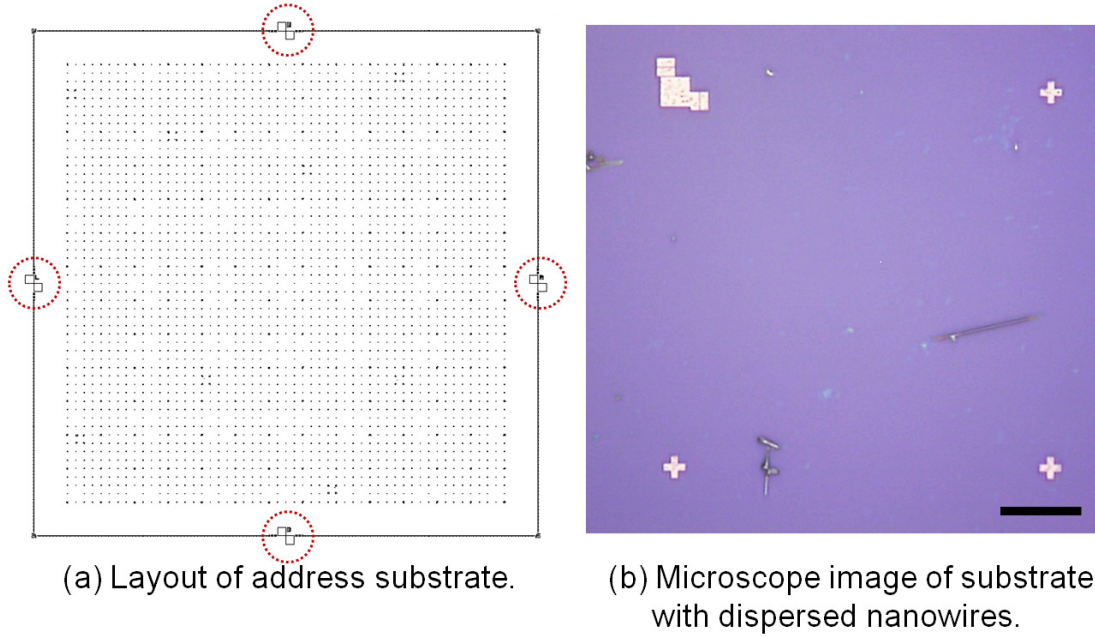


Figure 3.1: (a) The layout of a address substrate with alignment marks surround the address area. (b) Microscope image of the address substrate, the cross address marks are shown. The scale bar is $10\text{ }\mu\text{m}$.

2. Nanowire detachment and dispersion.

The nanowires are dissolved into ethanol solution (or deionized water) and detached from the growth substrate with strong ultra sonication for 1 min. The solution containing nanowires is transferred onto the Si address substrate with an injector. After a brief baking process, the nanowires are dispersed on the address substrate. The schematic of this process is shown as Fig.3.2.

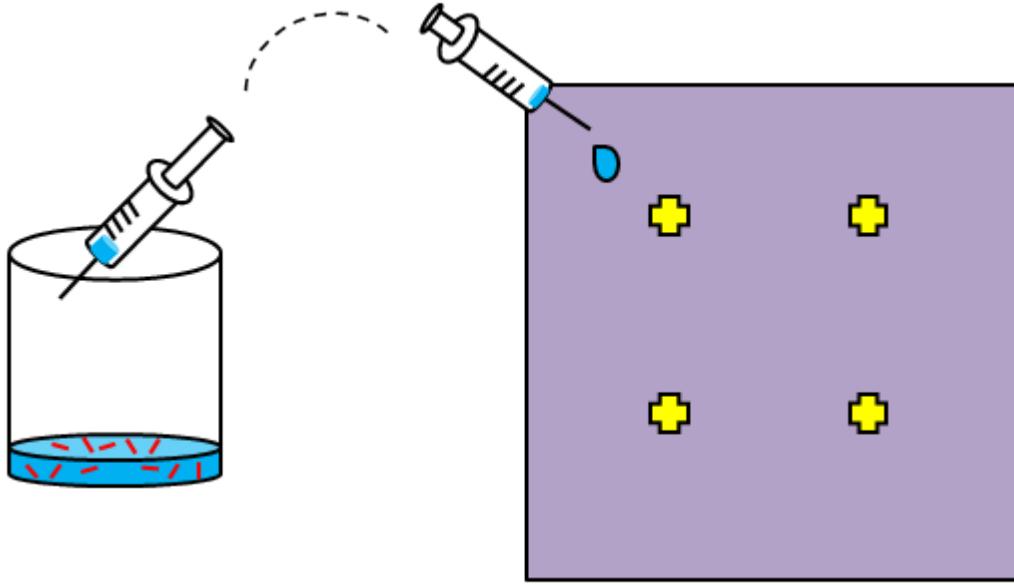


Figure 3.2: The schematic of the nanowire transfer and dispersion processes.

3. Device fabrications.

Device schematic structure and SEM micrograph are shown in Fig. 3.3. All of the lithograph patterns are defined by electron beam (EB) lithography and Ti/Au (20 nm/50 nm) are used as contact pads. InAn/InP core/shell nanowire is surface treated with solution of $\text{H}_3\text{PO}_4 : \text{HCl} = 3 : 1$ for 6 sec to remove the InP shell, following a rinse with deionized water for 2 min. For the common InAs nanowire, the native oxide is removed by the $(\text{NH}_4)_2\text{S}_x$ solution [9] to remove the native oxide. The pre-etched sample are transferred to the evaporator rapidly in order to carried out the formation of Ni (70 nm) electrodes without annealing process. As the reference, we fabricated the same structure devices with common InAs nanowires whose diameter is 40 nm.

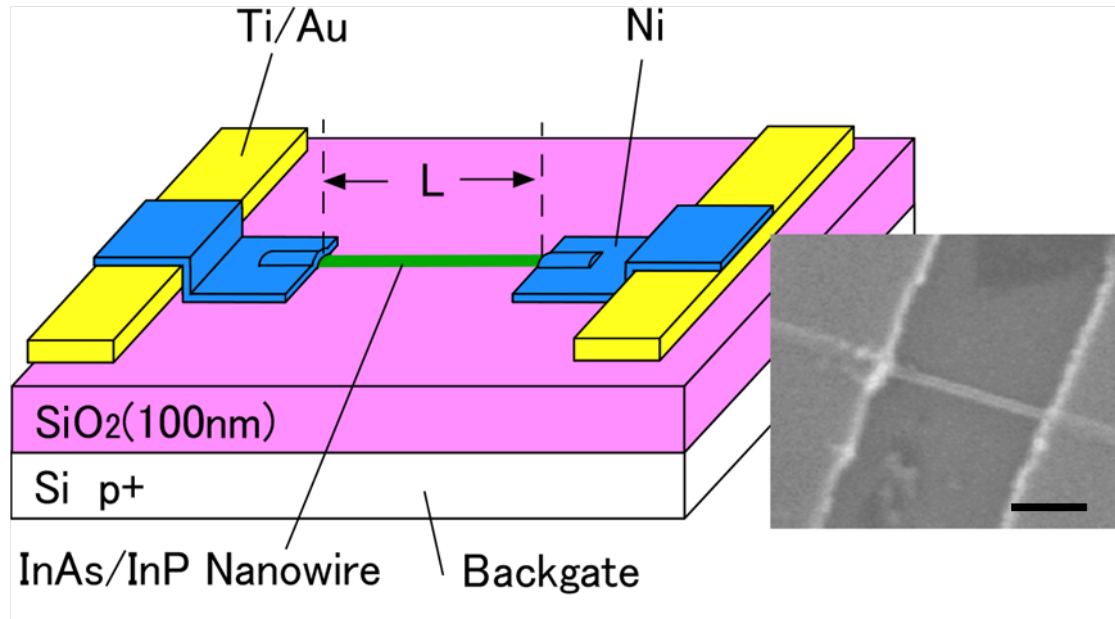
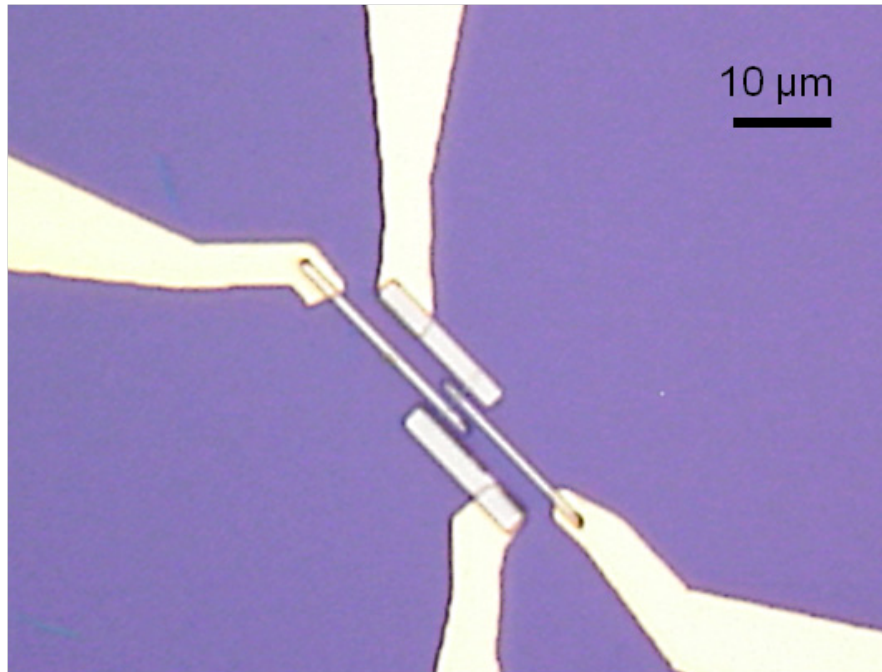


Figure 3.3: (a) Schematic image of the back gate nanowire devices InAs/InP core shell nanowire. Highly doped p-type silicon substrate with ~ 100 nm SiO₂ layer was used as address substrate with back gate electrode. Au/Ti pad area and Ni contact part were formed by EB lithography. L is the channel length. Inset is the SEM image of core shell nanowire device. The scale bar is 500 nm.



(b) A microscope image of the 4-terminal device for nanowire resistance measurements.

3.3 Characterization of FET Devices

By characterizing the transistor performances, the electrical transport properties of δ -dope core shell nanowire were studied. Room temperature transistor characteristics of a δ -dope core shell nanowire device with a diameter of 40 nm and channel length (L) of 1 μm are shown in Fig. 3.4(a) and (b). Both I_{ds} - V_{ds} and I_{ds} - V_{gs} curves of core shell transistor show stable characteristics compared with the simple InAs nanowire transistor. This is presumably caused by the better InAs surface (InAs/InP interface) in the core shell structure.

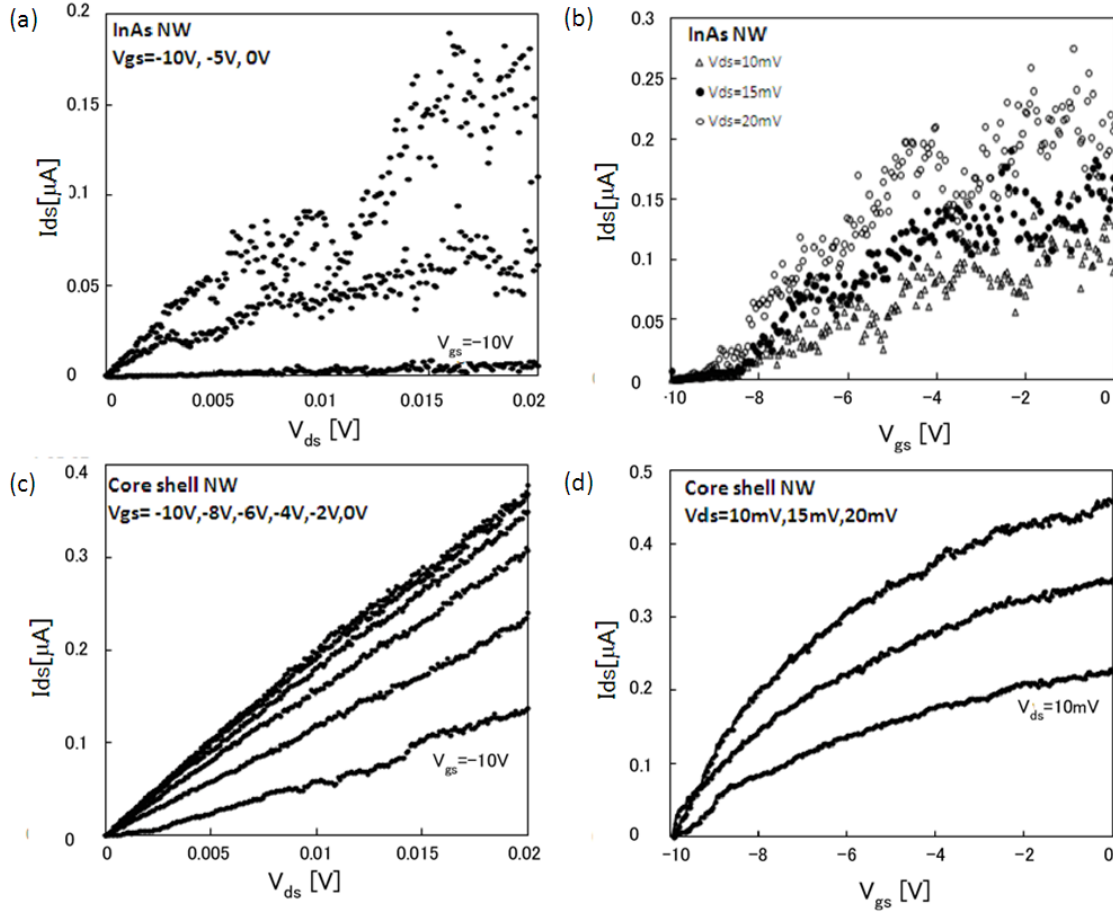


Figure 3.4: (a), (b) Characteristics of a simple InAs nanowire fabricated in parallel with the same device scales as the core shell nanowire device. (c), (d) The I_{ds} - V_{ds} and I_{ds} - V_{gs} of a representative δ -dope core shell nanowire device with a diameter of 40 nm (28 nm InAs core) and channel length (L) of 1 μm (Fig. 3.2).

In the linear operating region, the accumulation charge is given by $Q_{acc} = C(V_{gs} - V_t)$, where C is the gate capacitance and V_t is the threshold voltage. The source-drain current, I_{ds} , can then be derived as:

$$I_{ds} = \int qnvdA = \mu_{FE} Q_{acc} V_{ds} / L_g^2 = \mu_{FE} C(V_{gs} - V_t) V_{ds} / L_g^2, \quad (3.1)$$

where q is the electron charge, n is the electron concentration, v is the drift velocity, μ_{FE} is the field-effect mobility, L_g is the gate length, and A is the cross-sectional area of the nanowire.

At a drain-source voltage (V_{ds}) of 20 mV, a peak transconductance (g_m) of $\sim 0.11 \mu\text{S}$ and on-current of $0.5 \mu\text{A}$ are able to be recognized from drain-source current (I_{ds}) versus gate voltage (V_{gs}) data (Fig. 3.4b). According to Eq.3.1, the field-effect mobility μ_{FE} can be expressed as following.

$$\mu_{FE} = \frac{g_m L_g^2}{C V_{DS}} \quad (3.2)$$

To obtain an estimate for the field-effect mobility of the nanowire, the gate capacitance of $\sim 30 \text{ aF}/\mu\text{m}$ is calculated using a cylinder on a conducting plate model of Eq.3.3, which is the general form for back-gate nanowire FETs and nanotube FETs and have been used extensively [10-13].

$$C = 2\pi\epsilon L_g / \ln \left[\left(t_{ox} + a + \sqrt{(t_{ox} + a)^2 - a^2} \right) / a \right], \quad (3.3)$$

where ϵ is the insulator dielectric constant, t_{ox} is the SiO_2 insulator thickness of 100 nm, and a is the nanowire radius. This model is based on the assumption that the nanowire is an equipotential surface like in metals and owns infinite length. Since our nanowires have not been intend doped during the growth, the doping concentration should be relatively low, particularly the core/shell nanowire with the InP shell. Meanwhile, other effects such as the interface-charge capacitance corrections have not been taken into account, thus, the expressions above may not

be quite accurate. However, our interesting in this chapter is to confirm the superiority of the core/shell structure nanowire, thus, these lower-bound field-effect mobility values are able to provide a fair comparison between the core/shell structure nanowire and the common nanowire. In order to calculate the field-effect mobility, contact resistances (R_c) were taken into account because the ohmic contact formation in these devices had not been optimized. The two-terminal resistance could be valued from Fig. 3.3(a) at $V_{gs} = 0$ V which is ~ 50 k Ω . With a four-terminal device, as shown in Fig. 3.2(b), we measured the nanowire resistance as ~ 28.1 k $\Omega/\mu\text{m}$. For this transistor device case which is $L = 1$ μm and $D = 28$ nm, the resistance of nanowire ($R_{nanowire}$) was estimated as 28.1 k Ω . At $V_{ds} = 20$ mV, $V_{channel} = V_{ds} R_{nanowire} / (R_{nanowire} + R_c) = 11.2$ mV was used to replace V_{ds} of Eq. 3.2 for mobility calculation, while the field-effect mobility μ_{FE} was calculated as ~ 4600 cm²/Vs. For comparison, InAs nanowire devices were also fabricated in parallel with the same device scales whose transistor characteristics were shown in Fig. 3.3(c) and (d). Comparison of our δ -dope InAs/InP core shell nanowire and simple InAs nanowire device g_m at $V_{ds} = 20$ mV shows an increase for core shell ($g_m = 0.11$ μS) versus simple nanowire ($g_m = 0.04$ μS), which corresponds to the enhanced electron mobility. Mobility of InAs nanowire device at $V_{ds} = 20$ mV was also calculated to be ~ 800 cm²/Vs with same model as Eq. 3.2. An approximately 6-fold increase of mobility was obtained for core shell InAs/InP nanowire device. Drastically improved mobility is presumably caused by the InP shell passivation which reduced the surface scattering and formed a quantum confined electron gas in the InAs/InP core shell nanowire heterostructure. The effect of strain to the transport properties cannot be separated from the improved interface effect at the moment. Moreover, the drain-source current degradation during measurements, which is a common phenomenon for the simple InAs nanowire devices, was not observed in InAs/InP core shell nanowire transistors, which indicates the enhanced robustness of core shell nanowires.

We also investigated the temperature dependence of the InAs/InP core shell nanowire transistor performance. I_{ds} versus V_{gs} measurements were carried out at room temperature (RT), 90 K, 25 K and 1.5 K respectively (Fig. 3.5a). At low temperature less than 90K, the on current decreased from 2 μ A (RT) to 0.9 μ A which could be caused by the contact resistance increase. Field-effect mobility at $V_{ds} = 0.1$ V of each case was calculated and increased from ~ 4600 cm^2/Vs at RT and then saturated at ~ 5600 cm^2/Vs for the temperature less than 90 K (Fig. 3.5b). The weak temperature dependence of mobility might reflect the interface scattering domination with such a narrow InAs core diameter even though the better interface passivation was obtained.

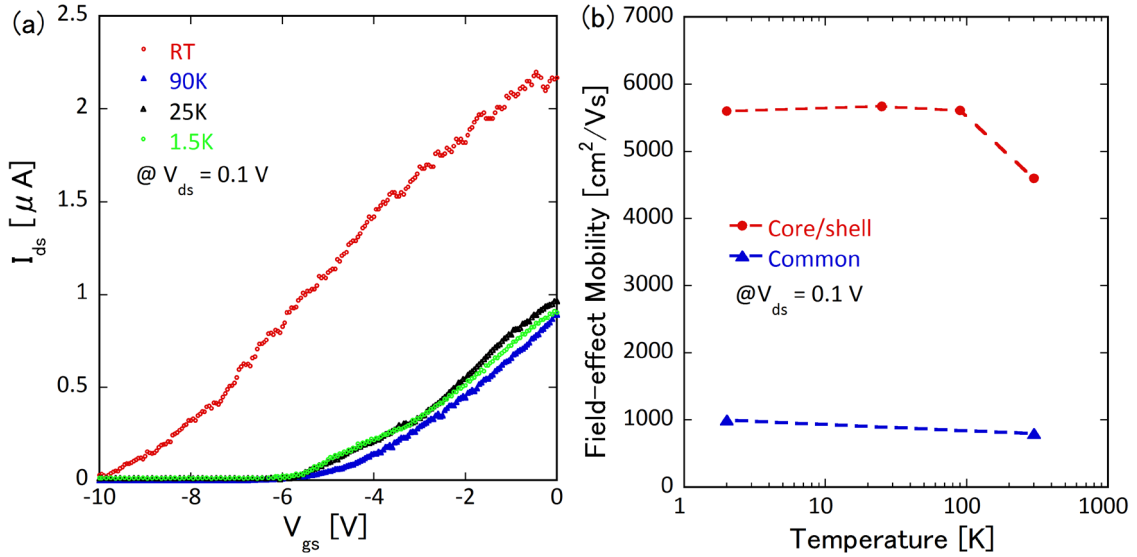


Figure 3.5: (a) The I_{ds} - V_{gs} characteristics of a representative δ -dope core shell nanowire device at RT, 90K, 25K and 1.5K respectively. (b) Calculated electron mobility of the representative core shell InAs/InP nanowire device at different temperatures.

The modulated carrier concentration in the nanowire FET channel underneath the gate can be calculated from Eq.1 and is given by:

$$n = \frac{I_{ds} L}{q \mu_{FE} V_{ds} A} \quad (3.4)$$

The calculated carrier density is around $\sim 2.4 \times 10^{17} \text{ cm}^{-3}$. If assume the electron transport only occurs on the interface between InAs core and InP shell, a two-dimension carrier density n_{2D} as $\sim 1.8 \times 10^{11} \text{ cm}^{-2}$ can be obtained.

3.4 Spin Transport Properties in Core/shell Nanowire

3.4.1 Weak Localization and Weak Anti-localization

The quantum diffusion called weak localization can be described qualitatively as below. Consider an electron diffusing at low temperature in 2-dimensional system at the origin at time $t = 0$, whose diffusion path is shown as Fig. 3.6. In the case of classical diffusion, the electron could propagate along the solid lines and return to the original position due to several times scattering, otherwise, propagate along the dash lines and return to the original. And the possibility of $1/(4\pi Dt)$, which is the algebraic sum of these two cases, can be deduced by the diffusion equation of Eq.3.5 as :

$$p(\vec{r}, t) = \frac{1}{4\pi Dt} \exp\left(\frac{-r^2}{4\pi Dt}\right) , \quad (3.5)$$

where D is diffusion coefficient, r is the position, and t is the time. However, in the quantum diffusion, due to the wave-like character of electron, the electron can be considered as waves propagate along the solid lines and dash lines simultaneously. If the several times of scattering at low temperature are elastic, the waves return to the original without losing of phase, therefore, the phases of the two partial waves are coherent. The amplitudes of solid lines wave (A') and the dashed lines wave (A'') are equal, $A' = A'' = A$, because their partial waves propagated on the same path in opposite directions. Thus, instead of the algebraic sum of possibility, their amplitudes add so that the possibility of return to the original is $|A' + A''|^2 = 4|A|^2$, which is twice as great as the classical one. For other states sufficient far away from the original, there is only incoherent superposition of every two sequences. This

tendency of return to the original or localization, which is result in a decrease of the conductance, is called weak localization (WL) [4]. In a magnetic field, however, the phase coherence of the two partial waves is weakened or destroyed. Therefore, this phenomenon in a low dimensional system can be confirmed with the observation of the magneto-conductance at low temperature.

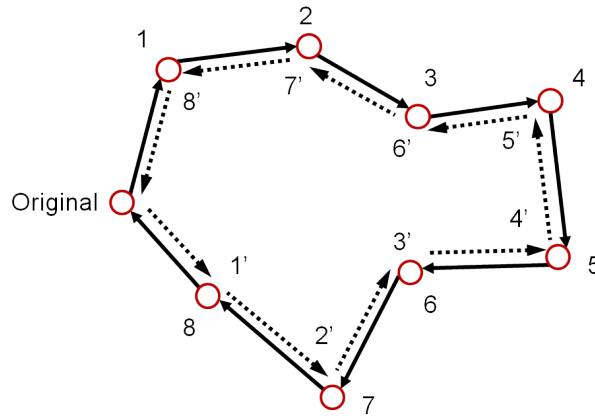


Figure 3.6: Schematic of electron diffusion paths. Since in the quantum diffusion, the electron which considered as wave can propagate along the solid lines and the dashed lines simultaneously. The probability to return to the origin is twice as great as in classical diffusion in the case of inelastic scattering.

Meanwhile, if we consider this diffusion occurred in a conductor owing spin orbit interactions, the electron spin would rotate during the propagations due to the effective magnetic field, even the scattering is elastic. The electron is a spin $1/2$ particle which has to be rotated by 4π to return to the original function. In the case of elastic scattering diffusion talked above, if the electron waves return to the original with a rotation of 2π which reverses the sign of the spin state. Instead of constructive interference, a destructive interference, due to opposite spin states of the two waves, reduces the possibility of return to the original. Averagely, the sum of amplitudes of the two partial waves is only $1/\sqrt{2}$. This corresponds to a forward propagation and an increase of the conductance, which is so called weak

anti-localization (WAL) [4]. And this phenomenon is also can be confirmed with the observation of the magneto-conductance at low temperature in the low dimensional system owns spin orbit interactions.

3.4.2 Enhancement of Spin Transport Properties in Core/shell Nanowire

As discussed above, the WL and WAL are the quantum corrections to the conductance of the low dimensional systems caused by the interferences such as spin orbit interactions. On the other hand, one can evaluate the spin orbit interactions by the investigations of the WL and WAL of a low dimensional conductor. Meanwhile, the Rashba spin orbit interaction can be controlled by an external voltage, therefore, the observation of the external voltage dependent WAL is a valid method to investigate the Rashba spin orbit interaction. In the case of the InAs nanowires, the spin orbit interactions were investigated by the observations of the magneto-conductance of similar nanowire back gate FET structures above [6, 7].

In this thesis, an enhance spin transport properties due to the structure of core/shell nanowire is expected, so that, with a tunable back gate voltage at low temperature, the magneto-resistance of a single core/shell nanowire is investigated. As shown in Fig.3.7, the measurements are carried out with a similar back gate FET structure based on a single InAs/InP core/shell nanowire at low temperature of ~ 10 K. An external magnetic field is applied to the back gate FET perpendicular to the core/shell nanowire. At a gate voltage of 60 V, the magneto-resistance is showing a valley in the vicinity of the zero magnetic fields. This valley-like magneto-resistance is consistent with the discussions of WAL above. In particular, the large gate voltage enhanced the Rashba spin orbit interaction, correspondingly, the WAL emerge due to the destruction of WL. In order to confirm this analysis, the magneto-conductance at different gate voltage are measured. As shown in Fig. 3.8, magneto-conductance $\Delta G = G(B) - G(0)$, offset to zero at the zero magnetic field, is plotted at different gate voltages without smoothing process. Along with the

decrease of the gate voltage, WAL became WL eventually, because the spin orbit interaction was lowered by the gate voltage. This crossover of magneto-conductance from WAL to WL dependant on the gate voltage is also reported in the previous reports on the common InAs nanowires [6-8]. Significantly, the measurements of the variation in conductance as a function of magnetic field allow us to abstract the phase coherence length l_ϕ and spin-orbit relaxation length l_{so} .

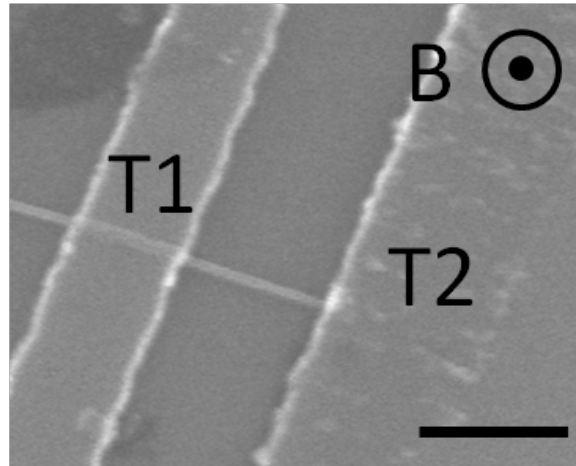
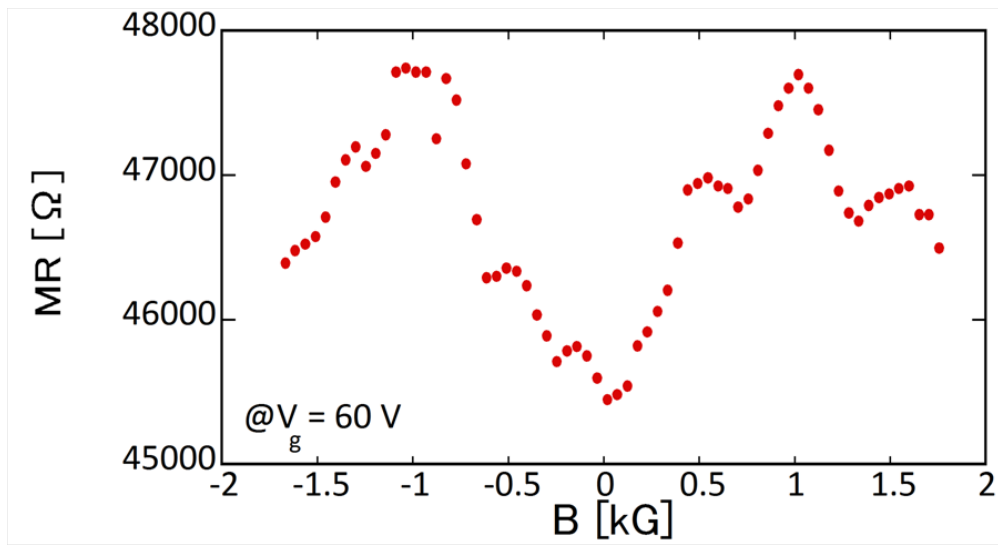


Figure 3.7: The magneto-resistance of a back gate FET structure (SEM) at the $V_g = 60$ V. The scale bar is 1 μm .

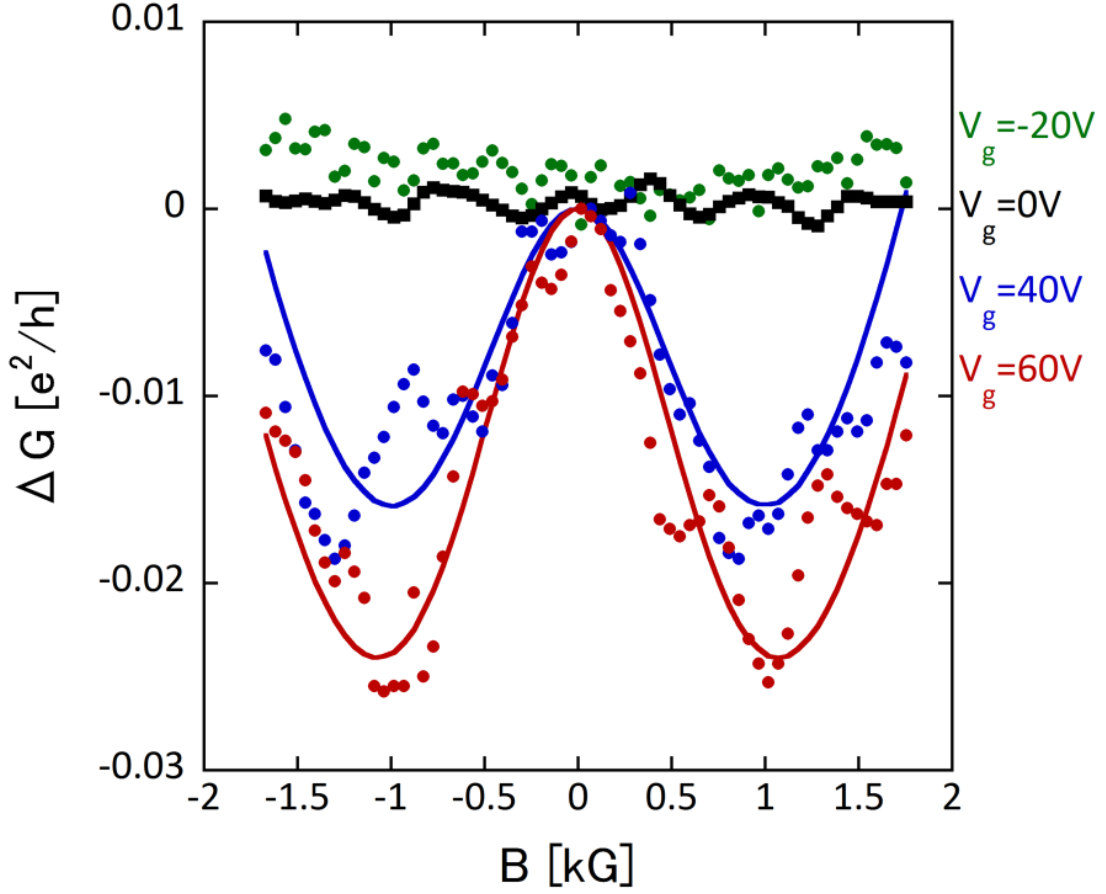


Figure 3.8: The magneto-conductance, offset to zero at zero magnetic field, plotted for 4 different gate voltages at a temperature of ~ 10 K. A crossover from WL to WAL takes place as the gate voltage is increased. Solid lines are fits to Eq. 3.2.

To characterize this transition, we consider a quasi-one-dimensional model which assumes $L \gg l_\phi \gg D \gg \lambda_F$, where L is the length of the nanowire and D is diameter. In the case the core/shell nanowire is considered as a tube-like electron transport channel, the Fermi wave vector $k_F = 1.06 \times 10^6 \text{ cm}^{-1}$ can be calculated by:

$$k_F = (4\pi n_{2D} / g_s g_v)^{1/2}, \quad (3.6)$$

where n_{2D} is the two-dimension carrier density as $\sim 1.8 \times 10^{11} \text{ cm}^{-2}$, $g_s = 2$ is the spin degeneracy, and $g_v = 1$ is the valley degeneracy of InAs. Correspondingly, the elastic mean-free path l_e can be calculated as $\sim 37 \text{ nm}$:

$$l_e = v_F \tau_e = \frac{\hbar k_F}{m} \frac{m \mu_{FE}}{q} = \frac{\hbar k_F \mu_{FE}}{q}, \quad (3.7)$$

where v_F is the Fermi velocity, τ_e is elastic scattering time, m is the effective mass of the electron in InAs. This result is larger than the previous reports [6, 7], which implies our core/shell nanowire owes better transport properties. One can fit the results according to the theory of the dirty metal regime ($l_e \ll$ diameter) or the theory of the pure limit ($l_e \gg$ diameter) [3, 4]. Since the mean-free path of ~ 37 nm is slightly less than the diameter of the core/shell nanowire, in order to extract the spin relaxation length (l_{so}) and coherence length (l_ϕ) meanwhile and compare our result with the previous reports, we fitted the correction of the conductance $\Delta G(B)$ as the solid lines in Fig. 3.7 by dirty metal regime with Eq.3.8 below,

$$\Delta G(B) = -\frac{2e^2}{hL} \left[\frac{3}{2} \left(\frac{1}{l_\phi^2} + \frac{4}{3l_{so}^2} + \frac{1}{D_c \tau_B} \right)^{-\frac{1}{2}} - \frac{1}{2} \left(\frac{1}{l_\phi^2} + \frac{1}{D_c \tau_B} \right)^{-\frac{1}{2}} \right], \quad (3.8)$$

with D_c being the diffusion constant and τ_B the magnetic relaxation time. For large gate voltages, we extracted $l_{so} \sim 290$ nm and $l_\phi \sim 360$ nm. Assume the Rashba spin orbit interactions without external electrical fields are equal in the core/shell nanowires and the common nanowires, we can compare our results with the previous reports of the common InAs nanowires [6, 7]. The spin relaxation length and coherence length in our core/shell nanowire are both longer than the previous reports of the common nanowires whose spin relaxation lengths are $100 \sim 200$ nm even in the weak Rashba rang (low back gate voltage cases). Since the spin relaxation length $l_{so,R}$ due to Rashba is inversely proportional to the strength of Rashba according to the Eq. 3.9, this enhanced spin relaxation length in our core/shell nanowire should be caused by the reductions of other spin relaxation mechanisms.

As discussed in Sec.1.3, the major physical spin relaxation mechanisms in nanowire spin FET are the DP and EY mechanism. DP mechanism is the spin

relaxation processes due to the spin orbit interaction including Rashba and Dresselhaus spin orbit interactions. And EY mechanism is the spin relaxation due to the scattering of ionized defects. Since these three spin relaxation mechanisms providing different spin relaxation length, we can investigate and compare them with the results of our core/shell nanowires.

First, the effects of Dresselhaus are discussed as following. In our $\langle 111 \rangle$ -oriented InAs/InP core/shell nanowire, according to the transport properties characterizations with the back-gate transistor structures, the electron transport alone the $[111]$ direction on the interface of InAs core and InP shell, which is a conclusion of the mobility temperature dependency discussed above. The $\langle 111 \rangle$ -oriented InAs nanowires grown on the (111) substrate own a hexagonal cross-section and six $\{110\}$ side-walls (facet). Therefore, it can be assumed that the electrons propagates on a tube-like $\{110\}$ 2-dimentional channel along the $[111]$ direction. According the effective magnetic fields calculations of 2-dimentional InGaAs system [14], the propagation of electron in $\langle 111 \rangle$ -oriented nanowire can be described schematically with Fig. 3.9. The 2-dimentional InGaAs system with $k_x // [00-1]$ and $k_y // [-110]$ provides the effective magnetic field perpendicular to the plane. This situation is remarkable, if the spin is vertically injected into the system, DP due to Dresselhaus spin relaxation can be totally suppressed [15].

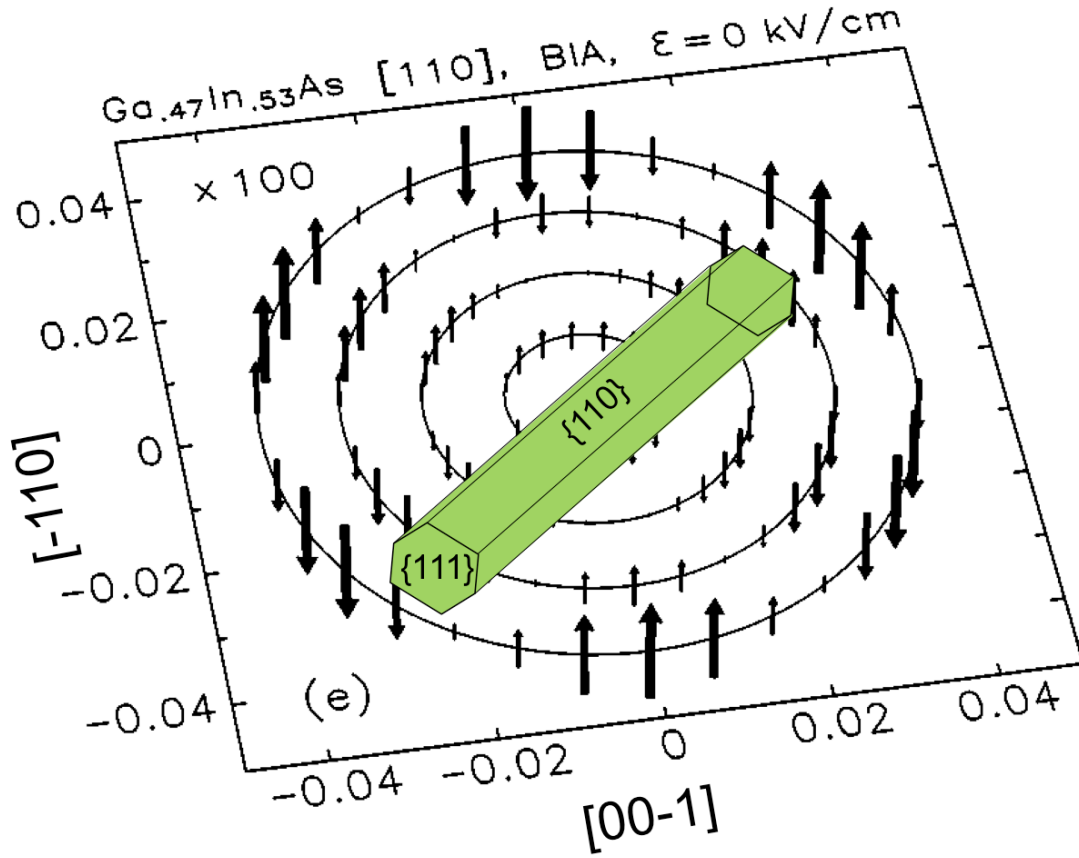


Figure 3.9: The schematic of $\langle 111 \rangle$ -oriented InAs nanowire with $\{110\}$ side-walls along with the effective magnetic field calculation due to Dresselhaus spin interaction of (110) plane. The interface between InP shell and InAs core including six $\{110\}$ facets is a tube-like 2-dimensional transport system, so that, the Dresselhaus DP spin relaxation factor is a (110) type. The calculation of the InGaAs (110) plane shows the effective magnetic fields perpendicular to the plane

And the spin splitting is absent in the $\langle 111 \rangle$ direction in our nanowire [16], so that, the relaxation due to Dresselhaus might be sufficient long to be negligible in this core/shell case. This assumption can be supported by calculation with Eq. 3.8 using the parameters of bulk InAs and the Fermi wave vector k_F of $\sim 1.06 \times 10^6 \text{ cm}^{-1}$ of our core/shell nanowire.

$$l_{so,D} = \frac{\hbar^2}{m_e k_F^2 \gamma} \quad (3.8)$$

The estimated spin relaxation length dependent on the Dresselhaus is $\sim 11 \mu\text{m}$, which is much larger than our results deduced from the fitting of WL and WAL measurements. This implies than Dresselhaus parts of DP spin relaxation in our core/shell nanowire system is negligible, so that, the Rashba is the dominant factor of the DP mechanism. If we ignore other spin relaxation factors except Rashba, the Rashba coefficient α can be deduced as $\sim 1.1 \times 10^{-11} \text{ eVm}$ using $l_{so} \sim 290 \text{ nm}$ with the Eq. 3.9 as following. And this result agrees with the typical Rashba coefficient of the conventional InGaAs heterojunction HEMT structure, which is around $0.5 \sim 1.5 \times 10^{-11} \text{ eVm}$ [17].

$$l_{so,R} = \frac{\hbar^2}{m_e \alpha} \quad (3.9)$$

Another spin relaxation mechanism working in our system is the EY mechanism, which causes spin relaxation in the case of ion scattering. Every time the electron scatters to a new state, during the collision, there is chance to couples a different spin from the ion impurity. The typical spin relaxation length is expressed with Eq. 3.10 [18]

$$l_{so,EY} = \frac{0.61 l_e E_g (E_g + E_{SO}) (3E_g + 2E_{SO})}{E_F E_{SO} (2E_g + E_{SO})}, \quad (3.10)$$

where E_g is the band gap of 0.35 eV, E_F is the Fermi energy, and E_{SO} is the spin splitting of valance band of 0.41 eV. And the relaxation length due to EY mechanism is about $\sim 360 \text{ nm}$. This estimation abased on the calculation is comparable to the results deduced from the WL-WAL fitting, so that, the EY mechanism could be an important factor to our $\langle 111 \rangle$ -oriented InAs/InP core/shell nanowire. Furthermore, it is well known that the electron accumulation occurs at

the surface of the nanowires, in case of the common InAs nanowire with the bare side-walls, the surface scatterings play a dominant role for the electron transports. Including surface roughness scattering, surface ionized impurity scattering and native oxide charge traps, produce strong scattering potentials [19, 20], which could limit the electron mobility and spin relaxation length. Therefore, the enhanced spin relaxation length in our core/shell nanowires probably due to suppression of the EY mechanism, particularly on the surface of the InAs nanowires. Another important issue, which could explain the low field-effect mobility and less spin relaxation length, is the band discontinuous due to structural defects of WZ/ZB. Since the WZ InAs has a $\sim 20\%$ larger band-gap than ZB InAs [21], so that for electrons and spins, stacking faults correspond to potential wells, which would limits the mobility and spin relaxation length. These transport properties due to the band discontinuous are discussed in chapter 5 specifically as well.

Another point should be mentioned is that the interface of InAs core and the InP shell would provide a better transport channel compare with the bare surface of the common nanowires, even there should be lattice mismatch between InP and InAs, the scattering is much lower than the surface of the common nanowire. On the other hand, the lattice mismatch and impurities in the InAs core close to the interface might be the dominant reasons for the EY mechanism in core/shell nanowires.

As conclusions of this chapter, enhanced spin transport properties and electrical transport properties in our core shell nanowires are confirmed, which are presumably attributed to the InP shell passivation. Decent transport properties and reduced spin relaxation were revealed by extracting l_{so} and l_{ϕ} from a crossover from WL to WAL. By comparing with common InAs nanowire devices fabricated separately, superiority of core/shell nanowire structures were verified in field-effect mobility and spin relaxation length, suggesting the effectiveness of the InP shell passivation which reduced the EY mechanism due to the surface scatterings. In

summary, the InAs/InP core/shell nanowire structure is suitable to be applied to spin transport devices particularly the Datta-Das spin FET. Also, lower impurity growth of nanowire in MBE system will not only lead better electrical transport properties but also an enhanced electron spin transport, since the spin relaxation due to the ion scattering is playing an important role in InAs nanowires.

Bibliography

- [1] S. A. Dayeh and D. Wang, *Small*. 2, 326 - 332 (2007).
- [2] S. Chuang, Q. Gao, R. Kapadia, AC. Ford, J. Guo, and A. Javey, *Nano Lett.* 13, 555–558 (2013).
- [3] B. L. Altshuler and A. G. Aronov, *JETP Lett.* 33, 499 (1981).
- [4] G. Bergmann, *Solid State Commun.* 42, 815 (1982).
- [5] S. Hikami, A. I. Larkin, and Y. Nagaoka, *Prog. Theor. Phys.* 63, 707 (1980).
- [6] S. Dhara, H. S. Solanki, V. Singh, A. Narayanan, P. Chaudhari, M. Gokhale, A. Bhattacharya, and M. M. Deshmukh, *Phys. Rev. B* 79, 121311(R)(2009).
- [7] P. Roulleau, T. Choi, S. Riedi, T. Heinzl, I. Shorubalko, T. Ihn, and K. Ensslin, *Phys. Rev. B* 81, 155449 (2010).
- [8] A. E. Hansen, M. T. Bjork, I. C. Fath, C. Thelander, and L. Samuelson, *Phys. Rev. B* 71, 205328 (2005).
- [9] D. B. Suyatin, C. Thelander, M. T. Björk, I. Maximov, L. Samuelson, *Nanotechnology* 18, 105307 (2007).
- [10] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, *Appl. Phys. Lett.* 73, 17 (1998).
- [11] D. Wang, Q. Wang, A. Javey, R. Tu, and H. Dai, *Appl. Phys. Lett.* 18, 12 (2003).
- [12] O. Wunnicke, *Appl. Phys. Lett.* 89, 083102 (2006).
- [13] D. Vashaee, A. Shakouri, J. Goldberger, T. Kuykendall, P. Pauzauskie, and P. Yang, *J. Appl. Phys.* 99, 054310 (2006).
- [14] R. Winkler, *Phys. Rev. B* 69, 045317 (2004).
- [15] M. I. D'yakonov and V. Y. Kachorovski, *Sov. Phys. Semicond.* 20, 110 (1986).
- [16] G. Dresselhaus, *Phys. Rev.* 100, 580 - 586 (1955).
- [17] C. Hu, J. Nitta, T. Akazaki, and H. Takayanagi, *Phys. Rev. B* 60, 7736 (1999).
- [18] J. N. Chazalviel, *Phys. Rev. B* 11, 1555 (1975).
- [19] J. Salfi, N. Paradiso, S. Roddaro, S. Heun, S. V. Nair, I. G. Savelyev, M. Blumin,

- F. Beltram and H. E. Ruda, ACS Nano. 5, 2191–9 (2011).
- [20] J. Salfi, S. V. Nair, I. G. Savelyev, S. Roddaro, M. Blumin, and H. E. Ruda, Phys. Rev. B 85, 235316 (2012).
- [21] J. Bao, D. C. Bell, F. Capasso, N. Erdman, D. Wei, L. Froberg, T. Martensson and L. Samuelson, Adv. Mater. 21, 3654–8 (2009).

Chapter 4

$\langle 110 \rangle$ -oriented InAs Nanowire

4.1 Introduction

At room temperature, as discussed in Sec.1.2, electron spin relaxation due to the D'yakonov–Perel' mechanism, which involves Dresselhaus and Rashba spin orbit interactions, is the most dominant, while it has also been demonstrated that, when the Rashba and Dresselhaus SOI linear-in- k terms have equal strength, the spin orientation relaxation in one of the $\langle 110 \rangle$ axes is totally suppressed. Hence, compared with $\langle 111 \rangle$ -oriented nanowires, we anticipated that InAs nanowires with $\langle 110 \rangle$ orientation could be a more promising material for spintronics devices as an efficient 1D spin transport channel. Therefore, investigations into InAs nanowire growth and transport properties are desirable for the development and refinement of spintronics applications.

However, the most common nanowire growth by VLS techniques are Au-assisted $\langle 111 \rangle$ -oriented nanowires with $\{110\}$ side facets. Because of the inertness and the relative low alloying temperature, commonly, Au is utilized as the primary catalyst material. For the growth of $\langle 111 \rangle$ -oriented InAs, tremendous research effort has been devoted to this growth processes by various epitaxial growth techniques such as MBE [1], CBE [2], and metal organic vapor phase

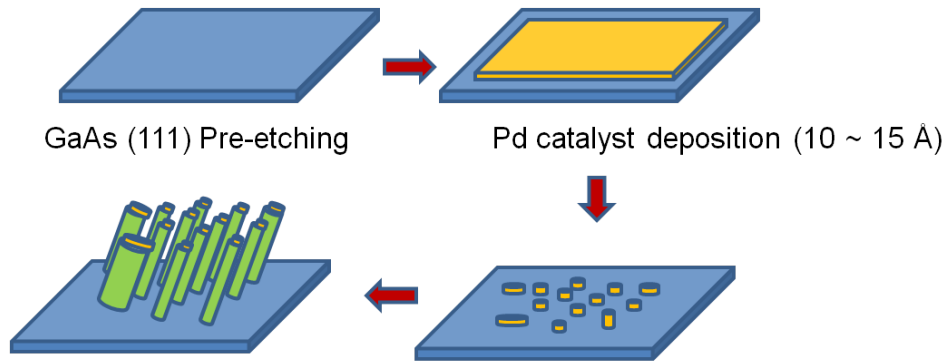
epitaxy (MOVPE) [3]. On the other hand, Au influences the semiconducting properties of the grown nanowires due to its fast diffusing as low doping features [4]. Furthermore, the harvested Au-assisted nanowires have suffered by having mixed zinc blende (ZB) and wurtzite (WZ) crystal phases together with numerous stacking faults. These kinds of structural defects seriously affect the device performance by increasing resistivity [5], suppressing carrier accumulation at the nanowire surface due to the polarization charge at the mixed crystal interfaces [6], decreasing the mean free path [4] and inducing non-radiative recombination centers [7]. Therefore, it is necessary to explore alternative promising catalyst materials, in order to eliminate undesirable phenomena.

Recently, palladium (Pd) has been proposed as an attractive catalyst material for the growth of InAs nanowire by various epitaxial growth techniques [7, 8]. Moreover, the grown Pd-assisted nanowires are projected along the <110> direction with respect to the GaAs (111)B substrate and exhibit excellent structural features [8]. The obtained nanowires have a defect free stable zinc-blende crystal phase throughout their length without any other crystal phase mixing, especially the wurtzite phase, which is to be commonly found in Au-assisted grown InAs nanowires. The absence of wurzite defects is extremely attractive property for the fabricated devices particularly electron spin transport devices. These interesting features of the Pd-assisted nanowires have tempted us to carry out this presented work using the MBE technique. As we discussed above, the nanowire growth process by MBE technique is able to provide higher quality of crystalline structure, which can is more prospective material for Spin-FET compared to other growth techniques. In this thesis, we have demonstrated the growth of Pd-assisted InAs nanowires based on the VLS growth mechanism using the same solid source molecular beam epitaxial technique. And this is the same MBE growth technique which is applied for the <111>-oriented InAs nanowires growth, consequently, we can compare the <111>- and <110>-oriented InAs nanowires of their transport

properties as well. Growth experiments have been carried out systematically by varying the density of the catalyst particles, growth temperature and In-flux and keeping the As-flux constant, and vice versa, in order to identify better growth conditions for getting device-quality InAs nanowires with reasonable density. The <110>-oriented InAs nanowires are grown with (111)B GaAs substrate and (111)B InAs substrate respectively.

4.2 VLS Growth of <110>-InAs Nanowire

Compared with the growth of <111>-oriented InAs nanowire using our solid source MBE system, the primary difference is that Pd catalyst is used for the growth of <110>-oriented InAs nanowire. Compared with <111>-oriented InAs nanowire growth, the formation of the catalyst particles is achieved in different technique. The Pd catalyst particles are fabricated by an annealing process of a Pd thin film in the MBE growth chamber as shown in Fig.4.1. The thickness of around 15 Å Pd is deposited on a GaAs (111)B or InAs (111)B substrate after a typical cleaning processes. After that, the annealing process is carried out at 600 °C (510 °C for InAs substrate) in As-atmosphere to scatter the Pd film and induce the alloying of Pd and In of the substrate. As shown in the Fig.4.2, the formation of Pd catalyst particles on the GaAs substrate due to the annealing process round 600 °C of a 15 Å thick Pd-layer before the growth is confirmed using a Nanoscope IIIa model AFM (atomic force microscope) [9]. Clearly, Pd particles are formed with reasonable density and with diameters around 30 nm. With these Pd nanoparticles or droplets, a typical VLS process can be carried out which leads the growth of <110>-oriented InAs nanowires growth. The purpose of this chapter is that define the growth parameters of <110>-oriented InAs nanowire in order to make the fabrications of the single nanowire device convenient.



Growth: 425°C, 1-hr, As/In = 125.

Annealing: 600°C, 10-min, As-atmosphere

Figure 4.1: The schematic of <110>-oriented InAs nanowire growth on a GaAs (111)B substrate.

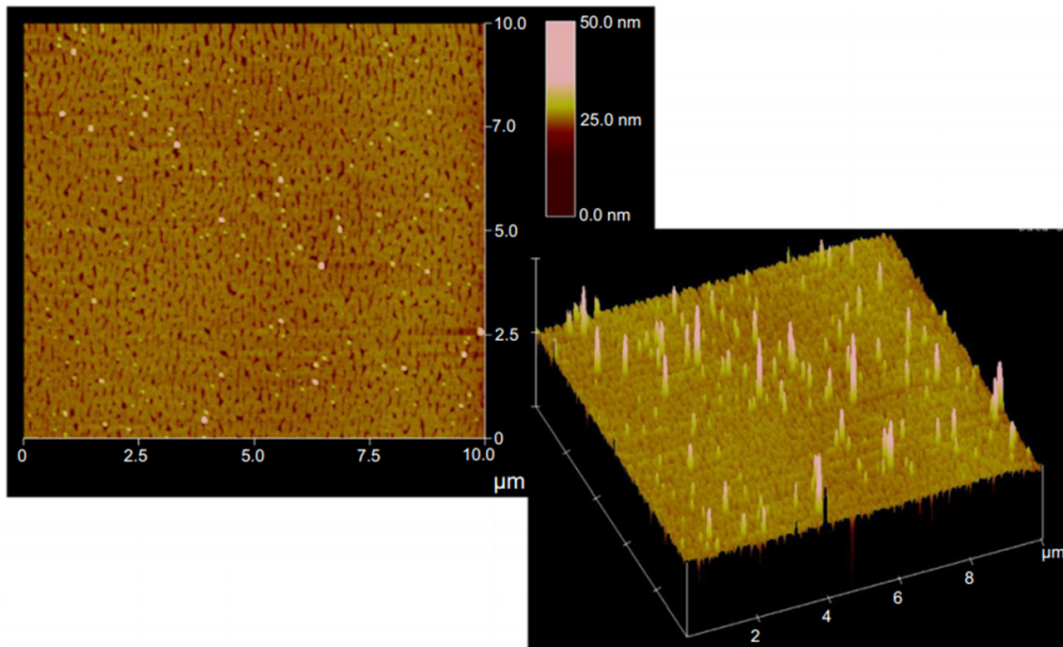


Figure 4.2: AFM images of Pd catalyst particles due to the annealing process of a 15 Å thick Pd-layer with 600 ° C for 10-min. A reasonable density and diameter of 30 nm are confirmed.

Following is the preparation of MBE growth substrate wafer and the MBE growth processes for <110>-oriented InAs nanowire growth.

First, the following is the preparation of the growth substrate wafer.

1. Cleaning: Dice a small fragment of epi-ready (111)B GaAs wafer, typically use sizes of around 1 cm. For the organic cleaning, sonicate the piece of wafer in acetone, ethanol, and isopropanol (IPA) for 3-min with weak power respectively. To remove the surface native oxide layer of InAs wafer, a brief etching around 30-sec with $\text{NH}_4 : \text{H}_2\text{O} = 1 : 10$ is preferred, following with a 1-min deionized water rinsing and blowing off with dry nitrogen.
2. Pd-catalyst layer deposition: Set the sample to the E-beam evaporation equipment, and wait the pressure vacuumed down to the 1.0×10^{-6} Torr. Start to evaporation after the degas process of Pd source. Since the thickness of the Pd layer is important for the formation of Pd catalyst particles, several thickness have been deposited. None of them is thicker than 50 Å, so a very low evaporation rate is preferred such as $1 \sim 2$ Å/sec.
3. After the Pd-catalyst layer deposition, the substrate wafer is set onto the MBE growth holder with melted In. Then, transfer the sample to the load-lock of MBE promptly.

After the preparation of growth substrate wafer, the growth process is carried out as following steps.

1. A pre-bake at 250 °C is carried out to remove water and other contaminant during transfer, before the growth substrate sample is transferred to MBE growth chamber.
2. Before the nanowire growth experiment, the Pd deposited substrate was annealed in the MBE growth chamber at 600 ~ 605 °C in an As atmosphere for 10 min to remove surface contaminants as well as to convert and agglomerate the Pd thin film into Pd nanoparticles.
3. Return the substrate temperature from the annealing temperature of 600 °C to the growth temperature of 425 °C.

4. Open the shutter of In source to start the growth, and the growth process is carried out for 1-hour to get enough length of nanowire. The flux of As and In is set to provide a large V/III ratio around 120 compared with <111>-oriented InAs nanowire growth. V/III ratio of 100, 125, and 152 are studied.

The nanowire growth processes based on the epi-ready (111)B InAs substrate wafer are similar to the growth processes of (111)B GaAs substrate wafer, except for the annealing temperature of Pd particles formation. Since InAs substrate is more fragile compared with GaAs, the annealing process of Pd-particles formation is around 500 ~ 510 °C. Certainly, the shutter of As source should be opened when the substrate temperature is increased to 250 °C, in order to form the atmosphere earlier to supply the As to the InAs substrate.

4.3 Results and Discussions

4.3.1 Dependence of Pd Film Thickness

Since the morphology and density of catalyst particles, growth temperature, and the V/III ratio are the key parameters of InAs nanowire VLS growth, three sets of growth experiments are carried out to indentify the thickness of Pd film, the growth temperature, and the V/III flux ratio. In order to verify these three parameters respectively, a set of parameters are defined as the standard condition which is confirmed in advance that can provide a reasonable nanowire growth. The standard condition is Pd thickness of 15 Å, growth temperature of 425 °C, and the V/III ratio of 125 with In flux of 2.0×10^{-7} Torr. The observations of Pd thickness by SEM are shown in Fig.4.3. With the other two parameters fixed as the standard condition, it is obvious that 15 Å, whose nanoparticles are confirmed by AFM as shown in Fig.4.2,

provides reasonable nanowire density. Despite the size of the droplet alloy, the higher In/Pd eutectic temperature [10] and lower chemical potential [11] give Pd the capability of replacing the Au. It should be noted that, according to the In-Pd binary phase diagram [10] showing in Fig.4.4, annealing temperature in this thesis around 600 °C is a eutectic temperature for the alloy dominating by In element. The red dash line marks the annealing temperature and the corresponding concentration of the Pd in the alloy droplet. This indicates that the In concentration of the In/Pd alloyed droplet is around 87 % which is contrary to the case of In/Au droplet.

The annealing process is not sufficient to form the nanoparticles with precise size and controllable density, therefore, for the thickness larger than 15 Å cases, nanowires are also grown successfully with little difference of density. It is believed that a range of Pd film can provide the growth of nanowire with the annealing temperature of 600 °C. However, nanoparticles formation have to be carefully because nanoparticles have strong van der Waals attractive force and thus agglomerate into larger particles. Furthermore, Ostwald ripening occurs between nanoparticles at high temperature because larger particles are more energetically favorable. Accordingly, small nanoparticles tend to accumulate into large particles to attain a lower energy state. Therefore, it is might difficult to obtain very small nanoparticles to grow extremely thin InAs nanowire with the annealing process. Actually, diameter from 40 to 400 nm of nanowire can be grown based on these nanoparticles, and this range of the nanowire diameter is proper for the single nanowire device fabrications.

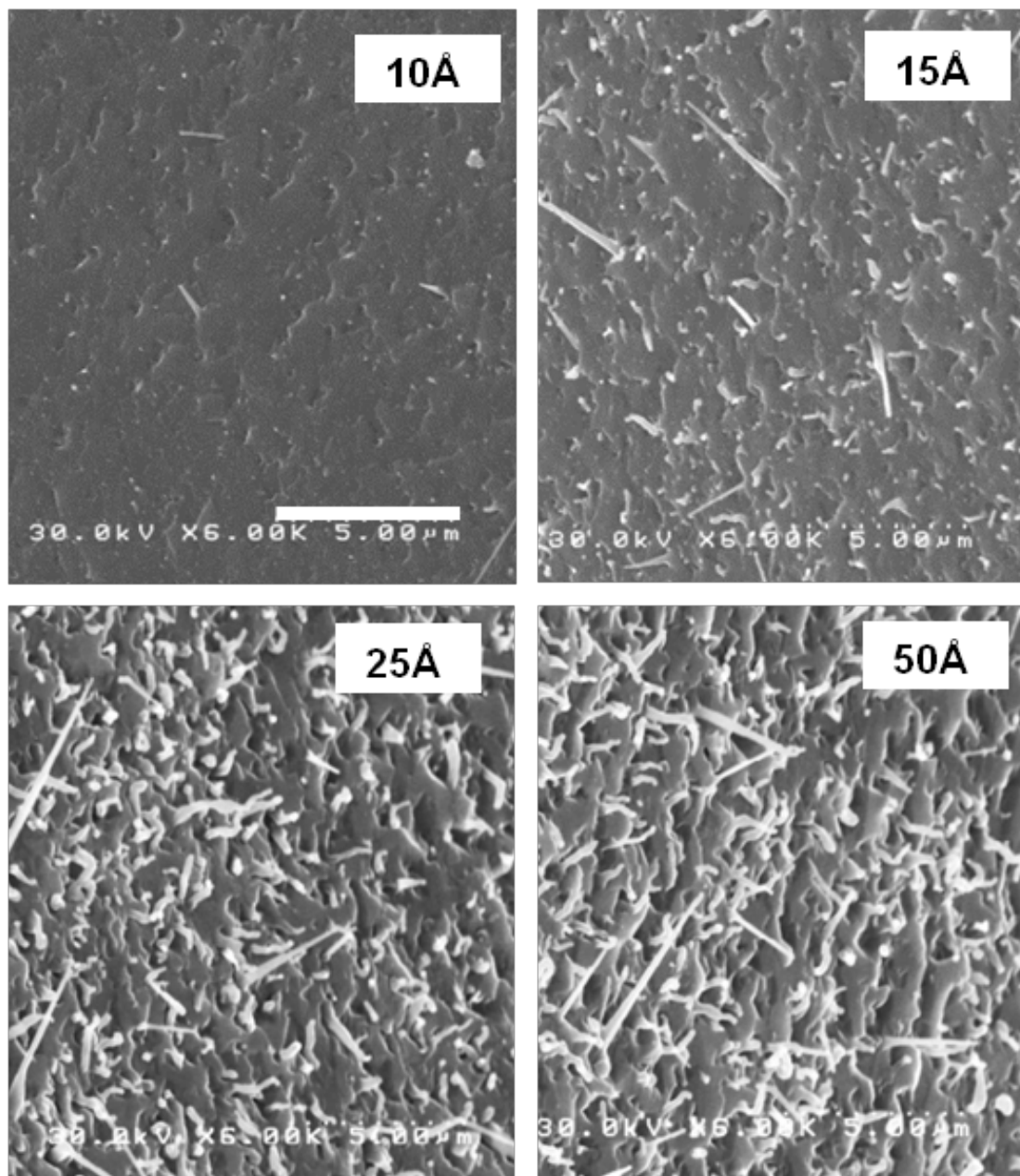


Figure 4.3: SEM images of <110>-oriented InAs nanowire grown with different thickness of Pd films. The scale bar is 5 μm.

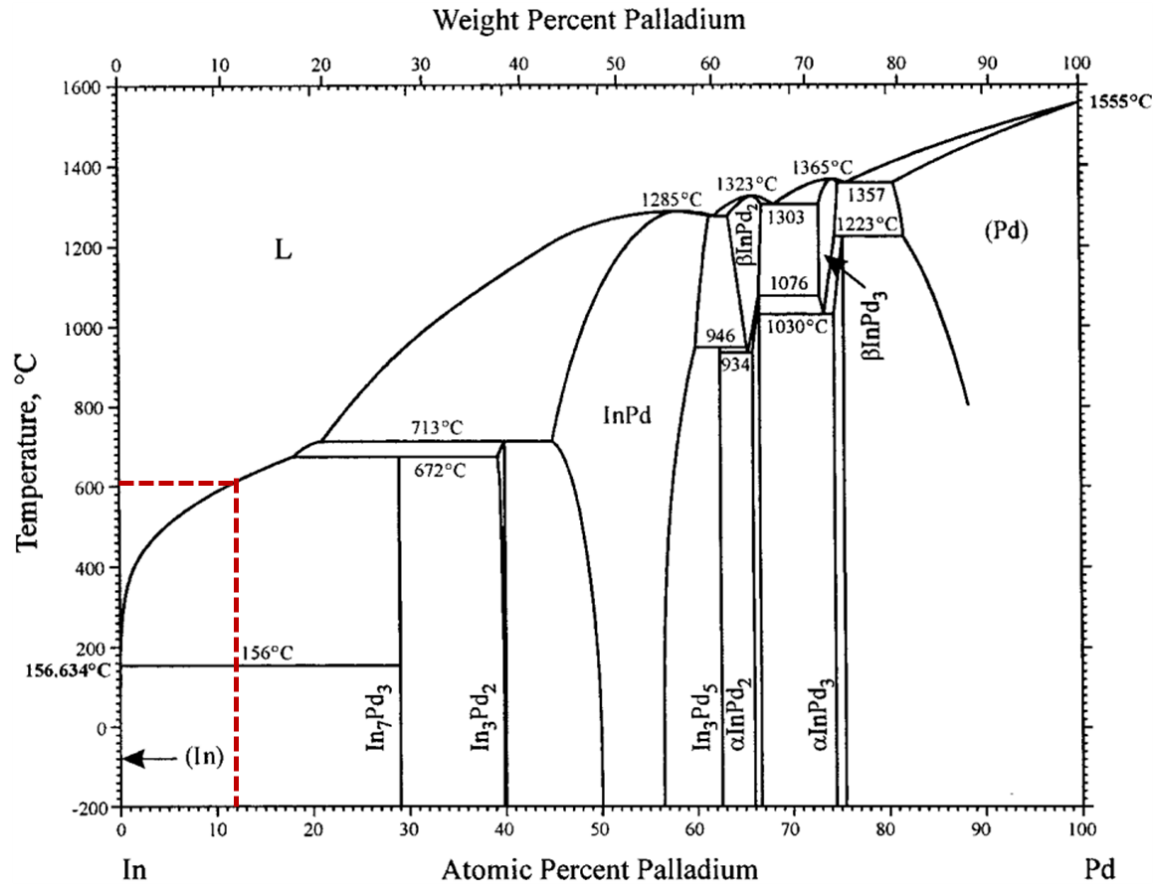


Figure 4.4: The binary phase diagram of In-Pd alloy. The red dash line marks the annealing temperature of the <110>-oriented InAs nanowire growth and the corresponding concentration of the Pd in the In/Pd alloy droplet.

4.3.2 Dependence of Growth Temperature

From the growth temperature verifications, SEM images of Fig.4.5 show the growth rate decrease while the temperature increases, until no nanowires were observed at 500 °C. This growth temperature dependence is common in the nanowire growth, and it can be explain the growth at high temperature turns to be 2-dimension growth. And it is believed that the diffusion length of In on the side facet of the nanowire is dependent on the growth temperature as well, so that, at low temperature such as 375 °C more tapering nanowire can be observed.

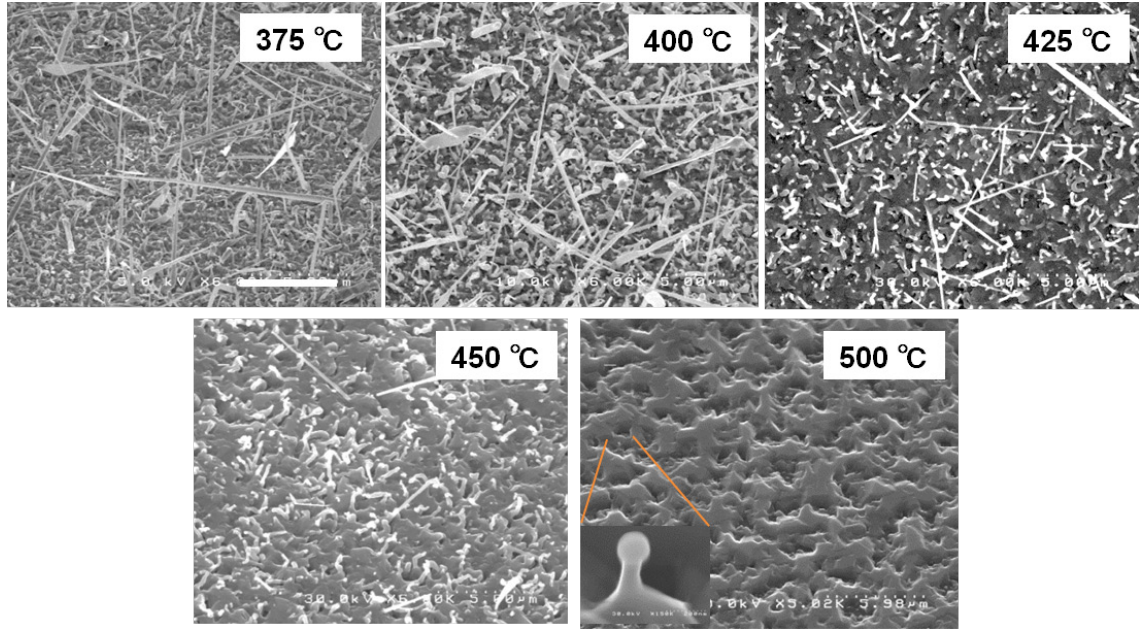


Figure 4.5: SEM images of <110>-oriented InAs nanowire grown with different growth temperature. The scale bar is 3 μm .

4.3.3 Dependence of As Flux and In Flux

Last, the V/III ratio of the nanowire growth is verified. Since the flux of As and In are both affect the growth of InAs nanowire vitally, they have been verified respectively with two sets of experiments. First sets are carried out for the dependence of As flux, so that, InAs nanowires have been grown at several As flux with other parameter as standard conditions and a constant In flux of 2.0×10^{-7} Torr. In the aspect V/III ratio, the growth processes were carried out from 52 to 152. From the SEM image of the harvested InAs nanowire as shown in Fig.4.6, at the low V/III ratio such as 52 and 76, no nanowires were observed except for dot-like structures. On the other hand, InAs are grown with reasonable growth rate and density at the higher V/III ratio such as 125 and 152. This As flux dependence is similar to the <111>-oriented InAs nanowire growth, a linear increase in growth rate is observed with the function of As flux. At low V/III ratio, the diffusion length of In is not long enough to proceed the axial growth. The increase in

As-flux has increased the As-species received by the catalyst particles. This eventually increases the mobility of the In-species towards the Pd-semiconductor interface and increases the effective number of In-adatoms consumed for the nanowire growth, which should be the reason that reasonable growth processes occurred at higher V/III ratio.

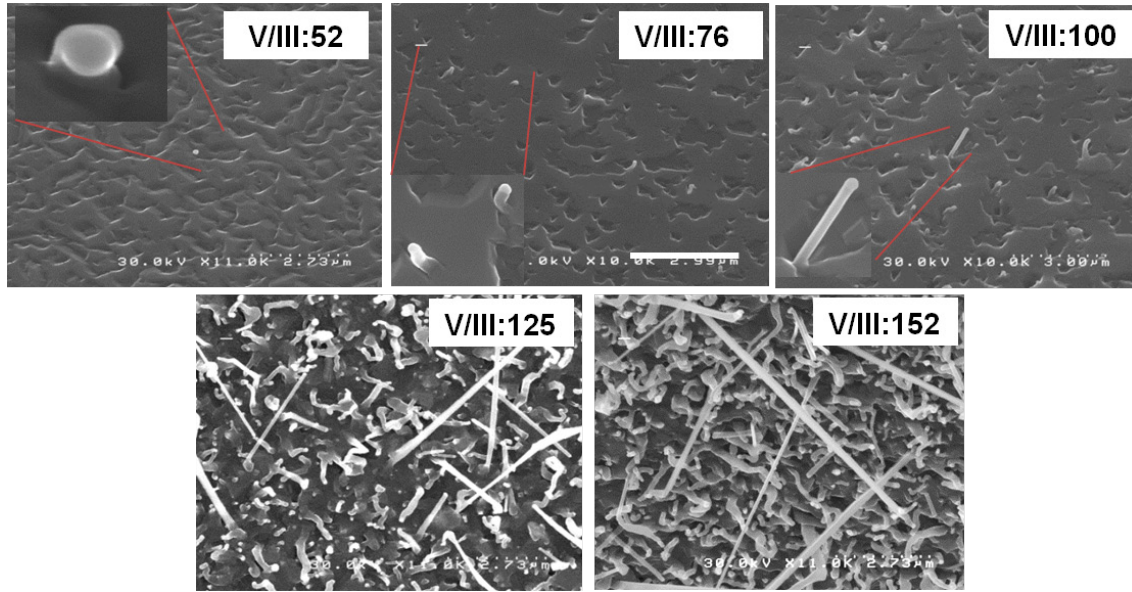


Figure 4.6: SEM images of <110>-oriented InAs nanowire grown with different V/III ratio with fixed In flux of 2.0×10^{-7} Torr. The scale bar is 3 μm .

In order to verify the dependence of the In flux, second sets growth processes are carried out at different V/III ratio such as 50, 70, 125, 150, and 225. The grown InAs nanowires are shown in Fig.4.7. It is obvious that nanowires at the V/III ratio of 50 are more tapering than other cases, and the tapering structure reduces with the decrease of In flux. In the high V/III ratio cases, the grown nanowire are more rod-like indicating the axial growth is dominated. Another variation during the changing of the V/III ratio is the density of nanowires, which decreased with the In flux as well. In the case of a lower V/III ratio (higher In-flux), the availability of In-adatoms exceeds the required level of nanowire growth, so radial growth becomes favored with the help of the excess In-adatoms, rather than axial growth by reducing indium diffusion length. The lower In-flux (higher V/III

ratio) effectively influences the density of the grown nanowires by changing the supersaturation level at the surface of the substrate, and as a result, fewer sites are only favorable for the nanowire growth, while the majority of the sites fail to reach the required critical supersaturation.

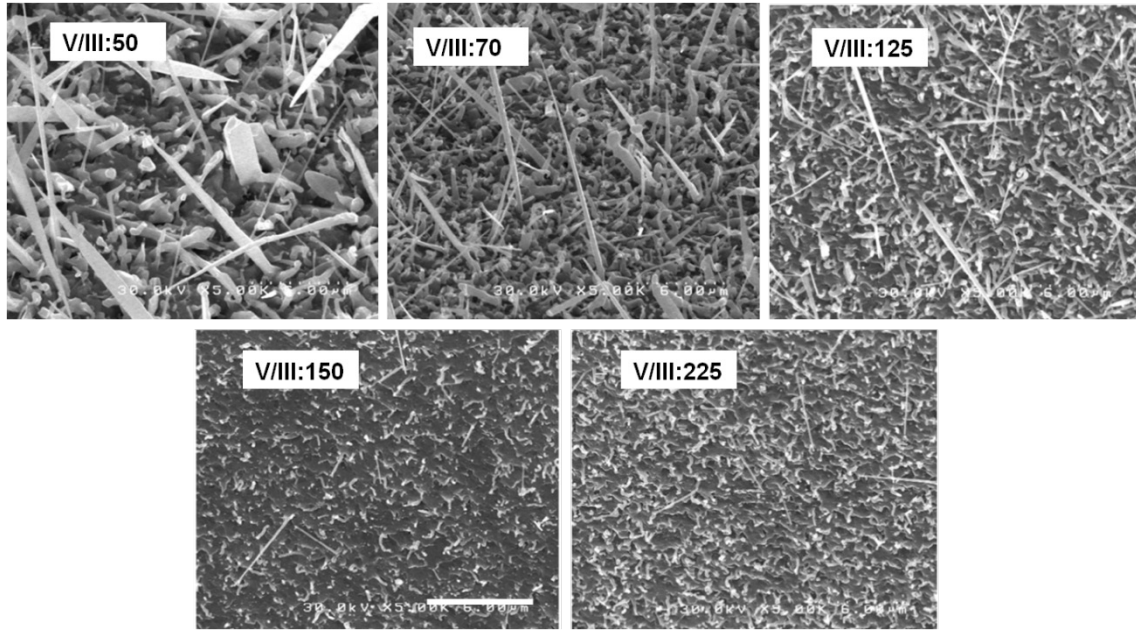


Figure 4.7: SEM images of <110>-oriented InAs nanowire grown with different V/III ratio with fixed As flux of 2.5×10^{-5} Torr. The scale bar is 6 μm .

Eventually, the dependence of the In flux and As flux at the standard condition are able to concluded as Fig.4.8, where the tendency of tapering, high growth rate and low density growth are denoted by the arrow signs. The growth points with their V/III ratios of the two sets are set along the dash lines. According to these growth results, the <110>-oriented InAs nanowire can be grown with sufficient diameter and length in order to fabricate the electronic devices based on a single nanowire. Since, in this thesis, nanowires with length of $\sim 10 \mu\text{m}$, diameters of $40 \sim 200 \text{ nm}$, and rod-like are favorable, growth conditions in the shadow area are utilized for the growth processes.

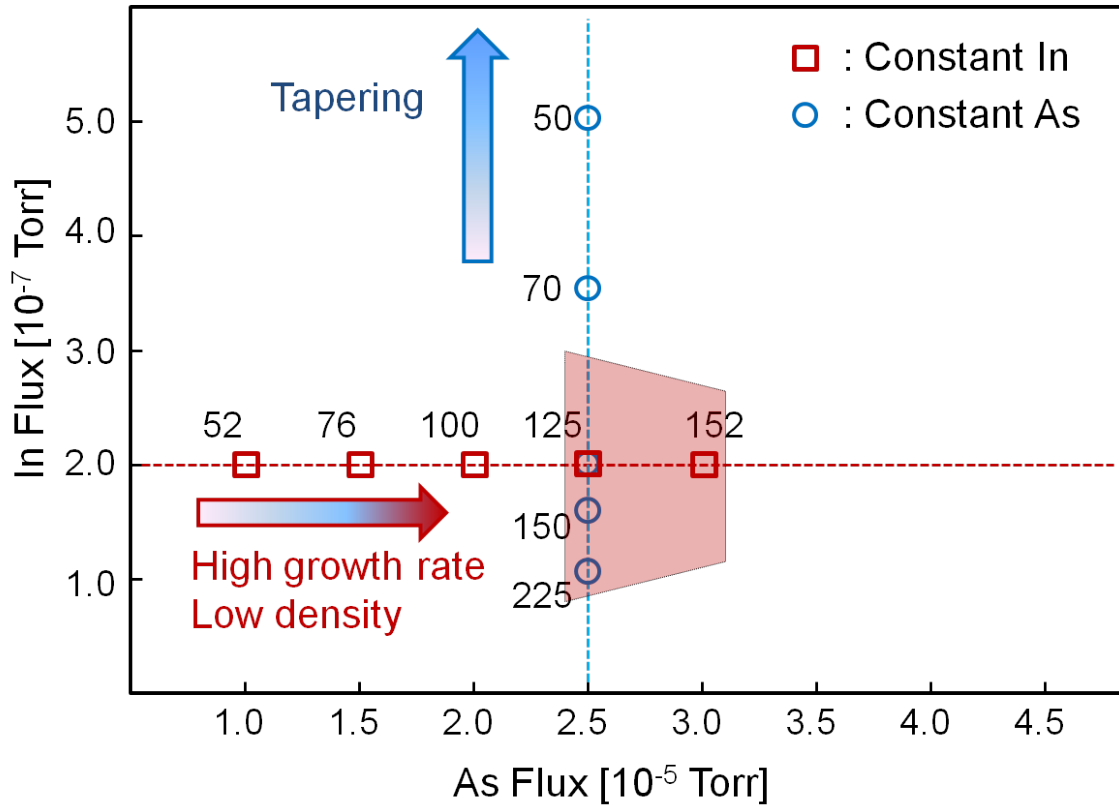


Figure 4.8: Conclusion of the In flux and As flux dependence. The growth points with their V/III ratios of the two sets are set along the dash lines. The tendency of tapering, high growth rate and low density growth are denoted by the arrow signs. Growth conditions in the shadow area are utilized for the nanowires with length of $\sim 10 \mu\text{m}$ and diameters of $40 \sim 200 \text{ nm}$.

4.3.4 Morphology of <110>-oriented Nanowire

The growth orientation of <110> is confirmed by SEM and TEM observations in order to confirm the morphology of the nanowires. Since the nanowires were grown on the GaAs (111)B substrate, the orientation of the nanowire can be confirmed by the angle between the nanowire and the substrate. As the schematic shown in Fig.4.9a, observation from $[-110]$ direction can obtain α as ~ 35 degree, which is the angle between $[111]$ direction and $[110]$ direction. Similarly, β , the angle between $[111]$ direction and $[101]$ direction, is can be observed as ~ 20 degree. Correspondingly,

the angles between the <110>-oriented InAs nanowire and the (111) plane are $\sim 55^\circ$ and $\sim 70^\circ$ which are confirmed by cross section SEM observation directly as well [9].

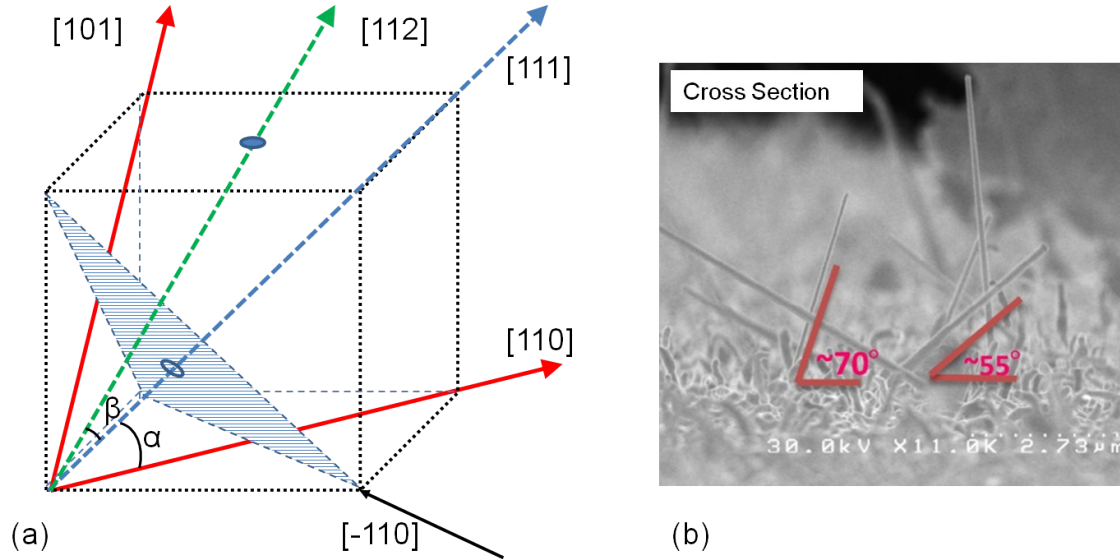


Figure 4.9: The schematic and SEM observation of the angle between [110] directions and [111] direction. (a) Observation from [-110] direction can obtain α as ~ 35 degree, β as ~ 20 degree, which are the angle between [111] direction and [110] directions. (b) The angles between the <110>-oriented InAs nanowire and the (111) plane are $\sim 55^\circ$ and $\sim 70^\circ$ which are confirmed by cross section SEM observation directly.

Meanwhile, the cross section of the nanowire is also confirmed by the SEM observations of the as grown nanowire and detached nanowire. A single as grown nanowire is shown in the SEM image of Fig.4.10(a), it is able to recognize two facets with one edge. And in the Fig.4.10(b), whose angle is 35° tilted to the (111)B GaAs substrate, a diamond cross section of an as grown nanowire can be identify clearly. The diamond cross section demonstrates these nanowires are <110>-oriented with four {111} side facets. This fact indicates that our <110>-oriented InAs nanowire growth is dominated by minimizing surface energy of the side facets, so that the facets are {111} which have the lowest surface energy in the zinc-blende structure. Detached nanowires of Fig.4.10(c) and Fig.4.11(d) show the facets and edge more

clearly.

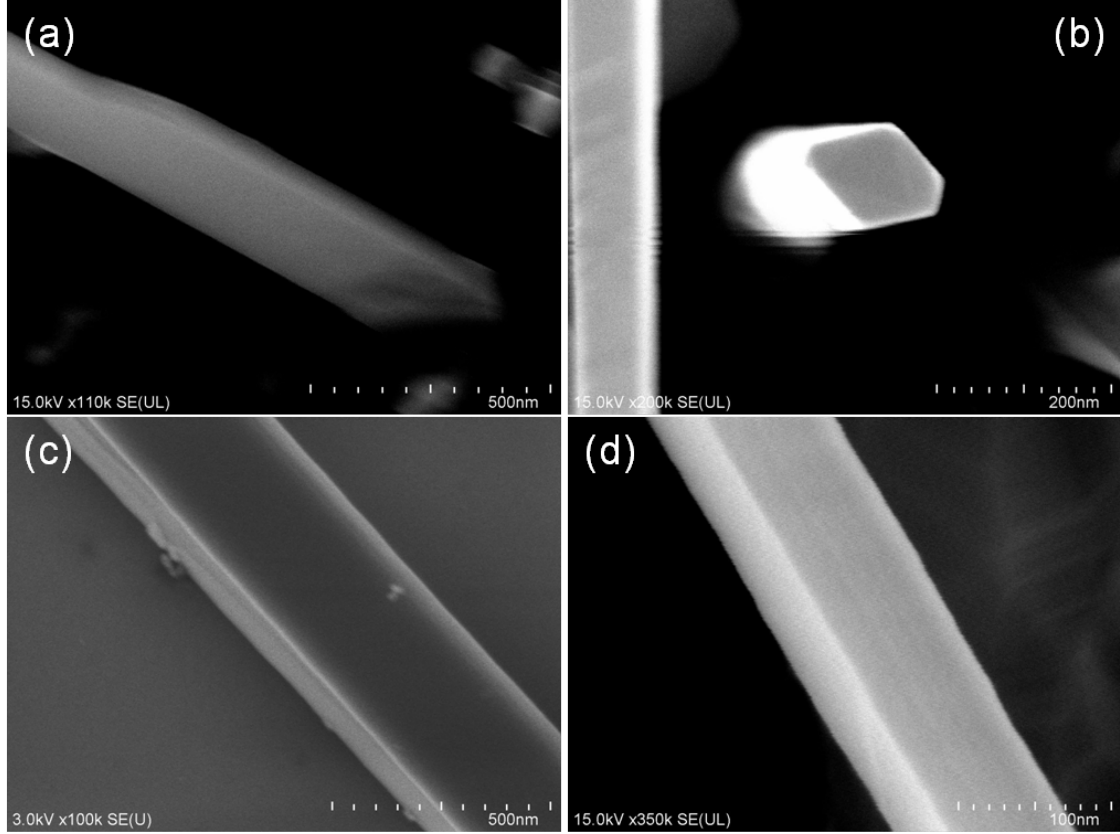


Figure 4.10: The SEM observations of the nanowire for cross section confirmation. (a). An as grown nanowire shows two side faces and one edges. (b). A diamond shape cross section is observed from the angle 35° tilted from the (111)B substrate which indicates the <110>-oriented nanowire owes four {111} facets. (c) and (d). SEM images of detached nanowires are showing the two side faces and on edge of the nanowire with diamond shape cross section.

Since the interface between alloyed droplet and nanowire is important to the growth as well, a detached nanowire has been observed by SEM (Fig.4.11). The angle of 60° indicates that is a {311} interface [8].

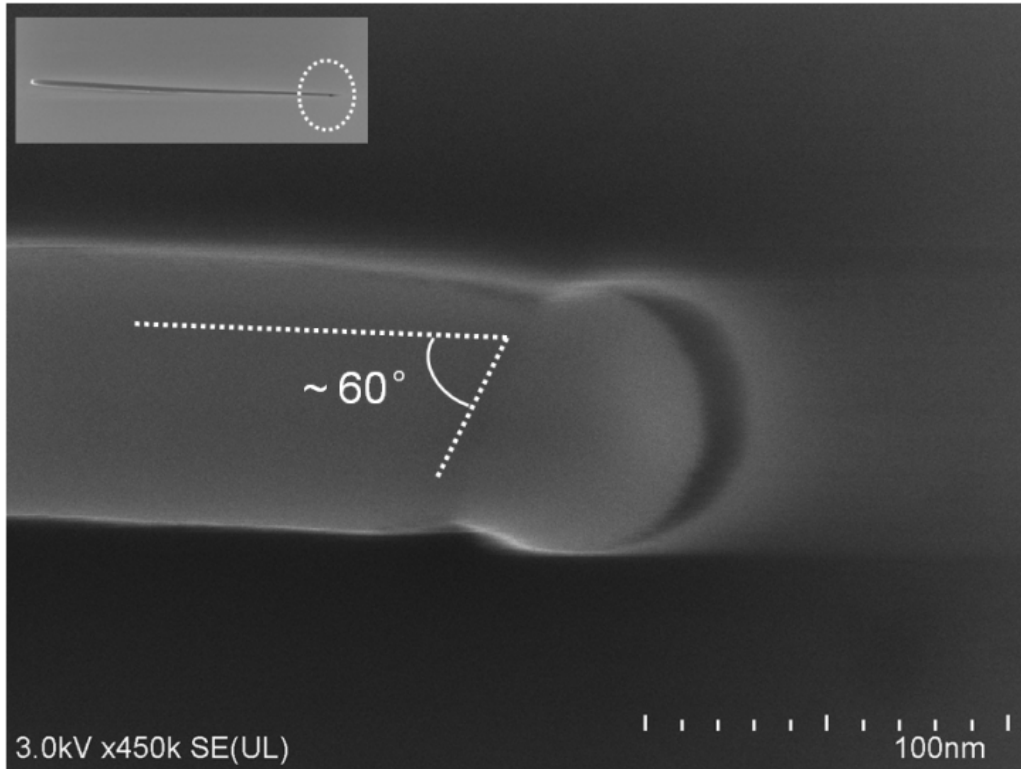


Figure 4.11: The SEM observations of a detach nanowire (inset) for interface between droplet and nanowire. The angle of 60° indicates the interface is $\{311\}$.

According to the Ref.[8], the grown nanowires are grown along the <110> direction with a stable ZB crystal structure without crystal imperfections such as WZ phase mixing and stacking faults. The results are also confirmed by the TEM observation as depicted in Fig.4.12. It can be found that the ZB type of grown nanowires exhibit a pure ZB crystalline structure free of stacking faults along with a <110> growth direction. This may be due to the effect of the Pd catalyst particle, which plays a vital role in the surface free energy during nucleation as well as growth. And this defect-free <110>-oriented InAs nanowire might provides more possibilities to the electronic devices particular spin device applications.

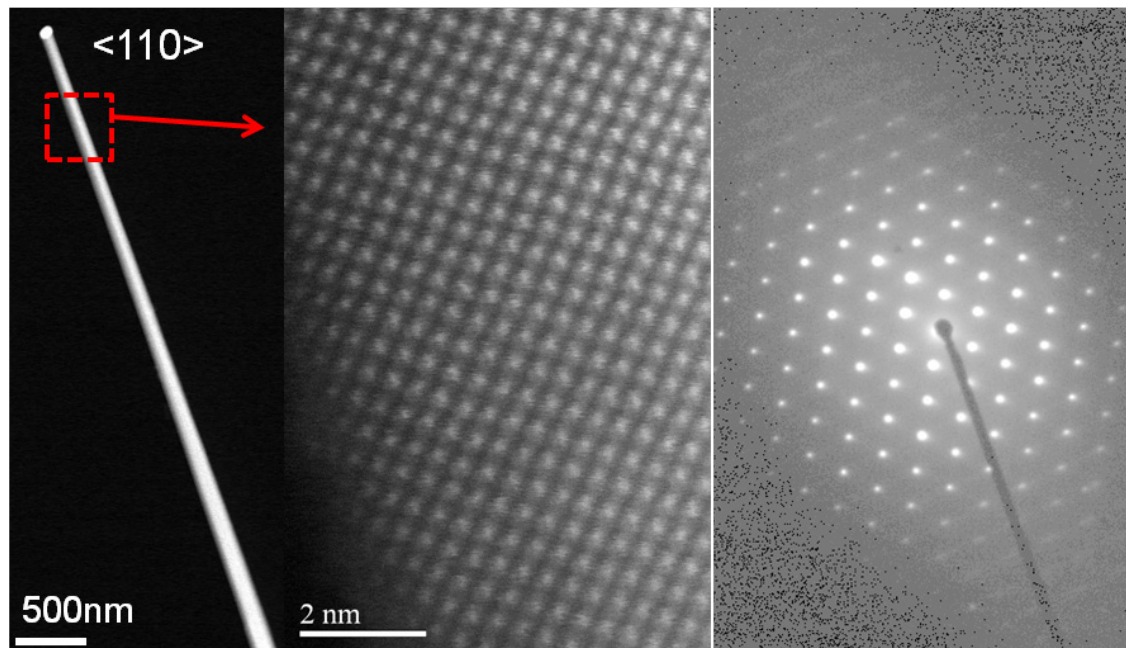


Figure 4.12: TEM images of $\langle 110 \rangle$ -oriented InAs nanowire. $\langle 110 \rangle$ -oriented and stable ZB crystalline structure can be observed clearly.

Bibliograph

- [1] J. B. Babu, K. Yoh. J. Cryst. Growth 322. 10 (2011).
- [2] M.T. Bjork, B.J. Ohlsson, T. Sass, A.I. Persson, C. Thelander, M.H.Magnusson, K. Deppert, L.R. Wallenberg, L. Samuelson, Appl. Phys. Lett. 80. 1058 (2002).
- [3] K. A. Dick, Deppert K, L. Samuelson, and W. Seifert, J. Cryst. Growth 297. 326–33 (2006).
- [4] H. Shtrikman, R. Popovitz-Biro, A. V. Kretinin, and P. Kacman, IEEE J. Sel. Top. Quant.17. 922–34 (2011).
- [5] C. Thelander, P. Caroff, S. Plissard, A. W. Dey, and K. A. Dick, Nano Lett. 12. 2424–9 (2011).
- [6] S. A. Dayeh, D. Susac, K. L. Kavanagh, E. T. Yu, and D. Wang, Adv. Funct. Mater. 19. 2102–8 (2009).
- [7] S. Heun, B. Radha, D. Ercolani, G. U. Kulkarni, F. Rossi, V. Grillo, G. Salviati, F. Beltram, and L. Sorba, Cryst. Growth Des. 10. 4197–9 (2010).
- [8] H. Xu, Y. Wang, Y. Guo, Z. Liao, Q. Gao, H. H. Tan, C. Jagadish, and J. Zou, Nano Lett. 12. 5744–9 (2012).
- [9] R. Perumal, Z. Cui, P. Gille, J-C. Harmand, and K, Yoh. Semicond. Sci. Technol. 29. 115005 (2014).
- [10] H. Okamoto, J. Phase Equilib. 24. 481 (2003)
- [11] J. R. Knight, D. W. J. Rhys, Less-Common Met. 1. 292 (1959).

Chapter 5

Transport Properties of $\langle 110 \rangle$ -oriented InAs Nanowire

InAs nanowire with $\langle 110 \rangle$ orientation is proposed for use as the electron spin transport channel for application to spintronics devices, particularly the Datta-Das spin transistor. Stable zinc-blende (ZB) crystal nanowires were grown by using molecular beam epitaxy system. Subsequently, global back-gate nanowire field effect transistors were fabricated, and the superiority of electrical transport properties within our $\langle 110 \rangle$ nanowires was demonstrated by comparing the effective mobility with our control $\langle 111 \rangle$ nanowire sample. Additionally, single nanowire Hall-bar devices, which allowed us to obtain the transport properties accurately, were fabricated, and Hall effect measurements were successfully taken at different temperatures.

5.1 Introduction

Among numerous InAs nanowire growths with VLS techniques, the $\langle 111 \rangle$ -oriented nanowires grown on the (111) substrate are the common type, which have stimulated the experimental investigation of physical phenomena and quantum

devices [1-3]. In particular, InAs nanowire was reported as a 1D nanostructure with outstanding promise for device applications because of its high electron mobility and strong quantum confinement effects [4-6]. In our proposal for spintronics devices particularly the Datta-Das Spin-FET [7, 8], however, the strong spin orbit interactions are paid more attentions [9]. Therefore, how to apply the strong spin orbit interactions of InAs nanowire skillfully become the primary target of this thesis. At room temperature, electron spin relaxation due to the DP mechanism, which involves Dresselhaus and Rashba spin orbit interactions, is the most dominant spin relaxation factor. While it also has been demonstrated that when the Rashba and Dresselhaus SOI linear-in-k terms have equal strength, the relaxation of spin orientation in one of the $\langle 110 \rangle$ axes is totally suppressed [10]. Hence, we expected that InAs nanowire with $\langle 110 \rangle$ orientation might be applied to spintronics devices as an efficient 1D spin transport channel, therefore, investigating growth and transport properties is desirable for spintronics applications.

In previous chapter, we demonstrated InAs nanowires with $\langle 110 \rangle$ orientation by employing VLS growth with a palladium (Pd) catalyst [11]. We here characterized the transport properties by using nanowire-FETs with back-gate and Hall effect measurements.

5.2 Comparison of the Nanowires with $\langle 111 \rangle$ and $\langle 110 \rangle$ orientations

5.2.1 Device Fabrications

InAs nanowires with $\langle 110 \rangle$ orientation were grown by using the VLS process in a Riber MBE system with a Pd catalyst on a GaAs (111)B substrate. Basically, the growth conditions described in Sec.4.3.3 is used for the following devices. Prior to growth, the native oxide layer of the GaAs substrates was removed by using an

ammonia solution. Subsequently, a 15-Å-thick Pd catalyst layer was deposited with an electron-beam evaporator under a vacuum of $\sim 10^{-7}$ Torr. Before the actual nanowire growth, the Pd deposited substrate was annealed in the MBE growth chamber at 600 °C in an As atmosphere for 10 minutes to remove surface contaminants, mostly the surface oxidations formed during the growth sample transfers, as well as to convert and agglomerate the Pd thin film into Pd nanoparticles. Subsequently, the substrate temperature was reduced to a growth temperature of 425 °C and kept for a growth time of 1 hour, and the corresponding length of the nanowires was around 10 μm for this study, which made device fabrication convenient. And these nanowires are along the <110> direction and have a stable ZB crystal structure without crystal imperfections such as WZ stack defects.

Subsequently, the transport properties of this nanowire were characterized. First, we expected to compare the <110> InAs nanowire with the <111>-oriented InAs nanowire by investigating their field-effect mobility at room temperature. To ensure comparability, identical conditions discussed in Sec.3.3 [12], including fabrication processes, an nanowire diameter of ~ 40 nm, and evaluation method, were used to fabricate and investigate a back-gate FET structure based on a single <110> nanowire. The schematic image and SEM image are shown in the Fig. 5.1(a) and (b).

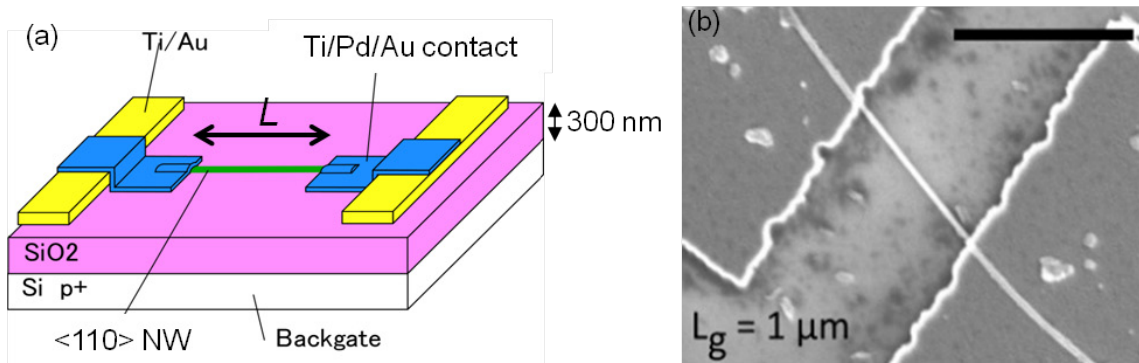


Figure 5.1: (a) The schematic image of the back gate FET device of single <110>-oriented nanowire. (b) SEM image of the back gate device. The scale bar is 1 μm .

5.2.2 Results and Discussion

Room temperature FET characterizations of the <110> InAs nanowire with a diameter of 40 nm and back-gate length (L_g) of 1 μm were carried out. The typical I_{ds} - V_{gs} and I_{ds} - V_{ds} curves depicted in Figs. 5.1(a) and 5.1(b) showed stable FET characteristics. At a drain-source voltage (V_{ds}) of 30 mV, a peak transconductance (g_m) of $\sim 0.24 \mu\text{S}$ was obtained from I_{ds} - V_{gs} curve (Fig. 5.2a). According to the FET charge control model, field-effect mobility μ_{FE} can be expressed as:

$$\mu_{FE} = \frac{g_m L_g^2}{C V_{DS}}, \quad (5.1)$$

where C is the gate capacitance. For back-gate nanowire FETs and nanotube FETs, the general form of capacitance is:

$$C = 2\pi\epsilon L_g / \ln \left[\left(t_{ox} + a + \sqrt{(t_{ox} + a)^2 - a^2} \right) / a \right], \quad (5.2)$$

where ϵ is the insulator dielectric constant, t_{ox} is the gate insulator thickness, and a is the nanowire radius. Since a highly doped Si substrate with 300 nm of SiO_2 was used as the back-gate of this FET, the gate capacitance was calculated as 62.1×10^{-18} F. A nanowire channel resistance of $\sim 26.1 \text{ k}\Omega/\mu\text{m}$ was calculated using the sheet resistance deduced from four terminal devices, and the mobility was calculated as $\sim 6415.6 \text{ cm}^2/\text{Vs}$ at room temperature.

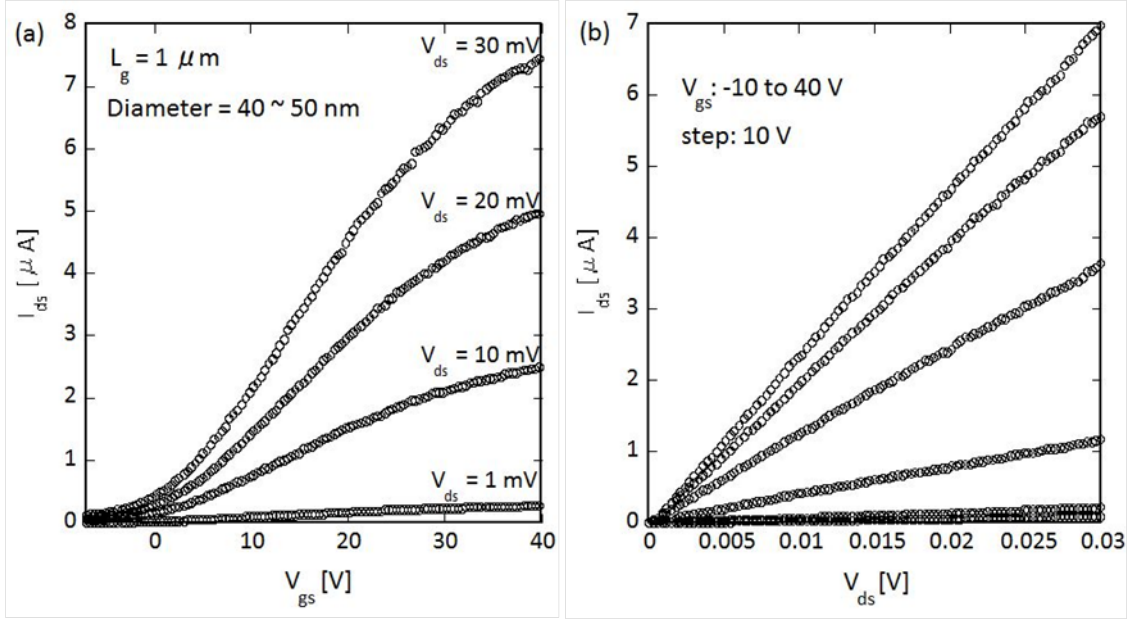


Figure 5.2: (a) and (b) Room temperature FET characteristics of a <110> InAs nanowire with a diameter of 40 nm and back-gate length (L_g) of 1 μm .

We will now discuss the transport behavior obtained with the two structures above. Compare with our <111>-oriented InAs nanowires, whose mobility were around $\sim 1000 \text{ cm}^2/\text{Vs}$, [12] our <110> InAs nanowire showed an outstanding transport property. We attribute this transport superiority to the stable ZB crystal structure without WZ stack defects. As the band gap of WZ is larger than that of ZB in InAs [13, 14], nanowires with a mixed crystal structure could have discontinuities of approximately 30 ~ 90 meV in the conduction band, which is shown in the Fig.5.3 (a) and (c). In our <110> InAs nanowires, as shown in the Fig.5.3 (b), the carrier mobility increased correspondingly without these conduction band discontinuities, which can present like electron transport barriers. The ZB and WZ mixed crystalline structure is the common defect in the <111>-oriented InAs nanowire. This can be explained by the following models of the nanowire growth. In the case of VLS Au-assisted nanowire growth on the (111) substrate, the common grown nanowire owns a <111> orientation and a {111} interface with the Au-alloy, since the {111} planes having the lowest growth energy. During the growth, however, the

lattice defects are generated at the nanowire catalyst interface. And the growth free energetic difference for the ZB and WZ stacking of their $\{111\}$ or $\{0001\}$ planes is small. Consequently, the WZ/ZB stack defects easily occur in the growth processes of $\langle 111 \rangle$ -oriented InAs nanowire, since the interface between the catalyst and the nanowire is a $\{111\}$ plane. On the other hands, in the case of our $\langle 110 \rangle$ -oriented InAs nanowire, the growth direction is $\langle 110 \rangle$ and the interface between the Pd catalyst and nanowire is a $\{311\}$ plane, which was discussed in Sec.4.3.

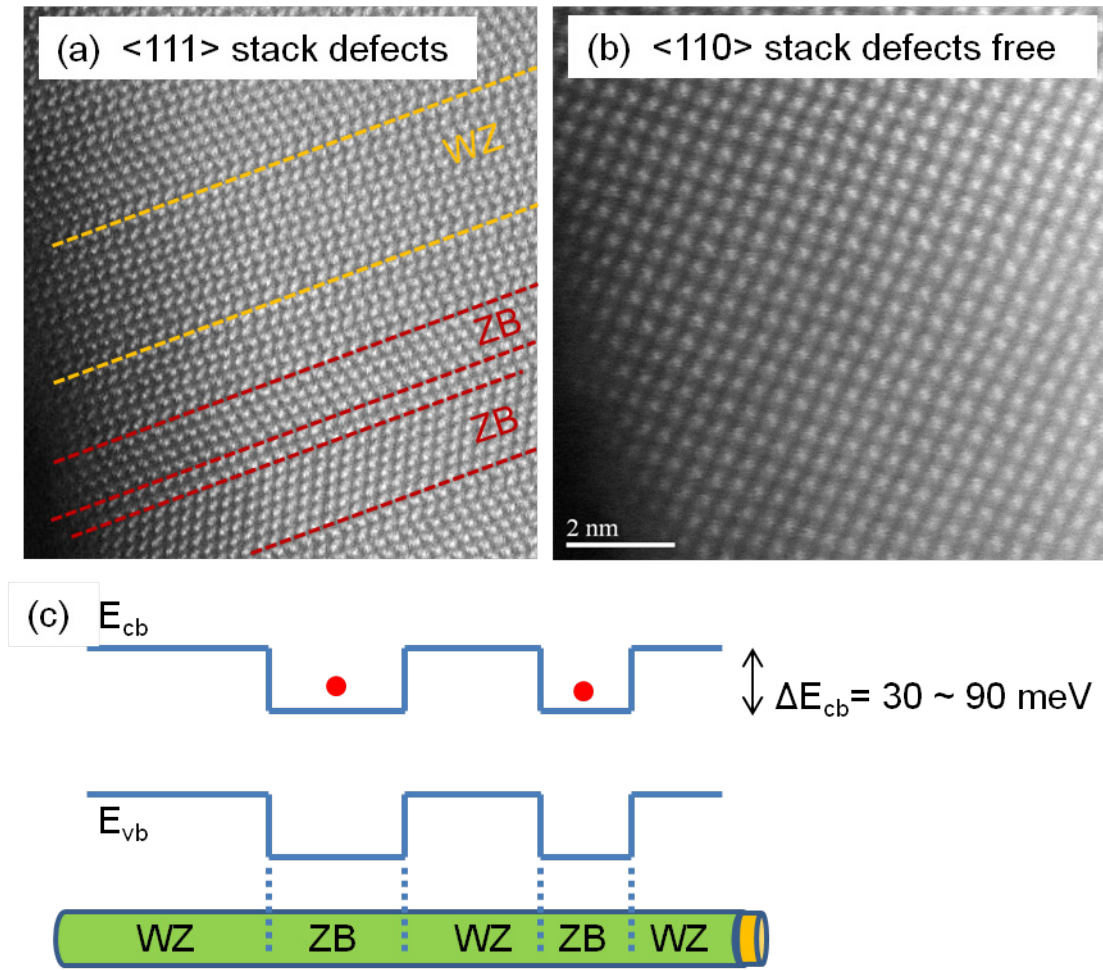


Figure 5.3: (a) TEM image of $\langle 111 \rangle$ -oriented InAs nanowire grown by VLS techniques using MBE. The WZ crystalline layers are depicted by orange dash lines, and the ZB crystalline layers are depicted by red dash lines. This mixed crystalline structures are common defects in the $\langle 111 \rangle$ -oriented InAs nanowires. (b) TEM image of $\langle 110 \rangle$ -oriented InAs nanowire grown by VLS techniques using MBE. A stable ZB structure without WZ defects can be

recognized. WZ defects are absent in our $\langle 110 \rangle$ -oriented InAs nanowires. (c) The schematic of nanowire with mixed crystalline defects and corresponding band structure. Since band of WZ is larger than that of ZB in InAs, there are 30 ~ 90 meV band discontinuities due to this kinds of defects.

And the two cases of nanowires growth can be depicted as Fig. 5.4. The energetic difference of ZB and WZ at non- $\{111\}$ plane is larger, therefore, the lattice defects of mixed WZ/ZB are barely observed in this case. This pure ZB structure of $\langle 110 \rangle$ -oriented nanowire grown by Pd assistance should provide an outstanding transport property. Especially, the structure without band discontinuous is important for the spintronic devices. Since the Rashba spin orbit interaction could be influenced at the edges between ZB and WZ stacks, manipulation of spin would be difficult at this region. Therefore, the nanowire with $\langle 110 \rangle$ orientation is not only provide a chance to spin manipulations but also a sufficient spin transport channel. Certainly, the $\langle 110 \rangle$ -oriented InAs nanowires are more suitable for the application than the $\langle 111 \rangle$ -oriented InAs nanowires.

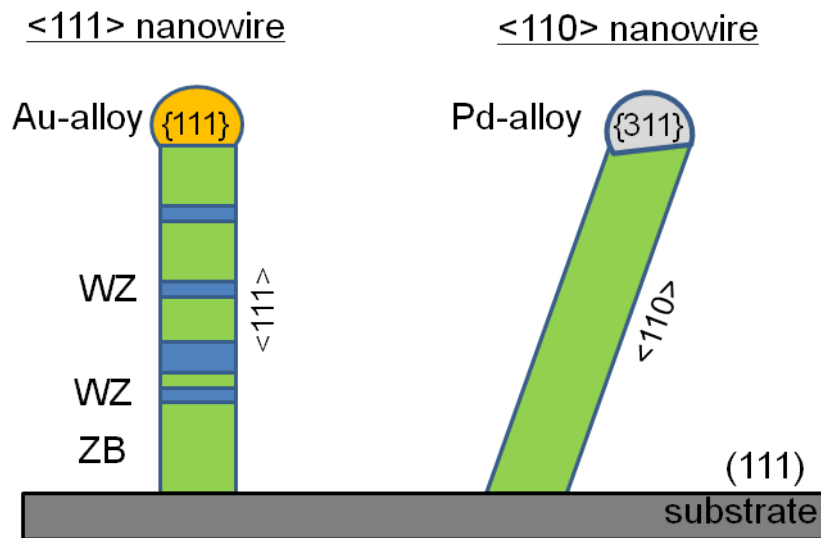


Figure 5.4: The schematic of the nanowire with $\langle 111 \rangle$ and $\langle 110 \rangle$ orientation grown on the

(111) substrate. In the case of Au-assistant <111>-oriented nanowire, the lattice defects easily occur at the {111} interface between Au-alloy and InAs nanowire, therefore, it is difficult to attain pure <111>-oriented InAs nanowires. In the case of Pd assistant <110> nanowire, the growth interface between nanowire and Pd-alloyed is a {311} plane, where WZ/ZB lattice defects barely occur.

5.3 Hall measurements of a Single Nanowire

5.3.1 Fabrications of a Single Nanowire Hall-bar Device

Since the free carrier concentration and mobility of nanowires are crucial parameters for fabricating spintronics and other quantum devices on the nanoscale, evaluations with back-gate FETs are insufficient as they overestimate the free carrier change caused considerably by many inherent uncertainties [15, 16]. Especially, in the case of back-gate FET, there might be many interface/surface states between the nanowire and the back-gate oxidation layer, since the back-gate is just formed by the dispersion of nanowires. Therefore, fabricating a Hall-bar structure based on a single <110> InAs nanowire is investigated and carried out with the following procedure, and this structure allow us to obtain a relatively accurate carrier concentration and mobility results with Hall effect measurements. The grown nanowires were detached from the substrate in DI water by using a knife blade and dispersed onto a heavily doped p-type Si substrate with a 300-nm-thick SiO₂ layer. Different from the fabrications of other nanowire devices, the position of nanowires must be defined more precisely. Therefore, for the fabrication of the single nanowire Hall bar device, address markers with more density are fabricated on the address substrates, and the precise positions of nanowires are determined by SEM. And the SEM image of the observed InAs nanowire is shown in the Fig.5.5, including four address marks.

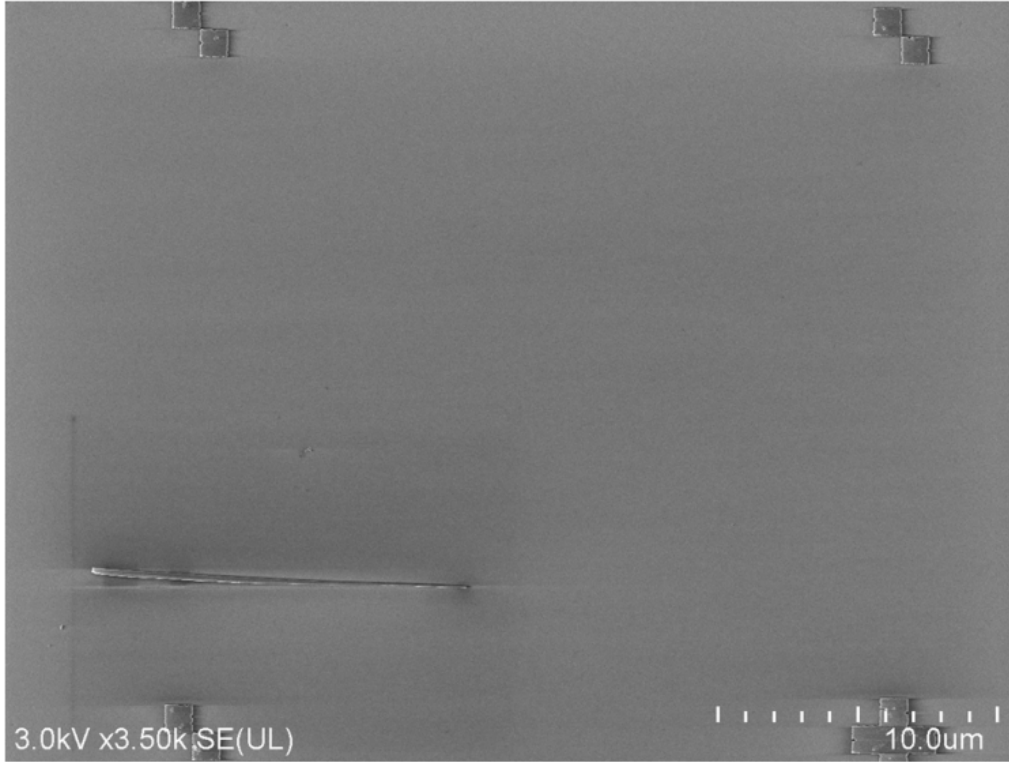


Figure 5.5: SEM image of a dispersed nanowire on the address substrate. The four address marks can be observed.

Because the diameters of the nanowires for Hall-bar fabrication nanowire which were around 150 ~ 250 nm, were relatively large and much thicker than the metal film thickness of the electrodes in our common process, a planarization process with a hydrogen silsesquioxane (HSQ) lift-layer was performed prior to electrode formation. This process is advantageous in electrode formation because it eliminates the need for thick metal layers and improves the spatial resolution for the Hall terminals. Thus, an HSQ solution diluted with methyl isobutyl ketone (MIBK) was coated onto the nanowire dispersed substrates at 3000 rpm to form a layer with thickness of around 250 nm to cover the horizontally lying nanowires lightly. After 170 °C hard bake, an HSQ layer is transformed into a well insulating oxidic SiO₂-like structure. This process is schematically depicted as Fig. 5.6(a) and (b). Subsequently, the nanowires are uncovered again by reactive dry etching with

CF₄ and O₂, so that a height of only 50 ~ 100 nm from the top of the nanowire is exposed from the HSQ layer, as depicted in Figs. 5.6(b) and 5.6(c). The electrodes of the Hall-bar devices are defined on a selected nanowire in a ZEP520A resist layer with electron beam lithography. Prior to depositing the electrodes, the native oxide layer of the nanowires is removed by dry etching with Ar gas for 4.5 min at 30 mW, the etching rate is low enough to be negligible for other structures such as the HSQ lift-layer and ZEP520A resist layer. This yielded devices with a contact resistance typically in the range of 1 ~ 50 k Ω , which is small compared with the channel resistance and independent of the temperature change. For the electrodes, a combination of Ti (15 nm)/Pd (15 nm)/Au (10 nm) is used as deposited without annealing, which included a Pd barrier layer to prevent In diffusion into the Au [17]. As a result, contact resistance degeneration during electrical measurements, which is a common phenomenon in nanowire devices, is barely observed. Schematic and SEM images of the Hall-bar device after the lift-off process are shown in Figs. 5.6(d). In order to increase the yield of the Hall terminals, a useful technique is that design several sets (one set is 4 Hall terminals) along a nanowire with a shift of 20 nm in the direction perpendicular to the nanowire. For this reason, a relative long nanowire with length larger than 10 μm is preferred. With these processes, the Hall terminals can be formed properly on the two sides of the InAs nanowire, shown in Fig. 5.6(e) and (f). With this method, three devices with different diameters of nanowires were fabricated. The Hall measurements are carried out with the terminals depicted.

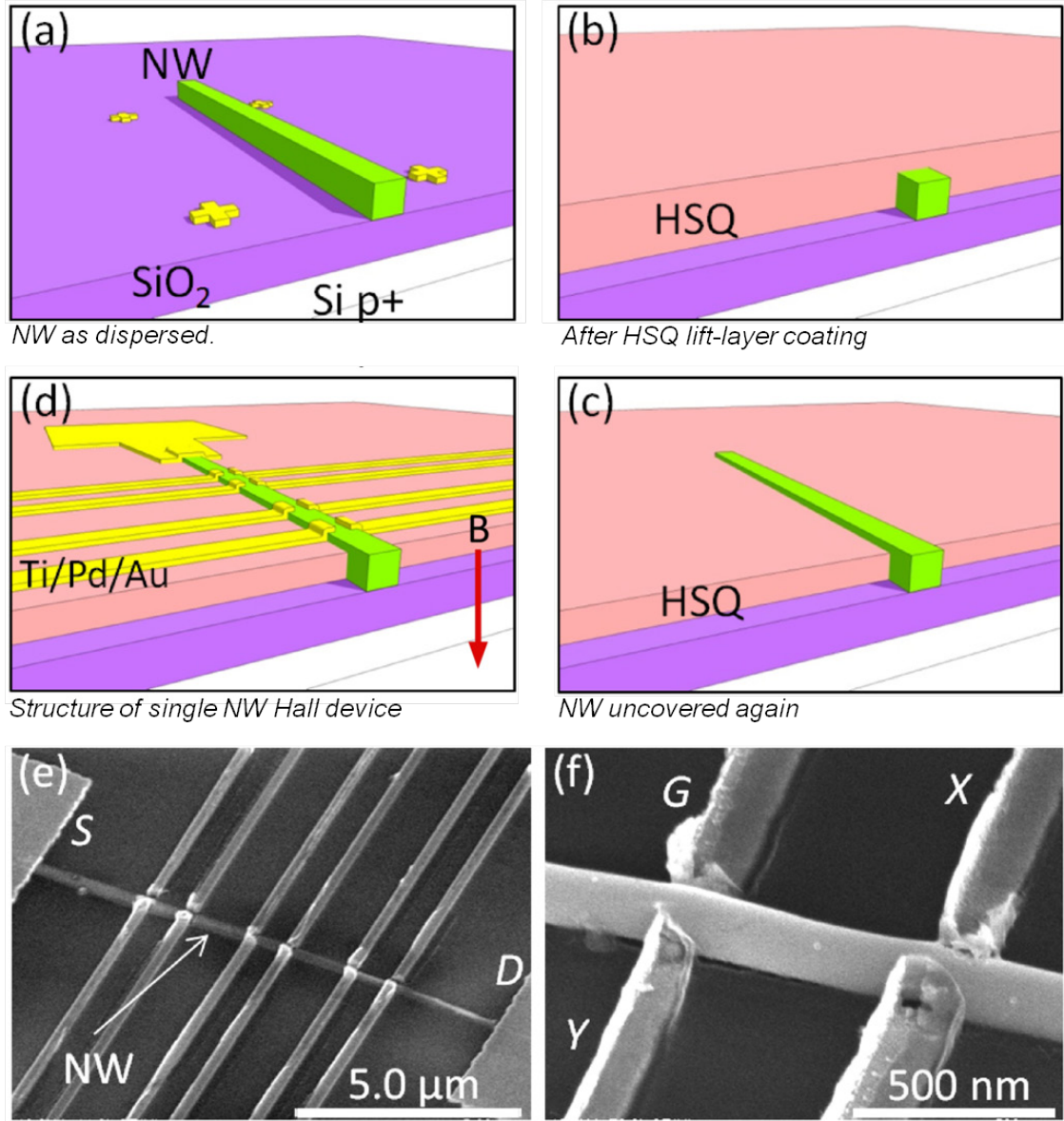


Figure 5.6: Schematic and SEM images of the single nanowire Hall bar fabrication. (a). A nanowire is dispersed on the address substrate which is a highly doped Si substrate with a SiO_2 layer with 300 nm thickness. (b). Nanowire is covered by the HSQ lift-layer with a thickness around 300 nm. (c). Nanowire is uncovered again by a dry etching process, a height of only 50 ~ 100 nm from the top of the nanowire is exposed from the HSQ layer. (d). Hall bar electrodes are formed by a typical EB lithography process, several sets of the Ti/Pd/Au Hall contacts are form on the side wall of nanowire. (e) and (f) SEM images of a single nanowire Hall bar devices.

5.3.2 Hall Measurements of a Single Nanowire

The Hall effect is measured with a standard setup in a He-4 cryostat system, from 140 to 1.5 K, with the magnetic field B oriented perpendicular to the substrate. As shown in Figs. 5.6(e) and 5.6(f), a constant current I_{ds} of 1 μA was driven through the drain (D) and source (S) electrodes, and the voltages between terminals XG and YG were measured simultaneously. Figure 5.7 shows the Hall voltage $V_H = V_{YG}$ normalized to the drain current I_{ds} as a function of the magnetic field B measured at different temperatures. Each curve was shifted by 5 Ω for clarity.

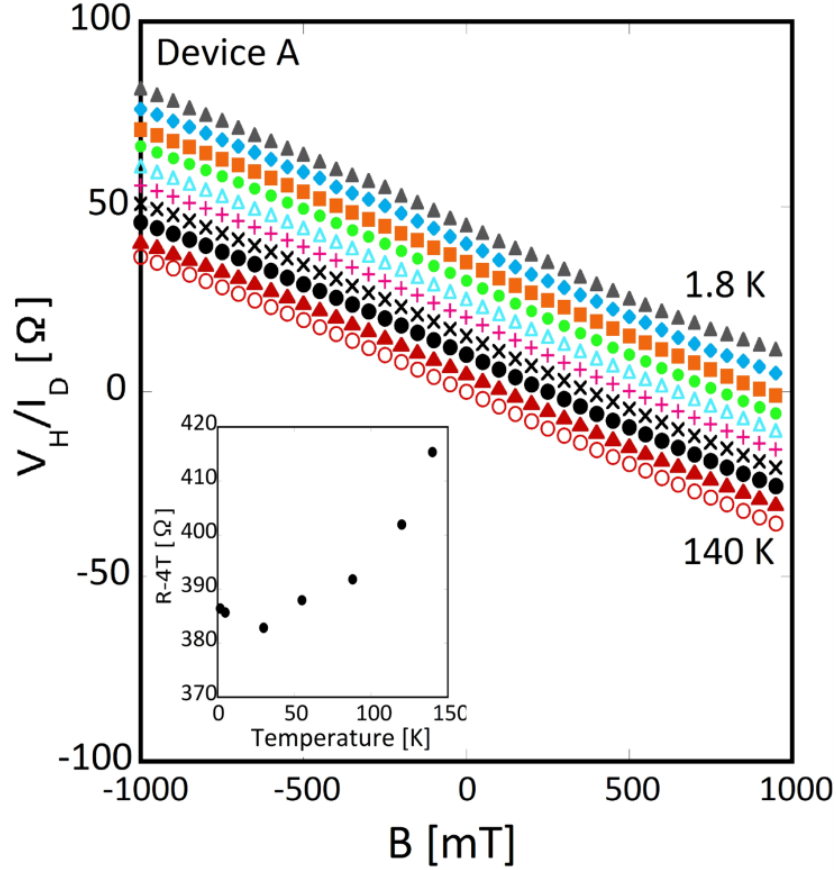


Figure 5.7: Hall voltage $V_H = V_{YG}$ normalized to the drain current I_{ds} as a function of the magnetic field B measured at different temperatures. Inset: $R_{4T} = V_{XG}/I_{ds}$, the four-terminal resistance temperature dependency of device A.

The Hall voltage changed linearly with a negative slope as along with magnetic field B , which indicates that the nanowire is an n-type one. In 3D, the Hall voltage V_H can be expressed as

$$V_H = -\frac{I_{ds} w_H}{qnS} B, \quad (5.3)$$

where w_H is the distance between Hall voltage terminals YG , q is the elementary charge, n is the electron concentration and S is the cross sectional area. We used the same expression for nanowires and calculated the electron concentration and Hall mobility by combining four-terminal resistivity measurements. The inset of Fig. 5.7 shows $R_{4T} = V_{XG}/I_{ds}$, the four-terminal resistance temperature dependency of device A, and that the sheet resistivity was calculated to be $4.18 \times 10^{-3} \Omega\text{cm}$. Figure 5.8 shows the temperature dependence of the carrier density and mobility of the three devices with different values of nanowire diameters. The carrier concentrations were almost independent of temperature below 140 K for all three devices; the results between 6.5×10^{16} and $1.2 \times 10^{17} \text{ cm}^{-3}$ agreed with the typical values obtained for intrinsic InAs [16]. The Hall mobility deduced from the carrier concentration and four-terminal resistivity showed a gradual enhancement from 140 to 30 K and a saturation below 30 K; similarly, this behavior was observed as well with the InAs nanowire FET devices [18].

The weak temperature dependence of the carrier density determined by Hall-bar structure could be explained by the electron accumulation that occurred at the surface of the nanowires, which was due to the pinning of the Fermi level above the conduction band [19, 20] and to the formation of 2D electron gas. At low temperature, these electrons at the surface dominated the carrier concentration rather than the electrons in the bulk region. One can easily deduce the carrier concentration n_{2D} of this 2D electron gas from Fig. 5.8. The extracted values between 3.6×10^{11} and $1.5 \times 10^{12} \text{ cm}^{-2}$ agreed well with the 2D systems within the surface accumulation layer in InAs [20, 21]. It has been demonstrated that the 2D electron

gas can provide the sufficiently large conductance even at low nanowire radius; furthermore, electron spin propagating through this cylindrical tube-like channel can be strongly modulated by Rashba SOI [22].

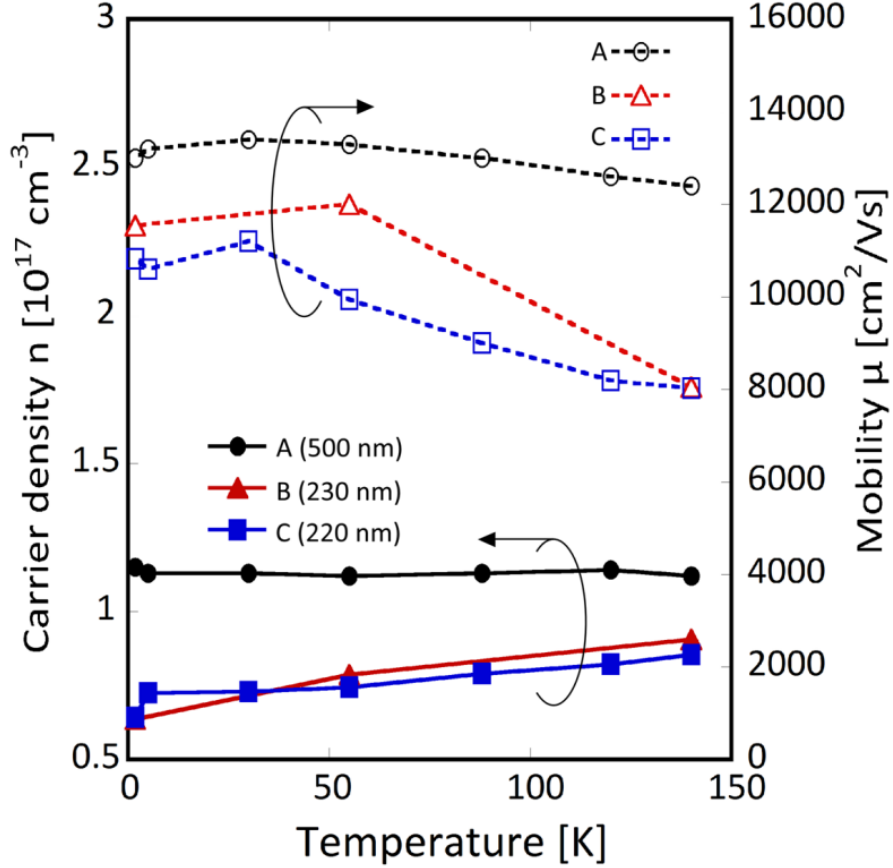


Figure 5.8: The temperature dependent carrier density and transport properties of three devices with different diameters of nanowire. The carrier concentrations (solid dots) are almost independent of temperature below 140 K for all three devices, and the results were between 6.5×10^{16} and $1.2 \times 10^{17} \text{ cm}^{-3}$. The Hall mobility (open symbols) deduced from the carrier concentration and four-terminal resistivity shows a gradual enhancement from 140 to 30 K and a saturation below 30 K.

The gradual increase of Hall mobility from 140 to 30 K is mainly attributable to the reduction of phonon scattering. Below 30 K, the surface scattering, including surface roughness scattering and surface ionized impurity scattering, dominated

over other scattering events. Since our nanowires were not intentionally doped, ionized scattering caused by impurity in the bulk region should not be a factor. As discussed above, the electron transport near the surface dominated the electrical characteristics. The observed weak temperature dependence, therefore, is mainly due to the surface roughness scattering which in general leads to weak temperature dependence [23]. It is also likely that fluctuation of the surface impurity or surface states also gave rise to fluctuation of the surface potential and to electron scattering similar to the surface roughness scattering [24]. Since our <110>-oriented InAs nanowires have a stable ZB crystal structure, surface state scattering caused by ZB/WZ crystal phase mixing [25, 26] is eliminated. It is believed that proper surface passivation scheme of the nanowire or core/shell structure would further reduce the scattering effects mentioned and make it highly possible to increase the transport properties of our nanowire.

5.4 Spin Injection of a Single InAs Nanowire

In order to realize the electron spin transport in an InAs nanowire, the direct measurement is the spin injection which is a typical application of the giant magneto-resistance. For the electrical spin injections and detections, the nonlocal measurement of a spin imbalance [27, 28] is generally regarded as the best configuration to exclude misleading effects that leave the same signature. Recently, in the semiconductor nanowire systems, several materials such as Si [29, 30], Ge [31], GaN [32] and InN [33] are reported, spin have been successfully injected and detected by nonlocal methods. Importantly, most of these nanowires owe lower spin orbit interaction comparing to InAs. To our knowledge, there are still no spin injection reports on the InAs nanowire devices. Even though only some primary results are attained in this thesis, in this section we will discuss the observations of the spin injection in our InAs nanowire devices. We have measured the nonlocal

spin signal on both InAs with <111> orientation and <110> orientations for each more than 30 InAs nanowire samples with the structure shown in the Fig.5.9. However, spin-valve like signals have never been observed in <111>-oriented nanowires, and only several ambiguous magneto-resistance signals in <110>-oriented nanowire, depicted in Fig. 5.10(a). Obviously, besides the peaks of spin-valve signal, there is a redundant peak at magnetic field $B = -0.05$ kGauss. This appearance of excrescent peaks might due to the distortions of the ferromagnetic electrodes at the nanowire intersection which would impact the magnetic switching field. Since the successful observation of spin injection is depends on the efficient devices with proper electrical contacts, the fabrications of the effective spin injection contact is another key reason besides the strong spin orbit interactions in InAs nanowires. Meanwhile, local spin-valve measurements also have been carried out with two ferromagnetic terminals in both <111>- and <110>-oriented InAs nanowires. As shown in the Fig. 5.10(b), compared with the nonlocal signals, the local spin-valve like signal shows relative stable low-resistance and high-resistance states for the parallel and anti-parallel orientations of the magnetization of the FM electrodes. This device is fabricated with a similar process of Hall bar device except a shorter Ar⁺ dry pre-etching time, leading a relative high contact resistance of ~ 20 k Ω . If we assume the observed signal originate from the spin-valve but from spurious effects in the InAs nanowire itself or at the contacts, the equation below [34] lead to the following expression of ΔR

$$MR = \frac{\Delta R}{R_p} = \frac{\gamma^2}{1 - \gamma^2} \frac{2}{2 \cosh\left(\frac{L}{l_{sf}}\right) + \left(\frac{R_b}{R_{ch}} + \frac{R_{ch}}{R_b}\right) \sinh\left(\frac{L}{l_{sf}}\right)} \quad , \quad (5.4)$$

where R_p is the resistance of the device at parallel state, γ is the spin polarization of the contact around 32 % [35], L is the channel distance, R_b is the contact resistance, and R_{ch} is the channel resistance. Correspondingly, the spin diffusion length L_{sf} can be calculated around 300 nm, which is agree with the results deduced

from the WL-WAL measurements. Unfortunately, these signals have not been observed in another devices fabricated with same processes. Further efforts are necessary to complete the spin-valve measurements.

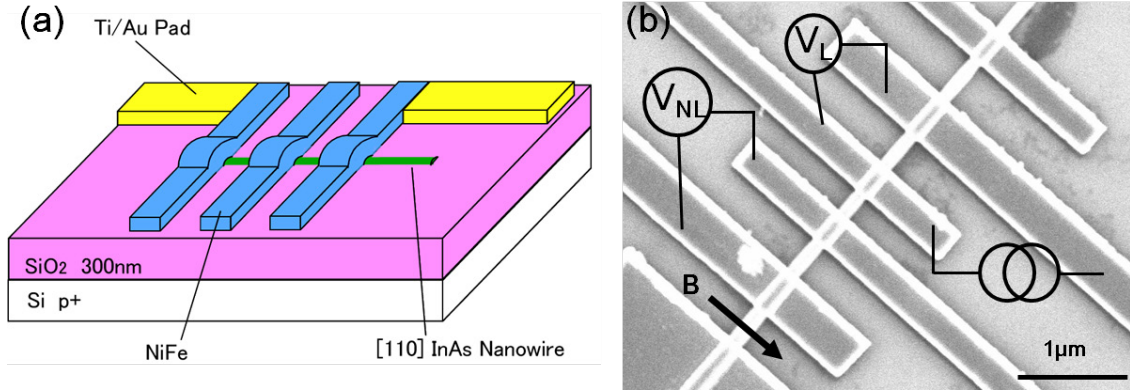


Figure 5.9: Schematic and SEM image of spin injection and detection device. (a) On the SiO_2/Si substrate, a single $\langle 110 \rangle$ -oriented InAs nanowire is covered by several ferromagnetic electrodes (NiFe). (b) SEM image of the device, the nonlocal spin-valve and local spin-valve are observed with the terminals V_{NL} and V_L respectively.

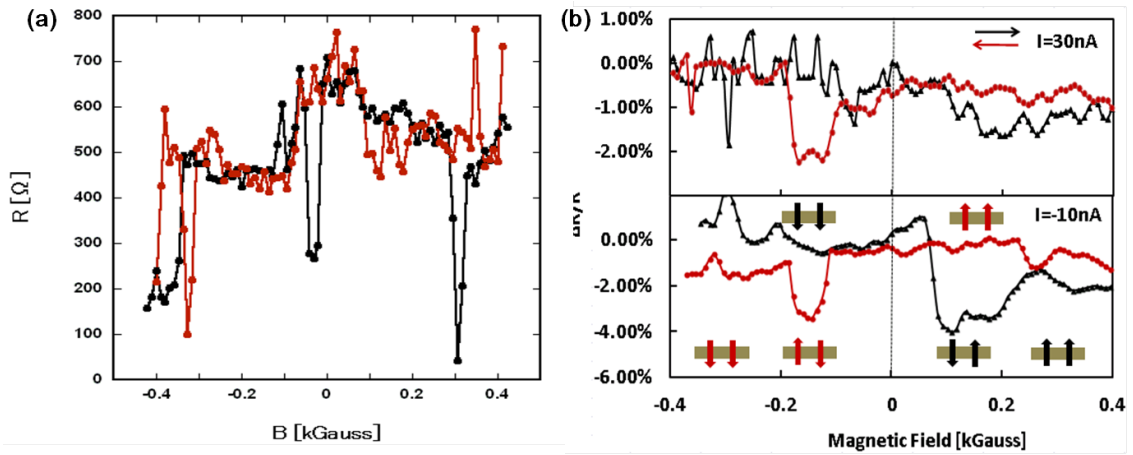


Figure 5.10: (a) A typical nonlocal spin-valve magneto-resistance. (b) Results of local spin injection measurements at 20 K.

Bibliography

- [1] Das, Y. Ronen, Y. Most, Y. Oreg, M. Heiblum, and H. Shtrikman, *Nature Physics*. 8, 887-895 (2012).
- [2] S. Heedt, C. Morgan, K. Weis, D. E. Bürgler, R. Calarco, H. Hardtdegen, D. Grutzmacher, and Th. Schäpers, *Nano. Lett.* 12, 4437 - 4443 (2012).
- [3] J. Tarun, S. Huang, Y. Fukuma, H. Idzuchi, Y. Otani, N. Fukata, K. Ishibashi, and S. Oda, *Appl. Phys. Express* 5, 045001 (2012).
- [4] S. Chuang, Q. Gao, R. Kapadia, AC. Ford, J. Guo, and A. Javey, *Nano Lett.* 13, 555–558 (2013).
- [5] S. A. Dayeh and D. Wang, *Small*. 2, 326 - 332 (2007).
- [6] T. Bryllert, L-E. Wernersson, T. Lowgre, and L. Samuelson, *Nanotechnology*. 17, 227 - 230 (2006).
- [7] H. C. Koo, J. H. Kwon, J. Eom, and J. Chang, *Science*. 325, 1515 (2009).
- [8] T. Ishikura, L-K. Liefeth, Z. Cui, K. Konishi, K. Yoh, and T. Uemura, *Appl. Phys. Express* 7, 073001 (2014).
- [9] T. Matsuda and K. Yoh, *Physica E* 42, 979 - 983 (2010).
- [10] M. Ohno and K. Yoh, *Phys. Rev. B* 75, 241308 (2007).
- [11] R. Perumal, Z. Cui, P. Gille, J. -C. Harmand, and K. Yoh, *Semicond. Sci. Technol.* 29, 115005 (2014).
- [12] Z. Cui, T. Ishikura, F. Jabeen, J. -C. Harmand, and K. Yoh, *Journal of Crystal Growth* 378, 511 - 514 (2013).
- [13] M. Murayama and T. Nakayama, *Phys. Rev. B* 49, 7 (1994).
- [14] A. De and C. E. Pryor, *Phys. Rev. B* 81, 155210 (2010).
- [15] Ch. Blomers, T. Grap, M. I. Lepsa, J. Moers, St. Trellenkamp, D. Gutzmacher, H. Luth, and Th. Schapers, *Appl. Phys. Lett.* 101, 152106 (2012).
- [16] S. A. Dayeh, C. Soci, P. K. L. Yu, E. T. Yu, and D. Wang, *Appl. Phys. Lett.* 90, 162112 (2007).

- [17] T. Nittono, H. Ito, O. Nakajima, and T. Ishibashi, *Jpn. J. Appl. Phys.* **27**, 1718 - 1722 (1988).
- [18] C. Ford, J. C. Ho, Y. Chueh, Y. Tseng, Z. Fan, J. Guo, J. Bokor, and A. Javey, *Nano. Lett.* **9**, 360 - 365 (2009)
- [19] W. Mönch, *Semiconductor Surfaces and Interfaces* (Springer, Berlin, 1993).
- [20] M. Noguchi, K. Hirakawa, and T. Ikoma, *Phys. Rev. Lett.* **66**, 2243 (1991).
- [21] C. Schierholz, T. Matsuyama, U. Merkt, and G. Meier, *Phys. Rev. B* **70**, 233311 (2004).
- [22] A. Bringer and Th. Schapers, *Phys. Rev. B* **83**, 115305 (2011).
- [23] B. R. Nag, *Electron Transport in Compound Semiconductors* (Springer, Berlin, 1980).
- [24] J. Motohisa and H. Sakaki, *Appl. Phys. Lett.* **60**, 1315 (1992).
- [25] Q. Hang, F. Wang, P. D. Carpenter, D. Zemlyanov, D. Zakharov, E. A. Stach, W. E. Buhro, and D. B. Janes, *Nano. Lett.* **8**, 49 - 45 (2008).
- [26] C. Thelander, P. Caroff, S. Plissard, A. W. Dey, and K. A. Dick, *Nano. Lett.* **11**, 2424 - 2429 (2011).
- [27] M. Johnson, R. H. Silsbee, *Phys. Rev. Lett.* **55**(17), 1790–1793 (1985).
- [28] F. J. Jedema, H. B. Heersche, A. T. Filip, J. J. A. Baselmans, B. J. van Wees, *Nature* **416**, 713–716 (2002).
- [29] J. Tarun, S. Huang, Y. Fukuma, H. Idzuchi, Y. Otani, N. Fukata, K. Ishibashi, and S. Oda, *J. Appl. Phys.* **109**, 07C508 (2011).
- [30] J. Tarun, S. Huang, Y. Fukuma, H. Idzuchi, Y. Otani, N. Fukata, K. Ishibashi, and S. Oda, *Appl. Phys. Express* **5**, 045001 (2012).
- [31] E-S. Liu, J. Nah, K. M. Varahramyan, and E. Tutuc, *Nano Lett.* **10**, 3297–3301 (2010).
- [32] H. Kum, J. Heo, S. Jahangir, A. Banerjee, W. Guo, and P. Bhattacharya, *Appl. Phys. Lett.* **100**, 182407 (2012).

- [33] S. Heedt, C. Morgan, K. Weis, D. E. Bürgler, R. Calarco, H. Hardtdegen, D. Grützmacher, and Th. Schäpers, Nano Lett. 12, 4437-4443 (2012).
- [34] H. Jaffrès, J.-M. George, and A. Fert, Phys. Rev. B 82, 140408 (2010).
- [35] J.S. Moodera, G. Mathon, Journal of Magnetism and Magnetic Materials 200, 248 -273 (1999).

Chapter 6

Conclusions

In this thesis, we have proposed that InAs nanowire can be used as fine spin transport channel for spintronics device applications, particularly, the Datta-Das Spin-FET. InAs nanowires have been grown by VLS technique using MBE system. In addition, the electrical transport properties and the fabrications of single nanowire electrical device have been investigated. Furthermore, the spin transport properties of InAs nanowires with different structures and crystalline orientations have been evaluated and compared.

In chapter 2 and 3, we have reported the growth of the common $\langle 111 \rangle$ -oriented InAs nanowires and InAs/InP core/shell $\langle 111 \rangle$ -oriented nanowires. Then, the field effect mobility of these two kinds of nanowires have been characterized by using back gate FET structure respectively. Meanwhile, spin transport property such as electron spin relaxation length of the nanowire have been investigate by the observations of a gate voltage dependent crossover from weak localization to weak anti-localization were extracted the spin relaxation length of ~ 290 nm and coherence length of ~ 360 nm, which are both longer than the previous reports of the common InAs nanowires. Reduced spin relaxation and enhanced 1D transport properties in our core/shell nanowires are confirmed.

In chapter 4 and 5, we have focused on the InAs nanowire with $\langle 110 \rangle$

orientation. For the spin propagating along the $[110]$ direction, the effective magnetic fields due to spin orbit interaction of Rashba and Dresselhaus own same direction. Therefore, we expected that InAs nanowire with $\langle 110 \rangle$ orientation might be applied to spintronics devices as an efficient 1D spin transport channel. Correspondingly, investigating growth and transport properties have been reported. Using Pd as the new catalyst metal, stable ZB structure $\langle 110 \rangle$ -oriented InAs nanowire have been grown in similar VLS technique with MBE system. Compared with other $\langle 111 \rangle$ InAs nanowires, a superior transport property was determined with a back-gate FET structure at room temperature. Furthermore, the transport properties of a single nanowire were characterized with Hall-bar devices, and a proper electron concentration and sufficiently high carrier mobility were accurately determined. Meanwhile, temperature dependent transport behavior was investigated, and surface scattering was confirmed as the main factor of electron scattering. To improve the transport properties of this nanowire, future work will focus on investigating proper surface passivation or core/shell structure growth. Furthermore, the spin injection of semiconductor nanowires has been discussed and some primary results have been reported. The physics behind this observation is currently under investigation and further efforts are necessary to complete the spin-valve measurements. Regardless, these $\langle 110 \rangle$ InAs nanowires are expected to provide more opportunities to realize spintronics devices for spin transport and manipulation applications.

List of Publications/Conferences

1. Publications related to this work

- [1] Zhixin Cui, Tomotsugu Ishikura, Fauzia. Jabeen, Jean-Christophe Harmand, Kanji Yoh, “Fabrication and Characterization of a δ -Doped InAs/InP Core Shell Nanowire Transistor“, J. Crystal Growth, 378, 511–514 (2013).
- [2] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, Keita Konishi, Kanji Yoh and Junichi Motohisa, “Characterizing the electron transport properties of a single $\langle 110 \rangle$ InAs nanowire“, Appl. Phys. Express 7, 085001 (2014).
- [3] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, Keita Konishi, Kanji Yoh and Junichi Motohisa, “Characterization of Electron Transport Properties of $\langle 110 \rangle$ InAs Nanowires by Hall Effect Measurements“, Solid State Devices and Materials (SSDM2014), 8th – 11th September, Tsukuba, Japan, No: 6304.

2. Publications related to other works

- [1] Tomotsugu Ishikura, Zhixin Cui, Takashi Matsuda, Kanji Yoh, “Thermal Stability of Pd Gate in Pseudomorphic InGaAs Heterostructures“, Japanese Journal of Applied Physics, Japan Society of Applied Physics (JSAP), 50, 6GF19-1 (2011).
- [2] Keita Konishi, Zhixin Cui, Takahiro Hiraki, Kanji Yoh, “Spin-injection into epitaxial graphene on silicon carbide“, J. Crystal Growth, 378, 385–387 (2013).
- [3] Tomotsugu Ishikura, Zhixin Cui, L-K. Liefelth, Keita Konishi, Kanji Yoh, “Electrical spin injection from ferromagnet into an InAs heterostructures through MgO tunnel barrier“, cite as: arXiv:1304.1671 (2013)
- [4] Rajagembu Perumal, Zhixin Cui, P. Gille, J. -C. Harmand, and Kanji Yoh,

“Palladium assisted hetroepitaxial growth of InAs nanowire by molecular beam epitaxy”, *Semicond. Sci. Technol.* 29, 115005 (2014).

- [5] Tomotsugu Ishikura, L-K. Liefeth, Zhixin Cui, Keita Konishi, Kanji Yoh, and Tetusya Uemura, “Electrical spin injection from ferromagnet into an InAs quantum well through a MgO tunnel Barrier”, *Appl. Phys. Express* 7, 073001 (2014).

3. Presentations related to this work

International conferences

- [1] Zhixin Cui, Keita Konishi, Tomotsugu Ishikura, J.Bubesh Babu, J.C. Harmand, Kanji Yoh, “Fabrication of Spin Transistors Based on InAs Nanowire”, MNC 2010, 23rd International Microprocesses and Nanotechnology Conference (MNC2010), Kokura, Japan, 9th – 12th November, 2010.
- [2] Zhixin Cui, Keita Konishi, Tomotsugu Ishikura, J.Bubesh Babu, J.C. Harmand, Kanji Yoh, “A Non-ballistic InAs Nanowire Spin Transistor Operated at Room Temperature “, 19th International Conference on Electronic Properties of Two-Dimensional Electron Systems (EP2DS19), Tallahassee, Florida, USA, 25th – 29th July, 2011.
- [3] Zhixin Cui, Keita Konishi, Tomotsugu Ishikura, J.Bubesh Babu, J.C. Harmand, Kanji Yoh, “An InAs Nanowire-Spin-Transistor Measured at Room Temperature”, International Workshop on Spin Currents 2011 (IWSC2011), Sendai, Japan, 25th – 29th July, 2011.
- [4] Zhixin Cui, Keita Konishi, Tomotsugu Ishikura, J.Bubesh Babu, J.C. Harmand, Kanji Yoh, “Fabrication and Characterization of Spin Transistor Based on InAs Nanowire“, Materials Research Society 2011 (MRS2011), Boston, MA, USA, 28th November – 2nd December, 2011.

- [5] Zhixin Cui, Tomotsugu Ishikura, J.C. Harmand, Kanji Yoh, “Fabrication and Characterization of InAs Nanowire Spin Transistor “, International Conference of Physics of Semiconductor 2012 (ICPS2012), Zurich, Switzerland, 29th July–3rd August, 2012.
- [6] Zhixin Cui, Fauzia Jabeen, J.-C. Harmand and Kanji Yoh, “Fabrication and Characterization of a δ -Dope InAs/InP Core Shell Nanowire Transistor”, The 17th International Conference on Molecular Beam Epitaxy (MBE2012), Nara, Japan, 23rd – 28th September, 2012.
- [7] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, and Kanji Yoh, “Observation of Direct Spin Injection from NiFe into an InAs Nanowire”, 20th International Conference on Electronic Properties of Two-Dimensional Electron Systems (EP2DS20), Wroclaw, Poland, 1st -5th July, 2013.
- [8] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, and Kanji Yoh, “Observation of Direct Spin Injection into an [110] InAs Nanowire”, SPINTECH, Chicago, USA, 29th July- 2nd August, 2013.
- [9] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, Keita Konishi, Kanji Yoh and Junichi Motohisa, “Growth and characterization of transport properties of <110>-oriented InAs nanowires”, IEEE International Nanoelectronics Conference (IEEE INEC2014), Sapporo, Japan, 28th –31st July, 2014.
- [10] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, Keita Konishi, Kanji Yoh and Junichi Motohisa. “Characterization of Electron Transport Properties of <110> InAs Nanowires by Hall Effect Measurements”, Solid State Devices and Materials (SSDM2014), Tsukuba, Japan, 8th – 11th September, 2014.
- [11] Zhixin Cui, Rajagembu Perumal, Tomotsugu Ishikura, Keita Konishi, Kanji Yoh and Junichi Motohisa.” Growth and Transport Property Characterization of <110> InAs Nanowire”, Materials Research Society 2014 (MRS2014), Boston, USA, 30th November – 5th December, 2014.

Domestic conferences (Japan)

- [1] 崔 志欣, 石倉丈継, 松田喬, 陽完治, 「パラジウム・ゲート InAs 系 HEMT の電気特性評価」, 第 71 回応用物理学会学術講演会, 長崎大学, 2010 年 9 月 14 - 17 日.
- [2] 崔 志欣, 石倉丈継, 鈴木 健司, 小西 敬太, ブベシュ バブ, 陽完治, 「InAs ナノワイヤースピントランジスタの作製プロセス」, 春季第 58 回応用物理学会, 2011 年 3 月 24 - 27 日 (震災により発表キャンセル)
- [3] 崔 志欣, 小西 敬太, ブベシュ バブ, 陽完治, 「InAs ナノワイヤ・スピントランジスタの作製と評価」, 第 72 回応用物理学会学術講演会, 山形大学, 2011 年 8 月 29 - 9 月 2 日.
- [4] 崔 志欣, ブベシュ バブ, 陽完治, 「InAs ナノワイヤへのスピン注入」, 春季第 59 回応用物理学会, 早稲田大学, 2012 年 3 月 15 日 - 18 日.
- [5] 崔 志欣, ブベシュ バブ, 陽完治, 「InAs ナノワイヤへのスピン注入」, 第 73 回応用物理学会, 愛媛大学・松山大学, 2012 年 9 月 11 日 - 14 日.
- [6] 崔 志欣, ブベシュ バブ, 陽完治, 「 δ ドープ InP/InAs/InP コアシェルナノワイヤにおける電子スピン伝導の評価」, 第 60 回応用物理学会春季学術講演会, 神奈川工科大学, 2013 年 3 月 27 日 - 30 日.
- [7] 崔 志欣, ラガマンブ ペルマルブ, 石倉 丈継, 陽完治, 「InAs ナノワイヤへのスピン注入デバイスの作製と評価」, 第 74 回応用物理学会, 同志社大学, 2013 年 9 月 16 日 - 19 日.