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Study on Selectively Grown GaAs-based Nanowire Array Solar Cells

(有機金属気相選択成長法を用いた GaAs ナノワイヤアレイ太陽電池に関する研究)

Graduate School of Information Science and Technology,
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Dissertation Supervisor

Professor Takashi FUKUI

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Contents

Acknowledgements i

Contents v

List of figures ix

Chapter 1

General introduction 1

1.1 Overview 1

1.1.1 Background 1

1.1.2 History of photovoltaic cells.....3

1.1.3 Next generation photovoltaic cells.....5

1.1.4 Nanowire solar cells.....6

1.2 Objective 7

1.3 Outline of this thesis 9

Bibliography 11

Chapter 2

Nanowires and their photovoltaic application 15

2.1 Semiconductor nanowires.....15

2.1.1 History of vapor-liquid-solid growth.....15

2.1.2 History of selective-area metal organic vapor phase epitaxy.....16

2.1.3 Advantages.....17

2.2 Nanowire solar cells 19

2.2.1 History 19

2.2.2 Fundamentals of solar cells 21

2.2.3 Advantages of nanowire array solar cells 23
Bibliography 27

Chapter 3

Experimental techniques 33

3.1 Principles of MOVPE 33
3.1.1 Overview.... 33
3.1.2 MOVPE growth process 35
3.2 Selective-area metal organic vapor phase epitaxy 37
3.2.1 Selective area growth procedures 37
3.2.2 Growth of GaAs nanowires on GaAs(111)B 39
3.3 Experimental method..... 40
Bibliography 43

Chapter 4

GaAs core-shell junction nanowire array solar cells 45

4.1 Introduction 46
4.2 Experimental procedure 47
4.3 Results and discussion 48
4.3.1 Optical characterization of GaAs nanowire array and planar structure 48
4.3.2 Photovoltaic performance of GaAs core-shell nanowire array solar cells ..50
4.3.3 Core-multishell GaAs/InGaP nanowire array solar cells 52
4.4 Conclusions 56
Bibliography 57

Chapter 5

InGaAs axial junction nanowire array solar cells 61

5.1 Introduction 62

5.2 Experimental procedure 63
5.3 Results and discussion 65
5.3.1 InGaAs axial-junction nanowire array solar cells 65
5.3.2 InGaAs nanowire array solar cells with tin-doped contact layer 68
5.4 Conclusions 72
Bibliography 73

Chapter 6
Future prospects for nanowire solar cells.....77
6.1 Fabrication of flexible cells and reuse the substrates for the nanowire growth...78
6.2 Multi-junction nanowire solar cells 81
Bibliography 83

Chapter 7
Summary and conclusions 85
7.1 Summary 85
7.2 Outlook for nanowire solar cells 87

List of publications/conferences/awards 89

List of figures

Fig. 1-1 Global primary energy consumption by region. 1

Fig. 1-2 Global primary energy consumption with Oil, natural gas, coal, nuclear energy, hydroelectricity and renewable. 2

Fig. 1-3 Japan primary energy consumption with Oil, natural gas, coal, nuclear energy, hydroelectricity and renewable. 2

Fig. 1-4 Solar photovoltaic total global capacity. 3

Fig. 1-5 Classification of various solar cells such as 1st, 2nd, and next generation. ...4

Fig. 1-6 NREL's chart of best research-cell efficiencies. Especially, multi-junction solar cells are indicated by a red sphere. 5

Fig. 1-7 Schematic image of the transition from the first silicon solar cells to next generation solar cells using III-V compound semiconductor nanowire arrays. 6

Fig. 1-8 Number of publication on nanowire solar cells. (Data was obtained from the Web of Science database with "(nanowire or nanowhisker or nanorod) and (solar cell or photovotalic)"). 8

Fig. 2-1 Schematic illustration of catalyst-assisted VLS growth process for nanowires. (a) Gold seed particles are formed onto a substrate. (b) Gold-Silicon liquid alloys are formed by heating substrates and introducing the growth materials. (c) Nucleation occurs at the particle/substrate interface and the growth of nanowires occurs. 16

Fig. 2-2 Schematic illustrations of (a) epitaxial growth of lattice mismatched material in planar layer, and (b) in nanowire layer. 17

Fig. 2-3 Number of publication on nanowires. (Data is obtained from the Web of Science database with "(nanowire* or nanowhisker* or nanorod*)"). 18

Fig. 2-4 Schematic illustration of pn/hetero structures with (a) radial and (b) axial junction. 20

Fig. 2-5 (a) Equivalent circuit of photovoltaic cell, and (b) typical I-V characteristic of photovoltaic cell. 21

Fig. 2-6 (a) The effect of series resistance of solar cell, and (b) that of shunt resistance. 22

Fig. 2-7 Schematic view of core-shell nanowire array solar cell. The incident light that pass through the transparent electrode is absorbed in the entire surface of nanowires. 24

Fig. 2-8 (a) Schematic illustration of the nanowire with lattice mismatched materials, and (b) variations of the critical thickness of a misfitting layer growing on top of a nanowire as function of the radius, for various values of the misfit. 25

Fig. 3-1 The periodic table from II to V elements. The elements used in this study are indicated by boldface for III-V compound semiconductors and impurity doping. 34

Fig. 3-2 Schematic illustration of the MOVPE system for III-V compound semiconductor nanowires in this study. 35

Fig. 3-3 Schematic illustration of metalorganic sources provided by bubblers. Black valve indicates the pressure control valve. 36

Fig. 3-4 Schematic illustration of boundary layer above the susceptor in the reactor. (δ: boundary layer thickness, U: velocity of the gas) 37

Fig. 3-5 Schematic illustration of the mechanisms of selective area MOVPE in boundary layers. 38

Fig. 3-6 Fabrication process for GaAs nanowire arrays by SA-MOVPE. 39

Fig. 3-7 (a) Schematic illustration of scanning electron microscopy (SEM), and (b) 30˚- and 0˚- (inset) tilted SEM images of GaAs nanowire array by selective-area MOVPE. 40

Fig. 3-8 Optical property of ITO film deposited by magnetron sputter system. 41

Fig. 4-1 Schematic illustration of GaAs nanowire array with core-shell p-n junction. 46

Fig. 4-2 (a) SEM image of masked GaAs(111)B substrate for nanowire growth, and (b) cross-sectional illustration of GaAs core-shell nanowire array solar cells. 47

Fig. 4-3 (a) SEM image of GaAs core-shell nanowire array on a p-type GaAs(111)B substrate and (b) measured reflectance spectra of a GaAs nanowire array and a planar GaAs solar cell. 48

Fig. 4-4 2D simulation analysis of optical generation rate of electron-hole pairs for 400-, 500-, and 600-nm incident light. 49

Fig. 4-5 Schematic illustration of the fabrication process for nanowire array solar

cell. 50

Fig. 4-6 Cross-sectional SEM image of the GaAs core-shell nanowires, BCB layer, and ITO film. 51

Fig. 4-7 (a) *J-V* characteristics of core-shell nanowire array solar cells under AM1.5G (1 sun) illumination, and (b) that of nanowire array diode structure. 52

Fig. 4-8 Schematic illustration of GaAs/InGaP core-multishell nanowire-array solar cell structure with thin Ti/ITO hybrid electrode. 53

Fig. 4-9 (a) *J-V* characteristics of GaAs/InGaP core-multishell nanowire array solar cells, and (b) internal quantum efficiency comparison with GaAs core-shell nanowire solar cells. 54

Fig. 5-1 (a) Schematic illustration of InGaAs axial junction with AlInP layer, and (b) schematic illustration of InGaAs nanowire array solar cells. 63

Fig. 5-2 (a) 30˚- and 0˚- (inset) tilted SEM images of an InGaAs nanowire array with an axial p-i-n junction. (b) SEM image of the tips of nanowires after reactive ion etching and (c) deposition of ITO electrode. 64

Fig. 5-3 (a) Cross-sectional SEM image superposed with EBIC signals and (b) line profile of InGaAs axial-junction nanowire-array SCs. 66

Fig. 5-4 (a) Measured external quantum efficiency (EQE), internal quantum efficiency (IQE), and reflectance and (b) *J-V* characteristics under AM1.5G (1 sun) illumination and dark condition of InGaAs axial-junction nanowire-array solar cells on p-type GaAs(111)B substrate with a pitch of 600 nm. 67

Fig. 5-5 (a) Growth sequence of InGaAs p-i-n junction nanowire with TESn and (b) SEM image of as-grown nanowire with enhanced lateral growth and coalescing. 68

Fig. 5-6 (a) Growth sequence of the nanowire array with pulse doping of TESn and (b) SEM image of the nanowire array. 69

Fig. 5-7 *J-V* characteristic of InGaAs nanowire-array solar cells with and without pulse doping of TESn for n-type highly tin-doped layer. 70

Fig. 6-1 (a) SEM image of nanowire array on substrate, (b) SEM image of re-growth nanowires on reused substrate. 78

Fig. 6-2 Schematic illustration of fabrication process for flexible cells using nanowire array and reusing masked substrate for nanowire growth. 79

Fig. 6-3 (a) Photograph of peeled off PDMS film with embedded nanowires, and (b) SEM image of nanowire array embedded in PDMS after RIE. 79

Fig. 6-4 (a) Measured transmittance of InP nanowire arrays at three different states such as before peel off, after peel off and with metal layer, and (b) absorption of InP nanowire array calculated from measured reflectance and transmittance. 80

Fig. 6-5 (a) Schematic illustration of four-junction nanowire array solar cells , and (b) values of bandgap, lattice constant, and lattice mismatch between connected materials of each cells. 82

Chapter 1 General Introduction

1.1 Overview

1.1.1 Background

Recently, annual global consumption of energy is rising with the rapid economic development. And also, the consumption of fossil fuel such as oil, coal and natural gas has been increasing year by year. Global energy consumption has increased over 30% with rapid economic development especially in Asian nations in the past ten years, as shown in Fig. 1-1 [1]. Thereby, the amount of carbon dioxide (CO_2) emissions are also rising causes global warming. Additionally, since the Fukushima incident in Japan,

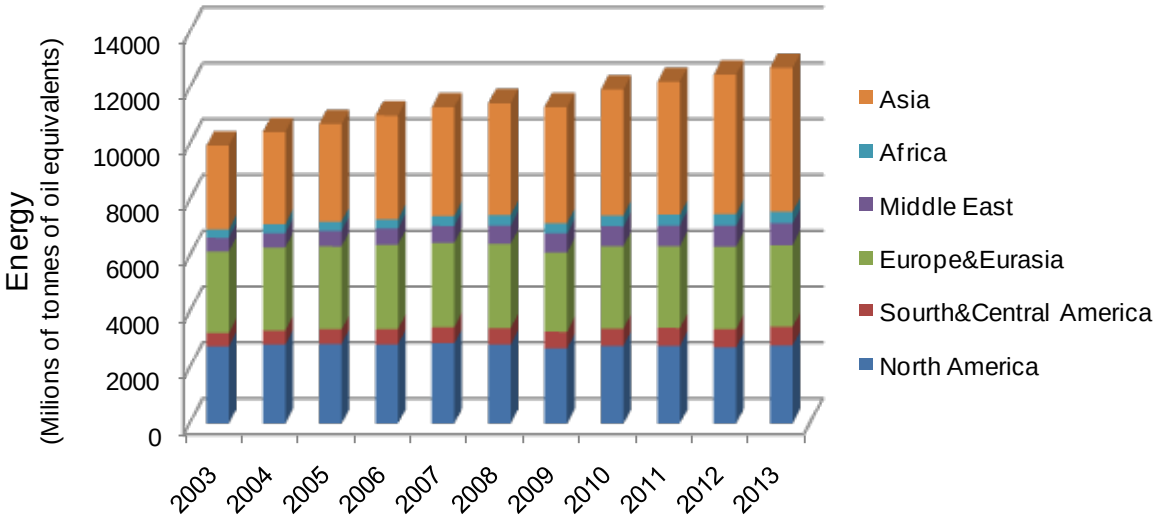

Fig. 1-1 Global primary energy consumption by region. [1]

safety of nuclear power generation has been considered a worldwide issue. To solve this issue, renewable energies such as solar, wind, biomass, and geothermal heat are expected to replace conventional methods of power generation. In order to save the exhaustible natural resources ensure safety, it is necessary for us to do a scientific effort to develop renewable energy resources. In particular, research on photovoltaic power generations using semiconductor solar cells have much attraction for exploiting renewable energy, in terms of scientific and practical view. Photovoltaic cell generates electrical power by converting solar light into direct current electricity using p-n junction of semiconductors. Photovoltaic power generation has plentiful advantages, for example, no moving parts, no environmental emissions during operation, running sound is quiet, and constant efficiency regardless of the power generation area. Therefore, photovoltaic generation has the potential for alternative to other power generations. However, renewable energy including photovoltaic power generation has some issues such as high cost, instability and low conversion efficiency, hence the use of renewable energy is still remains low.

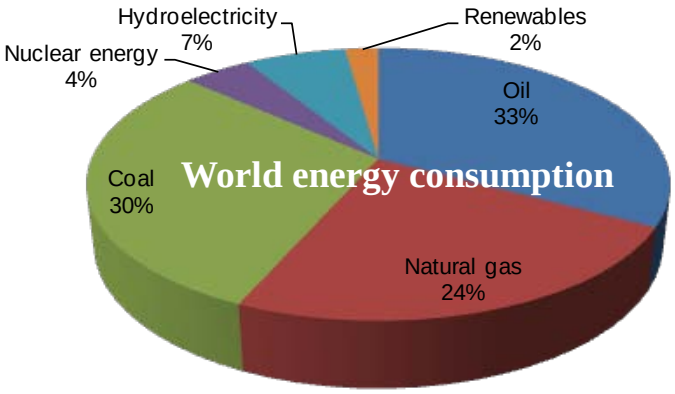

Fig. 1-2 Global primary energy consumption with Oil, natural gas, coal, nuclear energy, hydroelectricity and renewable. [3]

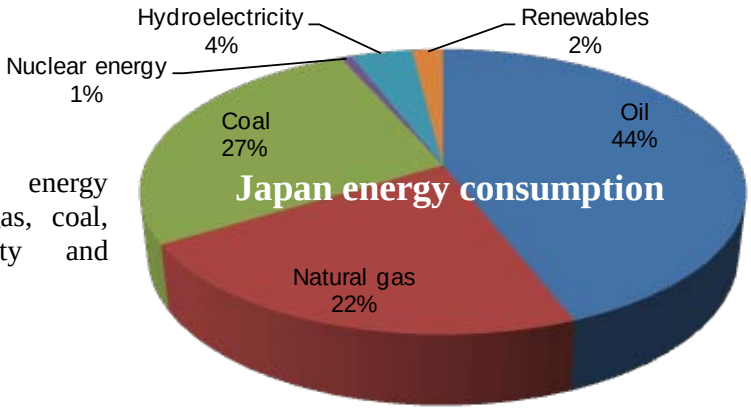

Fig. 1-3 Japan primary energy consumption with Oil, natural gas, coal, nuclear energy, hydroelectricity and renewable. [3]

Fig. 1-2 and 3 shows the energy consumption of world and Japan in 2013. Energy supply is depended on thermal power generation using oil, natural gas, and coal. Moreover the ratio of renewable is a few percent of overall energy consumption not only in Japan but worldwide [2,3]. On the other hand, capacity of photovoltaic power generation is only increasing with development of solar cells and government subsidies in recent as shown in Fig. 1-4 [4]. Under such circumstances, solar cells are expected to obtain higher efficiency to further replace conventional power generation methods.

1.1.2 History of photovoltaic cells

First of all, photovoltaic effect was demonstrated by French physicist Alexander Edmond Becquerel in 1839 [5]. Then, the first practical silicon solar cell was announced in 1954 with about 6% conversion efficiency [6], and commercial production of crystalline silicon modules began in 1963 by Sharp Corporation. After that, photovoltaic power generation has resulted in a general spread with the single crystalline [7], and multi crystalline silicon [8-11] as the first generation photovoltaic cells [Fig. 1-5].

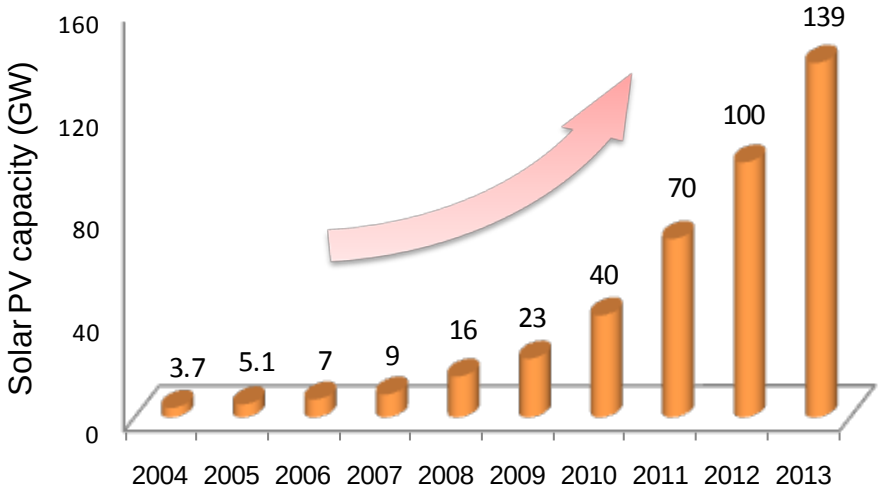

Fig. 1-4 Solar photovoltaic total global capacity. [4]

As second generation photovoltaic cell, thin-film solar cells are beginning to be researched and developed in recent days for achieving lower cost cells. Thickness of thin-film solar cell is about several microns and it can generate electricity, also it can be deposited onto inexpensive substrate such as glass [12,13], polymer [14], metal [15], and other flexible substrate [16,17]. For example, amorphous silicon is a common material used in thin-film solar cells. It's large light absorption coefficient compared to crystalline silicon and the capability to be deposited on a larger and cheaper substrate has resulted in much lower manufacturing cost than that of the first generation cell. However, the conversion efficiency of amorphous silicon solar cells is lower than that of crystalline silicon solar cells. For higher efficiency, tandem structure has been researched which consists of amorphous silicon and microcrystal silicon solar cells [18,19]. After the long history of research on silicon solar cell, the conversion efficiency has come to the theoretical limitation [20-22]. Along with these silicon solar cells, devices using cadmium telluride (CdTe) [23,24], copper indium diselenide (CIS) [25,26], copper indium gallium diselenide (CIGS) [27-29], and copper zinc tin sulfide (CZTS) [30,31] are also well-known as second generation thin-film solar cells achieved lower cost.

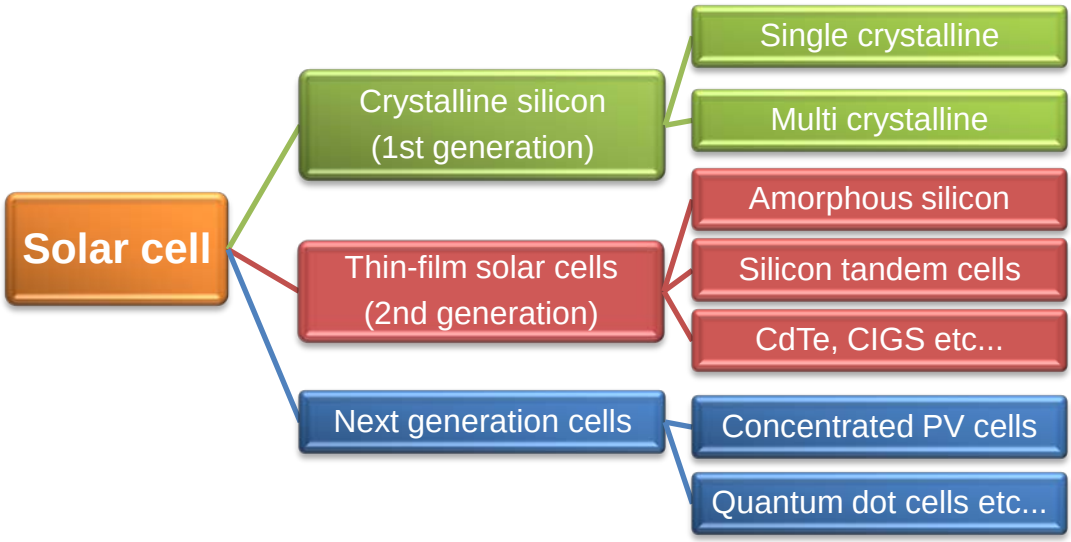

Fig. 1-5 Classification of various solar cells such as 1st, 2nd, and next generation.

1.1.3 Next generation photovoltaic cells

Recently, research of third generation solar cells attracted much attention against a background of environmental and safety problems with existing power generations. Next generation photovoltaic cells are promising for achieving a high conversion efficiency which exceeds Shockley-Queisser limit [20]. Especially, III-V compound semiconductor multiple junction solar cells have been studied intensively in recent years, which offer the highest photovoltaic conversion efficiency under concentration. Theoretical limitation of single junction solar cells is approximately 33%, whereas that of multiple junction solar cells has the potential for obtaining over 60% by four or more junctions made of III-V materials [32]. The difficulties of fabricating multiple junction solar cells are the design and choice of materials. It must consider current matching and light absorption within each cell. Additionally, the lattice constant of the each cells must be matched to keep crystal quality of the interface of each cell. Conventionally, we adopt additional technique such as buffer layer for relaxation of lattice mismatch stress or wafer bonding technology for packing different cells in the case of making heterojunction with lattice mismatch.

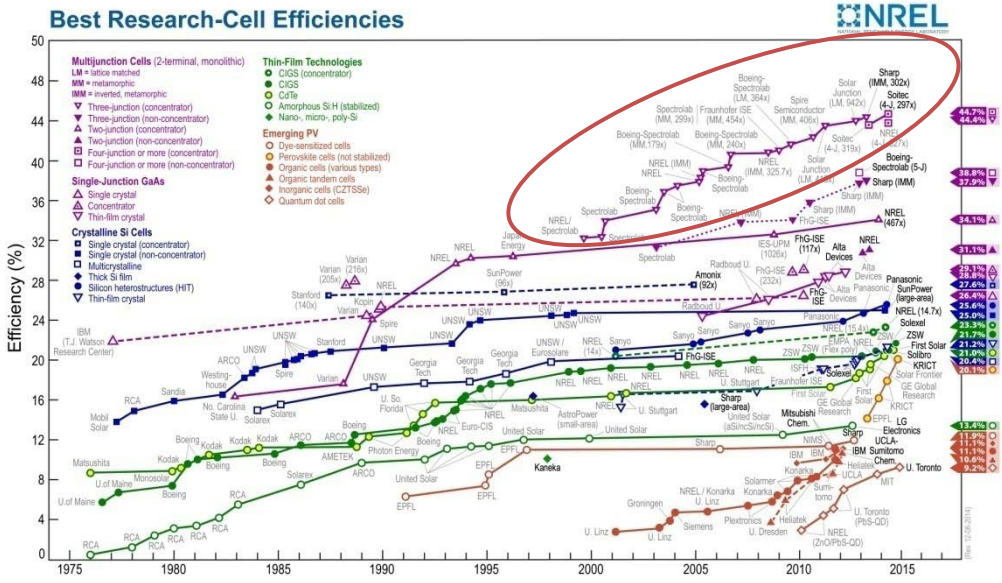

Fig. 1-6 NREL's chart of best research-cell efficiencies. [34] Especially, multi-junction solar cells are indicated by a red sphere.

Recently, for example, Sharp Corporation achieved InGaP/GaAs/InGaAs triple junction solar cells with 44.4% conversion efficiency at 302 suns [33], and four junction solar cells by Soitec achieved 44.7% conversion efficiency under 297 suns. NREL reports best research cell efficiencies with various structures and materials [34], and this report shows that efficiencies of each cells are increasing with small percent year by year as shown in Fig. 1-6. However, the restriction of lattice matching is makes it difficult for the realization of multiple junction solar cells with over 50% or more conversion efficiency. For the fabrication of next generation photovoltaic cells with multiple junctions, innovative technology and technical breakthrough is expected.

1.1.4 Nanowire solar cells

Semiconductor nanowires have attracted much attention for use in future nanometer-scale devices. Semiconductor nanowire solar cell is also expected as one of the most promising next generation photovoltaic cell for achieving high efficiency and low cost. Nanowires are one-dimensional structures with the diameter of hundreds nanometers or less and heights of several micrometers. This structure can endure very high lattice mismatch because of their small footprints, hence it is promising for multi-junction nanowire cells with higher efficiency than existing planar photovoltaic cell using GaAs-based materials [35].

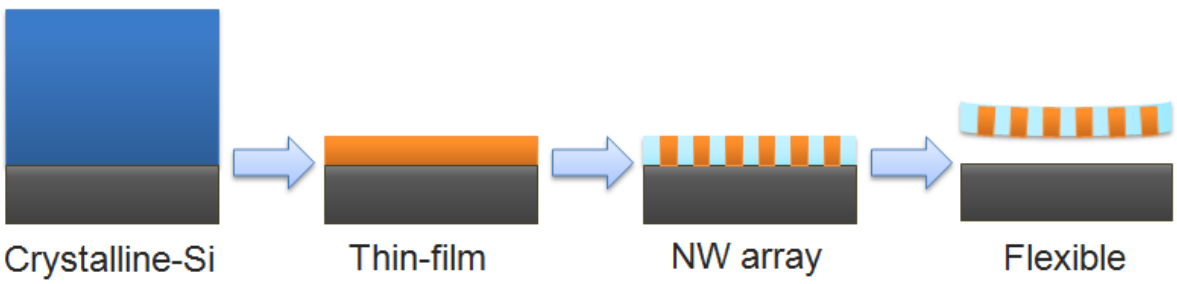

Fig. 1-7 Schematic image of the transition from the first silicon solar cells to next generation solar cells using III-V compound semiconductor nanowire arrays.

Furthermore, a uniformly aligned nanowire array which was optimized the size and position of nanowires has geometrical advantages for solar cell applications. Nanowire array geometry shows efficient absorbance of sunlight because of its low reflectance equal to antireflection effect [36,37]. Additionally, quantity of materials of nanowire array structure becomes much less than that of conventional planar structure, when the nanowire array part is peeled off from the substrate for nanowire growth. These advantages indicate that nanowire array structure has the great potential for the next generation solar cells solving the issues such as high cost and low efficiency of existing cell [Fig. 1-7].

In general, there are two approaches for creating nano-structure such as top-down and bottom-up technology. Nano-scale structures by top-down approach are using lithography and etching method and widely used for fabricating electronic devices in recent, but the damage of the fabrication process degrades the device performance. On the other hand, the bottom-up approach based on crystal growth technique is expected to have a potential for nano-scale devices without damage during fabrication process caused by lithography and etching.

There are two types of technique for forming nanowire on the field of bottom-up approach. The main approach to grow nanowire is based on vapor-liquid-solid (VLS) method, which uses catalysts and liquid phase underneath metal particles for crystallization [38-40]. And recently, nanowire solar cells using VLS technique are reported by many groups [41-43]. On the other hand, catalyst-free selective-area metal organic vapor phase epitaxy is researched and obtained well-aligned nanowires such as GaAs, InAs, InP and their ternary alloys. Mechanism of nanowire growth by SA-MOVPE is faceting growth on (111) substrate and good quality epitaxial layer can be obtained without using catalyst, consequently many novel results about mechanism of nanowire growth and their device application has been reported by this method [44-49]. Additionally, InP nanowire array solar cells by this method were reported in 2009 with well-aligned and position controlled nanowires [50].

1.2 Objective

As discussed in the previous section, III-V compound semiconductor nanowire arrays have great potential for high conversion efficiency and low cost solar cells. And recently, research on application of nanowires is increasing as shown in Fig 1-8. From the early 2010s, reports about III-V compound semiconductor solar cells using well-aligned nanowires are increasing, nevertheless there have been very few reports on well-aligned GaAs-based nanowire array solar cells because GaAs nanowire array solar cell has some issues that need to be solved for obtaining a good photovoltaic property. To solve these problems, this thesis deals with the epitaxial growth of III-V compound semiconductor nanowire, especially GaAs-based materials by selective-area metal organic vapor phase epitaxy (SA-MOVPE) formed on GaAs(111)B substrate. And also, additional idea and technique for obtaining higher efficiency with GaAs nanowire array solar cells are proposed. The objective of this work is to fabricate GaAs-based nanowire array solar cells and realize a good photovoltaic property. Additionally, new technique and the design of multi-junction nanowire array solar cells with lattice mismatched materials are proposed.

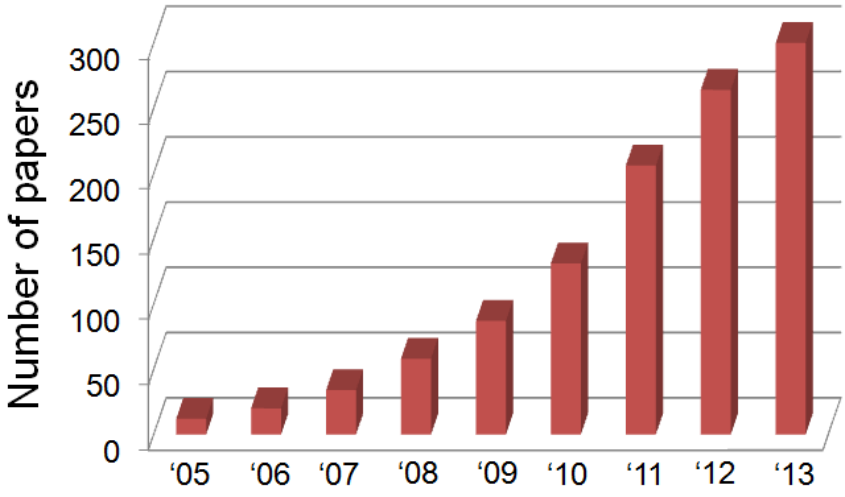

Fig. 1-8 Number of publication on nanowire solar cells. (Data is obtained from the Web of Science database with "(nanowire or nanowhisker or nanorod) and (solar cell or photovotalic)").

1.3 Outline of this thesis

This thesis divided into 7 chapters.

In chapter 2, an overview of the research field of semiconductor nanowire such as the history of nanowire, the way of nanowire growth, fundamentals of solar cells, and the advantages of one-dimensional epitaxial structure are described. Then, the basic principle, structure and performance of solar cell are explained. Finally, solar cell application of nanowire structure is described.

In chapter 3, details of fabrication techniques of semiconductor nanowire array and characterization method of as-grown nanowire and their photovoltaic application are described. First, we describe overview of MOVPE growth technique, advantages, system, and process. Then, principles of SA-MOVPE are explained. Finally, the experimental methods such as scanning electron microscopy, reactive ion etching, sputtering, and electron beam evaporation are described.

In chapter 4, growth and fabrication of core-shell GaAs nanowire arrays on p-type GaAs(111)B substrate by using SA-MOVPE and their photovoltaic application is described. Here, the optical property of as-grown nanowire array compared with GaAs planar solar cell is elucidated, and also two-dimensional simulation of optical generation rate of electron-hole pair in GaAs nanowire structure is discussed. Finally, GaAs/InGaP core-multishell nanowire array solar cell is investigated in comparison with core-shell type cell.

In chapter 5, growth of axial p-i-n junction nanowire array solar cells with a position-controlled InGaAs ternary alloys on GaAs(111)B substrate are described. The main difficulty concerning the fabrication of GaAs-based nanowire array solar cells is the degradation of series resistance between the GaAs-based nanowires and the indium-tin oxide (ITO) deposited as a transparent electrode. To reduce the series resistance of the device, the contact layer with tin-doping is demonstrated. Here the

performance comparison of with and without tin-doping InGaAs layer is described.

In chapter 6, remarkable technology and idea of nanowire array solar cells which are reported in related studies are described. First, the technique of the photovoltaic cell detachment and transfer from semiconductor substrate to flexible carrier substrate is described for resource-saving cells. Then, the design of tandem nanowire array structure with lattice-mismatch materials is explained.

Summary, conclusions, and future prospects for next-generation nanowire array solar cells by SA-MOVPE are discussed in chapter 7.

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Chapter 2 Nanowires and their photovoltaic application

The semiconductor nanowires have become hot topics and have been studied for the last decades. Recently, synthetic control of nanowire growth has improved and application for future application based on III-V compound semiconductor nanowires on various substrates has been realized. Nanowire array solar cell is also expected as one of the future device application which can obtain higher conversion efficiency at lower cost compared with traditional cells. In this chapter, fundamentals of semiconductor nanowires and their solar cell applications are described.

2.1 Semiconductor nanowires

2.1.1 History of vapor-liquid-solid growth

In 1964, Wagner and Ellis at Bell Labs demonstrated the vapor-liquid-solid (VLS) growth of Si whiskers using gold as a catalyst as shown in Fig. 2-1 [1]. Droplets of gold made by heating on the silicon substrate catalyze the growth of Si nanowire-like structure under injection of $SiCl_4$ and H_2. In that work, the diameter of this nano-structure is comparable to the catalyst size in the range of micrometers, and they described Si nanowire-like structure as whisker. This method for fabricating

nano-structure as bottom-up technique has been popular because of its uncomplicated process.

Device application of nanowire structure was sparked by the fabrication of first GaAs p-n junction nanowires by VLS method reported by group of Hitachi in the early 1990s [2,3]. After that, the groups at Harvard University in USA [4,5], University of California, Barkley in USA [6], Lund University in Sweden [7,8], and other groups reported remarkable researches on the field of a huge variety of nanowires grown by VLS method [9,10].

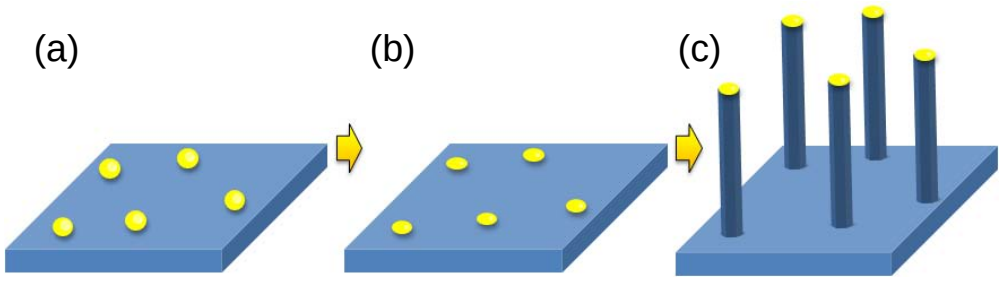

Fig. 2-1 Schematic illustration of catalyst-assisted VLS growth process for nanowires. (a) Gold seed particles are formed onto a substrate. (b) Gold-Silicon liquid alloys are formed by heating substrates and introducing the growth materials. (c) Nucleation occurs at the particle/substrate interface and the growth of nanowires occurs. [1]

2.1.2 History of selective-area metal organic vapor phase epitaxy

On the other hand, there is another fabrication method of semiconductor nanowires by using masked pattern, which is called selective-area growth. Originally, in the early 1960s, a group of Joyce and Baldrey was reported about chloride phase epitaxy of Si using Si(111) substrate with SiO_2 masked substrate for selective-area growth [11]. In 1987, a group from NTT lab fabricated narrow two-dimensional electron gas channels in GaAs/AlGaAs sidewall interfaces using selective-area MOVPE [12]. After that, small structures with {-110} facets vertical to the (111)B

substrate and its applications has been demonstrated [13-15]. In 1997, Hamano *et al.* reported GaAs pillar with small diameter on masked GaAs(111)B substrate with nanometer scale selectively grown as a new technique for fabrication of two-dimensional photonic crystals [16].

The group of Hokkaido University (group of professor T. Fukui) has been reported on the selective-area metal organic vapor phase epitaxy (SA-MOVPE) of III-V compound semiconductor nanowires over the past dozen years. For instance, growth of InGaAs [17,18], InP [19], and GaAs nanowire [20] were reported. And also, heterostrucutre such as InAs nanowires on Si(111) substrate [21], GaAs/InGaAs [22], GaAs/AlGaAs [23], InAs/InP [24], and GaAs/GaAsP [25] have been investigated.

2.1.3 Advantages

Semiconductor nanowires with several micrometers height have a high aspect ratio. Wire geometry allows vertical or lateral device process for one-dimensional structure and enables novel electrical and optical properties different from the bulk structure. Originally, nanowire geometry achieves large surface areas more than that of planar surface, so hetero- or p-n junction in radial direction are expected to indicate remarkable property due to large junction area.

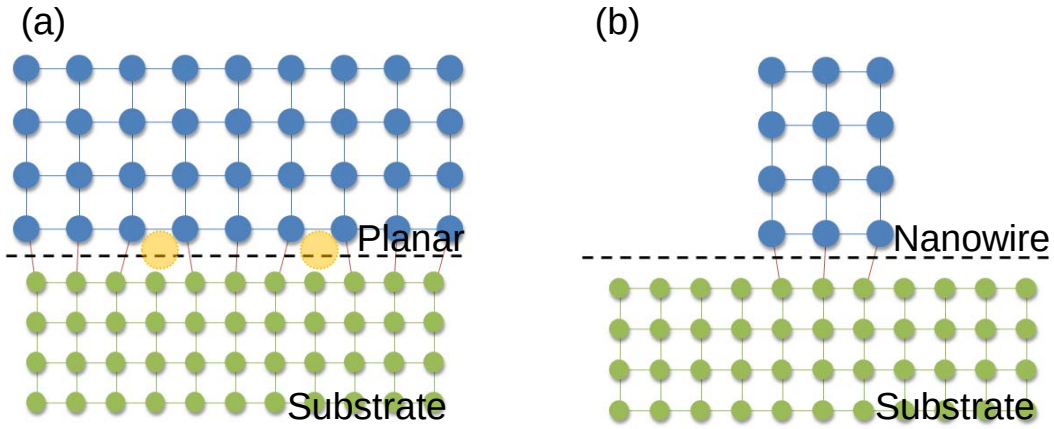

Fig. 2-2 Schematic illustrations of (a) epitaxial growth of lattice mismatched material in planar layer, and (b) in nanowire layer.

In the axial direction of nanowire growth, heteroepitaxy with lattice mismatch materials is possible because of its small diameter. In a normal epitaxial layer, large lattice mismatch causes high misfit dislocation density [Fig. 2-2(a)]. Poor interface with this misfit dislocation degrades the electrical and optical property of the devices. On the other hand, nanowire geometry can form good quality heterostructures with lattice mismatch materials because the requirement for lattice matching is relaxed in small diameter of nanowires [Fig. 2-2(b)]. This advantage allows the heteroepitaxy with high lattice mismatch. For example, K. Tomioka *et al*. succeeded InAs [21] and GaAs [30] nanowires epitaxialy grown on Si substrate with large lattice mismatch of 11.6 and 4.1%, respectively.

Additionally, semiconductor nanowires by SA-MOVPE can be formed in nanometer scale without damage caused by lithography and etching process, and obtained atomically smooth interfaces and surfaces. It can be said that semiconductor nanowires by SA-MOVPE are suitable for device application. To overcome the theoretical limitation of previous planar-based devices such as field-effect transistor sensors [26,27], LEDs [28,29], and photovoltaic cells have been researched.

These works on semiconductor nanowires became one of the most active research areas within the nanodevice community. Actually, the number of publication concerns with nanowires and associated research such as growth mechanism and their device application is still increasing exponentially as shown in Fig. 2-3.

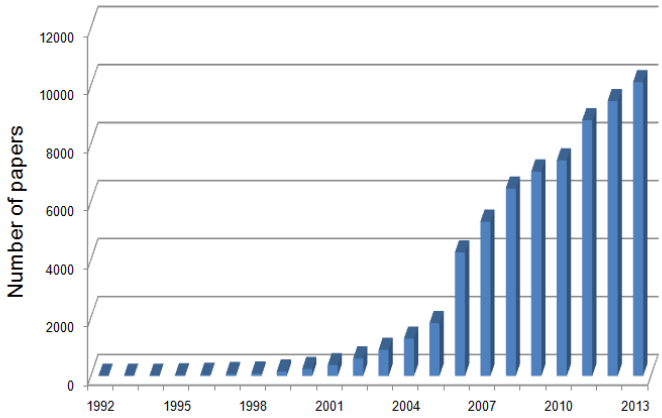

Fig. 2-3 Number of publication on nanowires. (Data is obtained from the Web of Science database with “(nanowire* or nanowhisker* or nanorod*)”).

2.2 Nanowire solar cells

2.2.1 History

Photovoltaic applications of single nanowire or nanowire array have been reported and increasing exponentially. B. M. Kayes *et al.* reported comparison of the device physics principle of planar and GaAs nanowire solar cells with radial p-n junction [31]. In that paper, the result showed that the new structure with core-shell nanowires has the potential for achieving efficient carrier collection in inorganic solar absorber materials with low minority-carrier diffusion length. And also, analysis of optical property of nanowire solar cells was simulated with Si [32] and InP [33]. These studies reveal that the nanowire arrays with low filling ratio compared with planar geometry can achieve much lower reflectance. The report about vertical arrays of all-inorganic nanowires was published by Tsakalakos *et al* [34] in 2007. They fabricated Si core-shell nanowire array solar cells by VLS method for p-type core nanowires and plasma-enhanced chemical vapor deposition for n-type shell. In 2000s, wide varieties of semiconductor nanowire array solar cells were also reported using Si [35], GaN [36], ZnO [37], and CdS/CdTe [38]. Especially, III-V compound semiconductor nanowires are considered as one of the most promising platforms for next-generation solar cells because of the direct band gap, high light absorption coefficient, and suitable bandgap to the solar spectrum, and Borgström *et. al.* said that the use of III-V compound semiconductor nanowires in photovoltaic cells allows us to respond to the demand of high efficiency and low production cost with radial [Fig. 2-4(a)] or axial [Fig. 2-5(b)] junction in nanowire geometry [39].

In 2009, H. Goto *et al*. described growth condition of InP core-shell periodical nanowire arrays by SA-MOVPE and fabrication process for photovoltaic application, and obtained good quality photovoltaic cell performance [40]. After that, reports deal with InP nanowire array solar cells increased. For instance, a group of Lund University demonstrated tandem junction InP nanowires on Si substrate [41]. In 2013, they

showed the remarkable device with 13.8% efficiency of InP nanowire array solar cells [42]. This performance was achieved in 180-nm-diameter nanowires that only covered 12% of the p-InP substrate surface. E. P. A. M. Bakkers's group also reported InP nanowire array axial p-n junction solar cells [43]. In this research, they showed that postgrowth piranha etching is critical for achieving good photovoltaic performance. And also, our group at Hokkaido University reported InP nanowire array solar cells with core-shell structure [44] and heterostructure [45]. In the papers of core-shell nanowire cells, we reported the effect of surface passivation using AlInP window layer. Additionally, we reported indium-tin-oxide (ITO)/InP heterojunction nanowire array solar cells. The ITO not only acted as a transparent electrode but also as forming a photovoltaic junction for nanowires.

In the case of GaAs-based nanowire solar cells, LaPierre *et al*. reported pioneering work with core-shell junction in 2009 [46]. And also, A. F. i. Morral *et al*. demonstrated a single GaAs nanowire solar cell with conversion efficiency of 4.5% by molecular beam epitaxy (MBE) [47]. In 2013, they reported standing GaAs core-shell nanowire solar cell and discussed about enhancement of light absorption due to a light-concentration property of nanowire vertical to the substrate [48].

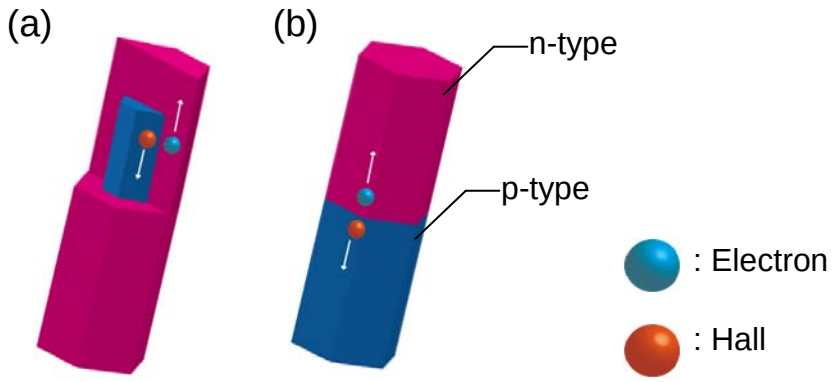

Fig. 2-4 Schematic illustration of pn/hetero structures with (a) radial and (b) axial junction.

2.2.2 Fundamentals of solar cells

P-n junction is basic form of commercial photovoltaic cells today. When p-type semiconductor layer is joined together with n-type semiconductor layer, the depletion region with built-in electric field is formed by diffusion of electrons and holes. When the solar light energy with higher than band gap energy is absorbed in the semiconductor, electrons are excited from the valence band to the conduction band and electron-hall pairs are generated. Especially, electron-hall pair made by photon is easily separated in depletion layer by internal electric field and contribute to current of solar cell. The current from photovoltaic effect is based on diode equation, and described as below:

$$I = I_{ph} - I_0 \left[exp\left\{ \frac{qV}{nkT} \right\} - 1 \right]$$

And also, the equivalent circuit of photovoltaic cell is shown in Fig. 2-5(a) and from this circuit, the photovoltaic equation can be rewrite to as below:

$$I = I_{ph} - I_0 \left[exp\left\{ \frac{q(V + R_s I)}{nkT} \right\} - 1 \right] - \frac{V + R_s I}{R_{sh}}$$

(I_{ph}: light-generated current, q: electron charge, R_s: series resistance, R_{sh}: shunt resistance, k: Boltzmann's constant, I_0: dark saturation current, n: ideality factor)

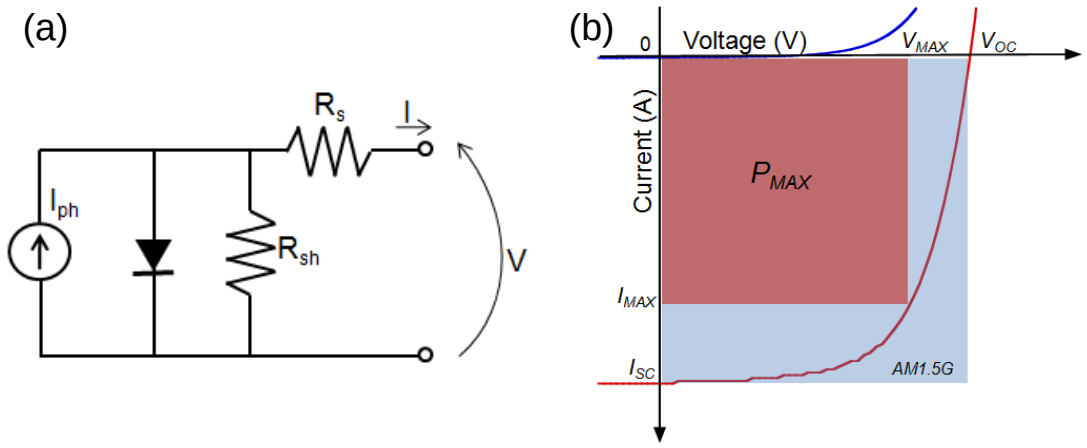

Fig. 2-5 (a) Equivalent circuit of photovoltaic cell, and (b) typical I-V characteristic of photovoltaic cell.

Fig. 2-5(b) shows the ideal performance of photovoltaic cell. Ideally, series and shunt resistances of solar cells are zero and infinitely large, respectively. Large series resistance including resistances of semiconductor itself and contact with electrode causes low fill factor and low current density [Fig. 2-6(a)]. On the other hand, small shunt resistance causes low open-circuit voltage by providing an alternate current path in solar cell structure for the light-generated current [Fig. 2-6(b)]. The conversion efficiency is occurred from the shift of the diode performance with photovoltaic effect, and this efficiency is determined by open-circuit voltage (V_{OC}), Short-circuit current density (J_{SC}), and the ratio between the maximum output power and the product of V_{OC} and J_{SC} (FF: fill factor) as below:

$$FF = \frac{V_{MAX} \cdot J_{MAX}}{V_{OC} \cdot I_{SC}}$$

$$\eta = V_{OC} \cdot J_{SC} \cdot FF$$

Maximum of conversion efficiency with single junction solar cell is calculated as Shockley-Queisser limit and its value is approximately 33% with 1.34 eV [49]. Thus, III-V compound semiconductors such as GaAs and InP are expected to be high-conversion-efficiency-cells, and in recent, actual photovoltaic cells with GaAs and InP achieved 28.8% and 22.1% conversion efficiency, respectively [50].

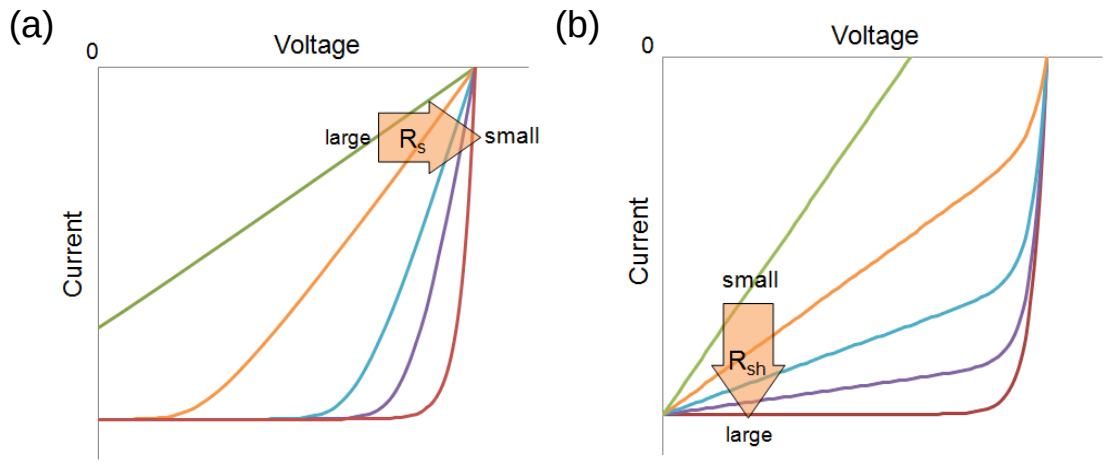

Fig. 2-6 (a) The effect of series resistance of solar cell, and (b) that of shunt resistance.

2.2.3 Advantages of nanowire array solar cells

Optical property

A lot of researches have focused on improving optical property of vertical standing nanowire arrays [32-33, 51]. The nanowire geometry can absorb the incident light and diffracted light by all of the surface of nanowires, when the diameter of the nanowire is comparable to or smaller than the radiation wavelengths, and actual photovoltaic device using vertically standing GaAs nanowire solar cell shows the effect of this absorption enhancement [52,53]. Additionally, nanowire arrays act as antireflection coating due to their geometry with intergradations of the effective refractive index of air, nanowire array, and substrate [32]. The actual reflectance measurements of nanowire showed lower percentage than that of conventional planar structures without antireflection coating generally have an average reflectance of ~40%. When we fabricate the p-n junction within the nanowire, we avoid the necessity of adding the antireflection coating or other surface processing for efficient light absorption.

Short Carrier Collection Length

Nanowire geometry can be extended p-n junction to three dimensions. The growth direction of nanowire is controlled by changing the growth conditions such as growth temperature and partial pressure of the sources. And then each dopant for p-type and n-type are used for the core-shell nanowire growth, we can obtain the radial p-n junction within the nanowires. In the core-shell p-n junction [Fig. 2-7] with vertically aligned nanowires, the electron-hole pairs are separated in radial direction and the photo-generated carriers only need to move much shorter length than the minority carrier diffusion length. On the other hand, conventional planar geometry needs long minority-carrier diffusion length to collect the photo-generated carriers.

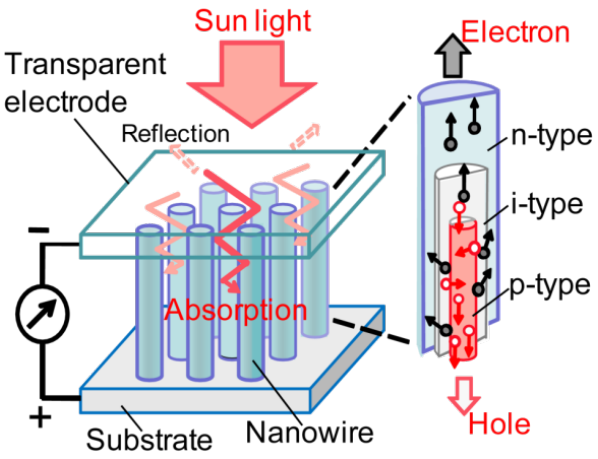

Fig. 2-7 Schematic view of core-shell nanowire array solar cell. [54] The incident light that pass through the transparent electrode is absorbed in the entire surface of nanowires.

Therefore, vertically aligned nanowire array solar cells with core-shell p-n junction are electrically superior compared with planar geometry. And also, the geometry of nanowire array has more than about ten times p-n junction area than the planar structure.

Peeling off

The use of expensive III-V substrates raises the production cost and disturbs the commercial spread. In the case of nanowire array solar cells with small junction area, the interface stress between nanowires and substrate makes it easy to remove the nanowire array, and this advantage enables to fabricate flexible cells and achieve low cost cells. Furthermore, this enables the substrate to reuse for growth of semiconductor nanowire arrays, and it would greatly reduce the production cost of nanowire array solar cells if the substrate can be used many times [55]. These advantages overcome the problems of the fabrication cost using III-V compound semiconductors, and thin-film flexible structures expand the design possibility of actual photovoltaic cells.

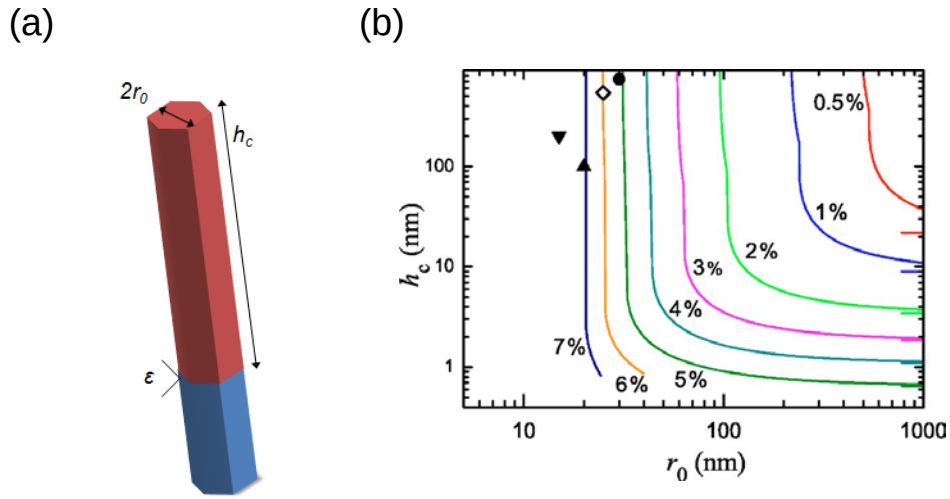

Fig. 2-8 (a) Schematic illustration of the nanowire with lattice mismatched materials, and (b) variations of the critical thickness of a misfitting layer growing on top of a nanowire as function of the radius, for various values of the misfit. [56]

Heterojunction with lattice-mismatch materials

The lattice mismatch between connected materials [Fig. 2-8(a)] is given as following equation,

$$\epsilon = \frac{a_{epi} - a_{sub}}{a_{sub}} \times 100$$

(ε (%): lattice mismatch, α_{epi}: lattice constant of epitaxial layer, α_{sub}: that of substrate)

The issue of large lattice mismatch is poor quality of interfaces with high misfit dislocation density, and this issue makes it difficult to grow thin film epitaxy with lattice mismatch materials. On the other hand, free-standing nanowires can obtain efficient lateral stress relaxation in nanometer-scale diameter. The relation between critical height and radius of nanowires with various lattice mismatches is calculated by Glas as shown in Fig. 2-8(b) [56]. This effect of nanometer-scale nanowires gives selectively enhancement of compound semiconductor materials for lattice-mismatched

window layer, tunnel junction, and multi-junctions cells in lateral direction. This advantage is very important for fabricating the next generation photovoltaic cell of the alternative to existing multi-junction solar cells using III-V compound semiconductors. Existing multi-junction solar cells must need to be considered lattice matching between each cell or add the buffer layer to form the good quality heterojunction with lattice mismatched materials. On the other hand, the geometry of nanowires with small diameters has high selectivity for each material of multi-junction solar cells and it enables to form the various junctions with lattice mismatch materials in one-time growth.

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Chapter 3 Experimental techniques

In this chapter, fundamentals of metal organic vapor phase epitaxy (MOVPE) and selective area growth are described refer to previous study [1]. In this study, nanowire arrays are formed by selective-area MOVPE which is one of the bottom-up techniques. This fabrication technique uses masked substrate as a template of crystal growth and brings well-controlled nanowire arrays. Here, detailed fabrication process for masked substrate and GaAs nanowire arrays is described.

Additionally, experimental methods for device application are investigated. Here, the fundamentals of scanning electron microscopy and actual image of nanowire array are demonstrated. Then, sputter system, reactive ion etching system, and electron beam evaporation system are described for the fabrication of new structure of solar cells using nanowire array.

3.1 Principles of MOVPE

3.1.1 Overview

MOVPE technique is used for realizing single crystalline thin-films as one of the methods of chemical vapor deposition. Especially, the III-V compound semiconductor films such as GaAs, InP, InAs and their ternary alloys are fabricated by MOVPE. III and V metal-organic and source gases are used for growing compound semiconductors

and II and IV elements for p-type and n-type doping are used. Especially, bold face elements in Fig. 3-1 are used for this study for fabricating of III-V compound semiconductors with p-n junctions. This technique can be controlled atomic composition of mixed crystal semiconductors by partial pressures of supplying sources, and steep heterojunctions or p-n junctions can be formed by precise control of source gas flow. Additionally, MOVPE method has the potential for high-volume production with uniformly growth of semiconductor layer at once and commercially uses for fabrication of semiconductor devices.

In this technique, the source materials for III-V compound semiconductor growth are provided with purified hydrogen gas and diffuse near the surface of the substrate. Then, these molecules react chemically in the surface of growth substrate which is heated and epitaxial layer occurs at the surface of substrate in relationship to the underlying crystal structure. In the case of GaAs layer growth, trimethylgallium (TMGa: $Ga(CH_3)_3$) and arsine (AsH_3) are used, and epitaxial film of GaAs can grow according to the following reaction.

$$Ga(CH_3)_3 + AsH_3 \rightarrow GaAs + 3CH_4$$

II	III	IV	V
	Boron 5 **B**	Carbon 6 **C**	Nitrogen 7 **N**
	Aluminum 13 Al	**Silicon 14 Si**	**Phosphorus 15 P**
Zinc 30 Zn	**Gallium 31 Ga**	Germanium 32 Ge	**Arsenic 33 As**
Cadmium 48 Cd	**Indium 49 In**	**Tin 50 Sn**	Antimony 51 Sb

Fig. 3-1 The periodic table from II to V elements. The elements used in this study are indicated by boldface for III-V compound semiconductors and impurity doping.

3.1.2 MOVPE growth process

In this study, epitaxy is carried out in a horizontal MOVPE system with 5.75 slm of the total gas flow rate, and the system is working at 0.1atm. The system consists of a gases delivery system, exhaust disposal system, and a reactor system with temperature controller [Fig. 3-2].

The gases delivery system consists of lines, bubblers, valves and mass flow controllers (MFCs). The MO sources are provided in bubblers as shown in Fig. 3-3. Pressure control valve maintains the pressure of bubbler at 760 Torr. The carrier gas of palladium diffused purified hydrogen is led through source materials in the bubbler. We can control vapor pressure of the metal organic sources by the combination of thermal bath temperature and MFCs in each line of bubblers. And gas sources are provided from gas cylinders (in this study, AsH_3 and SiH_4). During the epitaxial growth, MO and gas sources are transported to the reactor in each run lines with hydrogen carrier gas.

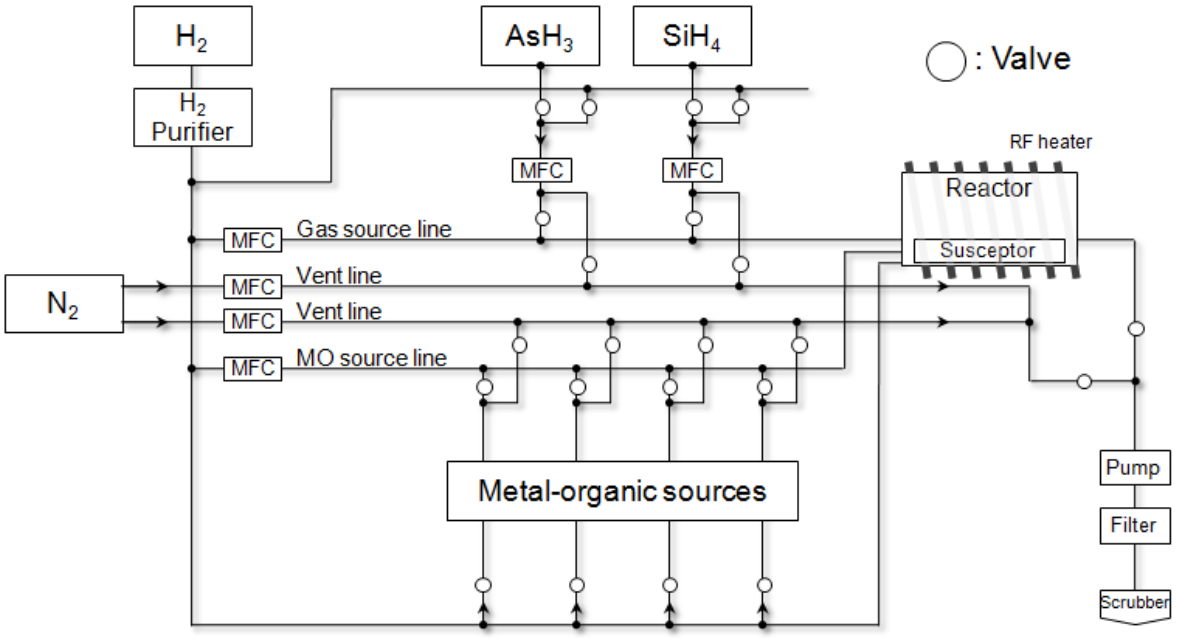

Fig. 3-2 Schematic illustration of the MOVPE system for III-V compound semiconductor nanowires in this study.

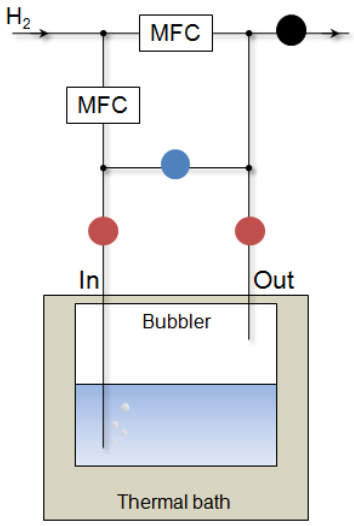

Fig. 3-3 Schematic illustration of metalorganic sources provided by bubblers. Black valve indicates the pressure control valve.

The exhaust disposal system consists of exhaust lines and rotary pump to maintain the reactor at low pressure. These are connected to exhaust toxic gas treatment system because toxic gases are used as the source materials in MOVPE.

The reactor system consists of a quartz reactor, a quartz tray, a carbon susceptor and radio frequency (RF) heater. The flow dynamics for crystal growth in MOVPE technique are divided into 4 general phases: mass and heat transport, physical surface processes, chemical reactions, and thermodynamics [2]. Especially, in the mass and heat transport phase, a boundary layer above the growing surface is formed by the laminar flow of the vapor in the reactor, and the source materials are transported to the surface of the growth substrate [Fig. 3-4]. The thickness of boundary layer is increasing related to the square root of the distance from front edge of susceptor.

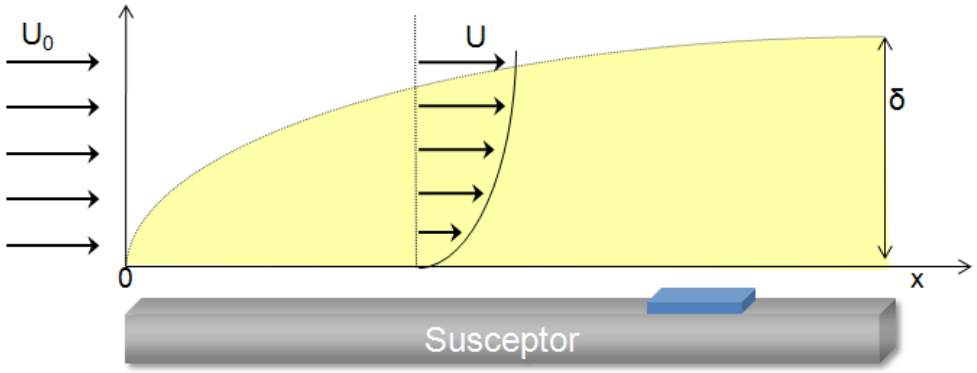

Fig. 3-4 Schematic illustration of boundary layer above the susceptor in the reactor. (δ: boundary layer thickness, U: velocity of the gas)

3.2 Selective-area metal organic vapor phase epitaxy

3.2.1 Selective area growth procedures

Selective area growth is one of the bottom-up techniques for forming the micro- or nano-scale epitaxial materials on the masked substrate using amorphous film. Selective-area metal organic vapor phase epitaxy (SA-MOVPE) technique can fabricate position- and size-controlled nanometer scale buildings by changing the design of masked substrate by lithography technique. And also, the three-dimensional function or geometry can be fabricated by controlling the precise growth temperature, partial pressure of source materials, impurity doping, and band engineering in nanowire structure. Fig. 3-5 shows schematic illustration of the different mechanisms of selective-area MOVPE process. Adsorption, desorption, and surface migration are

occurred not only in substrate area but also in mask region. In the case of nanowire growth, the masked region is the dominant area of the growth substrate, so that the species for the nanowire growth are diffuse from the mask region to openings. To improve the flatness and obtain the effective growth rate, selective area growth is need to grow under high temperature for longer diffusion length.

First, 20-nm-thick SiO_2 film is deposited by plasma sputtering system (Shibaura Mechatronics Corporation: CFS-4EP-LL) or plasma-enhanced chemical vapor deposition (PE-CVD). Thickness of the mask layer is verified by ellipsometry (ULVAC ESM-1AT). Then, EB resist (Nippon Zeon: ZEP520A-7) is coated on the substrate by spin coating technique. After the pre-bake at 180 °C for 2 min, EB lithography is carried out. In this study, EB lithography system (JEOL: JBX-6300SF) with ZrO/W field emitter with 100kV of accelerating voltage was used. Hexagonal openings of arbitrary diameter and pitch are formed by EB lithography and wet chemical etching with buffered hydrofluoric acid (BHF). Then, EB resist is removed by methyl-ethl-ketone (MEK) and 1165 remover (Rohm and Haas). Just before the nanowire growth, a native oxide on the surface of the masked substrate was removed by alkali solution (Furuuchi Chemical: Semicoclean) for 10 min in an ultrasonic bath. Then the nanowire growth was carried out in MOCVD system.

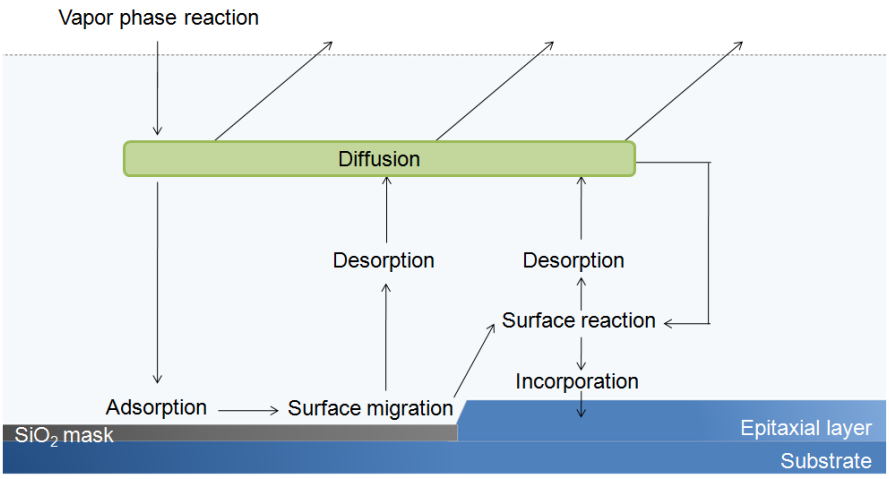

Fig. 3-5 Schematic illustration of the mechanisms of selective area MOVPE in boundary layers.

3.2.2 Growth of GaAs nanowires on GaAs(111)B

Here, the faceting growth of GaAs nanowires is explained by SA-MOVPE. The GaAs nanowire growth conditions and mechanism of SA-MOVPE is investigated by Fukui's group [3-5]. The dependence of growth mode on the substrate orientation and growth conditions was studied and it was found that the nanowires were formed only in a limited combination of growth conditions and substrate orientations, which identifies clearly that the formation of nanowires solely relied on the formation of facets during SA-MOVPE. The SA-MOVPE of GaAs nanowires is carried out on GaAs(111)B substrate partially covered with SiO_2 thin-film in a horizontal low-pressure MOVPE system [Fig.3-6]. The total gas flow rate was maintained at 5.75 slm and the system was working at 0.1 atm. The basic source materials are trimethylgallium (TMGa) and arsine (AsH_3). Basically, the partial pressures of TMGa and AsH_3 are 1.0×10^{-6} and 2.5×10^{-4}, respectively. Nanowire structure is formed in the vertical growth condition at 760 °C for 20 min. The average diameter of GaAs nanowires was about 140 nm and this was almost equal to that of the holes in the SiO_2 mask patterns. And also, the height of GaAs nanowires is about 1 μm which is almost the same with previous reports. The sidewalls of the hexagonal nanowires are {–110} facet surfaces vertical to the GaAs(111)B substrate.

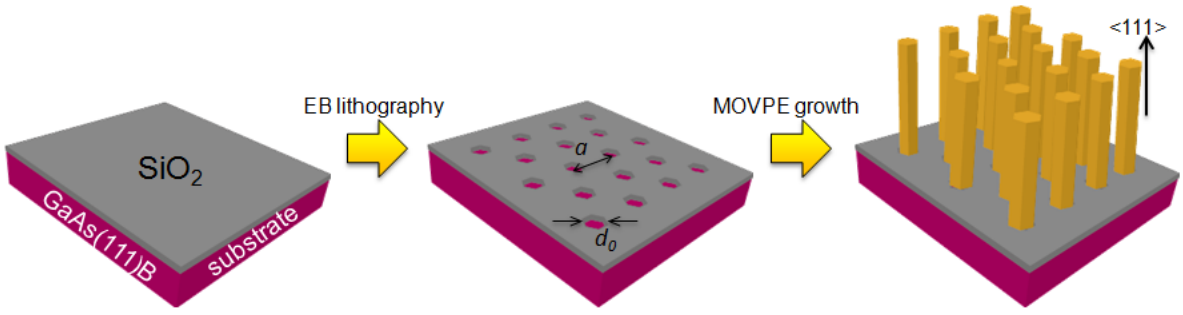

Fig. 3-6 Fabrication process for GaAs nanowire arrays by SA-MOVPE.

3.3 Experimental method

Scanning electron microscopy

Scanning electron microscopy (SEM) is used for structural characterization of grown nanowires or the results of fabrication process for nano-devices in this study (Hitachi hitec: S-4100, SU-8010). The general system consists of an electron gun, condenser lenses, scanning coils, an objective lens, and detector for secondary electron [Fig. 3-7(a)]. The electron beam is finely focused by a set of these lenses and scanning coil, and the image is generated by scanning over the sample. The screening and detection of secondary electron which is emitted by the surface of the target shows the valuable information about the surface morphology and geometrical features of the nanowires as shown in Fig. 3-7(b).

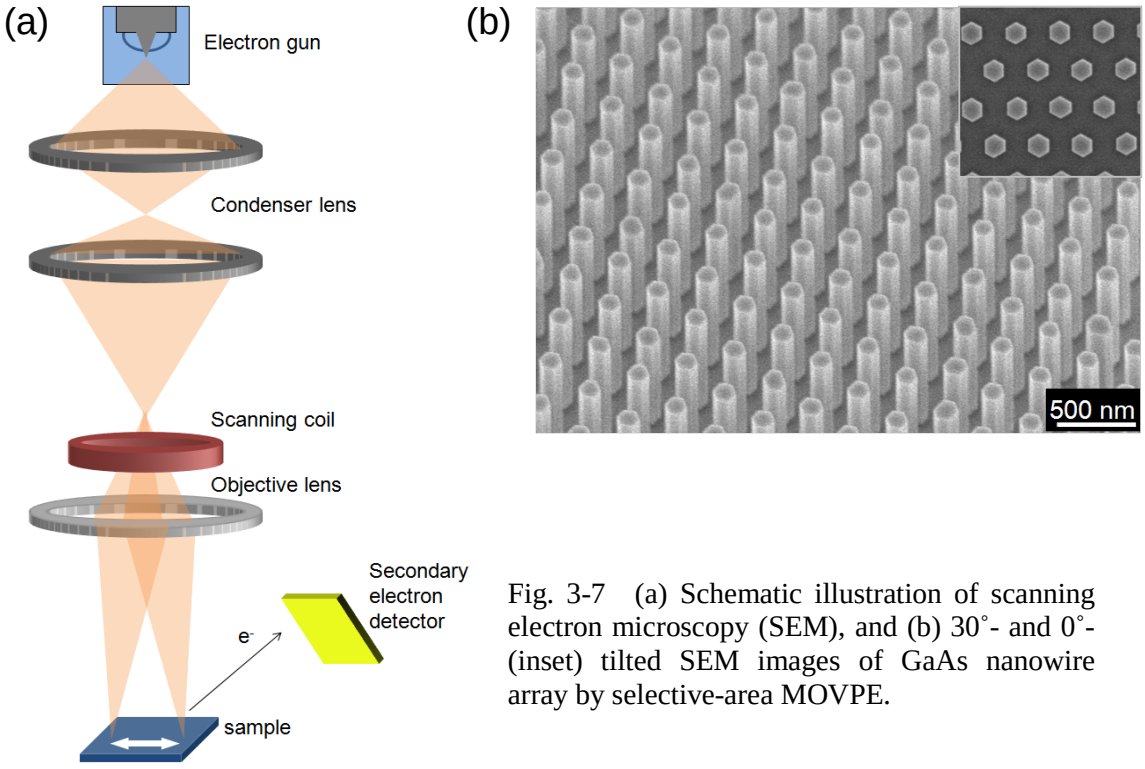

Fig. 3-7 (a) Schematic illustration of scanning electron microscopy (SEM), and (b) 30˚- and 0˚-(inset) tilted SEM images of GaAs nanowire array by selective-area MOVPE.

Sputtering

Sputtering is a physical vapor deposition technologies of films of various materials, and in this study, SiO_2 and indium-tin-oxide films are deposited for fabrication of nanowires and their device applications by magnetron sputtering systems (Shibaura Mechatronics: CFS-4EP-LL, Suga: AV301-0000). In argon atmosphere, gaseous plasma is creating and then accelerating ions collide with source material target. Sputtered atoms ejected from the target to the sample. Especially, in this study, magnetron sputtering is used which is different from general technology. In this method, magnetic field is used for keeping the plasma in front of the target and it can increase the probability of collision between target and ions. In the case of SiO_2 mask deposition, the RF output is 200W with 20 sccm of argon for 2 min. The growth rate of SiO_2 layer is about 0.2 nm/sec in this condition. Additionally, in the case of transparent electrode, ITO is deposited with 70 W and argon with a small amount of oxygen atmosphere for 45 min. In this condition, the thickness of ITO film is ~400 nm, and the transmittance of the thermally-processed layer is measured in 200-1100 nm of wavelength as shown in Fig. 3-8.

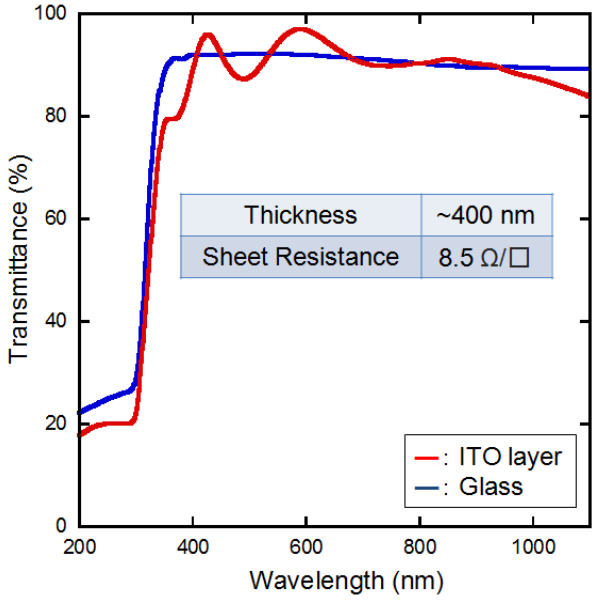

Fig. 3-8 Optical property of ITO film deposited by magnetron sputter system.

Reactive ion etching

Reactive ion etching is one of the dry etching technologies for micro- and nano-fabrication. Under low pressure condition, plasma is generated by an electromagnetic field. Accelerating ions from the plasma collide against the target surface and dry etching process is occured. In this study, RIE system (SAMCO Inc.: RIE-10NR) is used for dry-etching with SiO_2 and transparent resin. The condition of introduced gas is CF_4 : O_2 = 10 : 40 (sccm), the chamber pressure is 4 Pa, the RF generator output is 100W for transparent resin etching. The etching rate under this condition is about 3 nm/sec for transparent resin layer used in this work.

Electron beam evaporation

This technique is one of the physical vapor deposition methods for forming metal electrode. Electron beam is directed towards the evaporation targets to melt or sublimate by heating. Then, the evaporation materials are coated to the substrate. The chamber of this system must be used under high vacuum condition to obtain longer mean free path of the evaporation materials from the target to the substrate. In this study, the systems (Eiko engineering) is evacuated by using turbo-molecular pump and cryopump, and metals such as Au, Ge, Ni, Al, Cr, Ti are deposited with approximately 7.0 kV accelerating voltage.

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Chapter 4 GaAs core-shell junction nanowire array solar cells

Semiconductor nanowires are good candidate for light-absorbing material in next generation photovoltaic and III-V nanowire-based multi-heterojunction solar cells using lattice mismatched material system are expected as high energy conversion efficiencies under concentrated light. Here this chapter demonstrates core-shell GaAs nanowire arrays by using catalyst-free selective-area metal organic vapor phase epitaxy (SA-MOVPE) as a basis for nanowire solar cells and multi-junction solar cells. The actual measurement of reflectance of the nanowire array showed much lower reflection than that of a planar wafer without any anti-reflection coating. Additionally, FDTD analysis indicates that the well-aligned nanowire array designed for solar spectrum can achieve low reflectance. Next core-shell GaAs nanowire array solar cell with radial p-n junction is fabricated. Despite the low reflectance, the energy conversion efficiency was 0.71% since a high surface recombination rate of photo generated carriers and poor ohmic contact between the GaAs and transparent indium-tin-oxide (ITO) electrode. To avoid these degradations, an InGaP layer and a Ti/ITO electrode are introduced. As a result, we obtained a short-circuit current of 12.7 mA/cm^2 and an open-circuit voltage of 0.5 V for an overall efficiency of 4.01%. These results were published in 2013 [1].

4.1 Introduction

Semiconductor nanowire is a promising material for future nanometer-scale electronic and optical devices such as field-effect transistors [2], light-emitting diodes (LEDs) [3], and sensors [4]. Vertically aligned nanowire arrays have geometrical advantages for photovoltaic applications [5,6] such as low reflection and efficient light absorption [7-10]. Furthermore nanowires configuration with radial p-n junctions [Fig. 4-1] effectively collects photo-generated electrons and holes [11]. The small footprints of nanowires also overcome a formation of defects owing to lattice mismatch [12] therefore tandem nanowire solar cells with multiple axial junctions in the lattice-mismatched system can be achieve over 50%-energy-conversion efficiencies [13,14].

The vapor-liquid-solid (VLS) method is typical synthesis of these nanowires for photovoltaic [15]. This study used catalyst-free SA-MOVPE in which the size, position and direction is well controlled by changing growth conditions. Recently, well-aligned vertical InP [16] and GaAs [17] nanowire array-based solar cells have been demonstrated by the SA-MOVPE. In this study, GaAs core-shell nanowire array solar cells with radial p-n junction and passivation effect for achieving good photovoltaic property are investigated [Fig. 4-1].

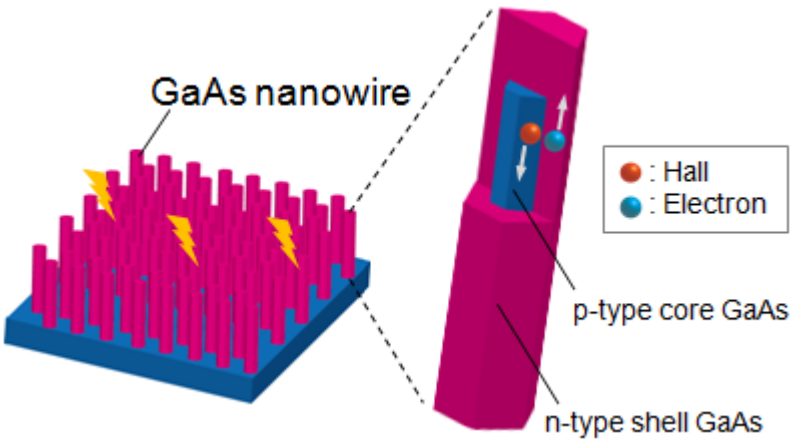

Fig. 4-1 Schematic illustration of GaAs nanowire array with core-shell p-n junction.

4.2 Experimental procedure

A 20-nm-thick SiO_2 film was deposited on p-type GaAs(111)B substrate by RF sputtering, and periodical openings with a diameter of 110 nm and a pitch of 400 nm were formed by electron beam lithography and wet chemical etching [Fig. 4-2(a)]. MOVPE growth on this masked substrate was carried out in a horizontal low-pressure MOVPE system. The total gas flow rate was maintained at 5.75 slm and the system was working at 0.1 atm. The source materials for GaAs nanowire growth were trimethylgallium (TMGa) and arsine (AsH_3), and dopant sources for the p-type core and n-type shell were respectively diethylzinc (DEZn) and monosilane (SiH_4). The partial pressures of TMGa, AsH_3, DEZn, and SiH_4 were 1.0×10^{-6}, 2.5×10^{-4}, 1.4×10^{-6}, and 5.0×10^{-8} atm, respectively. Previous study indicated that growth direction of GaAs nanowires can be controlled by changing growth condition such as temperature and AsH_3 pressure. Core-shell structure [Fig. 4-2(b)] was formed by changing the growth temperature from the vertical growth condition at 760 °C to the lateral condition at 680 °C with an AsH_3/TMGa pressure ratio of 250 [18]. Reflectance, photovoltaic performance, and quantum efficiency of nanowire array solar cells were measured by a Bunkokeiki CEP-25SR system.

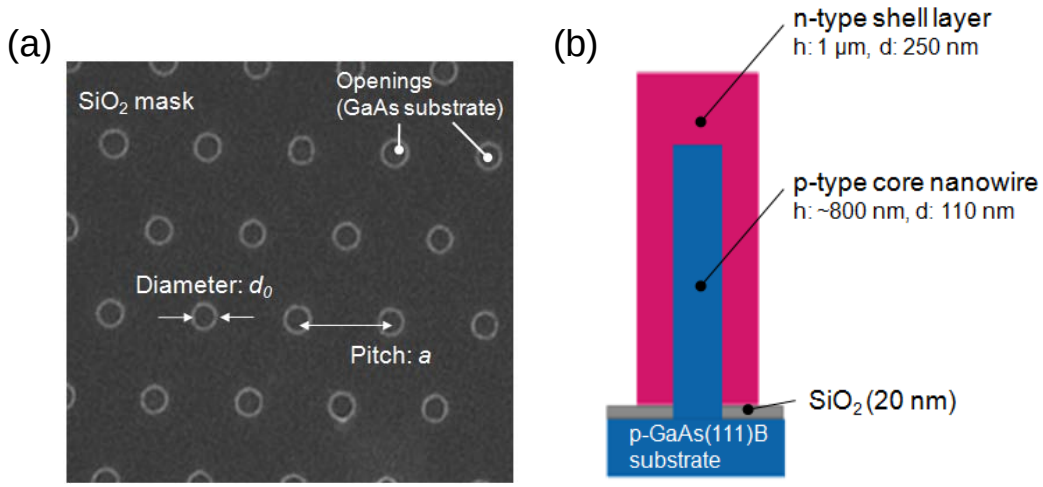

Fig. 4-2 (a) SEM image of masked GaAs(111)B substrate for nanowire growth, and (b) cross-sectional illustration of GaAs core-shell nanowire array solar cells.

4.3 Results and discussion

4.3.1 Optical characterization of GaAs nanowire array and planar structure

Fig. 4-3(a) shows scanning electron microscopy (SEM) image of GaAs core-shell nanowire array. The average height and diameter of core-shell nanowires were about 1 μm and 250 nm, respectively. As the diameter of core GaAs is almost the same to the opening hole diameter (110 nm), the shell thickness was estimated to be about 70 nm in the lateral direction. Surface area of the GaAs nanowire array is 1.0 × 1.0 mm^2, and the geometric fill factor (the fraction of the array area covered by nanowires) was 0.29.

Reflectance is one of the most important issues for solar cell applications, so the reflectance for the perpendicular incident light of the as-grown GaAs nanowire array is measured as shown in Fig. 4-3(b). Without any anti-reflection coating, the planar cell reflects almost half of the incident light.

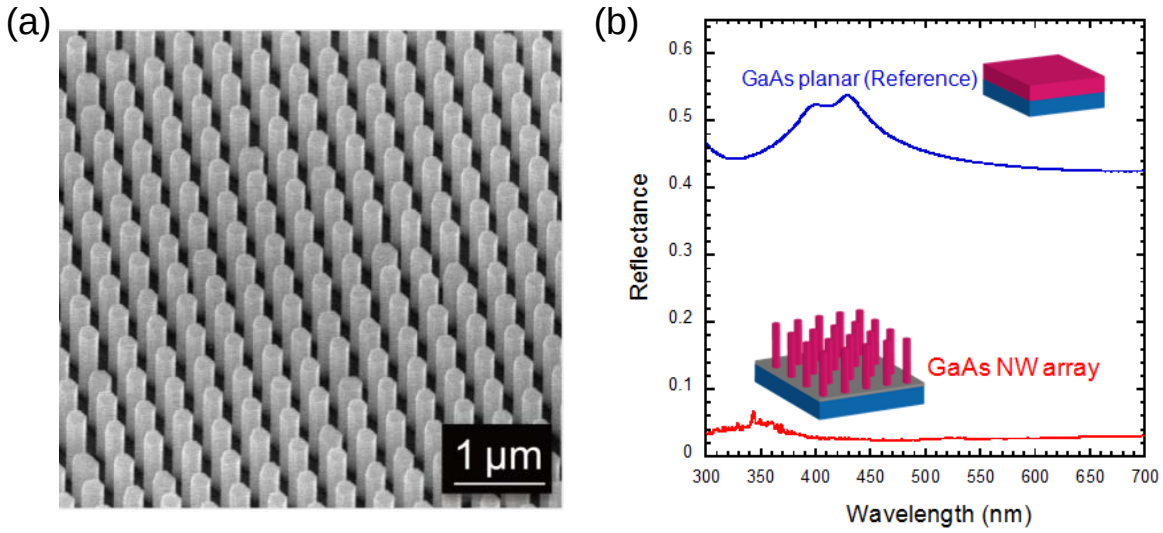

Fig. 4-3 (a) SEM image of GaAs core-shell nanowire array on a p-type GaAs(111)B substrate and (b) measured reflectance spectra of a GaAs nanowire array and a planar GaAs solar cell.

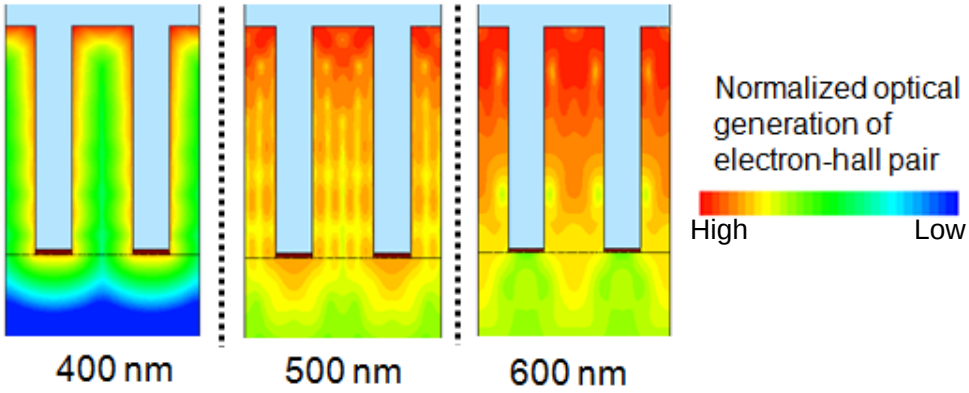

Fig. 4-4 2D simulation analysis of optical generation rate of electron-hole pairs for 400-, 500-, and 600-nm incident light.

The nanowire array, in contrast, reduces reflection less than 5% because absorption is enhanced. The actual measurement of reflectance indicates that nanowire array geometry act as anti-reflection coating in parallel with photoelectric conversion element when the p-n junction is formed in nanowires.

The 2-dimensional optical generation rate of electron-hall pairs in the GaAs nanowire is simulated by using the Sentaurus Device electromagnetic wave (EMW) solver in Fig. 4-4. In this calculation, the parameters such as pitch, diameter and height approximately same with as-grown nanowire array are configured in this study. Most of the shorter-wavelength light (400 nm) is absorbed near the surface because the light absorption coefficient of GaAs is large and almost the all penetration of incident light is occurred in shallow part. On the other hand, the longer-wavelength light (600 nm) is absorbed in the whole of the nanowires because not only incident light but also the diffracted light can be absorbed efficiently with large surface of nanowire array. The 2-dimensional simulation showed that approximately 80% of the perpendicular incident sunlight was absorbed by the wire array, which corresponds to the experimental results in Fig. 4-3(b).

4.3.2 Photovoltaic performance of GaAs core-shell nanowire array solar cells

The device fabrication process is shown schematically in Fig. 4-5. First the space between nanowires was filled, by spin coating, with benzocyclobutene (BCB) resin as a transparent electrical insulating layer. Next, active area is formed by photolithography technique in the middle of nanowire area. Then the uppermost part of this resin layer was removed by reactive ion etching to expose the n-type tips of the nanowires. After the photo-resist is removed, indium-tin-oxide (ITO) for 400 nm thick was deposited by plasma sputtering in Ar/O_2 atmosphere at room temperature and alloying for 15 min at 400 °C as the transparent electrode for the n-type shell. The ITO film transmittance in the visible-light area was about 90%. Finally, a Cr/Au (30/50 nm) electrode was formed on the backside of the substrate by vacuum evaporation. A cross-sectional SEM image of a cleaved array shows the GaAs core-shell nanowires, BCB layer, and the ITO film deposited on top of the nanowires [Fig. 4-6].

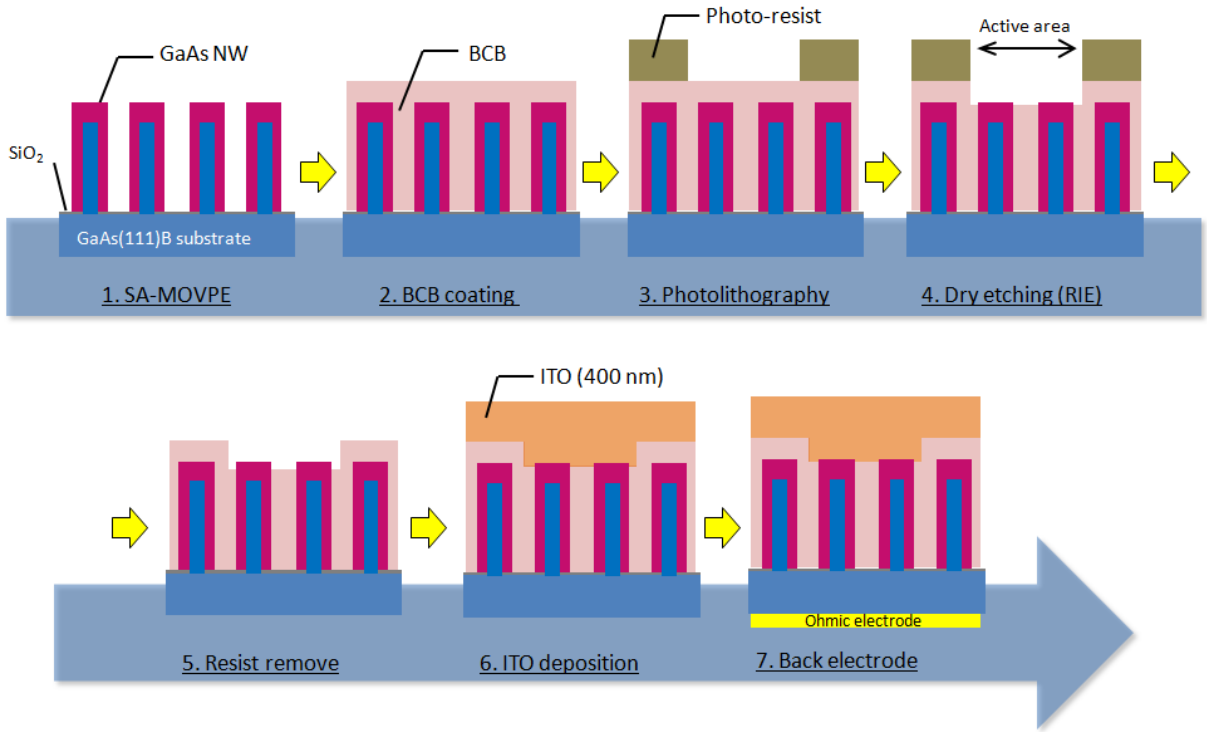

Fig. 4-5 Schematic illustration of the fabrication process for nanowire array solar cell.

The current density-voltage (*J*-*V*) characteristics were measured under AM1.5 global illumination (100 mW/cm^2) at room temperature with the active areas of the cell of approximately 600 × 600 μm^2. Fig. 4-7(a) shows the characteristics of core-shell GaAs nanowire array solar cells. This device exhibited a short-circuit current density J_{SC} of 6.4 mA/cm^2, an open-circuit voltage V_{OC} of 0.25 V, and a fill factor *FF* of 0.45 for an overall efficiency η of 0.71%. This device performance was much lower than that of the best planar GaAs solar cell ever reported [19] and the theoretical limit [20]. The nanowire array solar cell device showed poor diode characteristics (an ideality factor of 3.4). On the other hand, the same nanowire-diode using normal ohmic electrode (Au/Ge/Ni/Au) for an n-type GaAs layer showed good diode characteristics as shown in Fig. 4-7(b) (an ideality factor of 1.31). Large ideality factor (more than 2) is considered that there is additional rectifying junction in the nanowire array solar cell structure. Additionally, a short-circuit current density is only about one-fifth of theoretical limitation of GaAs solar cells despite the low reflectance of the nanowire array. Additional process is needed to solve these issues for obtaining higher efficiency.

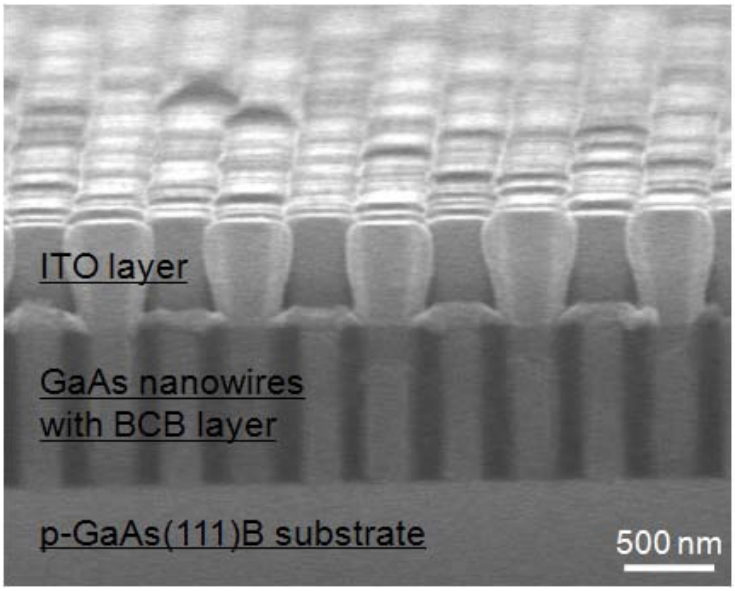

Fig. 4-6 Cross-sectional SEM image of the GaAs core-shell nanowires, BCB layer, and ITO film.

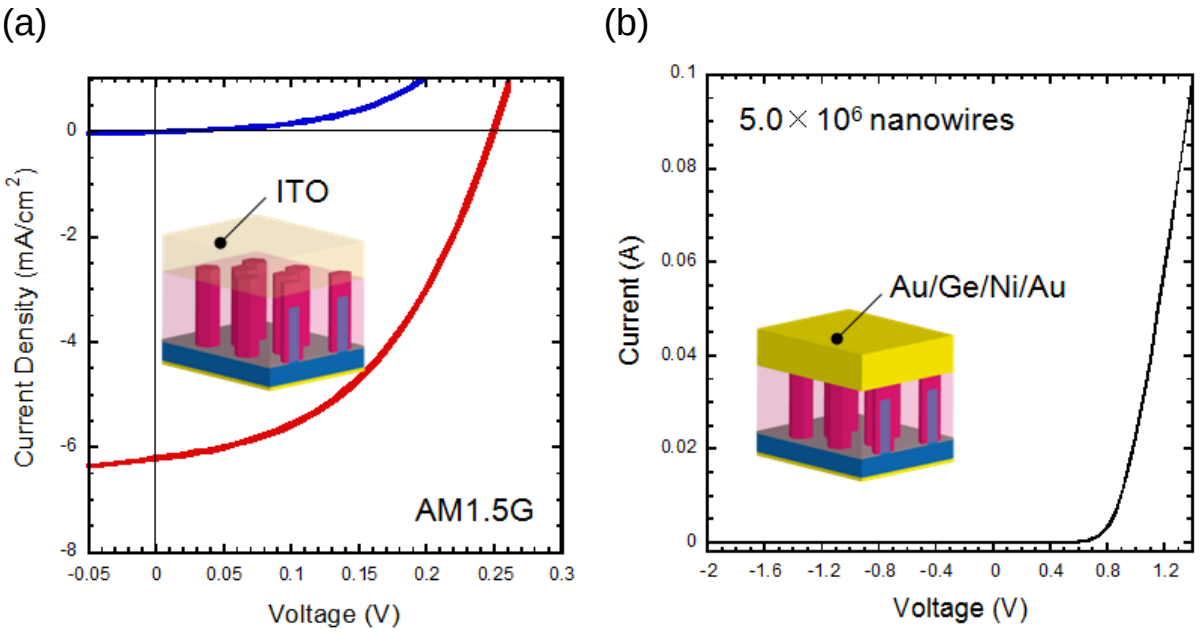

Fig. 4-7 (a) *J-V* characteristics of core-shell nanowire array solar cells under AM1.5G (1 sun) illumination, and (b) that of nanowire array diode structure.

4.3.3 Core-multishell GaAs/InGaP nanowire array solar cells

The bare GaAs nanowire has a lot of surface states. Although the high aspect ratio of a nanowire array reduces reflectance, but the GaAs surface area of a 1-mm-square array structure is about 7 times that of a 1-mm-square planar structure. The large surface area has high density of surface states, in which the short-circuit current density is reduced due to fast recombination velocity. For the passivation layer to reduce surface recombination of GaAs solar cells, various materials with wider bandgaps were reported, such as AlInP [21], AlGaAs [22], and InGaP [23]. The potential barrier should acts like mirror reflecting minority carriers in the valence band of the n-type GaAs shell layer. In the SA-MOVPE process, Trimethylindium (TMIn), TMGa, and tertiarybutylphosphine (TBP) were used to grow an $In_{0.5}Ga_{0.5}P$ layer at

680 °C for the surface passivation layer. The GaAs/InGaP core-multishell nanowire array structure contained an InGaP passivation layer about 5 nm thick.

Furthermore, large ideality factor (larger than 2) is considered that there is additional rectifying junction at heterojunctions or electrode/nanowire junctions. Especially, ITO/nanowire junction is estimated to be the cause of degradation because the diode characteristic with metal ohmic electrode without transparent electrode for n-type shell layer indicates lower number of ideality factor (smaller than 2). There are some reports of high contact resistance between ITO and III-V compound semiconductors and of methods for decreasing that resistance [24,25]. In this study, transparent thin Ti protection layer before sputtering the ITO film to avoid sputtering damage is used formed by vacuum evaporation method. The Ti layer was about 4 nm thick which is enough thin to transparent for sunlight (Fig.4-8).

In addition to these improvements of InGaP passivation layer and Ti/ITO hybrid electrode, a thin p-n junction is designed to obtain a high carrier concentration due to thin depletion layer. But the p-type core nanowire is not estimated to achieve high carrier concentration because it is hard to obtain highly doped zinc when using high-temperature MOVPE [26].

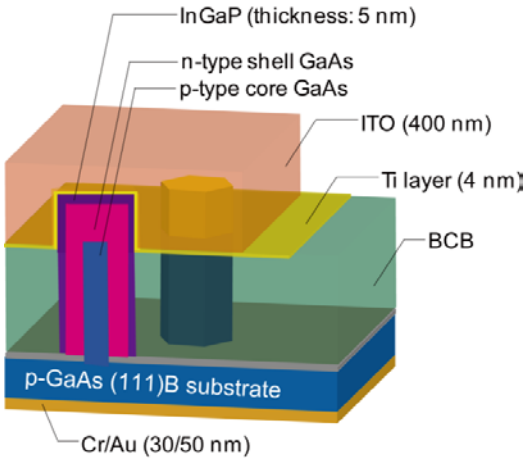

Fig. 4-8 Schematic illustration of GaAs/InGaP core-multishell nanowire-array solar cell structure with thin Ti/ITO hybrid electrode.

When the p-type core doping is low, the nanowire/p-type substrate junction mainly contributes photovoltaic effect over the core-shell junction. It causes low current density because the junction area between nanowire and substrate correspond to openings of masked substrate is small and formed in deep position. Therefore the growth temperature is decreased for p-type core GaAs nanowires from 760 °C to 700 °C and also decreased AsH_3/TMGa partial pressure ratio to enhance the vertical growth rate.

Finally, core-multishell GaAs/InGaP nanowire array solar cells show a J_{SC} of 12.7 mA/cm^2 and a V_{OC} of 0.5 V for an overall efficiency of 4.01% [Fig. 4-9(a)]. Fill factor is also improved from 0.45 to 0.65. Additionally, this device obtained better rectification with ideality factor of 1.48 than that of core-shell GaAs nanowire array solar cells. These additional processes achieved to take photovoltaic property from nanowire solar cells without another rectifying property at interface of transparent electrode and nanowires.

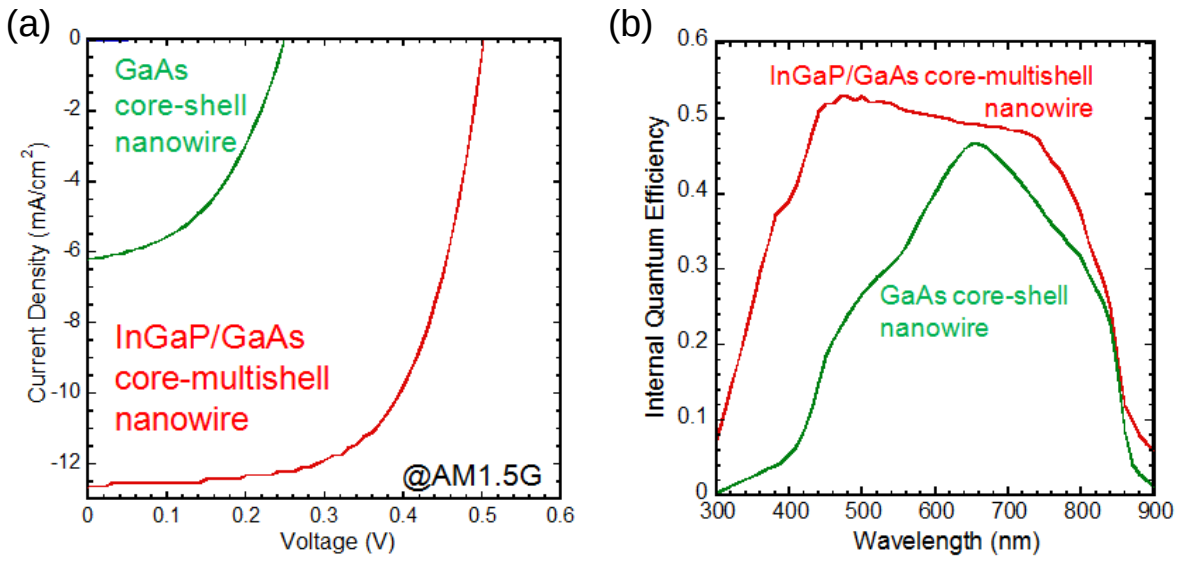

Fig. 4-9 (a) *J-V* characteristics of GaAs/InGaP core-multishell nanowire array solar cells, and (b) internal quantum efficiency comparison with GaAs core-shell nanowire solar cells.

The improved V_{OC} and *FF* are probably due to the lower growth temperature for core nanowires having resulted in a high carrier concentration with the thin depletion layer. Introducing the Ti protection layer decreased series resistance R_S from 8.71 Ω cm^2 for GaAs core-shell nanowire array solar cells to 3.43 Ω cm^2 for GaAs/InGaP core-multishell nanowire array solar cells.

The quantum efficiency properties of nanowire array solar cells are shown in Fig. 4-8. 2-dimensional calculation of optical generation rate of electron-hole pairs [Fig. 4-9(b)] shows that carriers appear near the surface of nanowires in shorter wavelength of incident light, so carrier recombination on the surface of GaAs nanowires is increasing. Therefore quantum efficiency for GaAs core-shell nanowire decreased especially in shorter wavelength area. On the other hand, quantum efficiency for GaAs/InGaP core-multishell nanowire improved by passivation layer because InGaP with wider band gap than GaAs prevents hole from flowing out to the surface. This InGaP passivation layer contributed to enhance J_{SC} and efficiency.

Furthermore, under lower growth temperature for GaAs core nanowire array, degradations of nanowire uniformity were observed. Some parts of adjacent nanowires coalesced with each other and shortening. After the solar cell fabrication process, about 30% of the nanowires remained buried under the BCB layer. Further optimization of the growth conditions is needed to make GaAs/InGaP core-multishell nanowire arrays with uniform structure and obtain higher conversion efficiency. Additionally, the nanowire has the complex geometry with various parameters and the results are dramatically changed by the structure of the device. Structural optimization such as pitch, diameter, height, doping, and position of p-n junction for nanowire array solar cells matched to solar spectrum is needed for achieving higher absorption and conversion efficiency.

4.4 Conclusions

In this study, GaAs core-shell and GaAs/InGaP core-multishell nanowire arrays were grown on p-type GaAs(111)B substrate by using a catalyst-free SA-MOVPE. First, quite low reflectance with well-aligned GaAs nanowire array without any anti-reflection coating was measured. 2-dimensional simulation demonstrated that nanowire structure with 400 nm pitch has the potential for efficient light absorption. GaAs core-shell nanowire array solar cell has some issues such as high surface recombination velocity and poor contact of transparent electrode and GaAs nanowires. Then, the additional process is introduced by using an InGaP passivation layer and a Ti/ITO electrode. Finally, we obtained GaAs/InGaP core-multishell nanowire array solar cells with a fill factor of 0.65 and an efficiency of 4.01%. The InGaP passivation layer improved internal quantum efficiency because it reduced surface recombination. These results demonstrate the potential utility of nanowire array solar cells in photovoltaic applications.

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Chapter 5 InGaAs axial junction nanowire array solar cells

Axial p-i-n junction nanowire solar cells with a position-controlled GaAs-based nanowire array were fabricated by selective-area metal organic vapor phase epitaxy (SA-MOVPE). Measured electron beam induced current (EBIC) signals showed formation of the axial p-i-n junction, which confirms power generation under sunlight illumination. The series resistance of the nanowire solar cells is much higher than that of conventional planar solar cells based on Si or other III–V compound semiconductors. The main difficulty concerning the fabrication of theses nanowire solar cells is degradation of series resistance between the GaAs-based nanowires and the indium-tin-oxide (ITO) deposited as a transparent electrode. The series resistance of the fabricated GaAs-based nanowire solar cells was reduced by introducing the tin-pulsed doping of the contact layer between the ITO and nanowire-array. As a result of this improved process, fabricated solar cells exhibited an open-circuit voltage of 0.544 V, short-circuit current of 18.2 mA/cm^2, and fill factor of 0.721 for an overall conversion efficiency of 7.14% under AM1.5G illumination. The series resistance of the solar cells could be decreased to 0.132 $\Omega \cdot cm^2$, which is one order of magnitude lower than that of the solar cells without highly doped contact layer. This reduced series resistance indicates that nanostructure solar cells with transparent electrodes and multi-junction nanowire solar cells with higher efficiency can be fabricated on a commercial basis in the near future. These results were published in 2015 [1].

5.1 Introduction

Previous chapter indicates the fabrication process for GaAs-based nanowire array solar cells. A core-shell nanowire solar cell structure is expected to effectively collect photogenerated electrons and holes across the entire junction area because the p-n junctions are aligned parallel to the incident light, and actual GaAs/InGaP core-multishell nanowire array solar cells shows the photovoltaic effect. Recently, some reports about free-standing nanowire array solar cell have been published using free-standing GaAs nanowire and nanowire array [2-4] and InP nanowire array [5-7]. Additionally, axial-junction nanowires are also published [8-11] in recent. This structure has the potential to form heterojunctions with lattice-mismatched materials because of their small footprints [12]. For next-generation solar cells, namely, high-efficiency multi-junction solar cells, lattice-mismatched heterojunctions must be grown [13]. In particular, an nanowire solar cell composed of four junctions, namely, $In_{0.3}Ga_{0.7}P$ (2.0 eV), $Al_{0.1}Ga_{0.9}As$ (1.5 eV), $In_{0.2}Ga_{0.8}As$ (1.1 eV), and $In_{0.5}Ga_{0.5}As$ (0.7 eV), can achieve a conversion efficiency above 50% [14] elucidates in next chapter. As for next-generation photovoltaic applications, it is therefore imperative to fabricate axial-junction nanowire-array solar cells with GaAs-based materials.

GaAs-based ternary alloy materials are often used for multi-junction solar cells for middle cells. Previous study indicates that InGaAs nanowires on GaAs(111)B substrate with a lattice mismatch of 2.1% can be grown coherently without misfit dislocations by catalyst-free SA-MOVPE [15]. In this study, an InGaAs axial-junction nanowire-array solar cell with an AlInP passivation layer is experimentally fabricated.

5.2 Experimental procedure

As the first step in the nanowire fabrication process, a 20-nm-thick SiO_2 mask was deposited on a GaAs(111)B substrate, and hexagonal openings were formed by electron beam lithography and wet chemical etching. Periodical openings, with an average diameter d_0 of 220 nm, were formed in 2.0 × 2.0 mm^2 regions on the substrate. InGaAs nanowires were grown in a horizontal MOVPE system operating at 0.1 atm [16,17]. Trimethylindium (TMIn), trimethylgallium (TMGa), and arsine (AsH_3) were used as source materials, and diethylzinc (DEZn) and monosilane (SiH_4) were used as p- and n-type dopant sources, respectively. The partial pressures of TMIn, TMGa, and AsH_3 were respectively 1.8×10^{-6}, 6.9×10^{-7}, and 1.0×10^{-4}. Prior to the nanowire growth, thermal cleaning was carried out at 680 ˚C in an AsH_3/H_2 atmosphere to remove the native oxide from the mask openings. InGaAs nanowires were grown epitaxially at 730 ˚C at a V/III pressure ratio of 115. The target composition ratio of indium is about 20%, which corresponds to a bandgap of 1.1 eV. The p-n junction was designed such that its depth was about 150 nm from the top of the nanowire tips. Then, a thin $Al_{0.1}In_{0.9}P$ passivation layer [18,19] (~ 10 nm) was formed laterally at 570 ˚C with a gas mixture of trimethylaluminum (TMAl), TMIn, and tertiarybutylphosphine (TBP) to reduce surface recombination.

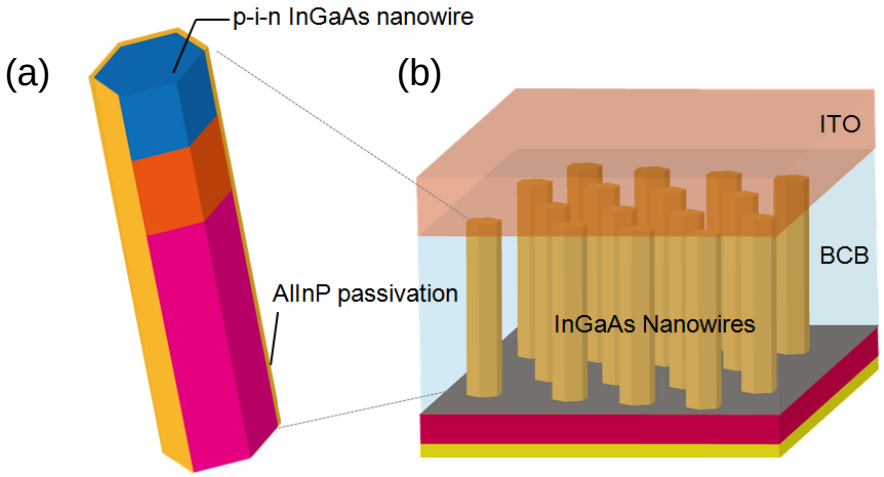

Fig. 5-1 (a) Schematic illustration of InGaAs axial junction with AlInP layer, and (b) schematic illustration of InGaAs nanowire array solar cells.

The fabrication processes for the axial p-i-n junction nanowire solar cells were almost the same as fabrication process for GaAs/InGaP core-multishell nanowire-array solar cells [20] described previous chapter. After the nanowires were grown, the space between them was filled with a transparent resin, called BCB (Dow Chemical CYCLOTENE 3022-35), to form an electrical separation layer by spin coating. Next, the top of the BCB was removed by reactive ion etching with CF_4/O_2 in the active area. After that, a thin-film titanium layer (4 nm) and a transparent indium-tin oxide (ITO) film electrode (400 nm) were deposited on the top surfaces of the nanowires by vacuum evaporation and plasma sputtering. Finally, an ohmic electrode was formed on the back surface of the substrate by vacuum evaporation.

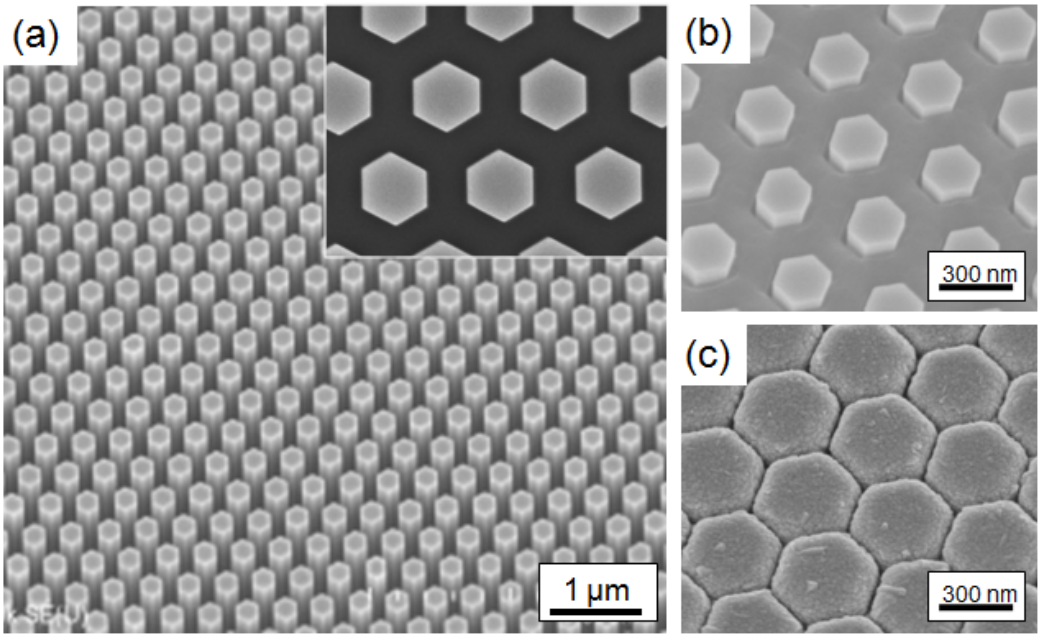

Fig. 5-2 (a) 30˚- and 0˚- (inset) tilted SEM images of an InGaAs nanowire array with an axial p-i-n junction. (b) SEM image of the tips of nanowires after reactive ion etching and (c) deposition of ITO electrode.

5.3 Results and discussion

5.3.1 InGaAs axial-junction nanowire array solar cells

A 30°-tilted scanning electron microscopy (SEM) image of an InGaAs nanowire array fabricated without using a tin-doped layer is shown in Fig. 5-2(a). A uniform array of vertically aligned nanowires are grown on a GaAs(111)B substrate, and the sidewalls of the hexagonal nanowires are {–110} facet surfaces vertical to the substrate. The average height and diameter of the nanowires are about 1.10 μm and 225 nm, respectively. Since the diameter of the as-grown nanowires is the same as that of the opening holes, it can be considered that the nanowires were completely grown vertically without any growth in the lateral direction. After BCB spin coating to bury the nanowires and succeeding reactive-ion etching, the tips of the nanowires were exposed by about 100 nm, and the sputtered ITO film was deposited on the nanowire array, as shown in Figs. 5-2(b) and 5-2(c). The dome-shaped ITO works as a "nanolens," which concentrates the incident sunlight efficiently onto the nanowire-array structure [21].

First, the formation of the p-i-n junction was confirmed by measuring the electron-beam-induced current (EBIC). By scanning over the sample from the direction perpendicular to the nanowire axis, the electron beam was irradiated on the cleaved surface of the device to form electron-hole pairs. As a result, minority carriers diffuse across the depletion region and produce a current. A cross-sectional SEM image with the measured EBIC signals superposed, taken at an electron acceleration voltage of 1.0 kV, is shown in Fig. 5-3(a), and the EBIC line profile is shown in Fig. 5-4(b). These EBIC measurements indicate that the dopants of both the p- and n-type layers are successfully activated and that the axial p-i-n junction works as an active photovoltaic component.

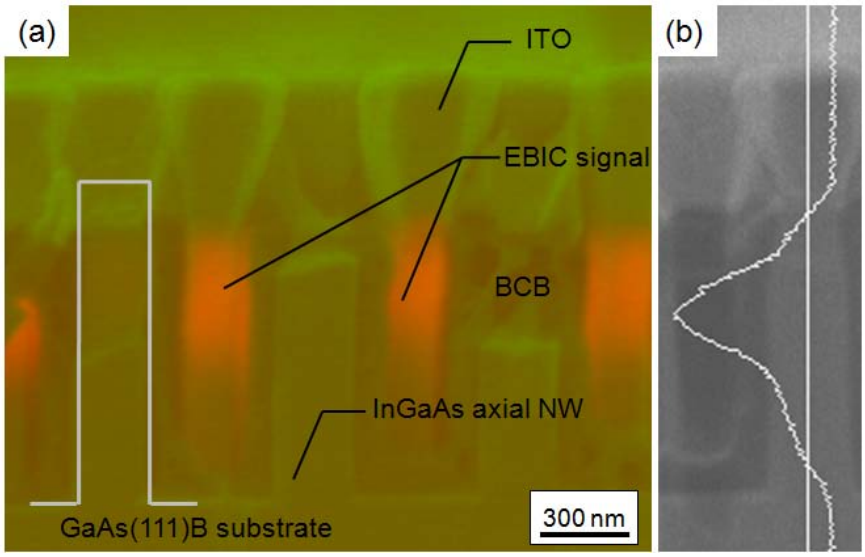

Fig. 5-3 (a) Cross-sectional SEM image superposed with EBIC signals and (b) line profile of InGaAs axial-junction nanowire-array solar cells.

Next, the quantum efficiency and reflectance properties of the fabricated nanowire solar cell with a pitch of 600 nm on p-GaAs(111)B substrate are shown in Fig. 5-4(a). Previous work showed that most of the light with a wavelength shorter than the pitch of the nanowires is reflected or absorbed near the surface of the solar cell, and the light with a longer wavelength is absorbed by the wire array, as calculated using an electromagnetic wave (EMW) solver [20]. Consequently, the nanowire-array solar cells with a pitch of 600 nm can absorb solar light efficiently in spite of a small geometric fill factor of 14% (the ratio of the footprint area of the nanowires to the cell area). The average reflectance of the solar cell with the pitch of 600 nm was 9.53% in the wavelength range from 300 to 1200 nm. The absorption edge of quantum efficiency indicates that the indium composition of the InGaAs nanowire is about 0.25, which is almost the same as the target of this study.

The photovoltaic performance of the fabricated nanowire solar cells was measured under AM1.5G (1 sun) illumination, the radiation intensity of which was

calibrated using a standard silicon photodiode (Bunkoukeiki BS-500). The current density-voltage (*J*-*V*) characteristics of the InGaAs axial p-i-n junction nanowire-array solar cells with AlInP passivation are shown in Fig. 5-4(b). The nanowire solar cell with a pitch of 600 nm on a p-type GaAs (111)B (carrier concentration: ~ 5.0×10^{18} cm^{-3}) substrate has an active area of 0.9×0.9 mm^2 containing about six million nanowires and exhibits a short-circuit current density of 17.0 mA/cm^2, an open-circuit voltage of 0.468 V, and a fill factor of 0.585 for an overall efficiency of 4.66%. Calculated from the *J*-*V* characteristics of the device, the ideality factor and series resistance are respectively 1.46 and 4.72 $\Omega \cdot cm^2$. In particular, the series resistance of the nanowire solar cell is much higher than that of conventional solar cells.

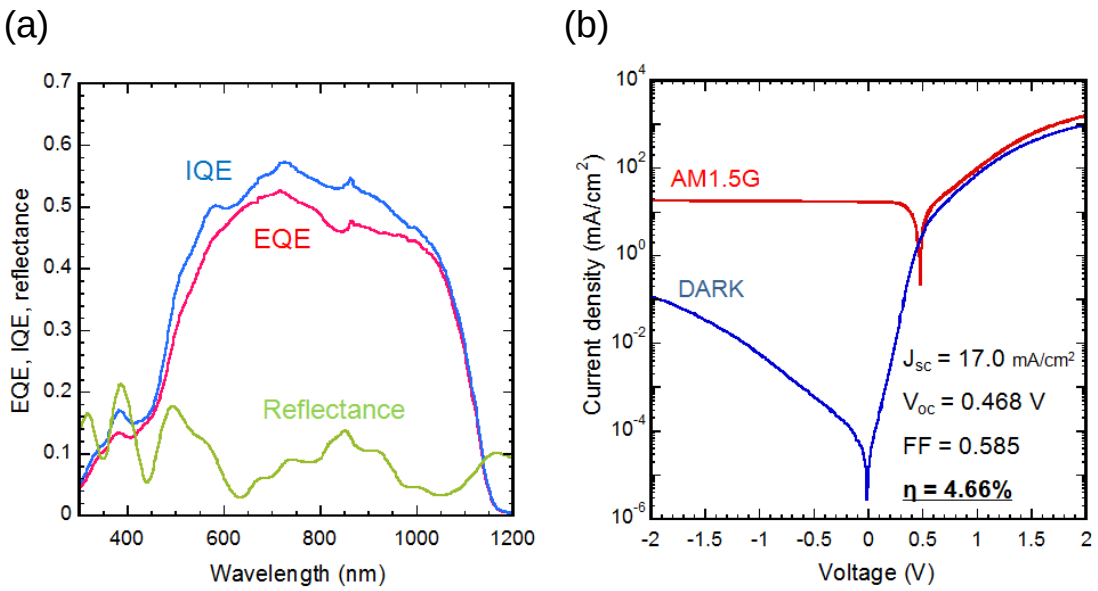

Fig. 5-4 (a) Measured external quantum efficiency (EQE), internal quantum efficiency (IQE), and reflectance and (b) *J*-*V* characteristics under AM1.5G (1 sun) illumination and dark condition of InGaAs axial-junction nanowire-array solar cells on p-type GaAs(111)B substrate with a pitch of 600 nm.

5.3.2 InGaAs nanowire array solar cells with tin-doped contact layer

To achieve low resistance and high conversion efficiency of InGaAs nanowire solar cells, highly doped contact layer between ITO and InGaAs nanowire must be introduced. Therefore, prior to laterally growing the AlInP window layer, a highly doped contact layer was formed on the top of the nanowires. However, it is difficult to obtain high-doping-concentration condition by using silicon dopants for nanowire growth [22-24]. A heavily doped contact layer was therefore formed by using tin as dopant to reduce the contact resistance between nanowire and ITO electrode [25]. Using tin is also expected to lower contact resistance because it is one of components of ITO (In_2O_3+SnO_2).

The same patterning mask as mentioned in the previous section was fabricated on a p-type GaAs(111)B substrate, and a p-i-n nanowire structure was grown using an MOCVD system. An n^+ contact layer with tetraethyltin (TESn) and finally an AlInP window layer was formed, as shown in Fig 5-5(a).

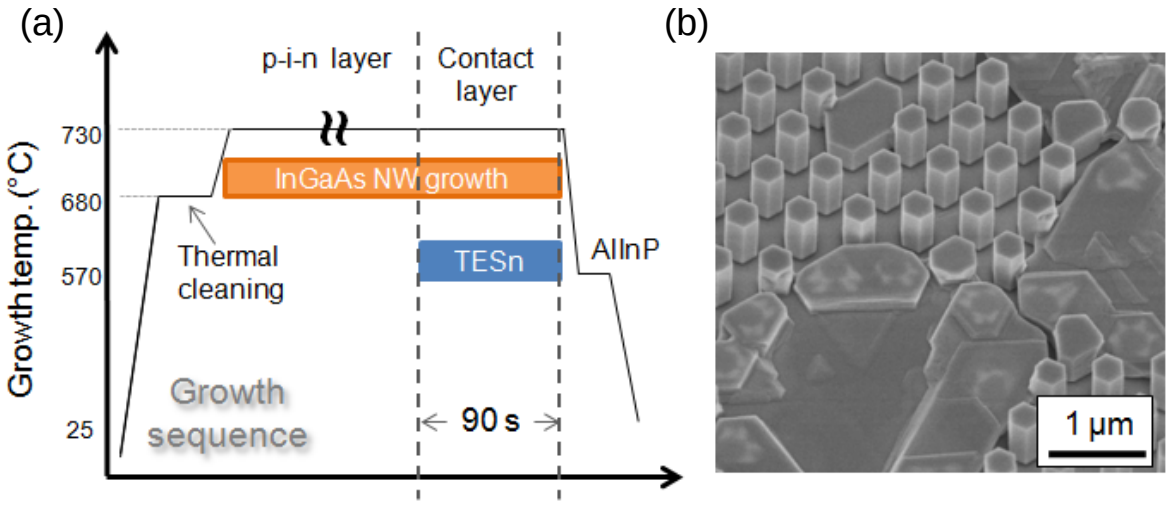

Fig. 5-5 (a) Growth sequence of InGaAs p-i-n junction nanowire with TESn and (b) SEM image of as-grown nanowire with enhanced lateral growth and coalescing.

The thicknesses of the p-i-n layers were chosen as 800, 150, and 150 nm to obtain a depletion layer at almost the same depth as the InGaAs nanowire solar cells reported above. Here, the partial pressure of TESn in the reactor was 6.3×10^{-10} atm when the temperature of the bubbler was –15˚C. However, the results indicate that the nanowires were grown highly laterally and coalesced with adjacent nanowires under the heavily doping condition [Fig. 5-5(b)]. The height of the coreless nanowires is much lower than that of normal nanowires; consequently, some of the nanowires were buried between the BCB layer after the excess overlaid resin etching process by reactive-ion etching. To fabricate the nanowire array solar cells structure, high-uniformity nanowires and a high-quality ITO electrode (in which all the nanowires are isolated from each other and contact of ITO electrode electrically) must be formed. Although TESn partial pressure is as low as possible, tin dopant has strong effect on the nanowire growth mode, and growth rate [26,27]. Hence, pulse doping was used to further decrease the practical IV/III ratio [28]. TESn was supplied for 1 s during non-doped InGaAs growth for 6 s. That sequence was repeated 15 times, as shown in Fig. 5-6(a).

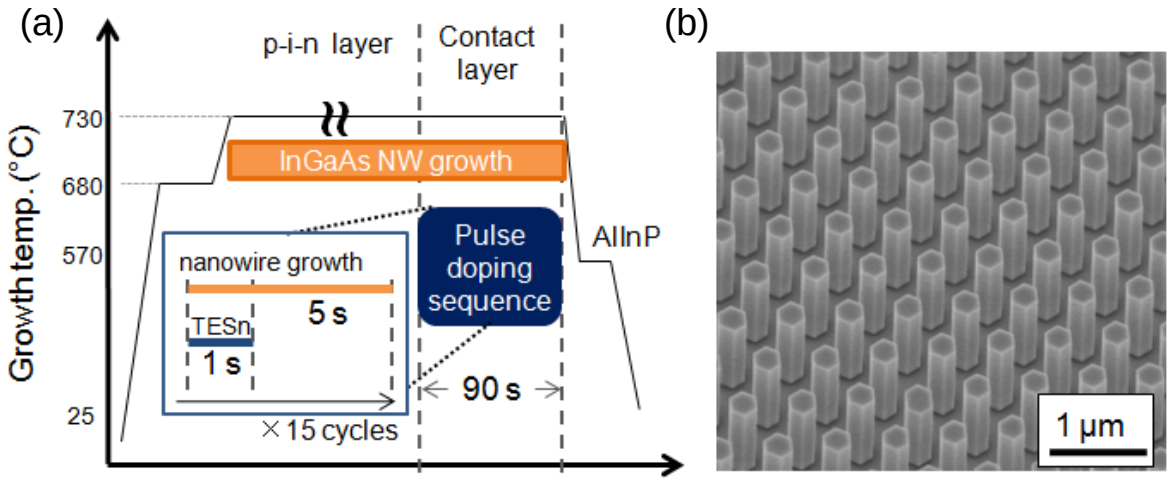

Fig. 5-6 (a) Growth sequence of the nanowire array with pulse doping of TESn and (b) SEM image of the nanowire array.

As a result of using this pulse-doping technique, lateral growth and coalescing of the nanowires was suppressed, especially in the solar cell with pitch of 600 nm [Fig. 5(b)], and highly doped n-type nanowires were obtained. The thickness of the n^+ contact layer was estimated to be 30 nm. The proposed nanowire array was used to fabricate solar cells with a similar sequence to one previously reported. A Cr/Au (30/50 nm) electrode was deposited on the backside of the substrate by vacuum evaporation.

As a result, uniform InGaAs p-i-n axial-junction nanowire-array solar cells with a tin-doped n^+ contact layer on the p-type GaAs substrate were obtained. The *J-V* characteristics of InGaAs nanowire-array solar cells with and without a tin-doped contact layer are shown in Fig. 5-7. The fabricated solar cells showed a series resistance of 0.132 $\Omega \cdot cm^2$, which is one order of magnitude lower than that of the previous one.

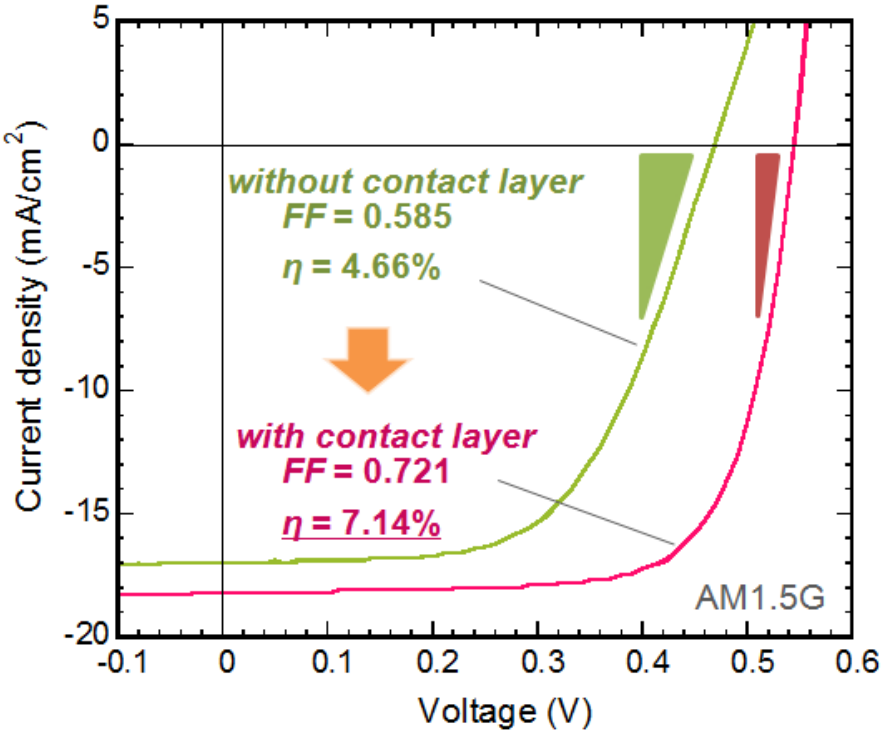

Fig. 5-7 *J-V* characteristic of InGaAs nanowire-array solar cells with and without pulse doping of TESn for n-type highly tin-doped layer.

The current density did not change substantially, but the fill factor and open-circuit voltage increased to 0.721 and 0.544 V, respectively. The resistances of the nanowire itself and electrode also did not change, indicating that the contact resistance between the Ti/ITO electrode and the nanowires decreased owing to the use of the highly tin-doped contact layer. This was also expected to lower the contact resistance with tin as a component of ITO (In_2O_3+SnO_2). Compared with the open-circuit voltage of previously reported nanowire-array solar cells based on GaAs, which was only 50% of the theoretical limitation [29], the above-mentioned method produced an open-circuit voltage of nearly 80% and realized a conversion efficiency of 7.14% with a geometric fill factor of 14%.

Compared with the quantum efficiency of previously reported InGaAs or Si solar cells (which have similar band gaps), that of the present InGaAs nanowire-array solar cell is low, so its short-circuit current density is also low [30-32]. As indicated in other papers about nanowire-array solar cells, the diameter and height of the nanowires, as well as the depth of the junction, affect the solar cell performance significantly; accordingly, the authors believe that it is possible to increase the conversion efficiency by optimizing the nanowire-array solar cell structure.

5.4 Conclusions

InGaAs p-i-n junction nanowire array solar cells with an AlInP passivation layer were fabricated by SA-MOVPE. From EBIC measurements, the nanowires were determinate to have an axial junction and work as active photovoltaic components. An solar cell with an InGaAs nanowire array with a height of 1.1 μm and a diameter of 225 nm showed a fill factor of 0.585 and a conversion efficiency of 4.66% under AM1.5G illumination with about six million nanowires, although it had a higher contact resistance between the ITO and the nanowires than conventional reference cells. The contact resistance was reduced by introducing a tin-doped high-carrier-concentration layer between the ITO and the nanowires. Although continuous tin impurity doping during nanowire growth increased the growth rate in the lateral direction and deteriorated the nanowire uniformity, pulse doping of TESn produced an appropriate contact layer grown axially with highly uniform nanowires. The fabricated solar cell exhibited a short-circuit current density of 18.2 mA/cm^2, an open-circuit voltage of 0.544 V, and a fill factor of 0.721 for an overall conversion efficiency of 7.14%. Its series resistance was 0.132 $\Omega \cdot cm^2$, which is much lower than that of an solar cell without a tin contact layer. This approach for fabricating GaAs-based nanowire array solar cells is expected to provide the required low resistance contact layer and tunnel junctions for high-efficiency tandem nanowire array solar cells.

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Chapter 6 Future prospects for nanowire solar cells

Numerous reports about nanowire-array solar cells have been published recently, and this study has also reported III-V material nanowire array solar cells. However, the use of expensive III-V materials and complicated fabrication process raise the production cost, which impedes the upcoming widespread commercialization for application of nanowire array solar cells. Therefore, transferring the nanowire array to an inexpensive foreign substrate is of great importance to the development of nanowire array solar cells. In this technique, the amount of materials used to fabricate nanowire array solar cells can be reduced with reusing the masked substrate for the nanowire array growth. Furthermore, the peeled-off nanowire array is lightweight and flexible. This characteristic enables the wide application of the solar cells.

Next, the approach to higher conversion efficiency of solar cells is suggested. The nanometer-scale footprint of the nanowire allows lattice-mismatched material to be stacked on each other without additional buffer layer or introducing lattice misfit dislocations. Then, for the higher efficiency of next-generation structures for the solar cells, this study proposes the four-junction nanowire array solar cells with lattice mismatch materials.

6.1 Fabrication of flexible cells and reuse the substrates for the nanowire growth

The masked substrate for the nanowire growth was fabricated by deposition of SiO_2 layer and electron beam lithography, so it has a lot of process before the nanowire growth and takes high cost for fabrication. To solve this issue, related studies indicate some ways to peel off the nanowire part from masked substrate [1]. For example, after the growth of well-aligned nanowire array, the transparent resin is deposited onto the nanowire array. This device is fixed to the supporting substrate and peeled off from the growth substrate by the difference of thermal contractility of growth substrate and transparent resin. Thin-film structure of nanowire part can be used for light weight and flexible cells. At the same time, the remaining substrate after the peeling off process can be reused for the nanowire growth. After the peeling off process, nanowire stubs in the openings are easily removed by wet chemical etching. Figs. 6-1(a) and (b) show that the SEM image of re-growth nanowire array is almost the same with the first growth of nanowire array. This potential for reuse substrate and re-growth can be said to reduce the number of fabrication process and fabrication cost.

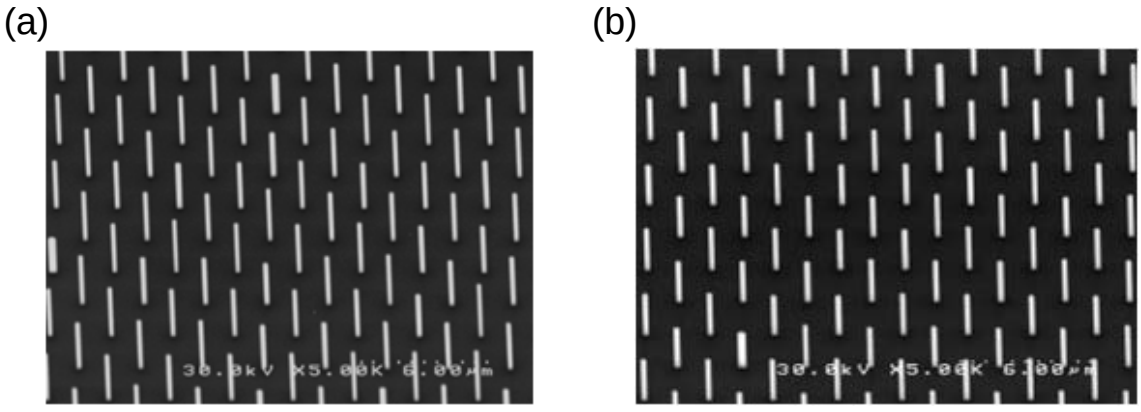


Fig. 6-1 (a) SEM image of nanowire array on substrate, (b) SEM image of re-growth nanowires on reused substrate. [1]

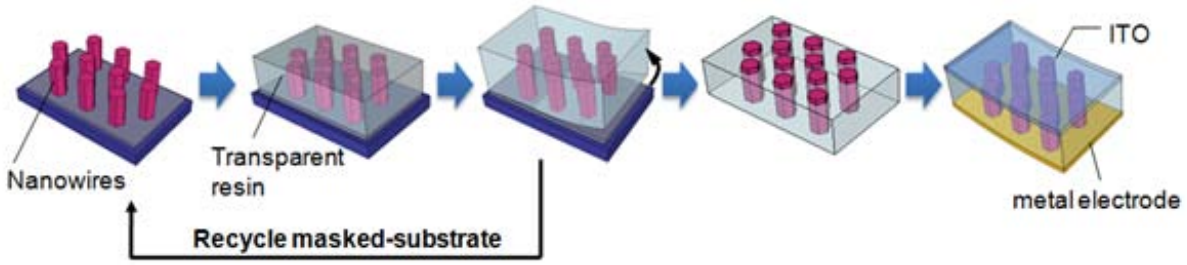


Fig. 6-2 Schematic illustration of fabrication process for flexible cells using nanowire array and reusing masked substrate for nanowire growth.

Actual peeled-off nanowire array photovoltaic cells on low-cost and flexible substrates were demonstrated by Z. Fan *et. al* in 2009 with CdTe/CdS structure [2]. In 2015, flexible structure [3] using p-InP/ITO heterojunction nanowire array is reported [4]. After growth, the nanowire array was embedded in polydimethylsiloxane (PDMS) [5] and peeled off from the original substrate. The PDMS membranes embedded with nanowires were peeled off with tweezers. Then the PDMS film is etched by RIE to expose the nanowire tips. Finally, 200-nm AuZn film is evaporated onto the back side of the PDMS film [Fig. 6-2]. A image of the PDMS membranes after peel-off is shown in Fig. 6-3(a), and Fig. 6-3(b) shows a 30 °-tilted SEM image of the exposed nanowire tips. This result shows that the nanowires remain their orientation with respect to each other also in the PDMS layer after the process of peeling off.

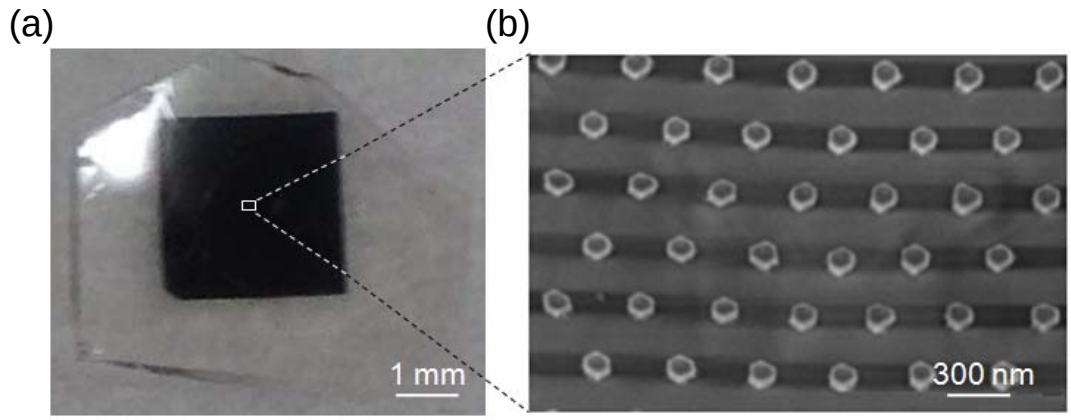


Fig. 6-3 (a) Photograph of peeled off PDMS film with embedded nanowires, and (b) SEM image of nanowire array embedded in PDMS after RIE. [3]

After the PDMS was peeled off from the substrate, the transmittance of the nanowire array is increased [Fig. 6-4(a)] because the geometric fill factor of this nanowire is very small and incident light pass through between nanowires. Then a 200-nm AuZn is formed not only for ohmic contact but also for enhancement layer of light trapping effect contact onto the nanowire array in order to achieve flexible nanowire array solar cells. AuZn contact blocked the light which resulted in transmittance decrease in all wavelength regions. We can conclude the AuZn electrode increased the effective optical path length and then the results of the absorption of peeled-off nanowire array shows 82.7% [Fig. 6-4(b)]. Flexible thin-film solar cells with nanowire array can absorb the incident light efficiently in a few micro-meters of thickness. These results revealed that the nanowire array structure have superiority for the fabrication of resource saving cells.

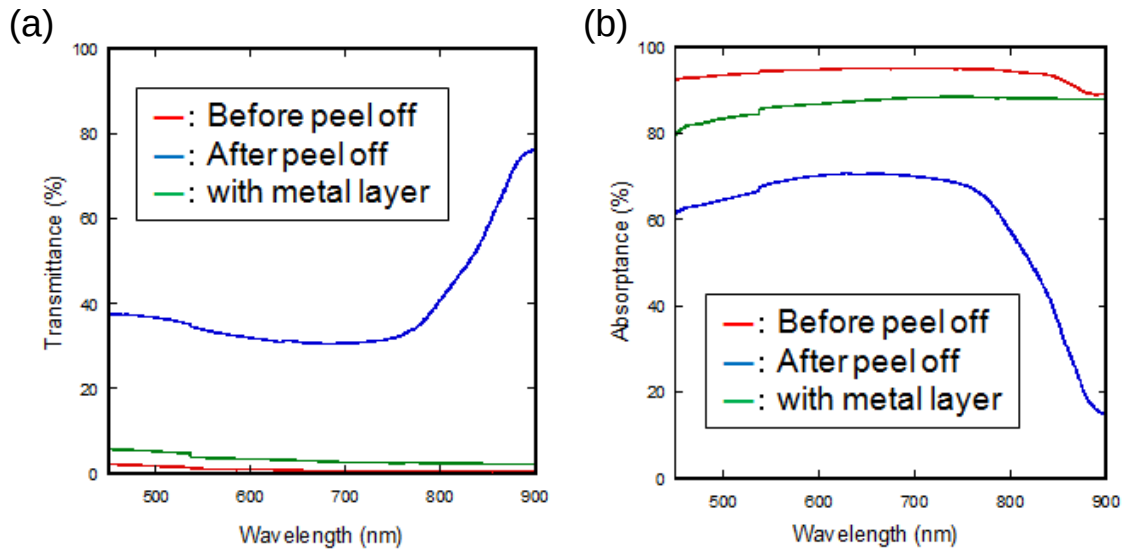


Fig. 6-4 (a) Measured transmittance of InP nanowire arrays at three different states such as before peel off, after peel off and with metal layer, and (b) absorption of InP nanowire array calculated from measured reflectance and transmittance. [3]

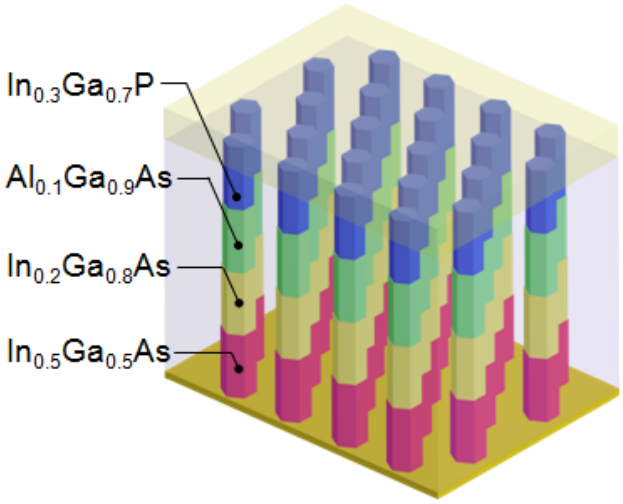
6.2 Multi-junction nanowire solar cells

Up to now, the highest solar cell efficiency in three-junction solar cell is reported by Sharp Corporation with 44.4% conversion efficiency under concentration of 302 suns such as InGaP/GaAs/InGaAs [6]. And also, four-junction solar cell with 44.7% efficiency at a concentration of 297 suns was made by Soitec in 2013 [7]. However, conversion efficiency of multi-junction solar cells is increasing only a few tenth of a percent with each passing year [8], and technical breakthrough such as new technology and design is expected for solving the problem of lattice-mismatch of connected materials. In this back ground of tandem solar cells, axial junction of nanowires with lattice-mismatch materials is an important building block for multi-junction solar cells with three or more junctions [9,10]. With the advantage of nanowires described in the previous section, hetero-junction structure with lattice mismatch can be obtained because of its small diameter [11]. For instance, a group of Lund University have grown dual junction InP nanowires on Si substrate and achieved to increase V_{OC} by 67% compared to single junction InP nanowire array solar cell [12]. This result reveals that III-V compound semiconductor nanowire solar cell with axial p-n junction can be applied to multi-junction solar cells using tunnel junction within the nanowire structure.

Additionally, remarkable design of GaAs-based multi-junction nanowire array solar cells with highly lattice mismatched materials has been proposed [13]. Good quality axial junction nanowires can be formed despite high lattice mismatched, for example, no threading dislocation is formed in about 200-nm diameter with as much as 3% lattice mismatch. This is an important advantage for tandem nanowire array solar cells for higher efficiency than existing planar structure. Alternative to existent cells, four-junction nanowire array solar cells of $In_{0.3}Ga_{0.7}P$ /$Al_{0.1}Ga_{0.9}As$ /$In_{0.2}Ga_{0.8}As$ /$In_{0.5}Ga_{0.5}As$ have been proposed [Fig. 6-5(a)] and this study aims to realize these structure. Nanowire solar cells with stacked structure in the axial direction has the

almost the same electrical generation mechanism with the traditional multi-junction solar cells where the solar light can pass from materials with larger bandgap to lower bandgap materials. This design of tandem nanowire array solar cells has 2.0, 1.5, 1.1, 0.7 eV bandgap respectively, and the combination of these bandgap has the potential for achieving 55.3% conversion efficiency under AM1.5 global illumination [14] [Fig. 6-5(b)]. The combination of peeling off technique and stacking technique of lattice mismatched materials with nanowire array structure can reduced the amount of materials to approximately 0.1% of that for existent solar cells. Therefore, nanowire array solar cells can be used as resource-saving solar cells in the future.

(a)



(b)

	Material	Band gap (eV)	Lattice constant (Å)	Lattice mismatch (%)
1st	$In_{0.3}Ga_{0.7}P$	2.0	5.594	—
2nd	$Al_{0.1}Ga_{0.9}As$	1.5	5.654	1.1
3rd	$In_{0.2}Ga_{0.8}As$	1.1	5.738	1.5
4th	$In_{0.5}Ga_{0.5}As$	0.7	5.868	2.3

Fig. 6-5 (a) Schematic illustration of four-junction nanowire array solar cells , and (b) values of bandgap, lattice constant, and lattice mismatch between connected materials of each cells. [13]

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Chapter 7 Summary and conclusions

In this study, vertically aligned GaAs core-shell and core-multishell nanowire array solar cells by selective-area metal organic vapor phase epitaxy (SA-MOVPE) are demonstrated. Additionally, for the tandem axial junction nanowire array solar cells, photovoltaic application of InGaAs axial p-n junction nanowire is demonstrated. Finally, peeling-off technique and 4-junction nanowire array solar cells are suggested. Summary, conclusions and future prospects of the present work are the following.

7.1 Summary

In chapter 4, GaAs core-shell nanowire array solar cell by catalyst-free SA-MOVPE is investigated. The actual reflectance measurement of the nanowire array without any anti-reflection coating showed much lower reflection than that of planar structure. Additionally, the 2-dimensional simulation shows the more than 80% of the incident sunlight was absorbed by the wire array. This device exhibited a conversion efficiency η of 0.71%. There is photovoltaic performance degradation because of a high surface recombination rate of photo generated carriers and poor ohmic contact between the GaAs nanowires and transparent ITO electrode. Finally, InGaP passivation and contact layer for GaAs nanowire solar cells is introduced for solving these problems. This GaAs/InGaP core-multishell nanowire array solar cells shows a fill factor of 0.65 and a conversion efficiency of 4.01%.

In chapter 5, InGaAs p-i-n axial junction nanowire array solar cells with an AlInP passivation layer are investigated. EBIC measurements show the axial junctions of nanowires and array works as active photovoltaic component. This cell exhibits a short-circuit current density of 17.0 mA/cm^2, an open-circuit voltage of 0.468 V, and a fill factor of 0.585 for an overall efficiency of 4.66% with 1.10-μm-height and 225-nm-diameter. To achieve lower series resistance of the device, TESn source is used for n-type highly doping layer. Although continuous tin impurity doping during nanowire growth deteriorated the nanowire uniformity, pulse doping produced an appropriate contact layer in axial direction with uniform nanowires. The device with the tin-doped contact layer shows a short-circuit current density of 18.2 mA/cm^2, an open-circuit voltage of 0.544 V, and a fill factor of 0.721 for an overall conversion efficiency of 7.14%.

In chapter 6, related reports about new technology and idea of nanowire array solar cells are described. First, the peeling-off technique, reuse of substrates for nanowire growth and optical properties of nanowire array solar cell structure are investigated. The sample with the substrate showed high average absorption, but optical property degraded when the nanowire array is peeled off from the substrate. On the other hand, after the metal electrode is deposited on the back side of the nanowire array, the absorption increased because this metal layer increas the effective optical path length of longer wavelength light. This technique is expected to be a new approach for lower cost photovoltaic cell compared with conventional cell. Finally, the idea of tandem structure using nanowire array solar cells is described. GaAs-based four-junction nanowire array solar cells with lattice-mismatched materials have the potential for achieving over 50% conversion efficiency under AM1.5 global illumination.

7.2 Outlook for nanowire solar cells

From the early 1960s, the research of semiconductor nanowires has been studied for over half a century ago, and attracted much attention as promising materials for future device applications. In 2000s, the research of semiconductor nanowires is dramatically moving from fundamental phase to actual fabrication phase. In this context, application for photovoltaic cell is also dramatically accelerating in recent years. The advantages of nanowire and nanowire array discussed in previous chapter are promising for next generation photovoltaic cells requiring low cost and high efficiency. In the case of GaAs-based materials, most papers, however, demonstrated solar cell applications using only one nanowire or randomly grown nanowires, and could not shows superiority of this structure. In this situation, this work demonstrates the photovoltaic cell using position-controlled GaAs-based nanowire array and their architectural effects.

Additionally, in the near future, next generation solar cell is required to achieve low cost and high efficiency compared with existing cells. In this study, we demonstrate some approaches for achieving these issues. First, peeling-off technique is expected for low cost fabrication. Compound semiconductor substrate is much more expensive than silicon substrate, and it is important to transfer the nanowire solar cell from substrate to flexible carrier substrate and also need to reuse the substrate many times. In this study, we demonstrated peeling-off technique and flexible cell structure. Secondly, the multijunction nanowire array solar cells can overcome the restriction of materials because nanowire can be grown in axial with lattice mismatch. This is the strong advantage for new structure of III-V compound semiconductors solar cells and we proposed four junction nanowire array solar cells with lattice mismatch. From these perspectives, we are hoping for the continuous research and progress, and photovoltaic application using position-controlled nanowire array will become next generation photovoltaic cell as an alternatives to existing power generations.

List of publications/conferences/awards

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1. Publications related to this work

[1] E. Nakai, M. Yoshimura, K. Tomioka, and T. Fukui, “GaAs/InGaP Core-Multishell Nanowire-Array-Based Solar Cells”, Japanese Journal of Applied Physics, Vol. 52, No. 5, pp. 055002-1-4 (2013). IF=1.057 (Time Cited=7)

[2] E. Nakai, M. Chen, M. Yoshimura, K. Tomioka, and T. Fukui, “InGaAs axial-junction nanowire-array solar cells”, Japanese Journal of Applied Physics, Vol. 54, No. 1, pp. 015201-1-4 (2015). IF=1.057 (Time Cited=0)

2. Publications related to other work

[1] T. Fukui, M. Yoshimura, E. Nakai, and K. Tomioka, “Position-Controlled III-V Compound Semiconductor Nanowire Solar Cells by Selective-area Metal-Organic Vapor Phase Epitaxy”, AMBIO, Vol. 41, No. 2 (Supplement), pp. 119-124 (2012). IF=2.973 (Time Cited=13)

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3. Presentations related to this work

International conference

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Domestic conference

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4. Presentations related to other work

International conference

[1] M. Yoshimura, K. Tomioka, E. Nakai, and T. Fukui, “Fabrication of InP nanowire-array solar cell using Selective-Area Metal-Organic Vapor Phase Epitaxy”, JSPS-RSAS Joint Conference “Capturing the Sun”, Stockholm, Sweden, May, 2011.

[2] T. Fukui, M. Yoshimura, E. Nakai, and K. Tomioka, “III-V semiconductor nanowires and their electronics and photonic device applications **(invited)**”, Japan-Sweden Quantum Nanophysics and Nanoelectronics (QNANO) Workshop, Visby, Sweden, June, 2011.

[3] T. Fukui, M. Yoshimura, E. Nakai, and K. Tomioka, “Compound-Semiconductor Nanowire Solar Cells **(invited)**”, 9th Topical Workshop on Heterostructure Microelectronics (TWHM), Gifu, Japan, August, 2011.

[4] M. Yoshimura, E. Nakai, K. Tomioka, and T. Fukui, “Characterization of InP nanowire array solar cells using selective-area metal-organic vapor phase epitaxy”, the 2011 Material Research Society (MRS 2011) Fall Meeting, Boston, Massachusetts, USA, November, 2011.

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[8] T. Fukui, M. Yoshimura, E. Nakai, and K. Tomioka, “Compound Semiconductor Nanowire Solar Cells **(Invited)**”, The 16th International Conference on Metalorganic Vapor Phase Epitaxy (ICMOVPE-XVI), Busan, Korea, May, 2012.

[9] M. Yoshimura, E. Nakai, K. Tomioka, and T. Fukui, “InP/AlInP core-multishell nanowire array solar cells by Selective-Area MOVPE”, the 31st Electronic Materials Symposium (EMS-31), Shizuoka, Japan, July, 2012.

[10] M. Yoshimura, E. Nakai, K. Tomioka, and T. Fukui, “InP/AlInP core-multishell nanowire array solar cells”, the 39th International Symposium on Compound Semiconductor (ISCS 2012), Santa Barbara, California, USA, August, 2012.

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[19] T. Fukui, M. Yoshimura, E. Nakai, and K. Tomioka, “III-V Compound Semiconductor Nanowire Solar Cells **(Invited)**”, IUMRS-ICAM 2013, Qingdao, China, September, 2013.

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[24] K. Tomioka, M. Yoshimura, F. Ishizaka, E. Nakai, and T. Fukui, "Integration of III-V nanowires on Si: From high-performance vertical FET to steep-slope switch **(Invited)**", the 2013 IEEE International Electron Devices Meeting (IEDM 2013), Washington DC, USA, December, 2013.

[25] K. Tomioka, F. Ishizaka, E. Nakai, and T. Fukui, "Selective-area growth of vertical InAs nanowires on Ge(111) **(invited)**", 17th International Conference on Metalorganic Vapor Phase Epitaxy (ICMOVPE-XVII), Lausanne, Switzerland, July, 2014.

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Domestic conference

[1] 吉村 正利, 冨岡 克広, 中井 栄治, 福井 孝志, “MOVPE選択成長法によるInPナノワイヤアレイ太陽電池の作製”, 第58回応用物理学関係連合講演会, 神奈川, 2011 年 3 月.

[2] 吉村 正利, 中井 栄治, 冨岡 克広, 福井 孝志, “InPナノワイヤアレイ太陽電池の特性評価”, 第 72 回応用物理学会学術講演会, 神奈川, 2011 年 9 月.

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[4] 吉村 正利, 中井 栄治, 冨岡 克広, 福井 孝志, “InPナノワイヤアレイ太陽電池の表面パッシベーション”, 第 59 回応用物理学関係連合講演会, 東京, 2012 年 3 月.

[5] 冨岡 克広, 吉村 正利, 中井 栄治, 遠藤 隆人, 池尻 圭太郎, 石坂 文哉, 福井 孝志, “MOVPE選択成長法によるシリコン上のGaAs/InGaPコア・マルチシェルナノワイヤ成長”, 第 73 回応用物理学会学術講演会, 松山, 2012 年 9 月.

[6] 吉村 正利, 中井 栄治, 冨岡 克広, 福井 孝志, “InP/AlInPナノワイヤアレイ太陽電池の改善と結晶解析**(講演奨励賞受賞記念講演)**”, 第 73 回応用物理学会学術講演会, 松山, 2012 年 9 月.

[7] 遠藤 隆人, 中井 栄治, 吉村 正利, 冨岡 克広, 福井 孝志, “InPナノワイヤアレイの剥離とフレキシブル素子への応用”, 第 73 回応用物理学会学術講演会, 松山, 2012 年 9 月.

[8] 冨岡 克広, 吉村 正利, 中井 栄治, 遠藤 隆人, 福井 孝志, “III-V族化合物半導体ナノワイヤ選択成長と太陽電池応用**(招待講演)**”, 第 42 回結晶成長国内会議, 春日, 2012 年 11 月.

[9] 吉村 正利, 中井 栄治, 冨岡 克広, 福井 孝志, “ITO/p-InPヘテロ接合ナノワイヤアレイ太陽電池”, 第 60 回応用物理学会春季学術講演会, 神奈川, 2013 年 3 月.

[10] 吉村 正利, 中井 栄治, 冨岡 克広, 福井 孝志, “ITO/p-InPヘテロ接合ナノワイヤアレイ太陽電池の特性解析”, 第 74 回応用物理学会秋季学術講演会, 京都, 2013 年 9 月.

[11] 冨岡 克広, 石坂 文哉, 中井 栄治, 福井 孝志, “Si/InAsヘテロ接合縦型トンネルFETのチャネル層ドーピング効果”, 第 61 回応用物理学会春季学術講演会, 神奈川, 2014 年 3 月.

[12] 冨岡 克広, 石坂 文哉, 中井 栄治, 福井 孝志, “Ge(111)基板上の垂直InAsナノワイヤの選択成長”, 第 75 回応用物理学会秋季学術講演会, 札幌, 2014 年 9 月.

[13] 冨岡 克広, 石坂 文哉, 中井 栄治, 福井 孝志, “III-V族化合物半導体ナノワイヤ選択成長と電子素子応用(**招待講演**)”, 2014 年電気化学秋季大会, 札幌, 2014 年 9 月.

[14] 陳 慕テツ, 中井 栄治, 冨岡 克広, 福井 孝志, “省資源型太陽電池に向けた自立したInPナノワイヤアレイの光学特性”, 第 50 回応用物理学会北海道支部/第 11 回日本光学会北海道地区 合同学術講演会, 旭川, 2015 年 1 月.

5. Awards

[1] SPOTLIGHTS: Editors’ Choice from APEX and JJAP, 2013
(2013 年 JJAP 注目論文)

対象論文：E. Nakai *et al.*, “GaAs/InGaP Core-Multishell Nanowire-Array-Based Solar Cells”, Japanese Journal of Applied Physics, Vol. 52, No. 5, pp. 055002-1-4, 2013.

[2] 36th JSAP Outstanding Paper Award – JSAP Young Scientist Award
(第 36 回 2014 年度応用物理学会論文奨励賞)

対象論文：E. Nakai *et al.*, “GaAs/InGaP Core-Multishell Nanowire-Array-Based Solar Cells”, Japanese Journal of Applied Physics, Vol. 52, No. 5, pp. 055002-1-4, 2013.