A Dual-Parameter Multichannel Analyzer Using a Personal Computer

TADASHI AKIMOTO, IKUO MURAI, SHIN CHAKI, YUICHI OGAWA, AND ISAO SHOJI

Abstract—**The design of a practical system for measuring two-parameter signals is reported. To obtain constantly changing energy spectra of nuclear reactor assemblies due to repeated insertion of pulsed neutron sources, the simultaneous acquisition of time and energy data are needed. A computer-based dual-parameter multichannel pulse-height analyzer (MCA) has been developed; it employs a personal computer, two analog-to-digital converters (ADC's), and a parallel interface board for handling these signals. The system showed excellent performance characteristics with a minimum data processing time of about 14 μs; a maximum conversion gain of 2^{18} channels (for example, 512 × 512 ch); a count capacity of 2^{32}-1/ch (2^{16}-1/ch at 512 × 512 ch); and the time required for graphic display of approximately 3 s/2^{16} dots (contour display) or about 0.1 s/(2^{16}/16) dots (isometric display). Large data arrays were handled dynamically with a segment register. The data processing speed was improved by transferring the data from the ADC to the central processing unit (CPU) in 16-bit words and simultaneously reading the status flag and the data. The graphic display process was speeded up by writing the data bit corresponding to the locations directly into the graphic video random access memory (VRAM). The system is simple to operate, and by changing the memory size and coincidence resolution time by software operations, it is highly flexible.**

I. Introduction

MANY extensive benchmark studies have been reported on the spectra of leakage neutrons from test bulk assemblies of reactor materials, thus evaluating the cross-sectional data and the adequacy of numerical methods [1]–[3]. These studies used time-of-flight (TOF) experiments, and the experimental results were compared with the theoretical values. Stationary spectra integrating the time-dependent neutron flux over the entire time period have been used primarily.

Spectra of repeating pulsed-neutron sources are time-dependent due to the nonstationary neutron moderation and migration (nonstationary state) [4]. At each neutron energy level, the intensity of the neutron flux in an assembly shows a decay behavior influenced by slowing down, absorption, and leakage after a short rise by the injection of pulsed neutrons. Two parameters are needed to estimate the time-dependent behavior of such neutron spectra, the neutron energy and the time elapsed after injection of the pulsed neutrons. If only a conventional multichannel pulse-height analyzer is available, the energy spectra are first measured at a set time, but this measurement must then be repeated by altering the set time appropriately [5]. As a result, considerable time is needed to obtain the data over many time points, and the accuracy of the measurements may be poor.

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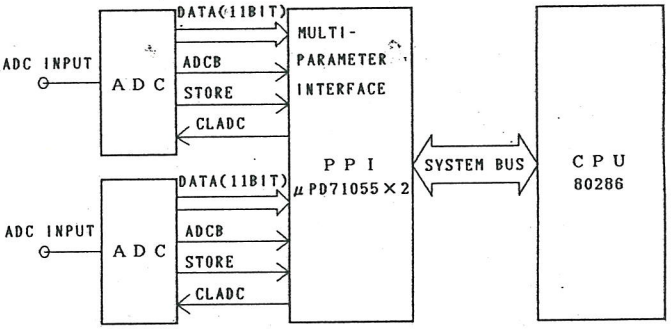

Fig. 1. Block diagram of dual-parameter MCA.

Such difficulty is avoided with a commercially available dual-parameter multichannel pulse-height analyzer (MCA), which allows the measurement of both parameters simultaneously and performs at high speed and/or with a great variety of displays. This commercially available dual-parameter MCA gives excellent performance. However, it is expensive and needs complicated hardware to display the data in real time, because large amounts of special memory are needed. In addition, equipment such as a personal computer is needed to process the data. To alleviate this problem, a compact and relatively convenient dual-parameter multichannel pulse-height analyzer was developed around a personal computer, two analog-to-digital converters (ADC's), and a parallel peripheral interface board. This system has performed well. This paper gives an outline of the system and provides some examples of its application.

II. Dual-Parameter Multichannel Pulse-Height Analyzer

A. Outline of the System

The system is composed of two ADC's (Nippon Atomic Industry Group (NAIG) E-551), a parallel peripheral interface board (Interface Co. Ltd. 98PPI(I/M)AZI-120; multiparameter interface), and a personal computer (NEC Corporation PC9801VX21). The personal computer controls the two ADC's through the multiparameter interface and also accumulates and analyzes the data. A block diagram of the system is shown in Fig. 1.

Reading and processing of data take place as follows. The signals from the two ADC's are stored in the 16-bit register of the CPU (80286) via the multiparameter interface. An X-row

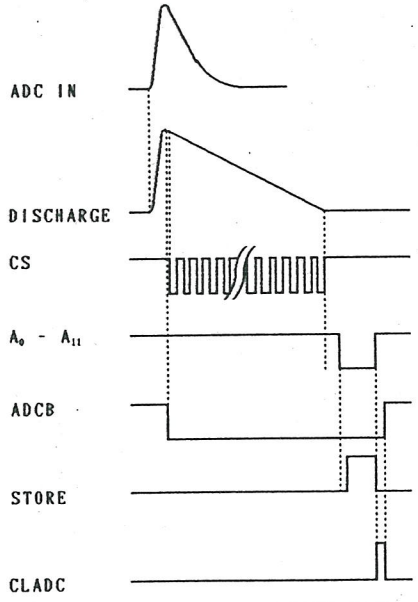

Fig. 2. Timing diagram of E-551 ADC.

and *Y*-column address is determined from a set of converted data, which are output from the two ADC's; then the value in the address is increased by one, and the system is ready to collect new data. The data being measured are shown by a contour display (with 16 colors) or an isometric display. A program written in Basic was initially employed to set the parameters and select the operational functions. The basic operation of the dual-parameter MCA (control of peripheral apparatus, reading data, etc.) and graphic display of the data being collected require high-speed processing in machine language.

B. Analog-to-Digital Conversion

Two 50-MHz Wilkinson-type ADC's (NAIG E-551) are used. Their characteristics are as follows: conversion gain is variable from 8 to 12 bits; conversion time is $0.02 \times N\ \mu$s (N is the size of converted data, in radiation measurements, the channel number). The external interface employs transistor–transistor logic (TTL) [6].

The timing diagram of the E-551 ADC is shown in Fig. 2. The ADC-BUSY signal (ADCB) is set to the "L" state when the conversion is started by an input signal. The DATA-READY signal (STORE) is set to "H" when the conversion is complete. Timing to detect signals and read data can be determined by monitoring the two words of data in the CPU. After receiving the AD-converted data, the CPU sends a positive logic pulse (about 600 ns pulsewidth) to the CLEAR terminal of the ADC. The ADCB's and STORE's are reset, and the ADC's are ready to receive the next signals. Data transfer between computer and ADC's is carried out via the multiparameter interface.

C. Multiparameter Interface

The multiparameter interface transfers data from the ADC to the computer by control signals from the computer. A commercially available parallel peripheral interface board 98PPI(I/M)AZI-120 was adapted to serve as the interface between the two ADC's and the CPU. Two programmable peripheral interfaces (PPI's) were installed on the board, each with a complementary metal–oxide–semiconductor (CMOS) peripheral large scale integration (LSI) μ PD71055C (equivalent to 8255) with three parallel 8-bit ports. The signals from the CPU controlling the ADC and status signals to select the memory size are transferred through the remaining upper 5 bits in PA2 and PC1.

D. Control of the Peripheral Instruments and Data Processing

1) Data reading and processing: Data from the two ADC's are fed to a personal computer through two integrated circuits (IC's) on the multiparameter interface board; the A ports (PA1, PA2) and B ports (PB1, PB2) of the μ PD71055C's are used as input ports for the 11 bits from the two ADC's. These data and the status signals together are treated as 16 bits of data. The maximum AD-conversion gain of this system has been set to 11 bits (2048 channels). Four out of five lines of the PA2 port are shared with the input lines of STORE's and ADCB's from X-ADC and Y-ADC. The last line is used as an external–interrupt request line to stop data collection. The PC1 port is used as a line to set up the operating conditions (memory size, etc.) and to reset the two ADC's.

Data from PA1 and PA2 are then written into the lower 8 and following 3 bits of the 16-bit register, respectively. The remaining 5 bits in the register are shared with STORE's and ADCB's from X-ADC and Y-ADC and the external–interrupt request signal. The input signals to X-ADC and Y-ADC must be generated by the same event; the ADCB's from X-ADC and Y-ADC (signals on the PA2 port) decide whether the signals originate from the same event or not. The ADCB can evaluate the simultaneity between input signals to X-ADC and Y-ADC, because the ADCB is generated at the same time as ADC starts the analysis. If both ADCB's come out at the same time, the process moves to the STORE's. The STORE comes out when the data are fed to the data line after the AD-conversion. If both STORE's come out, Y-ADC data on PB1 and PB2 are written into the 16-bit register and processed. A flowchart of data-reading routine is shown in Fig. 3.

The following describes data processing when the conversion gain is 256 × 256 ch and the data length is 2 bytes. When STORE generates an output, the data from X-ADC are put in the lower 8 bits of the register. The data correspond to the channel numbers. Data from both Y-ADC (which may be read later) and X-ADC decide the coordinates. A method to handle more than 64 kbytes of data is necessary because the address in the computer memory is partitioned in 64-kbyte blocks due to the CPU characteristics. By allocating the data from X-ADC (row data) to the segment register and the data from Y-ADC (column data) to the offset register, easy access in a large memory space becomes possible [7].

If the data length of an array is 2 bytes per data word, 512 (256 × 2) times the data from X-ADC means the top address of row data. The real address is 16 times the value of the segment register due to the characteristic of the segment register. First, the data from X-ADC are shifted 5 bits toward the most significant bit (a 32× increase) and are transferred to the segment register. As 16 times these data become the interval value of 512 bits, the X row is selected. Next, the data from Y-

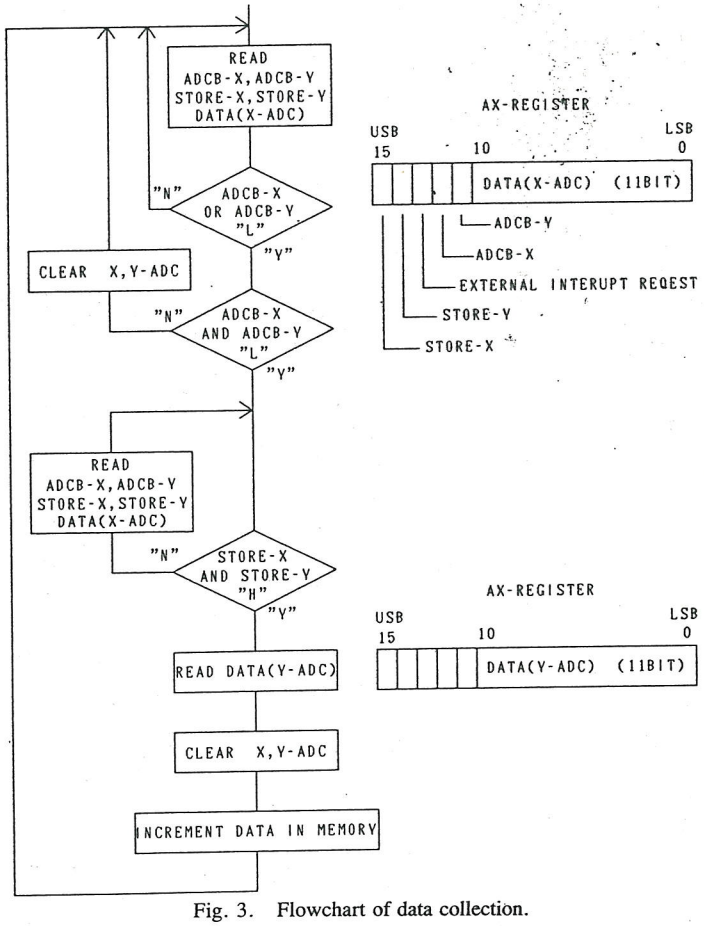

Fig. 3. Flowchart of data collection.

ADC are shifted 1 bit toward the most significant bit (a 2× increase), and the new data are transferred to the offset register. This means that the *Y* column is selected by every 2 bytes. This decides the address; then data in the memory corresponding to the address are accumulated. By this method, two addresses are allocated to one coordinate, and the count capacity becomes 2^{16}-1 (65535) per channel. After processing a pair of signals, the computer sends CLEAR signals to both ADC's, and the analyzer is ready to accept the next signals. The address decision process is shown in Fig. 4.

In this system the status of the flags and the data can be read simultaneously, since the transfer of data between ADC and CPU and the reading of flags are carried out by a single 16-bit word. This makes for efficient data processing since the flag signals that the data processing routine is being carried out at the same time.

2) Display of the measured data: Isometric (three-dimensional graphic display) or contour display (map and projection display) are useful in portraying dual-parameter information as well as monitoring the progress of the measurements. Much time is needed to process digitized dual-parameter data because of the large number of data points (2^{16}-2^{18}). It is not desirable for this system to refresh the graphic data frequently, unless the system includes two CPU's in which one is used only to read data; it may be noted that the efficiency of the measurement will be degraded if the data collection is interrupted during the display refresh cycle. It is possible to display all data graphically with 256 × 256 ch conversion gain, but with 512 × 512 ch conversion gain, some sampling of the data must be made.

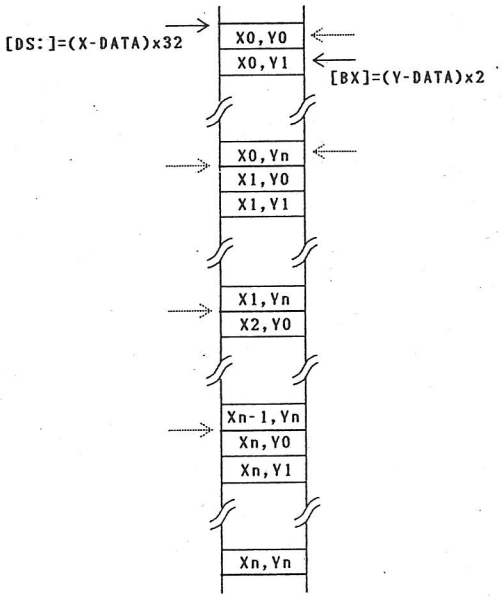

Fig. 4. Access to two-dimensional data array by dynamic segmentation.

This system allows the selection of either a 16-color contour display or an isometric display. Counting values are recorded in the address memory determined by the data. In the contour display the ordinate and the abscissa of the map are determined by the X-ADC and Y-ADC channel numbers, and the data are

displayed in the appropriate location by a color related to the counting values. In the isometric display, the data are displayed monochromatically at intervals of 16 channels.

The amount of data stored in this system is enormous (128 kbytes to 512 kbytes); thus a considerable amount of time is required for the graphic display. But the time required for the graphic display can be reduced by writing the data corresponding to display locations directly into the graphic video random access memory (VRAM). The VRAM displays information in three colors plus intensity: blue, red, green; each dot on the display corresponds to a data bit of VRAM. Since the VRAM can be accessed only one byte at a time, the VRAM address (one of the 8 dots) must be determined for each of the four screens to make one dot of a particular color on the display. After determining the bit corresponding to the dot to display, a 0 or 1 value with respect to the color to be displayed is assigned to the bit.

In the contour display, all data are displayed in 16 colors corresponding to counting values. The time to renew the graphic data changes with the counting value, because the number of accessed VRAM's (0–4 times) changes. The time to renew the graphic data in the isometric display is smaller than with the contour display and is nearly constant, since sampled data and monochrome graphics are employed.

E. Performance of the System

The performance of this system is as follows:

maximum conversion gain	$X \times Y = 2^{18}$ channels (for example, 512 × 512 ch); combinations of X and Y can be determined arbitrarily
count capacity	2^{32}-1/ch (2^{16}-1/ch at 512 × 512 ch)
minimum data processing time	13.6 ± 1 μs (at 256 × 256 ch, 2-byte-long data)
coincidence resolution time	about 200 ns
time to renew graphic data	3 ± 0.5 s/2^{16} dots (contour display); about 0.10 s/(2^{16}/16) dots (isometric display).

The maximum conversion gain is held within $X \times Y = 2^{18}$ ch (count capacity 65535/ch) due to the capacity of the computer memory and the operational mode of the CPU (80286). With appropriate software, arbitrary combinations of X and Y are feasible. The minimum data processing time (not including the ADC conversion time) is 13.6 ± 1 μs (in the case of 256 × 256 ch and 2-byte-long data). The data processing time is 15.6 ± 1 μs for 256 × 256 ch and 4-byte-long data, and 14.0 ± 1 μs for 512 × 512 ch and 2-byte-long data. Because of the 16-bit data processing, there was no appreciable difference in processing time between the case with 2 and 4 bytes. The time to process a large input pulse such as 8 V (linear input range of E-551 is 0–8 V) is about 33 μs (256 × 256 ch and 2-byte-long data), including the deadtime of the ADC.

The probability that the two input signals actually arise from the same event becomes higher as the coincidence resolution time becomes shorter. If required, the resolution could easily be improved to about 10 ns by using a coincidence circuit of the two ADCB's.

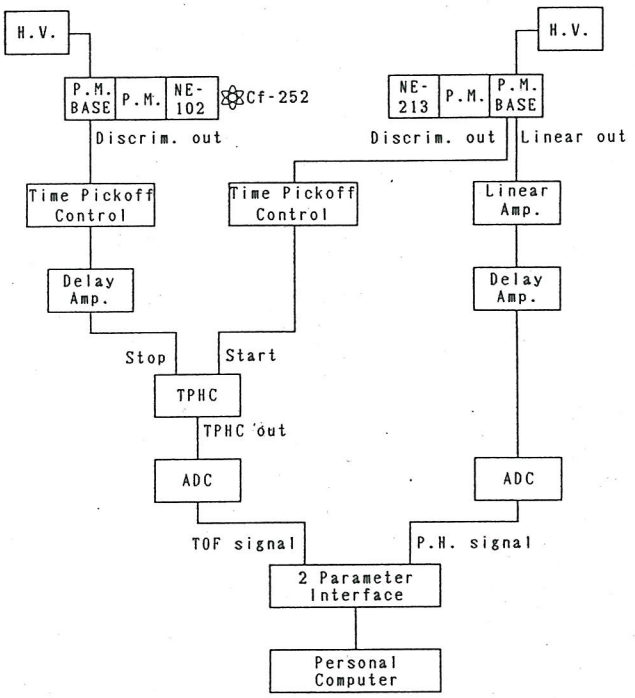

Fig. 5. Block diagram of electric circuit.

The personal computer in this system employs a μPD70116-10 CPU (V30), which is equivalent to a 8086, together with a 80286 CPU. The speed of data processing and graphics with the V30 CPU is lower than with the 80286 CPU. With V30 at 256 × 256 ch and 2-byte-long data, the minimum processing time is 30.0 ± 2 μs; the time required to renew graphic data is 5 ± 2 s/2^{16} dots for contour display and about 0.17 s/(2^{16}/16 dots) dots for isometric display. These are about two times longer than with the 80286 CPU.

III. Experimental Results with the MCA System

The measured results of the response function for the liquid scintillator NE213 (5″φ × 5″t) using a spontaneous fission source ^{252}Cf are detailed here. The purpose of the measurement was to obtain the response function of NE213 by a combination of the TOF method and pulse-height analysis with ^{252}Cf as a pulsed neutron source [8]. The fission time is determined with a plastic scintillator NE102 in close contact to the ^{252}Cf source to detect the gamma ray emitted following the fission. Neutrons emitted by the fission are detected with NE213, 1.5 m from the ^{252}Cf source. The neutron energy was determined by the time difference between the arrival at the two detectors receiving the input signal. The pulse height of signals from NE213 caused by the same neutron was measured simultaneously. The pulse-height distribution for different neutron energies was obtained by a two-dimensional measurement of energy and pulse height. The block diagram of the measuring system is shown in Fig. 5.

Fig. 6 shows results of the measurements by a 16-color contour display, and Fig. 7 shows results of the measurements by an isometric display. Fig. 6 shows all measured data, but in Fig. 7 the row data (time of flight data or energy data) are

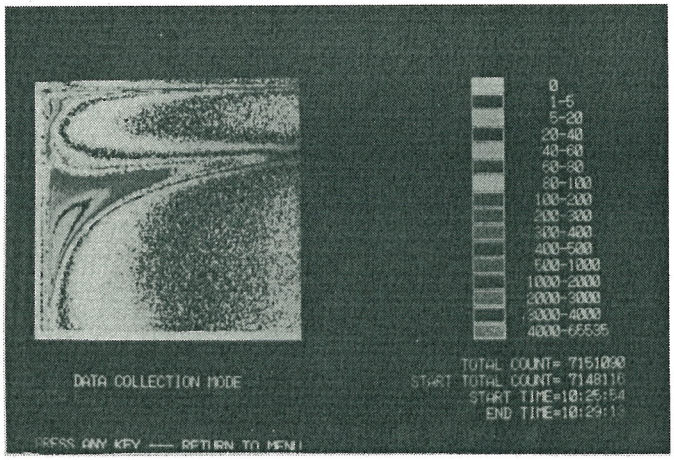

Fig. 6. Measured results of response functions for NE213 scintillator by contour display (original photograph is a 16-color map).

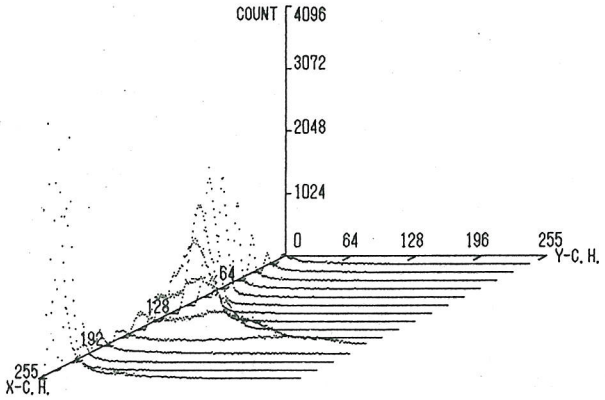

Fig. 7. Measured results of response functions for NE213 scintillator by isometric display.

sampled at intervals of 16 channels. The pulse-height distribution of signals from the NE213 for various neutron energies is seen clearly in Fig. 7. Though the intensity of the ^{252}Cf source was about 30 μCi, intensities of up to 1 mCi would be acceptable in view of the system performance.

IV. Conclusion

The principal features of the system can be summed up as follows.

1) The system can be constructed easily and cheaply from simple components without special hardware. It gives excellent performance with good resolution and high processing speed.
2) Handling of large data arrays is simple by dynamic application of the segment register.
3) The data-processing speed is improved by transferring data from ADC to CPU in 16-bit words and by a simultaneous reading of the status flag and data.
4) Graphic display during measurements has not been possible because of the very long time necessary to form the display. In this system, the graphic display processes were speeded up by directly writing the data corresponding to locations into VRAM. This makes graphic display feasible without decreasing the efficiency of the measurements, and evaluation of data for long measurements was thus facilitated.
5) The memory of the computer is restricted to the maximum conversion gain of $X \times Y = 2^{18}$ ch for 16-bit data. The combination of X and Y can be determined arbitrarily and easily by suitable software.
6) The system is simple to operate and flexible under different measurement conditions; the data length, memory size, and conversion gain are selected with suitable software.
7) The ease of handling and the ability of data processing are improved by a combination of Basic and machine language routines.

The system can be used to measure combinations of two parameters other than time and energy. It can also easily cope with simultaneous measurement of three or more parameters. The system could be improved by interruption of an external timer and a dual CPU system. Because the data can be easily converted to input data to a large-scale computer, processing of complicated data and large volumes of data would be feasible. By introducing the interface board and disk-recorded software, this dual-parameter MCA can be used at any laboratory with two ADC's and a personal computer. We used a PC9801 which is common in Japan, but any personal computer can be used.

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