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One electron-controlled multiple-valued dynamic random-access-memory

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We propose a new architecture for a dynamic random-access-memory (DRAM) capable of storing multiple values by using a single-electron transistor (SET). The gate of a SET is designed to be connected to a plurality of DRAM unit cells that are arrayed at intersections of word lines and bitlines. In this SET-DRAM hybrid scheme, the multiple switching characteristics of SET enables multiple value data stored in a DRAM unit cell, and this increases the storage functionality of the device. Moreover, since refreshing data requires only a small amount of SET driving current, this enables device operating with low standby power consumption. © 2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [<http://dx.doi.org/10.1063/1.4942901>]

Multiple switching on/off is a unique property of a single-electron transistor (SET). This enables us to realize the multi-valued (MV) logic such as NAND/NOR, exclusive-OR (XOR) gates and even Half-Adder which have higher functionality with lower hardware complexity.¹⁻⁷ Considerable efforts toward room-temperature operation have recently been demonstrated by ultrasmall dot-based SET structures.⁸⁻¹³ Particularly, most recent works¹¹⁻¹³ reported the implementation of CMOS-compatible sub_5nm Si SET whose charge stability features three and a half clear multiple Coulomb diamonds at 300K, showing high peak-to-valley current ratio (PVCR). However, despite such aggressive downscaling silicon nanotechnology, the conventional state-of-the-art dynamic random-access-memory (DRAM) has been keeping the binary scheme, and this makes further increasing storage functionality difficult in the future terabit device applications. Here we propose a new architecture scheme for a DRAM capable of storing multiple value data by using a single-electron transistor. In this SET-DRAM hybrid scheme, the multiple switching characteristics of SET as a function of gate voltage enables to store multiple value data in a DRAM unit cell, and this increases the storage functionality of the device. Moreover, since refreshing data requires only a small amount of SET driving current, this enables device operating with low standby power consumption.

Figure 1 is a schematic diagram showing a multivalued DRAM using a SET device (called hereafter, MV SET-DRAM hybrid) according to an implementation of the present architecture scheme. A plurality of DRAM unit cells are arrayed at intersection of word lines (WL) and bitlines (BL). The unit cells include one transistor M3 and one capacitor Cs similar to the DRAM. The bitline is connected to a current source transistor M2 for performing a refresh operation on the unit cells. The bitline is also connected to a SET device and a MOSFET M1 that comprises a literal

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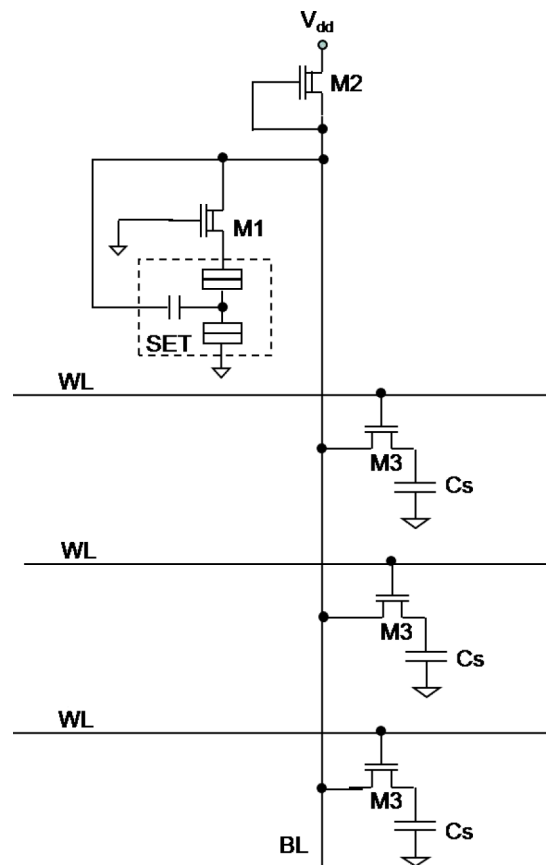


FIG. 1. A schematic diagram showing a multiple-valued DRAM using a SET device proposed by the present architecture scheme.

gate. In each unit cell, multiple value data can be stored unlike the conventional DRAM where only binary data is stored. In the binary data storing method, a cell can store only one bit. However, in this new multiple data storing scheme, a cell can store two or more data, thus increasing the storage density of the device. For an instance, Table I shows the difference between the conventional binary method and the MV scheme proposed by the SET-DRAM hybrid. In the conventional DRAM, the binary data stored in the storage node V_{SN} has a logic high value “1” or a logic low value “0”, corresponding to the power supply voltage level V_{dd} or the ground voltage level, respectively. In contrast, for the SET-DRAM hybrid scheme two bit multiple value data may have “00”, “01”, “10”, and “11”, each corresponding to the ground voltage value $V_{SN} = 0V, 250mV, 500mV,$ and $750mV$, respectively. These multiple values are adapted from a typical SET Coulomb oscillations which will be seen in the following Fig. 2.

TABLE I. The difference between the conventional binary method and the MV scheme proposed by the SET-DRAM hybrid. In the conventional DRAM, the binary data stored in the storage node V_{SN} has a logic high value “1” or a logic low value “0”, corresponding to the power supply voltage level V_{dd} or the ground voltage level, respectively. In contrast, for the SET-DRAM hybrid scheme two bit multiple value data may have “00”, “01”, “10”, and “11”, each corresponding to the ground voltage value $V_{SN} = 0V, 250mV, 500mV,$ and $750mV$, respectively.

Binary Data Storage	Multi-valued Level Storage
Data “0”: $V_{SN} = 0V$	Data “00”: $V_{SN} = 0V$
Data “1”: $V_{SN} = V_{cc}$	Data “01”: $V_{SN} = 250mV$
	Data “10”: $V_{SN} = 500mV$
	Data “11”: $V_{SN} = 750mV$

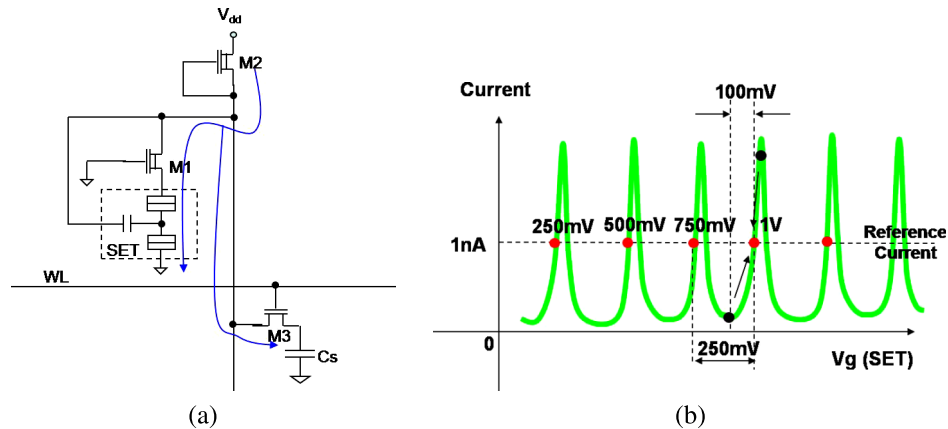


FIG. 2. (a) A diagram for explaining a refreshing method of the present MV SET-DRAM hybrid. In the off state of the word line, the electric charges stored in the cell capacitor C_s are decreased due to a junction leakage current or a sub-threshold current of a transistor M3. (b) Coulomb oscillations of a typical SET characteristics, where it is assumed that the difference between the multiple value levels is the Coulomb oscillation period of 250mV and the amount of current flow supplied from the current source transistor M2 is 1nA. Under these conditions, when a voltage loss of about 100mV is occurred in the OFF state of the word line, the Coulomb oscillation characteristic of the SET automatically restores the gate voltage back by a small amount of current supply, making the word line re-enabled.

Figure 2(a) is a diagram for explaining a refreshing method of the present MV SET-DRAM hybrid. In the off state of the word line, the electric charges stored in the cell capacitor C_s are decreased due to a junction leakage current or a sub-threshold current of a transistor M3. Therefore, the level of electric charges stored in the storage node is decreased over time. Accordingly, a refresh operation needs to be performed before the data are destroyed due to loss of the electric charges. In order to perform a refresh operation, the word line is enabled within a predetermined time before the data are destroyed due to loss of the electric charges. When the word line is enabled, the storage node of the cell and the gate of the SET have the same voltage level. The voltage level of the storage node V_{SN} is thus restored to a voltage level before the electric charge loss occurs according to the Coulomb blockade oscillation characteristic of the SET. Figure 2(b) displays Coulomb oscillations of a typical SET characteristics. It is assumed that the difference between the multiple value levels is the Coulomb oscillation period of 250mV and the amount of current flow supplied from the current source transistor M2 is 1nA. It is further assumed that the storage node stores a voltage level of $V_{SN} = 1V$ during the write operation. Under these conditions, when a voltage loss of about 100mV is occurred in the OFF state of the word line, the Coulomb oscillation characteristic of the SET automatically restores the gate voltage back to $V_{SN} = 1V$ by a small amount of current supply, making the word line re-enabled. Therefore, the voltage level of the storage node is restored to 1V level by the 1nA current supplied from the current source transistor M2. When the voltage level of the storage node is completely restored to $V_{SN} = 1V$ level, the word line is cut-off and the corresponding voltage is stored. In this manner, the word lines are sequentially enabled before the data stored in the cell capacitor C_s is destroyed, thereby maintaining the data stored in each cell.

Figure 3(a) is a diagram showing a cell array proposed by the MV SET-DRAM hybrid scheme. The DRAM cells are arrayed at intersections of word lines and bitlines. Note that a SET device and a transistor M1 for maintaining the drain voltage of the SET device under Coulomb blockade are connected to each of the bitlines. A current source transistor M2 is for refreshing multiple value data,

Figure 3(b) is a diagram for explaining a refreshing method of the MV SET-DRAM hybrid cell array shown in Fig. 3(a), where, the word line $WL<0>$, $WL<1>$, and $WL<2>$ are sequentially enabled for every refresh time period, T_{ref} . It is desirable that the refresh period T_{ref} is set so as to prevent the data stored in each cell capacitor C_s from being destroyed. Therefore, the voltage level V_{SN} stored in the cell capacitor C_s is maintained. Assuming C_s to be a typical value of 20-30fF, then in order to restore a voltage loss of 100mV, it would take 2 μ s if we use 1nA current source (or down

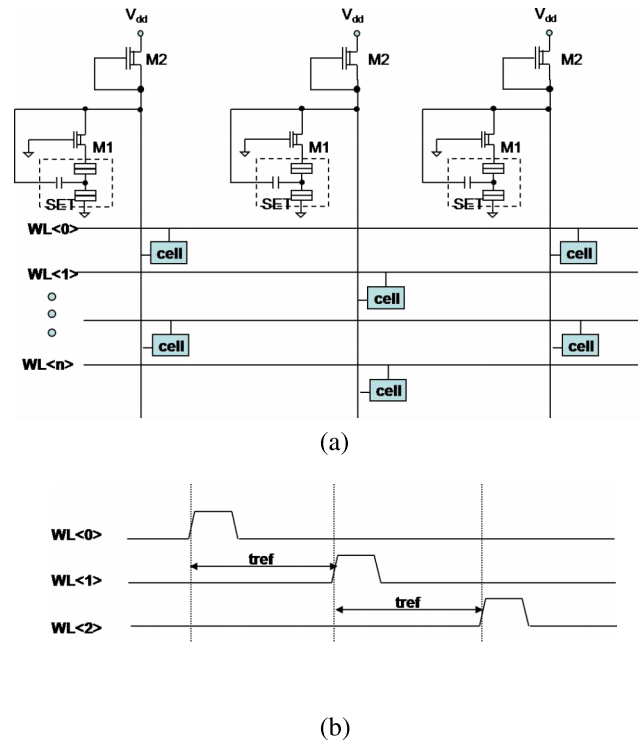


FIG. 3. (a) A cell array diagram proposed by the MV SET-DRAM hybrid scheme. The DRAM cells are arrayed at intersections of word lines and bitlines. Note that a SET device and a transistor M1 for maintaining the drain voltage of the SET device under Coulomb blockade are connected to each of the bitlines. A current source transistor M2 is for refreshing multiple value data, (b) A diagram for explaining a refreshing method of the MV SET-DRAM hybrid cell array shown in Fig. 3(a), where the word line WL<0>, WL<1>, and WL<2> are sequentially enabled for every refresh time period t_{ref} , typically 7.8 μ s required by the state-of-the-art DDR3.

to 0.2 μ s using 10nA current), which are sufficiently shorter than the T_{ref} of typically 7.8 μ s required by the state-of-the-art DDR3.

The MV SET-DRAM refresh method suggested in this architecture scheme is similar to the refresh method of conventional DRAM. However, the main difference is that the refresh in the present architecture scheme only needs to enable the word lines in order to rewrite the data, thereby eliminating the sense amplifier for a refresh operation that was required in the conventional refresh method where the sense amplifier needs to be operated after the word lines are enabled in order to rewrite the data. In addition, the conventional refresh method requires a large amount of standby current flow, whereas the refresh proposed in this SET-DRAM hybrid scheme needs only a small amount SET current flow in order to rewrite the data. Therefore, the MV DRAM proposed in this SET-DRAM hybrid scheme is more suitable for a future low-power circuit application. Finally, in the MV DRAM proposed in this scheme, two or more multiple value data can be stored in a DRAM cell, and thus it is possible to increase the storage density of the device.

The proposed SET-DRAM hybrid scheme can be usable as a multiple valued DRAM with a small number of device elements and ultra-low power consumption, which will be inevitably needed for the next-generation terabit-level nanoelectronics. Most recently, we made successful fabrication of the room-temperature multiple switching Si-SET¹¹⁻¹³ where the charge stability data feature the first exhibition of three and a half clear Coulomb diamonds at 300K, each showing a high peak-to-valley current ratio. However, as seen in Fig. 2(a) of ref. 12, the current levels of the first two Coulomb peaks are seen to be much lower than those of the 3rd and 4th peaks. Moreover, the leakage current between N=3 and N=4 peak is larger than the peak current of N=1 at 300K. So it is difficult to choose a proper current value of 1-10nA to achieve 4-level storage using the proposed design. The different current levels observed between multiple Coulomb peaks may be

a theoretical issue such as quantum effects enhanced in the ultra-small dot, but can be improved by the proper adjustment of critical process parameters of SET such as gate and junction capacitances as well as the Coulomb island dot size. This task is now being undertaken for the possible implementation of the proposed MV SET-DRAM hybrid operating at room-temperature.

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