Doctoral Dissertation

博士論文

Study on A Graphene Three-branch Nano-junction Device and Its Application to Boolean Logic Gates

（グラフェン３分岐ナノ接合デバイスとそのブール論理ゲート応用に関する研究）

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Dedicate to
My family, Xing Fan, and Jie Yin

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Chapter 1 Introduction

1.1 Background

Nowadays the world that we live in is totally relying on the information process systems composed of the integrated circuits (ICs). The ICs process digital signals on the basis of Boolean algebra implemented using the silicon complimentary metal-oxide-semiconductor (CMOS) technology. The core of CMOS is a pair of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFET). The performance of a MOSFET has mostly determined the performance of the IC including the operation speed and the power consumption. To boost the performance, a simple strategy brought up by G. E. Moore in 1965 [1] is increasing the number of transistors per chip. Later this is known as the famous Moore's Law; the transistor count per chip would be doubled every 18 month [2]. In fact, this prediction has guided the

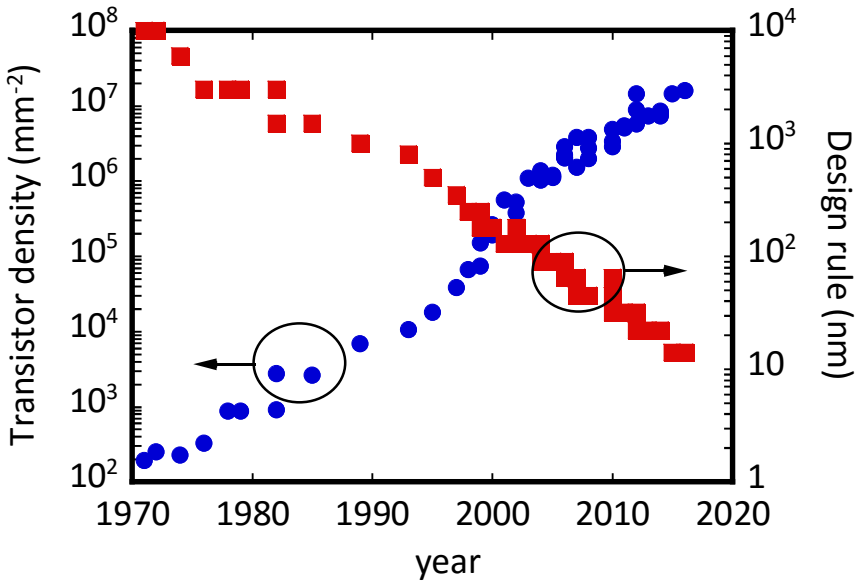

Fig. 1-1 The timeline of transistor density and design rule.

development of the Si CMOS IC technology over 50 years by scaling down the transistor size. Fig. 1-1 shows the timelines of the transistor density per chip and the minimum size of the device fabrication technology known as design rule [3]. International Technology Roadmap for Semiconductor (ITRS) indicates that the design rule will be reduced exponentially to few nanometers [4]. However, the fabrication process in atom scale will be confronted with the fundamental problems such as inhomogeneity of doping, variability of transistors, atom scale fabrication. On the other hand, it is no doubt that the demand on the high speed and large volume information processing grows more and more. Therefore, a novel electronic device based on the new material and mechanism is expected to overcome the limit of the current CMOS technology.

From viewpoint that the simple circuit configuration contributes to the high speed and low power consumption operation, the III-V semiconductor-based three-branch nano-junction (TBJ) device that implements AND gate function by itself has attracted the attention. The TBJ device has an ultimately simple structure which only consists of a T- or Y- shape nano-scale channel and three electrodes. It was firstly introduced by Q. Xu in 2001 [5]. In accordance with the theoretical calculation under assumption of ballistic conduction, the TBJ exhibits a unique nonlinear voltage transfer characteristic. This nonlinear behavior is applicable to AND gate function in digital circuits, and rectification and frequency mixing in analog circuits [6]. Our research group successfully demonstrated a SR-type flip-flop resistor integrating the GaAs-based TBJ devices [9,10]. Owing to the small size and ballistic transport with extremely high electron mobility of III-V compound semiconductors, the TBJ device can response to THz frequency signals [7]. Recently the nonlinear transfer characteristic was also found

in the diffusive transport regime [8]. Here it should be noted that the TBJ utilizing hole transport can achieve the nonlinear voltage transfer curve with the opposite curvature compared to that with electron transport. This also means that the p-type TBJ can operate as OR. However, the p-type TBJ has not been demonstrated yet.

Graphene is considered to be a more suitable material for the TBJ device. Graphene is a two-dimensional, atomic-scale carbon sheet. It exhibits extremely high carrier mobility for both electrons and holes even at room temperature [11]. In addition, by controlling the gate potential, the carrier density and conduction type can be changed. Therefore, the graphene-based TBJ is expected to operate as either AND gate or OR gate, which can be switched by changing gate voltage. Other advantages of the graphene are compatibility to the conventional semiconductor fabrication technology, non-toxic, and low cost. Therefore graphene is a very attractive material for the TBJ device.

The first graphene TBJ device was reported in 2010, however the observed nonlinear characteristics were far from the ideal ones [12]. Later the graphene TBJ made by the epitaxial graphene on SiC was reported in 2011 [13]. Although a bell-shape curve was observed, the gate controllability of the nonlinear characteristics was not confirmed. In 2012, another graphene TBJ was reported, in which the gate control of the polarity of the curvature in the nonlinear characteristics were exactly opposite to the prediction [14]. This was possibly due to the unexpected graphene-metal contact. Then, in the same year, the first demonstration of the correct gate control of the nonlinear characteristics was reported [15], although the nonlinear curves still inclined from the ideal ones. These two reports in 2012 suggested that the fabrication of the graphene TBJ was much more difficult than conventional graphene-based FET. This is because highly

symmetric structure is necessary. Due to lack of the mathematical model describing the TBJ characteristics and the suitable analysis method, it was difficult to understand the observed degraded nonlinear characteristics and it was unclear how to improve the device characteristics.

1.2 Objective of this work

Considering the background described above, the objective of this work is to establish a practical device model for the graphene TBJ in order to understand and analyze the nonlinear behavior, to achieve the ideal nonlinear transfer characteristic in the graphene TBJ device through the optimization of the fabrication process, and to demonstrate the AND and OR Boolean logic gate functions. Then, based on the obtained results, the guideline and method for improvement of the device performance are discussed. Through the demonstration of the logic operations in the graphene TBJ, the possibility of a graphene-based information process systems is opened up.

1.3 Synopsis of each chapter

This thesis is organized by eight chapters as follows.

Chapter 2 introduces the operation principle and analysis of the semiconductor TBJ device.

Chapter 3 summarizes the material and electrical properties of the graphene dealing with this study.

Chapter 4 describes the proposed graphene TBJ models and the analysis. A simple capacitor model is introduced to clearly explain the origin of the nonlinear

characteristic in the graphene TBJ. Utilizing this model, the influences of the asymmetries in contact resistance, geometry, and charge neutral point on the nonlinear characteristics are discussed. A comprehensive model based on the gradual channel approximation is also proposed for quantitative analysis. It is found that the gate capacitance and the minimum carrier density of the graphene are dominant parameters for the nonlinearity. These models make it possible to identify the origin of the non-ideal characteristics in the fabricated graphene TBJ devices and to provide the solutions. The Boolean logic operations of the graphene TBJ is derived using the models.

Chapter 5 describes the fabrication procedures of the graphene TBJ. This chapter focuses on the graphene formation, graphene-metal electrode formation and process optimization, T-shaped channel patterning and etching, and the charge neutral point control by chemical doping.

Chapter 6 shows and discusses the experiment results of the characterization of the fabricated graphene devices. Basic characterization of the graphene channel such as mobility and charge neutral point is presented. The obtained nonlinear curves in the fabricated TBJs are symmetric and successfully controlled by the gate, which are close to the ideal ones. Then AND gate and OR gate operations are obtained by inputting logic signals to the left and right branches and the voltage in the central branch is obtained as output. The switching of the AND and OR was achieved by changing gate voltage. In addition, the NOT gate operation is also demonstrated by applying the complementary supply voltages on the left and right branches, giving input signal to the back gate voltage, and monitoring the central branch voltage as output. Comparing the experiment results and the model calculations, it is found that the logic output swing is

limited by the residual carrier density of the graphene.

Chapter 7 discusses the performance improvement of the nonlinear characteristics and the gate controllability in the graphene TBJ. According to the discussion in the previous chapter, to reduce the residual carrier density in the graphene, a graphene TBJ having a small bandgap is proposed and analyzed. The relationship between the bandgap, the operation bias, and the maximum output swing is clarified theoretically. Then, in order to realize the graphene TBJ with a small bandgap, graphene nanoribbon crossbar produced by unzipping the carbon nanotubes and stacking them is investigated.

Chapter 8 summarizes the conclusions of this thesis.

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Chapter 2 Semiconductor three-branch nano-junction (TBJ) Device

2.1 Introduction

Three-branch nano-junction (TBJ) device and its nonlinear characteristic was proposed and studied by H. Q. Xu in 2001[1]. He firstly investigated TBJ device in an assumption of ballistic transport based on Landauer-Büttiker Formalism[2] and found out that the input and output voltages showed nonlinear transfer characteristics. Then his group fabricated TBJ device based on GalnAs/InP and achieved nonlinear voltage transfer characteristics [3]. They claimed that the nonlinearity arose from electron conduction in ballistic regime as theoretical predicts due to long mean free path of electron in semiconductor and small device size. Monte Carlo simulation also confirmed this mechanism and suggested that TBJ can operate at as high as 1THz[4]. However the nonlinear voltage transfer characteristics also were observed in a GaAs based TBJ device with wrap gates in diffusive regime [5-7]. By gating the channel, partial channel was depleted, resulting a different conductance between left and right branches. A further laser induced experiment revealed that acting as a gate, pinned surface potential can cause nonlinear behavior as well [8]. Although the mechanism of nonlinear voltage transfer characteristics in a TBJ device has not been clarified yet, TBJ operated in both ballistic regime due to left-right-asymmetric transverse mode and diffusive regime due to asymmetric carrier density.

The applications of this device were mentioned in Ref. 1, as for rectifier, frequency mixer and logic gates. A lot of researches demonstrated ultra high frequency

operation of TBJ as rectifier and second-harmonic generation in ballistic conduction[9-13]. There were also investigation on its logic gate function in both ballistic regime and diffusive regime [14-17].

2.2 Ballistic model and its nonlinear voltage transfer characteristics

A geometry of TBJ device is defined as in Fig. 2-1. Three quantum point contacts (QPCs) share a same connection at center that separating conduction band into discrete energy level due to quantum confinement. Three terminals connect to electron reservoirs that can provide or absorb any mount of electrons. the chemical potential in equilibrium for channel, left reservoir, right reservoir and central reservoir are μ_f, μ_l, μ_r, μ_c, respectively. When a push-pull fashion bias V is applied to left and right reservoirs, the potentials change as:

$$\begin{aligned} \mu_l &= \mu_f + eV \\ \mu_r &= \mu_f - eV \\ \mu_c &= \mu_f - eV_c \end{aligned} , \qquad (2.1)$$

where V_c is the output voltage from central branch and e is the element charge.

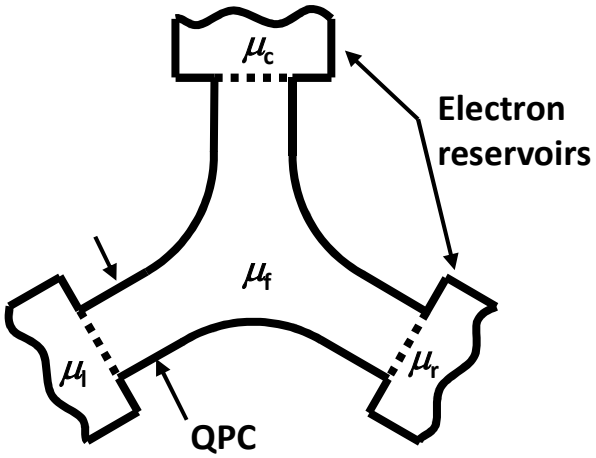

Fig. 2-1 Schematic of three-terminal ballistic junction

According to Landauer-Büttiker Formalism [2], the current in the central branch is given as:

$$I_c = \frac{2e}{h}\left\{\int [N_c(E) - R_{cc}(E)] f(E-\mu_c, T)dE - \sum_{i=l,r}\int T_{ci}(E) f(E-\mu_i, T)dE\right\}, \tag{2.2}$$

where T is the temperature, N_c is the total number of transverse mode in central branch, R_{cc} is reflection possibility and T_{ij} is transmission possibility from terminal i to c (i=l, r) [1]. The conductance of one branch is given as

$$G_i(E) = \frac{2e^2}{h}[N_i(E) - R_{ii}(E)] = \frac{2e^2}{h}\sum_j T_{ji}(E), \tag{2.3}$$

where i,j=c,l,r and i≠j [18]. Due to the geometry symmetry of TBJ, we have

$$\begin{aligned} &T_{rl}(E) = T_{lr}(E), T_{lc}(E) = T_{cl}(E), T_{cr}(E) = T_{rc}(E) \\ &G_r(E) = G_l(E) \end{aligned}. \tag{2.4}$$

With Eq. (2.3) and Eq. (2.4), a group of simple relations can be derived as

$$T_{cl}(E) = T_{cr}(E) = \frac{h}{4e^2}G_c(E). \tag{2.5}$$

Considering that the central branch is supposed to measure the potential between left and right branch, the current in central branch should be zero. Therefore Eq. (2.2) with Eq. (2.5) gives us as

$$2\int G_c(E) f(E-\mu_c, T)dE = \int G_c(E) f(E-\mu_r, T)dE + \int G_c(E) f(E-\mu_r, T)dE, \tag{2.6}$$

and replacing parameters with Eq. (2.1) as

$$\begin{aligned} &2\int G_c(E) f(E-\mu_f + eV_c, T)dE \\ &= \int G_c(E) f(E-\mu_f - eV, T)dE + \int G_c(E) f(E-\mu_f + eV, T)dE. \end{aligned} \tag{2.7}$$

Here if we expand the integration at μ_f in Taylor series, we can solve Eq. (2.7) as

$$V_c = -\frac{1}{2}\alpha V^2 + O(V^4)$$
$$\alpha = -e\frac{\int G_c(E)\frac{\partial^2 f(E-\mu_f,T)}{\partial E^2}dE}{\int G_c(E)\frac{\partial f(E-\mu_f,T)}{\partial E}dE}. \quad (2.8)$$

This expression can be simplified by assuming the temperature is 0K as

$$\alpha = -\frac{eG_c'(\mu_f)}{G_c(\mu_f)}. \quad (2.9)$$

Note that Eq. (2.3) and the total transmission possibility is linearly positive proportion to E [19], It further simplifies Eq. (2.9) as

$$\alpha = -\frac{e}{\mu_f} \quad (2.10)$$

and ignoring high order terms Eq.(2.8) becomes

$$V_c = -\frac{1}{2}\frac{e}{\mu_f}V^2. \quad (2.11)$$

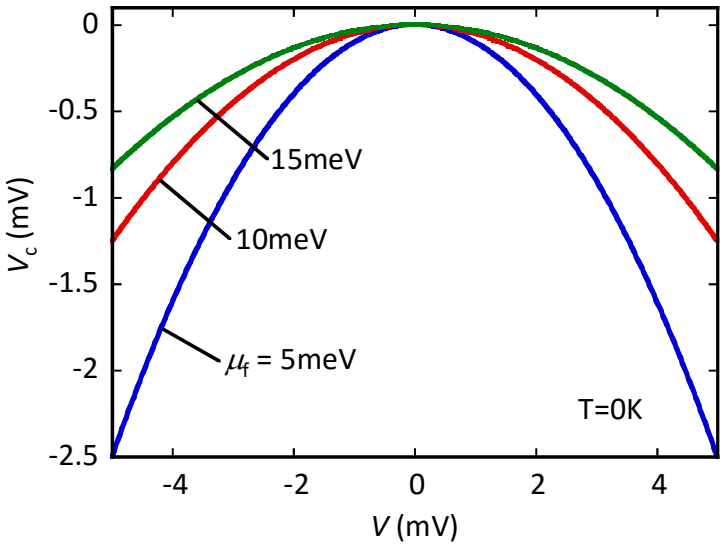

Fig. 2-2 Calculated nonlinear characteristics in ballistic regime

The nonlinear voltage transfer characteristics of TBJ are plotted in Fig. 2-2 based on Eq. (2.11). Since μ_f is positive for n-type semiconductor, V_c is always negative regardless of V. By reducing μ_f, it increases curvature of the parabolic curve.

2.3 Nonlinear voltage transfer characteristics in diffusive regime

The nonlinear voltage transfer characteristics were also observed in a AlGaAs/GaAs based three-branch nano-junction device [8] in diffusive regime. The nonlinearity can be even controlled by a pair of Shottky wrap gates (WPG) on the left and right branches as Fig. 2-3(a) [5]. This configuration can be simplified as two

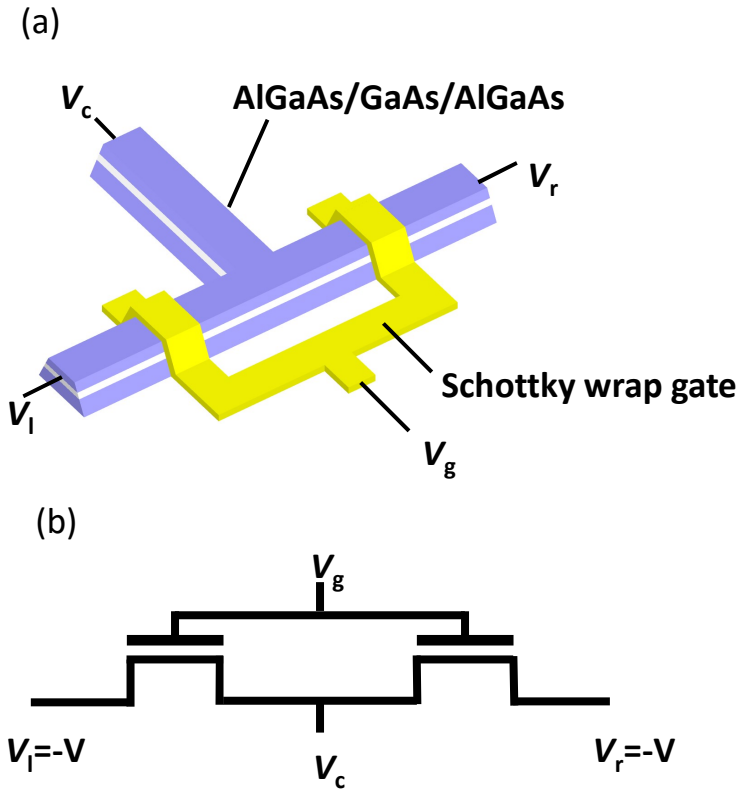

Fig. 2-3 (a) Schematic of GaAs-based three-branch nano-junction device with Schottky wrap gate and (b) its equivalent model

metal-oxide-semiconductor field effect transistors (MOSFETs) with the same conduction type in series connection as Fig. 2-3(b)[7]. The nonlinear behavior requires both MOSFETs working in linear regime. Assuming both MOSFETs are n-type, the current under such biases for the two FET are given as

$$I = \frac{\mu C_g W}{L}\left[\left(V_g - V_{th}\right)\left(V_c + V\right) - \frac{1}{2}V_c^2 + \frac{1}{2}V^2\right] \tag{2.12}$$

$$I = \frac{\mu C_g W}{L}\left[\left(V_g - V_{th}\right)\left(V - V_c\right) - \frac{1}{2}V^2 + \frac{1}{2}V_c^2\right] \quad \left(V < V_g - V_{th}\right), \tag{2.13}$$

where V is the bias in push-pull fashion as described in Section 2.2, V_g is the gate voltage, V_{th} is the threshold voltage, C_g is gate capacitance, μ is electric field effective mobility, L and W are the length and width of gate for both MOSFETs respectively. These two currents should be equal which gives us an equation of V, V_g and V_c as

$$V_c^2 - 2\left(V_g - V_{th}\right)V_c - V^2 = 0 \quad \left(V < V_g - V_{th}\right). \tag{2.14}$$

By solving this equation, the output V_c is derived as

$$V_c = \left(V_g - V_{th}\right) - \sqrt{\left(V_g - V_{th}\right)^2 + V^2}\ . \tag{2.15}$$

Note that V_c should be negative, another solution with positive sign before the root is discarded. Assuming V is a small value to V_g, this expression for V_c can be approximated as

$$V_c \approx -\frac{1}{2\left(V_g - V_{th}\right)}V^2\ . \tag{2.16}$$

It shows that V_c is proportion to the square of V similar to Eq. (2.11).

Another similar derivation can be achieved using gradual channel approximation (GCA) of MOSFET [19]. The carrier density in MOSFET at a distance x from source is given as

$$n\left(V(x)\right) = C_g\left(V_g - V_{th} - V(x)\right)/e\ , \tag{2.17}$$

and current is

$$Idx = \mu WC_g\left(V_g - V_{th} - V(x)\right)dV(x), \tag{2.18}$$

where the $V(x)$ is the surface potential at position x. By integrating left side from 0 to L and right side from -V to V, the current is given as

$$I = \frac{\mu WC_g}{L}\left(V_g - V_{th}\right)(2V). \tag{2.19}$$

Similarly by integrating left side from 0 to x, and right side from -V to $V(x)$, we can achieve the surface potential varies along with channel as

$$I = \mu C_g W\left[\left(V_g - V_{th}\right)\left(V(x)+V\right) - \frac{1}{2}V^2(x) + \frac{1}{2}V^2\right]. \tag{2.20}$$

By replacing I with Eq. (2.19), we can derive $V(x)$ as

$$V(x) = \left(V_g - V_{th}\right) - \sqrt{\left(V_g - V_{th}\right)^2 + V^2 + 2V\left(V_g - V_{th}\right)\left(1 - \frac{2x}{L}\right)}. \tag{2.21}$$

Apparently the central of the channel V_c equals to $V(L/2)$, we can have the same expression as Eq. (2.15) since the current expression Eq.(2.12) and Eq. (2.13) are derived from GCA. But we can obtain an inside view of the channel in the GCA model. Therefore the carrier density $n(x)$ is derived with Eq. (2.17) and Eq. (2.21) as

$$n(x) = C_g\sqrt{\left(V_g - V_{th}\right)^2 + V^2 + 2V\left(V_g - V_{th}\right)\left(1 - \frac{2x}{L}\right)}\Big/e. \tag{2.22}$$

These derivations above are all calculated assuming the MOSFET working in linear regime ($V < V_g - V_{th}$). For MOSFET in saturation regime ($V \geq V_g - V_{th}$) ignoring channel modulation effect, the process is similar as remaining -V on the source (left) and replacing V with $V_{Dsat} = V_g - V_{th}$ on the drain (right). Then the V_c, $V(x)$ and $n(x)$ can be achieved as

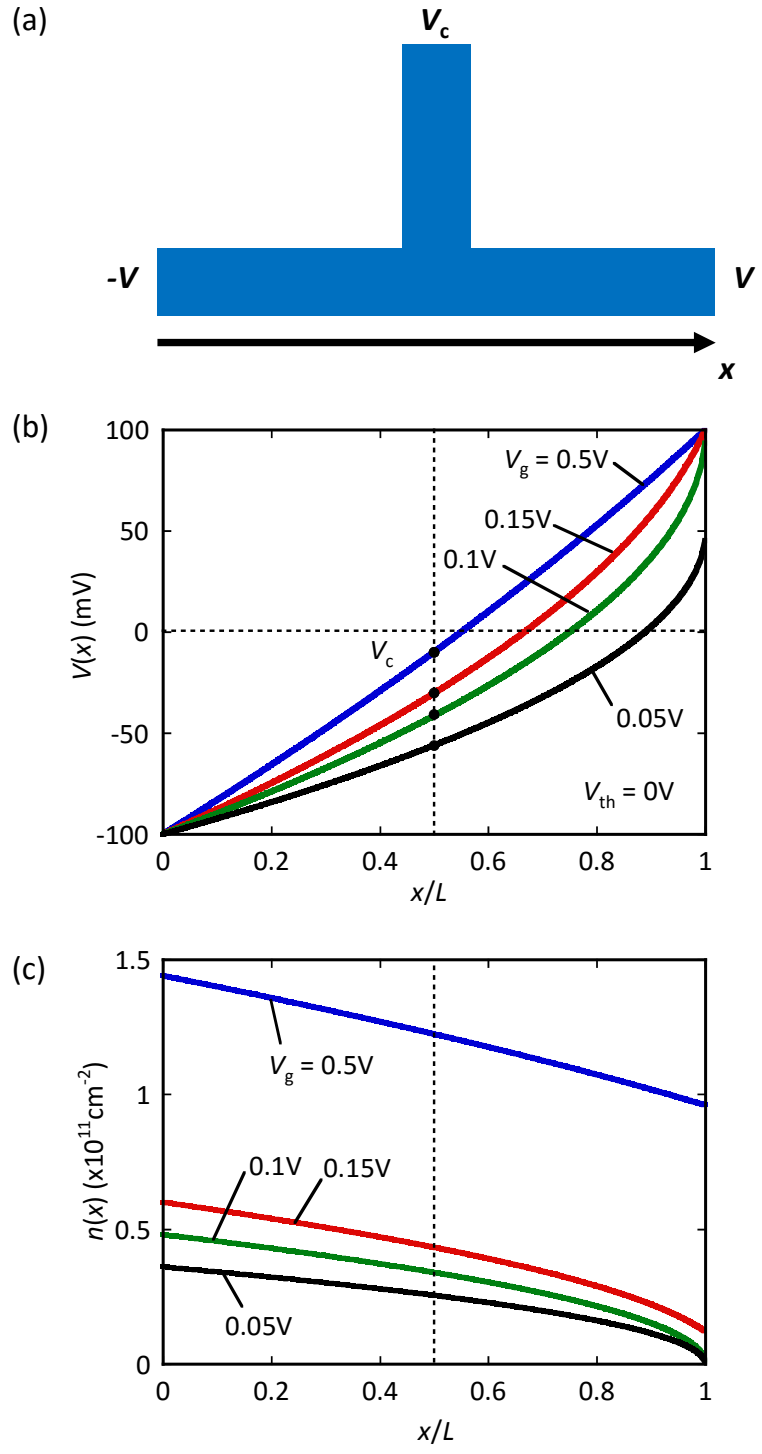

Fig. 2-4 (a) Schematic of TBJ, (b) surface potential profile and (c) carrier density profile in TBJ channel.

$$V_c = (V_g - V_{th}) - \frac{\sqrt{2}}{2}(V_g - V_{th} + V), \tag{2.23}$$

$$V(x) = (V_g - V_{th}) - \sqrt{1 - \frac{x}{L}}(V_g - V_{th} + V), \tag{2.24}$$

$$n(x) = C_g \sqrt{1 - \frac{x}{L}}(V_g - V_{th} + V) \Big/ e. \tag{2.25}$$

Using Eq. (2.15) and Eq. (2.21) - Eq. (2.25), the nonlinear voltage transfer characteristics along with surface potential and carrier density are calculated in a case of C_g = 38.4 nF/cm^2 and V = 100 mV at different V_g in Fig. 2-4 and Fig. 2-5. When V_g is much larger than V, both the surface potential and carrier density varies linearly along the channel. Therefore the nonlinearity is weak at this moment. When V_g - V_{th} reduces and approaches to V, the carriers at drain reduce much faster than source side. In order to maintain the current continuity of source and drain side, a much higher electric field is need at drain, bending the surface potential downwards and increasing the amplitude of output V_c and nonlinearity. Further reducing V_g - V_{th} equal to V, pinch off occurs at

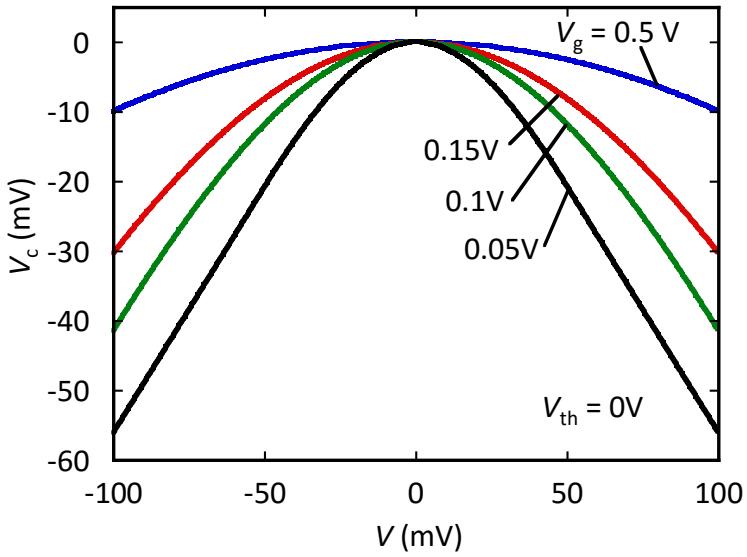

Fig. 2-5 Calculated nonlinear voltage transfer characteristics in diffusive regime

drain and the carriers vanish at this point. An almost infinite electric field at drain is required, causing a heavy bending of surface potential and further increasing in nonlinearity. After this point, any amount of potential that V is over V_g - V_{th} is dropped at drain, and small V_g - V_{th} forces V_c much closer to -V.

Thus the nonlinear voltage transfer characteristic in diffusive regime can be explained by pinch off effect causing unequal carrier densities and resistances at left and right branches. Besides intentionally fabricated gate, surface Fermi level pinning also acts as fixed gate potential to channel and yield nonlinear behavior [8].

2.3 Logic applications

The logic applications of TBJ were firstly proposed in Ref. 1 as an AND gate. The input-output relation of TBJ can be expressed as

$$V_c = \min(V_l, V_r), \tag{2.26}$$

since V_c is always following the lower input voltage. We can apply this relation into the truth table in Table 2-1. When applying (V_l,V_r) = (0,0) and (1,1), the output V_c equals to V_l and V_r due to the structure of TBJ. When applying (V_l,V_r) = (0,1) and (1,0), the V_c

Table 2-1 Truth table of TBJ device-based logic operation

V_l	V_r	V_c=min(V_l,V_r)
0	0	0
0	1	0
1	0	0
1	1	1

follows the input-output relation as Eq. (2.26) and outputs only 0 regardless to inputs. Therefore a TBJ device provides AND gate function itself.

There have been several demonstrations on the logic function of TBJ devices. Since the TBJ is a passive device, an amplifier or an inverter with gain over unity is important in a TBJ circuit. One way is utilizing a second TBJ with load resistance as a resistance-type inverter [15].Another approach was demonstrated in a GaAs-based TBJ with WPGs as Fig. 2-3(a). One TBJ operates in AND gate mode as Table 2-1, and the second TBJ operate as a NOT gate by connecting the output to one of the WPG of the TBJ and inputting signal to another SWG as working as a load FET and a drive FET [16]. Therefore a NAND gate was demonstrated by connecting this two TBJs. Furthermore a flip-flop register was demonstrated integrating two TBJ-based NAND gates [17].

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Chapter 3 Graphene

3.1 Introduction

Graphene is an atomic 2-dimensional (2D) sheet material where Carbon atoms array on the six vertexes of hexagon lattice. It can be seen as only one layers of graphite. Owing to its unique band structure and electric characteristics, Graphene has been widely investigated and researched since a simple formation method called micromechanical exfoliation or the Scotch tape technique proposed by Andre Geim and Kostya Novoselov at The University of Manchester in 2004[1]. Graphene has so many features and properties to study and apply to. For a channel material for TBJ device, the most attractive feature of graphene in terms of electron devices are its high mobility at room temperature and its ambipolar characteristic.

The mobility is defined as the electric field over carrier velocity. It also can be express in Boltzmann transport equation as $e\tau/m_c$ where e is element charge, τ is average collision time, and m_c is effective mass for carriers [2]. Since the energy dispersion in graphene band structure is linear and the valence band and conduction band contact a one point called Dirac point, the effective mass of carriers is proportion to the root of the carrier density. When the Fermi level lines with Dirac point, a small amount of intrinsic carrier density results small effective mass for hole and electron, leading to a huge mobility [3]. The mobility is also limited by τ, which is affected by column scattering from impurities or substrate, optical phonon scattering from substrates, and acoustic phonon scattering and defect scattering[4]. Currently reported highest graphene mobility on SiO_2 substrate was more than 15,000 $cm^2V^{-1}s^{-1}$ at room temperature, which is hundreds times of Si [4].

The ambipolar characteristic is also originated from the zero gap in band structure. By applying electric field graphene sheet, the carrier density and carrier type can be tuned easily.

3.2 Band structure

The lattice of graphene is shown in Fig. 3-1(a). The Bravais lattice is indicated with red dot line around atom A and atom B. The lattice vectors are give as

$$\overrightarrow{a_1} = \frac{a}{2}\left(3, \sqrt{3}\right), \overrightarrow{a_2} = \frac{a}{2}\left(3, -\sqrt{3}\right), \tag{3.1}$$

where a =1.42Å is the distance between the nearest atoms. The Brillouin zone of graphene is shown in Fig. 3-1(b) with high-symmetry points as

$$K' = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), K = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right), M = \left(\frac{2\pi}{3a}, 0\right). \tag{3.2}$$

The band structure of graphene is commonly calculated by tight-binding model [5]. It works under the assumption that an atom is only affected by nearest atoms. For graphene, it only needs to consider the p states with the hopping parameter t. And the Hamiltonian under tight-binding approximation is given as

$$H\left(\vec{k}\right) = \begin{bmatrix} 0 & h\left(\vec{k}\right) \\ h^*\left(\vec{k}\right) & 0 \end{bmatrix}, \tag{3.3}$$

where

$$h\left(\vec{k}\right) = t\left[1 + e^{-i\frac{3}{2}ak_x} \cos\left(\frac{\sqrt{3}}{2}ak_y\right)\right], \tag{3.4}$$

and $\vec{k}$ is the wave vector. Therefore the energy is

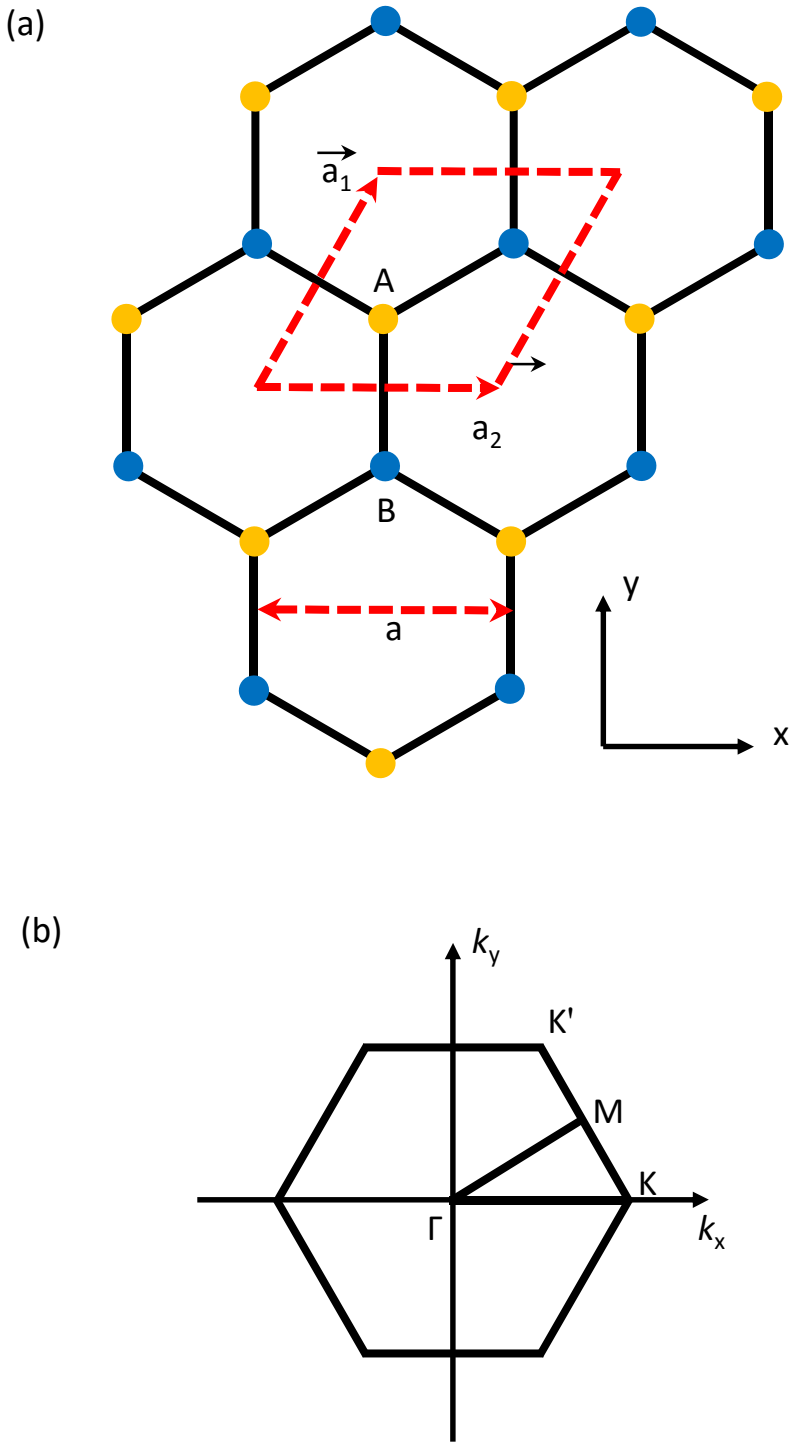

Fig. 3-1 (a) the lattice of graphene and (b) Brillouin zone of graphene

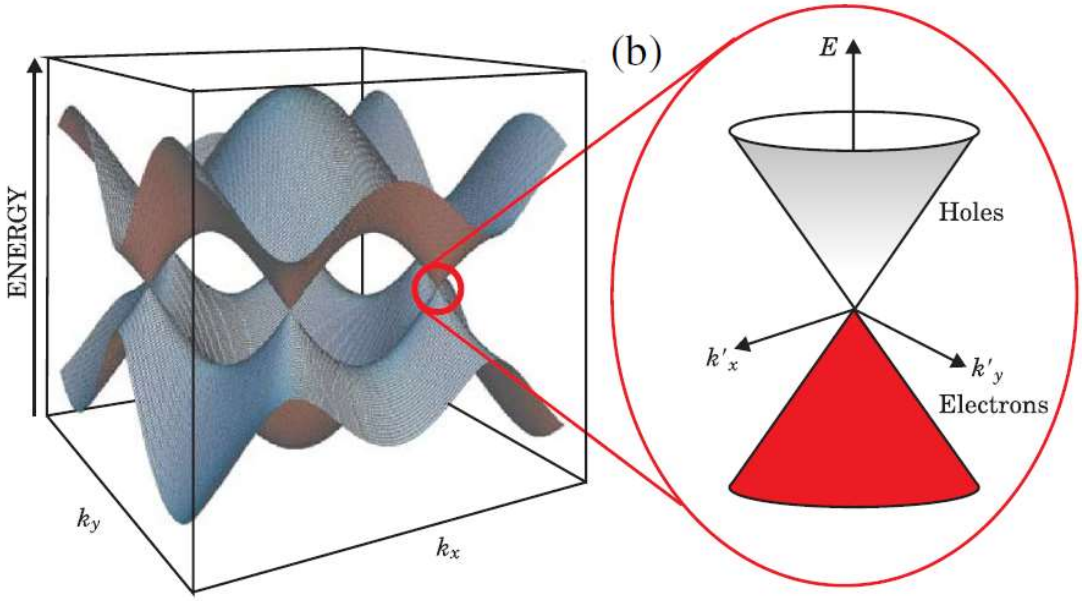

Fig. 3-2 Band structure of graphene and its detail at Dirac point [6]

$$E(\vec{k}) = \pm\left|h(\vec{k})\right| = t\sqrt{3 + 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right)}\,. \qquad (3.5)$$

Notice that $h(\vec{k})$ equals to zero at K(K') point. By expanding $h(\vec{k})$ at K(K') point, also named as Dirac point, a much simple *E-k* dispersion can be derived as

$$E(\vec{q}) \approx \pm\hbar v_F\left|\vec{q}\right|, \qquad (3.6)$$

where v_F is the Fermi velocity as a approximated constant of 10^6m/s, and $\vec{q}$ is a small dislocation from Dirac point. The E-k dispersion of graphene is plotted and more detailed band structure around Dirac point is shown in Fig. 3-2 [6]. Both from the figures and Eq. (3.6), it tells that the E-k relationship is linear near Dirac point for the conduction band and valence band, which is different from semiconductors.

3.3 Electrical characteristics

The carrier density of a graphene MOSFET can be derived from calculating the state number as:

$$N = g_s g_D \pi \left(\frac{k}{2\pi / L} \right)^2 = g_s g_D \frac{L^2}{4\pi} k^2 = g_s g_D \frac{A}{4\pi} k^2, \tag{3.7}$$

where $g_s = g_D = 2$ are spin and valley degeneracy factors, $A = L^2$ is the area in real space. Substituting Eq. (3.6) into Eq.(3.7) and take the differential of N over E, the density of state is derived as:

$$D(E) = \frac{1}{A}\frac{dN}{dE} = \frac{2}{\pi(\hbar v_F)^2}|E|. \tag{3.8}$$

Therefore the carrier density for electron in graphene at temperature T can be calculated according to Fermi-Dirac distribution as [9]

$$n = \int_0^\infty D(E)F(E)dE = \frac{2}{\pi(\hbar v_F)^2}\int_{E_D}^\infty \frac{E}{1+e^{(E-E_F)/k_BT}}dE = \frac{2}{\pi(\hbar v_F)^2} \cdot F_n(E_F, T) \tag{3.9}$$

where E_F is Fermi energy, k_B is Boltzman constant and F_n are

$$F_n(E_F, T) = \int_0^\infty \frac{E}{1+e^{(E-E_F)/kT}}dE = -(k_BT)^2 Li_2\left(-e^{\frac{E_F}{k_BT}}\right), \tag{3.10}$$

where $Li_2(x)$ is the dilogarithm function. And carrier density for is

$$p = \int_{-\infty}^0 D(E)[1-F(E)]dE = -\frac{2}{\pi(\hbar v_F)^2}\int_{-\infty}^0 \frac{E}{1+e^{-(E-E_F)/kT}}dE$$

$$= -\frac{2}{\pi(\hbar v_F)^2} \cdot F_p(E_F, T) \tag{3.11}$$

where

$$F_p(E_F, T) = -F_n(-E_F, T), \tag{3.12}$$

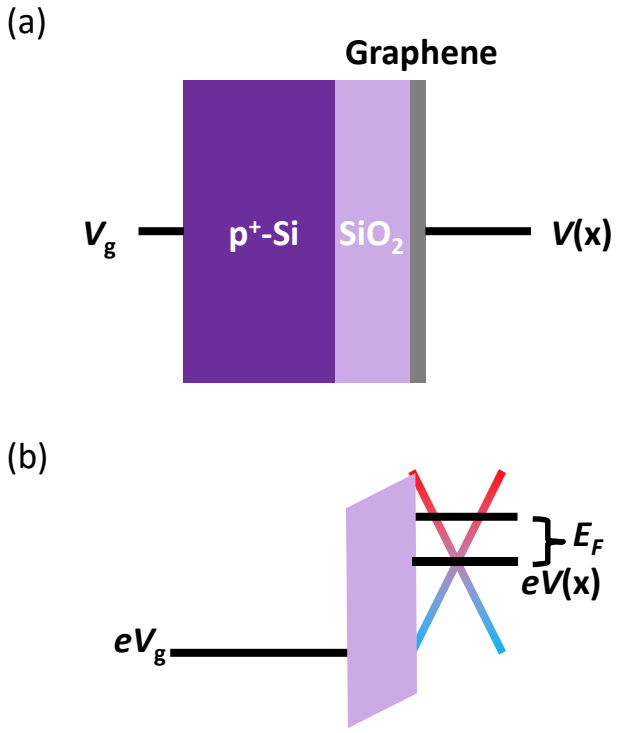

Fig. 3-3 (a) The schematic of a graphene MOS structure and (b) its band diagram.

according to the electron-hole symmetry. Then the charge density of graphene sheet is approximated using Eq. (3.11) and Eq. (3.12) as

$$Q_s = -e(n-p) = -\frac{2e}{\pi(\hbar v_F)^2}\left[F_n(E_F,T) - F_n(-E_F,T)\right]. \tag{3.13}$$

And the carrier density that contribute to conduction are the sum of the electron and hole density as

$$n_s = n + p = \frac{2}{\pi(\hbar v_F)^2}\left[F_n(E_F,T) + F_n(-E_F,T)\right]$$

$$\cong \frac{\pi}{3}\left(\frac{k_B T}{\hbar v_F}\right)^2 + \frac{2E_F^2}{\pi(\hbar v_F)^2}. \tag{3.14}$$

Note that when E_F = 0 eV, the carrier density remains a constant term which is the minimum carrier density n_{min} = 1.63x10^{11} cm^{-2} at room temperature.

The schematic of a metal-oxide semiconductor (MOS) structure for graphene

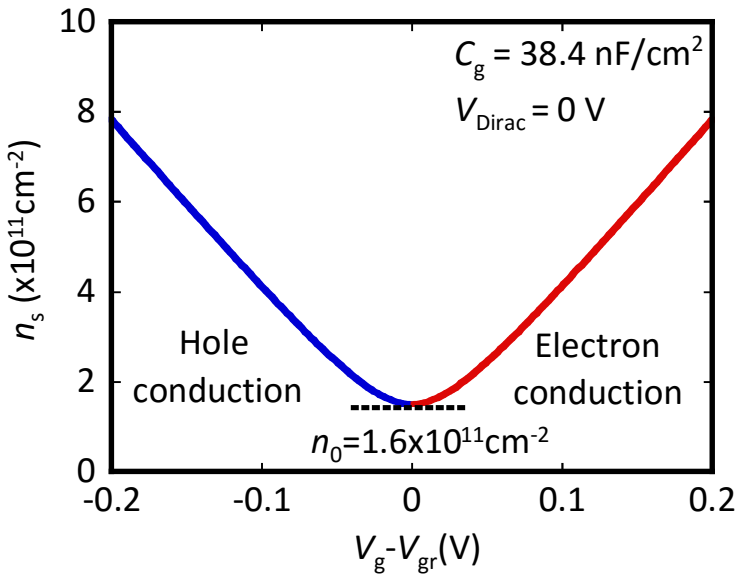

Fig. 3-4 Ambipolar characteristic of graphene

and its equivalent circuit are shown in Fig. 3-3. When the gate potential is lower than the potential drop $V(x)$ of graphene at position x, part of voltage is dropped on the channel of graphene to accumulate equal charges balancing the charges induced on oxide . It can be expressed in equation as

$$C_g\left(V_g - V(x)\right) = Q_s, \tag{3.15}$$

where C_g is the gate capacitance. Substituting Eq. (3.13) and Eq. (3.15) into Eq. (3.13), the carrier density n_s can be calculated and expressed in a complicated form of V_g and $V(x)$.

However in the reality this model is not practical. One of the reasons is that the contaminations on the surface of graphene and in the interface of graphene-substrate act as fixed charges and drift the Dirac point away from 0 V. Therefore the Dirac point is the gate voltage where the carrier density achieves minimum. This term can be inserted by replacing V_g to $V_g - V_{Dirac}$. Meanwhile it is reasonable assuming that the carriers in the graphene is all induced by gate to give

$$n_s = \frac{C_g}{e}\left(V_g - V(x)\right). \tag{3.18}$$

Then a simple empirical formula was proposed to describe the carrier density as

$$n_s = \sqrt{\left[\frac{C_g}{e}\left(V_g - V_{Dirac} - V(x)\right)\right]^2 + n_0^2}\ , \tag{3.19}$$

where n_0 is a fitting parameter to replace the combination of n_i and n_{imp} due to the minimum carrier density is much more dependent on the impurity concentration n_{imp} [7]. It is important to understand the reason that the intrinsic minimum carrier density n_i is not used because n_i showed only small temperature dependence suggesting other mechanism such as impurity charges dominate [8,9]. Fig. 3-4 Ambipolar characteristic of graphene shows n_s changing with V_g at $V(x)$ = 0 V. When V_g is larger than V_{Dirac}, the carrier density is increased by inducing electron. On the other hand, when V_g is smaller than V_{Dirac}, the carrier density is also increased by inducing hole. When V_g is 0 V, the channel achieves the minimum carrier density. This is the ambipolar characteristics of graphene.

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Chapter 4 Graphene TBJ device

4.1 Introduction

Graphene TBJ device is a device based on semiconductor TBJ as introduced in Chapter 2 except for replacing the semiconductor channel material by graphene. It was firstly proposed by A. Jacobsen *et al*. in 2010 [1]. The device was designed in three graphene QPC connecting in Y-shape and expected operating ballistic in low temperature. Obtained nonlinear characteristics were different at various temperatures from 4K to RT. And they were non-ideal due to asymmetry in electrical characteristics of left and right branches. A few more demonstrations were reported on the nonlinear characteristics in room temperature [2-4]. But they were also exhibiting asymmetric curves which were distinguished from the thorough simulated results [5]. Therefore a practical model is needed to analyze the obtained experimental results.

4.2 Basic operation

The basic structure of a graphene TBJ device is shown in Fig. 4-11(a). It consists of a T-shape graphene and three electrodes on a SiO_2/Si substrate. The Si is highly doped by Boron so that it works as a back gate.

The basic operation of graphene TBJ is also indicated in Fig. 4-1(a). The input voltages are applied to the left and right branch in a push-pull fashion, which is $V_l = V$ and $V_r = -V$. The output voltage is detected at central branch V_c. In classic resistance model, due to highly symmetry of the device, V_c should equal to the average of left and right input voltage which is 0 V. However V_c shows parabolic function of V as plotted in

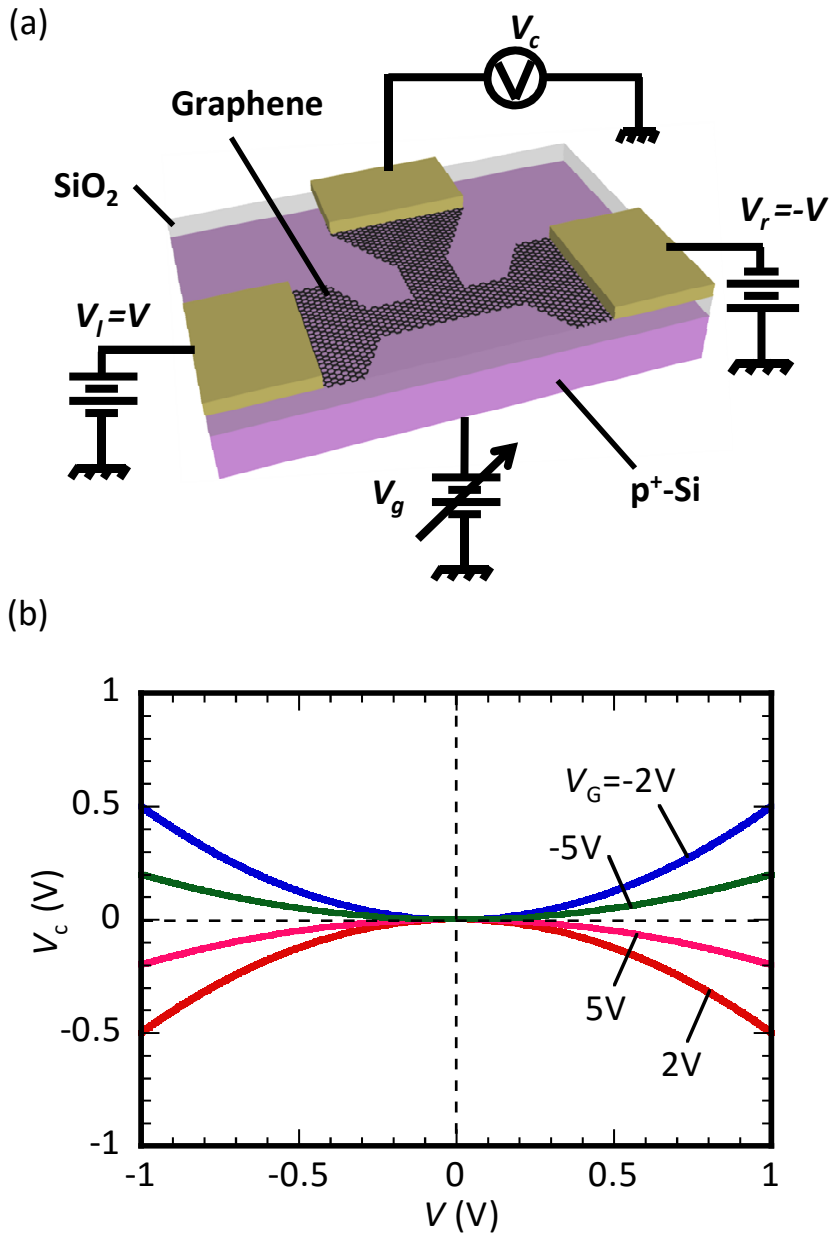

Fig. 4-1 (a) the schematic and operation setup of graphene TBJ, and (b) calculated nonlinear characteristics.

Fig. 4-1(b). It is assumed that the Dirac point V_{Dirac} is 0 V. The polarity of curvatures of the parabolic curves is switched by gate voltage. When V_g is large than V_{Dirac}, the curve is convex with a negative polarity. When V_g is smaller than V_{Dirac}, the curve is concave

with a positive polarity. Also the values of curvatures are controlled by the gate voltage. When $|V_g|$ is near V_{Dirac}, the curvature is large and the nonlinearity is strong. When $|V_g|$ is away from V_{Dirac}, the curvature becomes small and the curve turns into linear. This gate controlled V_c-V nonlinear voltage transfer characteristic explains the basic operation of a graphene TBJ device.

4.3 Ideal models for graphene TBJ

4.3.1 Capacitor model

This is extremely simple model that provides comprehensible mechanism of nonlinear behavior and semi-quantitatively analysis [3]. The schematic of this model is shown in Fig. 4-2. The model is based on several assumptions as 1) the branch is a capacitor of graphene/oxide/p^+-Si; 2) the branch is a resistance and its value is depended on the carriers induced by the capacitor; 3) the central branch is an ideal conductor; 4) the minimum carrier density of graphene is zero. Therefore the carrier densities of positively biased branch on the left and negatively biased branch on the right are

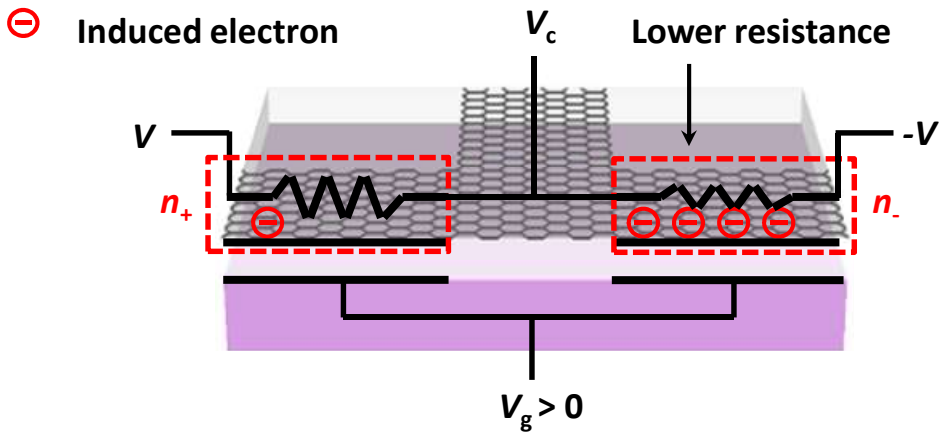

Fig. 4-2 Capacitor model of graphene TBJ

$$\begin{aligned} n_+ &= C_g\left(V_g - V_{Dirac} - V\right)/e \\ n_- &= C_g\left[V_g - V_{Dirac} - \left(-V\right)\right]/e = C_g\left(V_g - V_{Dirac} + V\right)/e \end{aligned}, \tag{4.1}$$

where V is assumed positive. According to the relation of carrier density and resistance, the resistances are

$$\begin{aligned} R_+ &= \frac{W}{L}\frac{1}{C_g\left(V_g - V_{Dirac} - V\right)} \\ R_- &= \frac{W}{L}\frac{1}{C_g\left(V_g - V_{Dirac} + V\right)} \end{aligned}, \tag{4.2}$$

where L and W are the branch length and width respectively. When V_g is larger than V_{Dirac}, electrons are induced in the channel as carriers. Apparently R_- is smaller than R_+. According to the Kirchhoff's rule, V_c is expressed as

$$V_c = \frac{R_- - R_+}{R_+ + R_-}V\,, \tag{4.3}$$

and substituting Eq. (4.2) into Eq. (4.3) can obtain

$$V_c = -\frac{1}{V_g - V_{Dirac}}V^2\,. \tag{4.4}$$

Eq. (4.4) shows that the V_c is the parabolic function of V with reciprocal of - V_g as its curvature. The plot of Eq. (4.4) is shown in Fig. 4-1(b) assuming V_{Dirac} is zero. It is also applicable to the hole conduction when V_g is negative. It states that the nonlinear characteristic originated from the asymmetric carrier distributions of left and right branch due to asymmetric biases. Note that this model is only valid when $|V_c| \leq |V|$ because the output will never be larger than the inputs.

4.3.2 Gradual channel approximation model

A more detailed model is conducted using gradual channel approximation model and current continuity to provide quantitative analysis. The derivation is similar to the semiconductor TBJ except that the empirical formula of graphene carrier as Eq. (3.19)

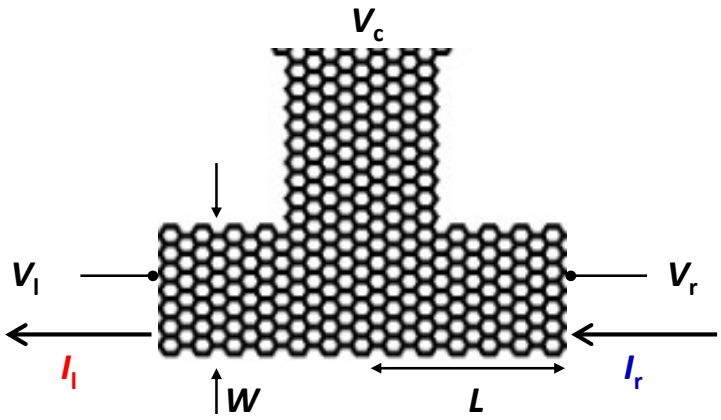

Fig. 4-3 Schematic for GCA model in a graphene TBJ

is used here. Therefore the current formula of graphene is

$$I = \frac{\mu We}{L}\int_{V_s}^{V_d} n(V(x))dV(x) = \frac{\mu WC_g}{L}\int_{V_s}^{V_d}\sqrt{(V_g - V_{Dirac} - V(x))^2 + \beta^2}\,dV(x)$$
$$= \frac{\mu WC_g}{L}\left[-\frac{1}{2}(V_g - V_{Dirac} - V(x))\sqrt{(V_g - V_{Dirac} - V(x))^2 + \beta^2}\right. \quad ,$$
$$\left. -\frac{1}{2}\beta^2 \log\left(\sqrt{(V_g - V_{Dirac} - V(x))^2 + \beta^2} + (V_g - V_{Dirac} - V(x))\right)\right]\Bigg|_{V_s}^{V_d} \tag{4.5}$$

where

$$\beta = \frac{en_0}{C_g}. \tag{4.6}$$

where μ is the mobility for both electron and hole. Note that the gate voltage where the current in Eq. (4.5) achieves minimum is shifted from 0 V even V_{Dirac} = 0 V. This is because that the integral part involves the effect of drain and source voltage. Here let's define the Dirac point for gate voltage V_{Dirac} is the band potential effected only by impurity charge, and charge neutral point V_{CNP} is included the drain source voltage with V_{Dirac} as $V_{\text{CNP}} = V_{\text{Dirac}} + 0.5(V_d + V_s)$. It is still assuming the Dirac point is 0 V. As in the schematic of graphene TBJ in Fig. 4-3, since there is no current in central branch, V_c

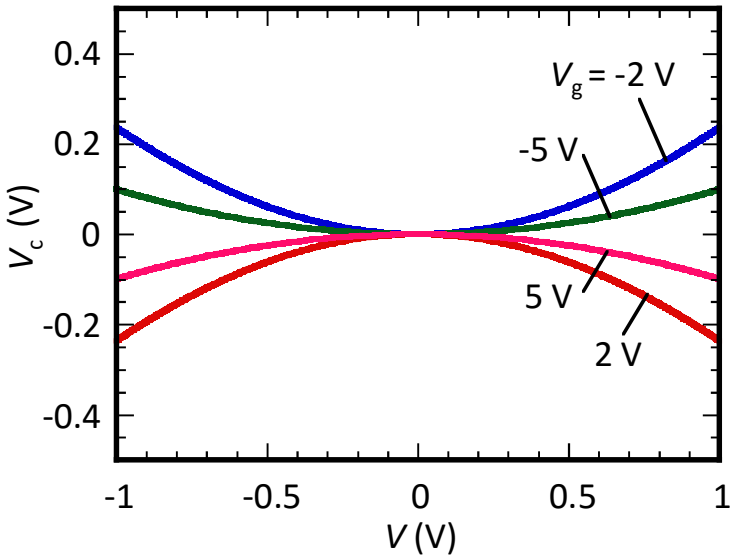

Fig. 4-4 Calculated nonlinear transfer characteristics base on GCA model

should be equal to the potential in the middle of left-right branch. Then the current through the left branch I_l is equal to current in right branch I_r as

$$\frac{\mu We}{L}\int_{V_c}^{V_l} n(V(x))dV(x) = \frac{\mu We}{L}\int_{V_r}^{V_c} n(V(x))dV(x). \tag{4.7}$$

Though the equation of V_c cannot be solved from Eq. (4.7) due to the complexity of integral part. The value of V_c can be found for a given set of V_g, V_l, V_r by programming. The calculated results are plotted in Fig. 4-4. It shows similar results but a smaller value of V_c due to the existence of n_0.

4.4 Asymmetries in graphene TBJ

As mentioned in Chapter 1, so far the reported nonlinear characteristics in fabricated graphene TBJ devices were unintentionally inclined as shown in Fig. 4-5 [3,4,7]. It was highly possible attributed to asymmetry in fabricated device. But due to lack of analysis method, the specific reason was still unknown. Here the most often appeared and

fundamental asymmetries in TBJ which are contact resistance, geometry and charge

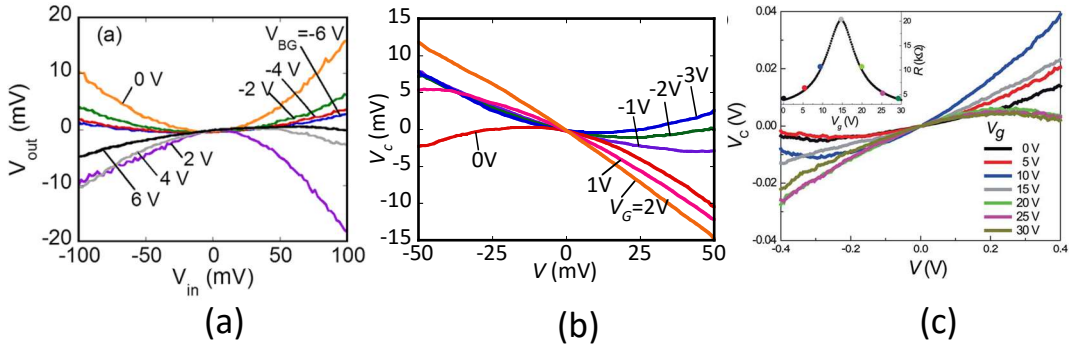

Fig. 4-5 Reported non-ideal nonlinear characteristics in (a)Ref. 3, (b)Ref. 6, (c)Ref. 4.

neutral point will be discussed using the capacitor model as introduced in section 4.2.

I) Asymmetric contact resistance

Consider there is constant small contact resistance at left and right branch as Fig. 4-6. For simplicity the voltage drop on the contact resistance is ignored and the channel resistances are still Eq. (4.2). However with existence of contact resistance on the left and right branch as R_{C+} and R_{C-} respectively, Eq. (4.3) becomes

$$V_c = \frac{(R_- + R_{C-}) - (R_+ + R_{C+})}{(R_- + R_{C-}) + (R_+ + R_{C+})} V . \tag{4.8}$$

Substituting Eq. (4.2) into Eq. (4.9) with the assumption of V_{Dirac} = 0V, Eq. (4.9) is approximated when $V << V_g$ as

$$V_c \approx -\frac{2}{V_g\left[2 + z|V_g|(R_{C+} + R_{C-})\right]} V^2 + \frac{z(R_{C-} - R_{C+})|V_g|}{2 + z|V_g|(R_{C+} + R_{C-})} V$$

$$= -\frac{2}{V_g\left(2 + z|V_g|\sum R_C\right)} V^2 + \frac{z|V_g|\delta R_C}{2 + z|V_g|\sum R_C} V , \tag{4.9}$$

where z = $\mu C_g W/L$, $\delta R_C = R_{C-} - R_{C+}$ and $\Sigma R_C = R_{C-} - R_{C+}$. V_g are replaced by its modulus to satisfy the situation of hole conduction. In case of $\delta R_C = 0$, the second term of Eq.

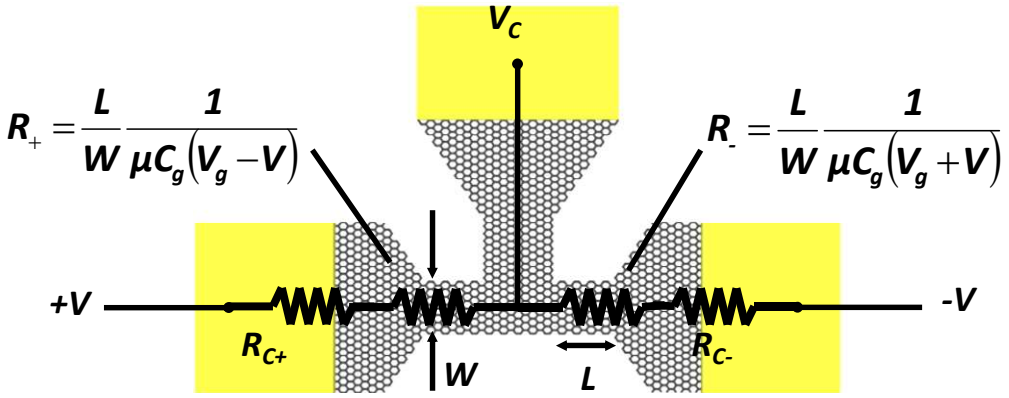

Fig. 4-6 Schematic for contact resistance involved model

(4.10) disappeared. The first term shows a similar function to Eq. (4.3) except a smaller absolute value of the curvature. Though the mount of reduction cannot be accurately estimated from Eq. (4.10) due to approximations and assumptions in this model, it depicts a straight-forward understanding of the affects. When $R_{C+} \neq R_{C-}$, Eq. (4.10) clearly shows that the symmetry of V_c - V curve is broken and inclines to one side. When V_g is small, the channel resistance dominated V_c generating the nonlinear characteristics as described earlier. However when V_g becomes large, the channel resistance reduces meanwhile the contact resistances dominate V_c resulting the asymmetry in the curves.

The fabricated device shown in Fig. 4-5(b) is used here to exam the validity of this model. The resistances of left branch, right branch and its total value of the device can be calculated from V_c and simultaneously measured current I as shown in Fig. 4-7(a). When V_g increased up to 1 V, the contact resistance dominate the total resistance because the graphene channel resistance was rapidly reduced by gate induced carrier. Therefore the observed 3 kΩ resistance difference of left and right branch should be considered as contact resistance difference. By using this value of difference of contact

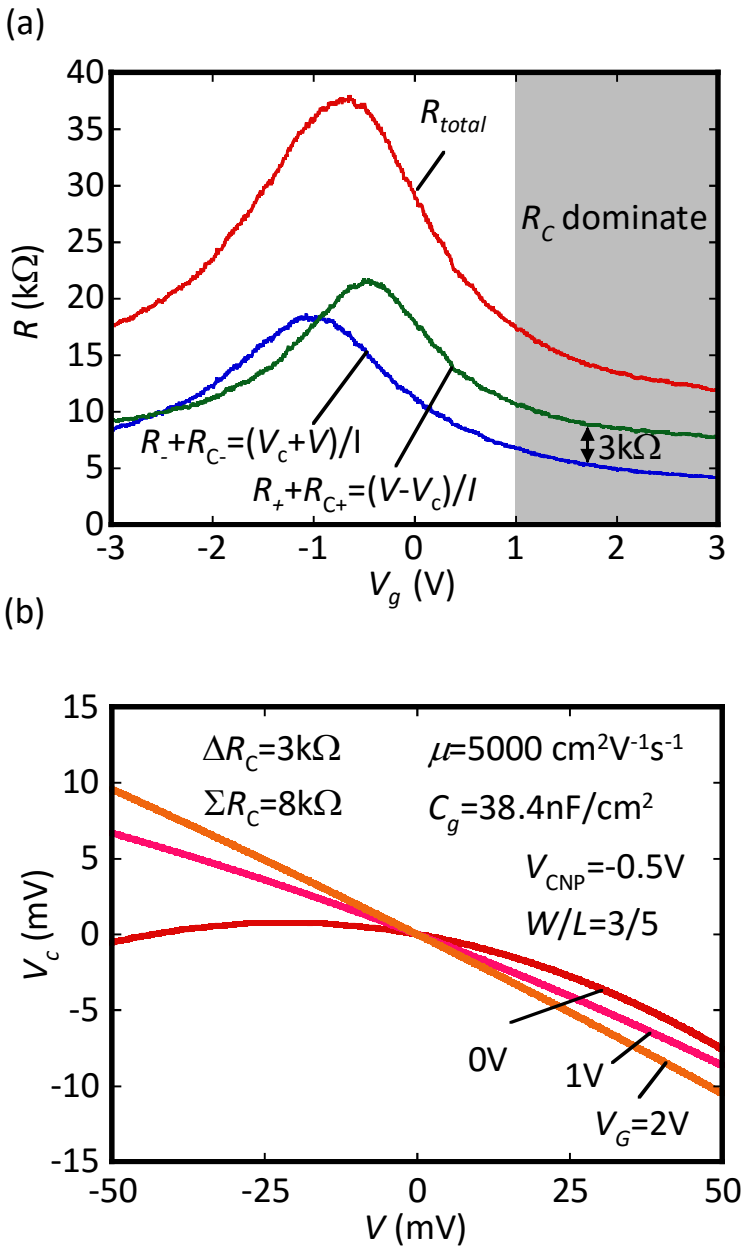

Fig. 4-7 (a) Branch resistances of a fabricated TBJ in Fig. 4-5(b), and (b) calculated nonlinear characteristics based on Eq. (4.9)

resistance and other known parameters, the non-ideal nonlinear characteristics are reproduced very well by Eq. (4.10) as shown in Fig. 4-7(b). Theoretical curves are shown for electrons only, because ΔR_C for hole could not be obtained in Fig. 4-5(b).

This result verified the validity of this model for semi-quantitative use.

By defining the asymmetry factor Δ as

$$\Delta = \frac{|V_c(V) - V_c(-V)|}{2|V|}, \tag{4.10}$$

the asymmetry factor for contact resistance asymmetry Δ_{cra} is

$$\Delta_{cra} = \left| \frac{zV_g \delta R_C}{2 + z|V_g| \sum R_C} \right|. \tag{4.11}$$

From Eq. (4.12), it concludes that the asymmetric contact resistances of left and right branch affect nonlinear characteristics in high carrier concentration regime of graphene.

II) Asymmetric geometry

In this case, the asymmetry in branch length and width is discussed with assumption that other factors are ideal. Eq. (4.2) is rewritten for different length and width as

$$\begin{aligned} R_+ &= \frac{L_l}{W_l} \frac{1}{C_g(V_g - V)} \\ R_- &= \frac{L_r}{W_r} \frac{1}{C_g(V_g + V)} \end{aligned}. \tag{4.12}$$

Then substituting Eq. (4.11) into Eq. (4.3) obtains

$$V_c = \frac{kV_g - V}{V_g - kV} V, \tag{4.13}$$

where

$$k = \frac{L_r/W_r - L_l/W_l}{L_r/W_r + L_l/W_l}. \tag{4.14}$$

Then expanding Eq. (4.12) for small value of V, it is approximated as

$$V_c \approx \frac{k^2 - 1}{V_g} V^2 + kV. \tag{4.15}$$

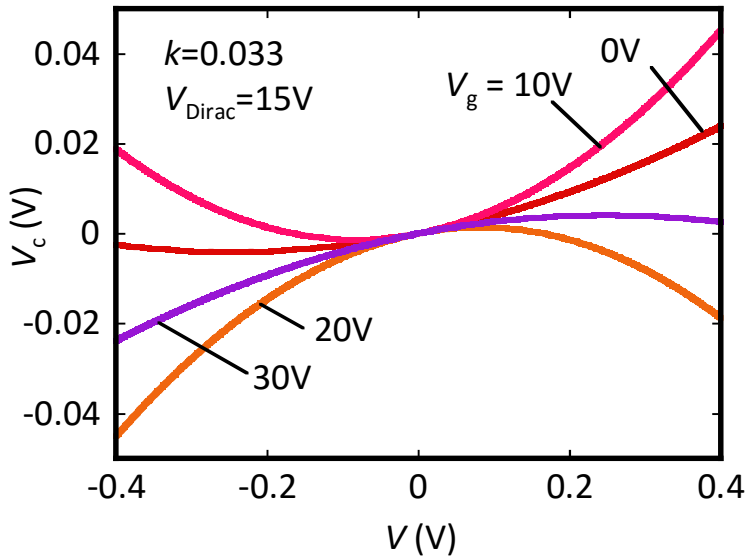

Fig. 4-8 Calculated nonlinear transfer characteristics base on Eq. (4.15)

In case of size asymmetry, the parabolic curve also inclines due to the second linear term. However the coefficient of the linear term does not change with gate voltage as the case of contact resistance asymmetry does. The asymmetry factor for size asymmetry is

$$\Delta_{sa} = |k| . \tag{4.16}$$

It means that despite of the change of V_g, the asymmetry of the curve remain constant as shown in Fig. 4-8 which reproduced the experiment data in Fig. 4-5(c). However the asymmetry in geometry is barely seen in a channel well defined graphene TBJ which is fabricated by electron beam lithography owing to the high precision of the fabrication technique.

III) Asymmetric Dirac point

Suppose the Dirac points for left and right branches are different. Eq. (4.2) is rewritten

as

$$R_{+} = \frac{L}{W}\frac{1}{C_g\left(V_g - V - V_{Dl}\right)}, \qquad R_{-} = \frac{L}{W}\frac{1}{C_g\left(V_g + V - V_{Dr}\right)} \tag{4.17}$$

where V_{Dl} and V_{Dr} is the Dirac point for left and right branch respectively. Then V_{c} becomes

$$\begin{aligned} V_{\mathrm{c}} &= \frac{\frac{1}{\left(V_g + V - V_{Dr}\right)} - \frac{1}{\left(V_g - V - V_{Dl}\right)}}{\frac{1}{\left(V_g + V - V_{Dr}\right)} + \frac{1}{\left(V_g - V - V_{Dl}\right)}} V_{bias} = \frac{-2V - \left(V_{Dl} - V_{Dr}\right)}{2V_g - \left(V_{Dl} + V_{Dr}\right)} V_{bias} \\ &= -\frac{1}{V_g - \left(V_{Dl} + V_{Dr}\right)/2} V^2 - \frac{V_{Dl} - V_{Dr}}{2V_G - \left(V_{Dl} + V_{Dr}\right)} V \\ &= -\frac{1}{V_g - \overline{V_{Dirac}}} V^2 - \frac{\delta V_{Dirac}}{2V_G - 2\overline{V_{Dirac}}} V, \end{aligned} \tag{4.18}$$

where dV_{Dirac} is the difference and $\overline{V_{\mathrm{Dirac}}}$ is the average of the Dirac point of left and right branches. Therefore asymmetry factor for Dirac point asymmetry is

$$\Delta_{dpa} = \left| \frac{\delta V_{Dirac}}{V_G - \overline{V_{Dirac}}} \right|, \tag{4.19}$$

which means that the asymmetry in nonlinear curves is obvious when V_{g} approaches $\overline{V_{\mathrm{Dirac}}}$ This is quit opposite to the situation of asymmetric contact resistance. The nonlinear behavior is plotted in Fig. 4-9 to reproduce the experiment nonlinear behavior in Fig. 4-5(a). This asymmetry is often observed due to difficulty of process in controlling the surface charge of graphene from impurities.

Fig. 4-10 shows the asymmetry factors changing with gate voltage in different ways under asymmetric structure of TBJ. In case of asymmetric contact resistance, the asymmetric nonlinear characteristics become obvious when gate voltage increases. In

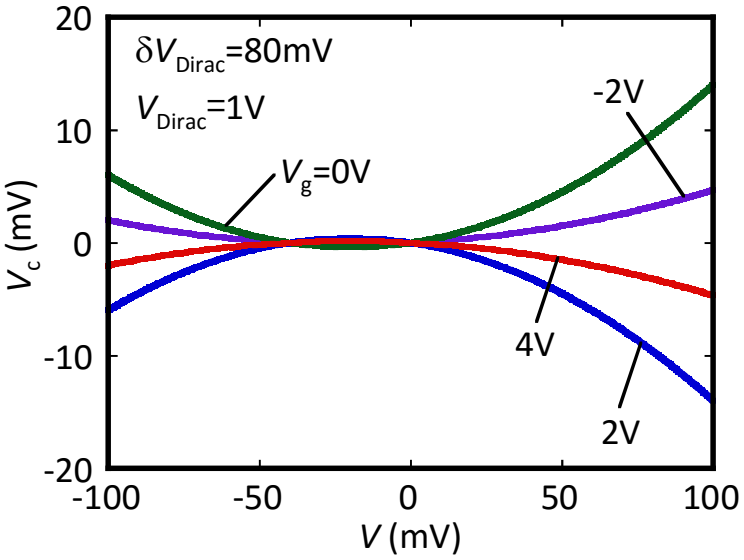

Fig. 4-9 Calculated nonlinear transfer characteristics based on Eq. (4.18)

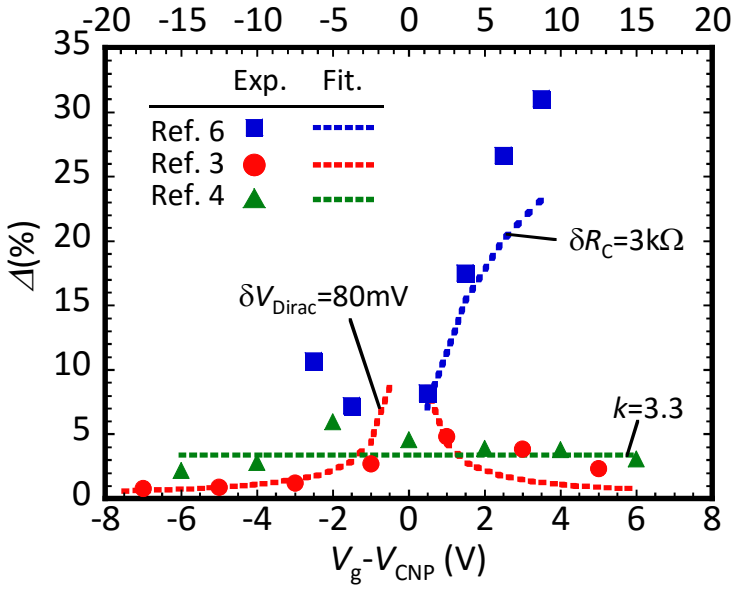

Fig. 4-10 Asymmetry factors varies with gate voltage

case of asymmetric geometry, the asymmetry factor is independent on gate voltage. In case of asymmetric Dirac point, the nonlinear characteristics incline when gate voltage approaches Dirac point. These models match the experimental data properly, give a

simple method to distinguish the reasons of inclined nonlinear characteristics in a fabricated graphene TBJ.

4.5 Logic operation of graphene TBJ

4.5.1 AND/OR gate operation and its reconfigurability

The Boolean logic gate function can be introduced from plotting a 3-D input-output plot by solving Eq.(4.7). Fig. 4-11(a) shows the result of Eq. (4.7) with V_l and V_r from 0 to 1 V at V_g = 1 V for electron conduction. It provide a directly readable results that when V_l = V_r = 0 V or 1 V, V_c outputs the exactly voltage as inputs. Meanwhile when V_l = 0 V and V_r = 1 V, due to the nonlinear behavior, the output of V_c indicated in blue point, is smaller than the average of V_l and V_r which can be defined as a threshold voltage of 0.5 V. In the digital definition V_c is as equal as 0. This is same for V_l = 1V and V_r = 0V. One can fill in the table of truth as shown Table 4-1. It appears that at V_g = 1 V, the graphene TBJ operates as an AND gate.

On the other hand, when V_g = 1 V, the outputs for $V_l \neq V_r$ are revered as shown in Fig. 4-11(b). Filling the truth table in Table 4-1 with the result in Fig. 4-11(b), it give the OR gate for graphene TBJ. The function of graphene TBJ is controlled by gate voltage. The switching of AND gate and OR gate occurs when V_g is around V_{CNP} = 0.5 V.

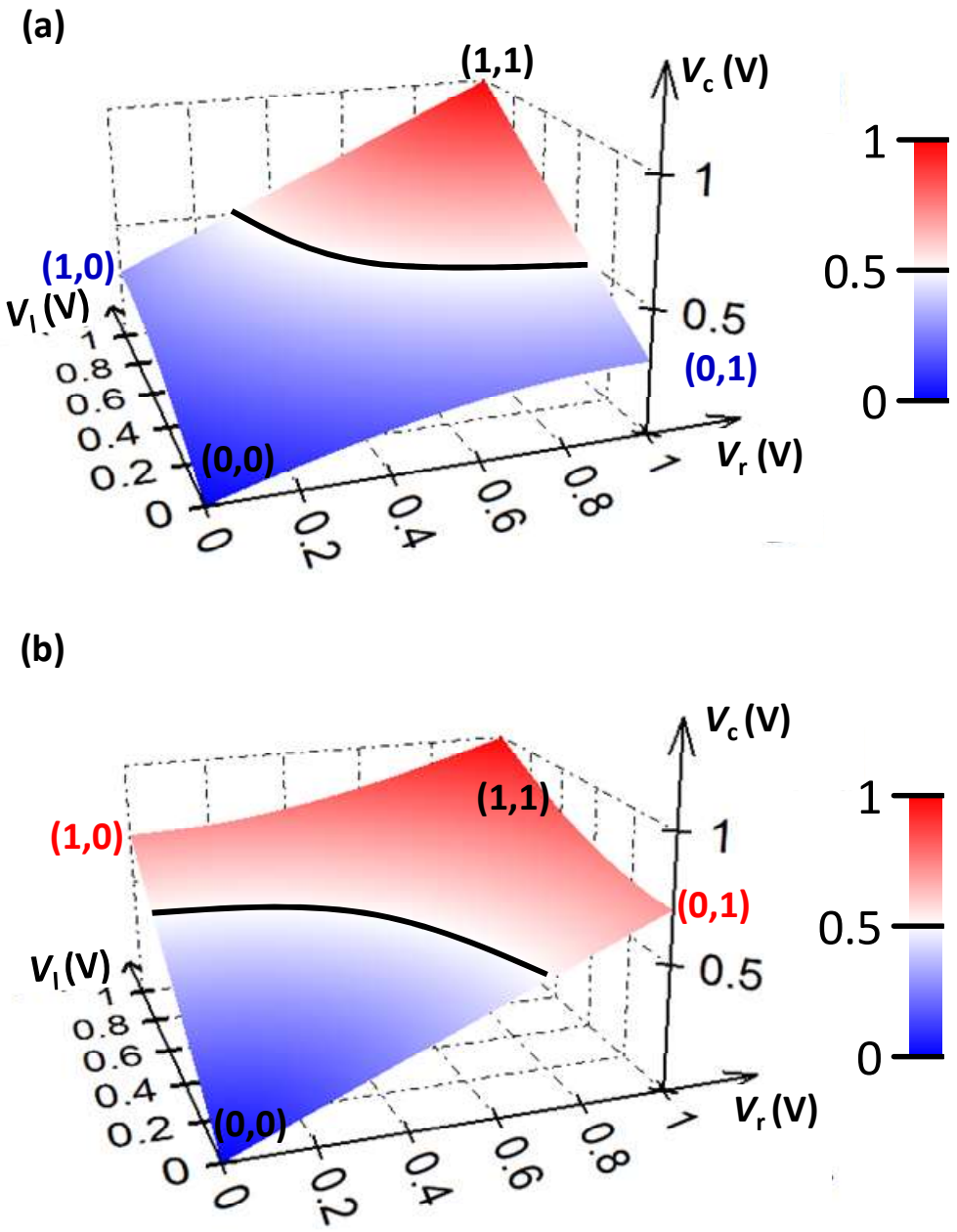

Fig. 4-11 3-D input-output plot calculated based on Eq. (4.7) (a) at Vg = 1 V for AND gate and (b) at Vg = 0 V for OR gate.

Table 4-1 Truth table of graphene TBJ

V_l	V_r	V_c	
		$V_g > V_{CNP}$	$V_g < V_{CNP}$
0	0	0	0
0	1	0 (<0.5 V)	1 (>0.5 V)
1	0	0(<0.5 V)	1(>0.5 V)
1	1	1	1

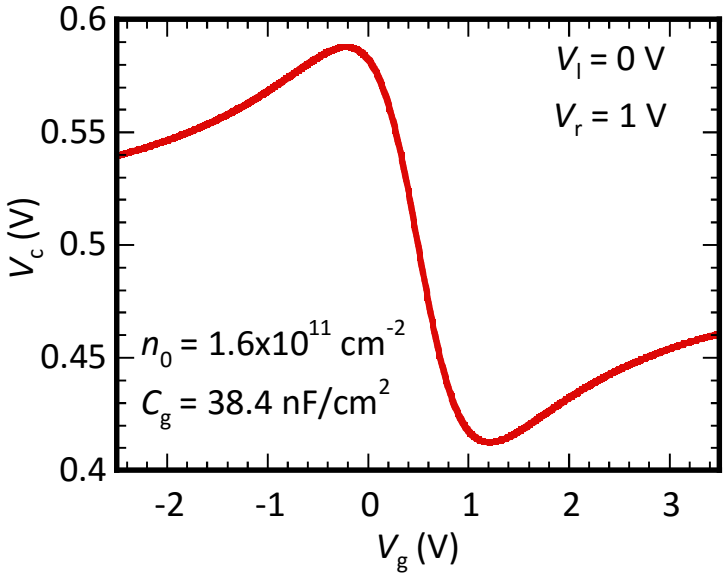

Fig. 4-12 Calculated inverter characteristic of graphene TBJ

4.5.2 NOT gate operation

When the voltages on the left and right are fixed as 0 V and 1 V as the power source, the V_c - V_g transfer characteristic can be plotted as Fig. 4-12. It clearly shows that V_c decreases rapidly when V_g increases around $V_g = V_{CNP}$. The inversed phase between V_c and V_g provides the inverter function for graphene TBJ. Therefore it also raise the

possibility that graphene TBJ operates as a NOT gate.

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Chapter 5 Device fabrication

5.1 Introduction

The fabrication of graphene TBJ consists of graphene formation, electrodes formation, graphene etching and chemical doping. Except etching process, the fabrication process for graphene electrical device has not been established and still been investigated. The difficulties are focusing on high quality graphene formation on wafer scale, formation of low contact resistance electrodes and charge neutral point control.

The most common method of formation graphene is the mechanical exfoliation process proposed by Andre Geim and Kostya Novoselov [1]. It is simple and forms high quality graphene. However the exfoliated graphene is located randomly on the substrate with a micron order size which is sufficient for research use but not fit for industry. A promising massive production of graphene was reported in 2008 [2]. By chemical vapor deposition (CVD) method graphene can be produced in a wafer scale [3]. Through constantly optimizing the growth condition, CVD graphene have achieved high quality and mobility [4].

A good contact to the electrode is essential in demonstration of the intrinsic performance for any electrical device. The art-of-state graphene-metal contact resistivity is still one order larger than the requirement [5]. Yet the mechanism of graphene-metal transport is unclarified at this moment. Though the graphene-metal contact will be important for research level for a long time, other researchers are trying to make few-layer graphene or Carbon nanotubes into interconnection for integrated circuit [6]. At that time graphene-metal should not be a problem because of replacing metal with Carbon materials as electrodes/interconnection.

Currently the most challenging problem may be the cleaning process for graphene interface and surface. For the reason that the impurities or contaminations from the process or environment attach to graphene acting as fixed charge, the charge neutral point of fabricated graphene shifts from 0 V and various from device to device leading to poor reproducibility. In addition, owing to its atom level thing and weak bond connection, graphene is too fragile to use common methods in Si process to clean surface such as UV irradiation, Oxygen plasma ashing and so on.

In this study, some basic processes were established on research uses.

5.2 Formation of graphene

5.2.1 Mechanical exfoliation

The basic procedure is described as below.

1) Prepare SiO_2 substrate with organic cleaning and bake at 140ºC to remove H_2O on the surface.

2) Put one or two piece of Kish-graphite on the sticky side of Scotch tape.

3)Fold the sticky side to another, make sure graphite is on both side, then separate them. This process will create mirror of graphite on the other side and reduce the thickness.

4)Do the process above for several times, until the tape is full of graphite pieces and semi- transparent.

5)Press the graphite on the SiO_2 substrate hardly to reduce the distance between graphite and SiO_2.

6)Remove the tape rapidly.

7)Find graphene using optical microscope.

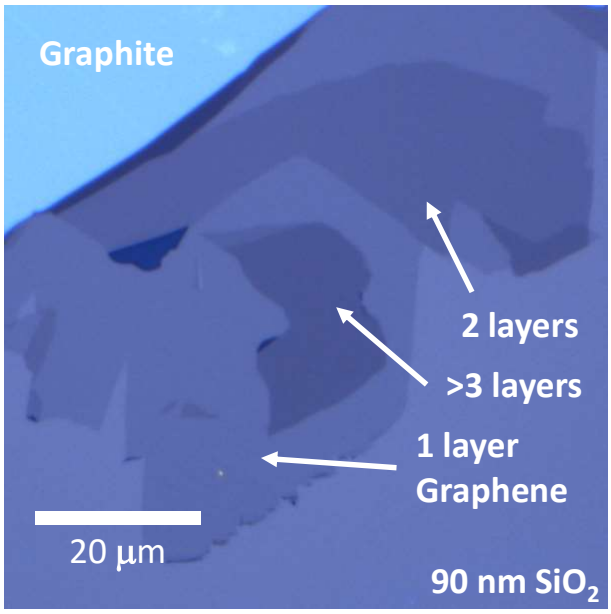

Fig. 5-1 Optical image of exfoliated graphene in single layer and few layers

This formation process was developed to increase the size and number of graphene for experiment use. These improvements are including using customized tapes and SiO_2 ashing process [7]. Despite that graphene is invisible due to its one layer atom thickness, graphene has small contrast to substrate on a 90 nm, 285 nm, 300 nm SiO_2 that can be distinguished under optical microscope [8]. Graphene has highest contrast under green light and its layer number can be determined the contrast [9]. It provides a very convenient method to find graphene and confirm the layers. The optical image of fabricated graphene is shown in Fig. 5-1.

5.2.2 Chemical-Vapor-Deposition graphene

CVD graphene is synthesized by using CH_4 and H_2 as source on Cu or Ni substrate as catalyst at high temperature [2]. By controlling deposition time and other parameter, the layer number can be managed in or multilayer or double layer even single layer. After the growth, a polymer, usually using PMMA (Polymethylmethacrylate) is coated on the

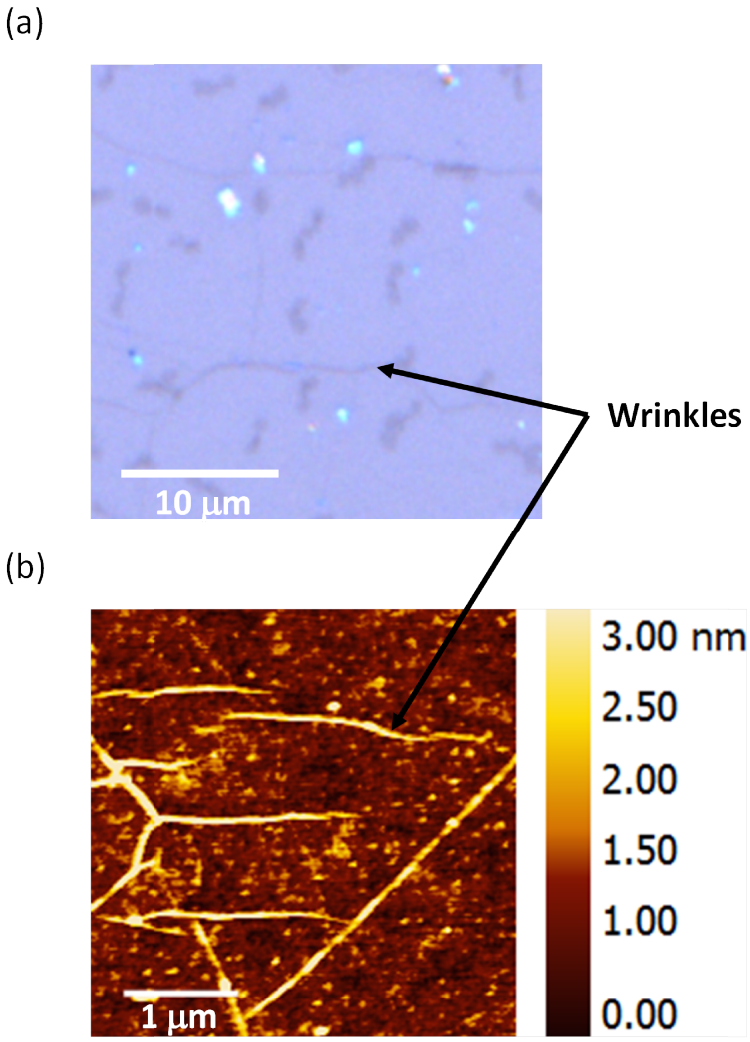

Fig. 5-2 (a) Optical and (b) AFM image of CVD graphene

graphene side as a mechanical support. After etching of the metal catalyst, graphene can be transfer to any other substrates. CVD graphene in this study shows wrinkles and metal contaminations on the surface as shown in Fig. 5-2. It is because of the metal etching and transfer process.

5.3 Formation of electrodes

Contact resistance of graphene-metal plays an essential role in operation of graphene

TBJ which can cause not only the voltage lost but also the asymmetry in nonlinear characteristics as discussed and demonstrated in chapter 4. The process of formation electrodes for graphene has not been established yet. Two main issues are still under investigation. First one is how to achieve clean graphene-metal interface. The fabrication of electrode usually involves organic resist. After the resist is coated on graphene sample and exposed to electron beam or UV light for patterning, the developing process will remove exposed resist to form electrode window. This developing process will possibly leave resist on the surface of graphene. After metal deposition, resist residual becomes a barrier between graphene and metal, effectively reduces the contact area. Number of methods were reported such as plasma clean and UV clean of the graphene surface in pattern window, but they also brings damage to graphene [10-12]. In this study, the process condition was optimized to achieve a clean graphene-metal interface.

The electrode formation starts from the electrode patterning by electron beam lithography (EBL) as below. After cleaning process of samples, a positive EB resist ZEP520A (Zeon Corp.) was spin-coated on the sample. The samples then proceed a softbake to evaporate the solution of resist. The designed pattern was exposed under proper dose on the resist of sample. After pattern drawing, the sample was developed in ZED-50N and rinsed in 2-propanol (IPA). An atomic force microscope (AFM) observation was conducted at this point to ensure that before the metal deposition the surface of graphene in open window region is clean. The AFM image as Fig. 5-3(a) shows that the graphene surface after developing was covered by resist spots and grains. The average height was 1.4 nm and RMS was 0.67 nm. Accordingly optimizations were carried focusing on softbake time and temperature, expose doze and developing time to

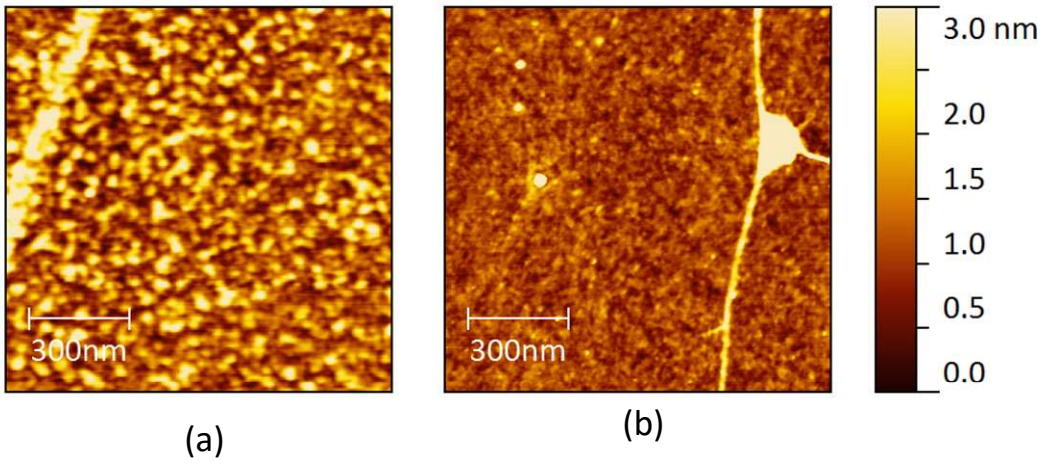

Fig. 5-3 Graphene surface in developed pattern (a) before and (b) after optimization

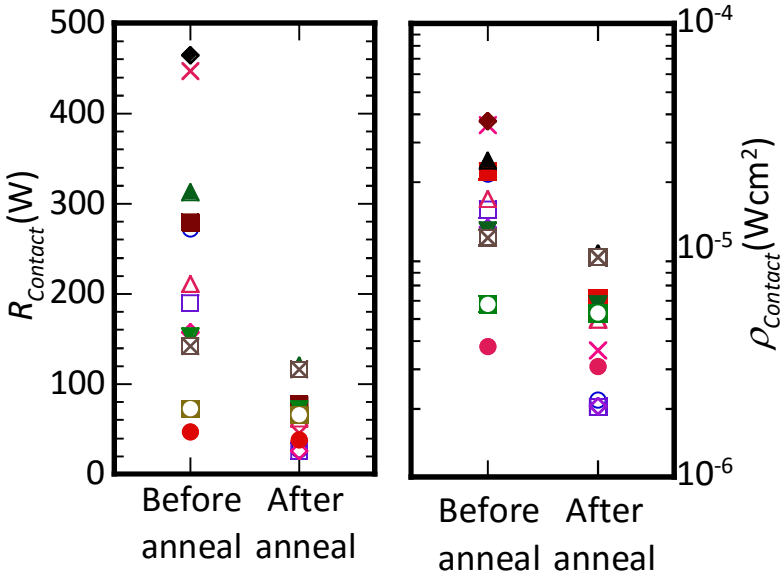

Fig. 5-4 Measured contact resistance and resistivity after optimizing process

reduce resist residual. Though the results were inconclusive, trends was observed that lower softbake time and temperature, higher doze and longer developing time result a clean graphene surface. In our process, we used 2min 170 ℃ oven soft bake at proper dose and 1min developing. The result is as shown in Fig. 5-3(b) that the average height was reduced to 1.2 nm and RMS was 0.28 nm which was quit clean surface.

The second issue are which metal to use. Theory and experiment data suggest that Ti, Ni and Pd have lower contact resistivity due to their good wetting and strong interaction with graphene atoms [13-15]. Here we investigated two metal materials: 40 m PtPd alloy deposited by sputtering and 10nm/50nm Ni/Au deposited by electron beam evaporation were investigated using CVD graphene. The contact resistance was characterized using the cross-bridge Kelvin method [16]. The contacts using the PtPd metal exhibited nonlinear current-voltage characteristics. The contact resistivity was approximately 8×10^{-5} Ωcm^2. This is probably because of poor deposition environment, large metal grain size, and damage induced in graphene sheet [16,17]. However Ni/Au contacts showed lower contact resistance less than 500 Ω for 2×2 μm^2 and the resistivity distributed around 2×10^{-5} Ωcm^2. Furthermore, after 450 °C annealing for 5 min, the resistivity was reduced by 1/5 as summarized in Fig. 5-4. The obtained value was reasonably agreed with the reported values [5]. Though this value is still larger than required one [5], the contact resistance can be reduced further by increasing contact area. Further fabrication technique has to be investigated.

5.4 Formation of T-shape channel

The pattern of a TBJ channel was written on the sample with ZEP520A resist by EBL. After developing and rinse, the sample was etched by reactive ion etching (RIE) machine (RIE-10NR, Samco Inc.). The etching conditions are gas O_2 20sccm, pressure 20 Pa, and power 100W. The etching time was investigated for both resist and graphene. ZEP520A shows a etching rate as 7 nm/s at such condition. For graphene made by exfoliation, it takes about 6s to etch one layer. But for CVD-grown graphene, it only

takes 3s. Hence the proper etching time was chosen as 10s in case of 300 nm resist.

5.5 Control of charge neutral point

After the process as stated above, the surface and interface of graphene were usually attached by impurities and contaminations such as resist residual. These residuals act as fix charges inducing impurity carriers and shift the charge neutral point beyond measure rang. A number of cleaning processes were proposed such as vacuum anneal, current anneal, hydrogen anneal and so on [18]. The basic idea is that using thermal energy to decompose the organic residual. Through these method the contaminations on the surface of graphene can be removed, the interface remains unprocessed. On the other hand the chemical doping was useful in research level experiment to control the charge neutral point of graphene [19]. Mostly fabricated graphene device exhibited charge neutral point over 40 V indicating that the residuals act as negative charges and induce holes when gate is 0 V. Thus a polycationic polymer called Polyethylenimine (PEI) was employed as chemical doping. By immersing sample in PEI solution and rinse in ethanol, self-determined amount of PEI covers on sample to cancel the negative charges of residuals. So the procedure in this study was annealing samples at 250ºC ~ 300ºC for 1 hour in N_2, and then carrying out PEI doping process.

5.6 Fabrication process flow

The fabrication process flow is summarized. Firstly the graphene was exfoliated from graphite on a 90 nm SiO_2 substrate. Then after clearing out large graphite residuals, a set of marker was fabricated on the sample by EBL, PtPd sputtering deposition and lifting

off process. Secondly the metal electrodes were fabricated by EBL and Ni/Au electron beam deposition following lift off. Thirdly the T-shape channel was patterned and etched by EBL and RIE. Before chemical doping, the sample was annealed at 300ºC in N_2 for 1 hour. Chemical doping was proceed as immersing the sample in PEI solution for few hours, and then rinsing sample in 70ºC ethanol.

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Chapter 6 Characterization of fabricated graphene TBJ

6.1 Introduction

Utilizing the optimized processes as described in chapter 5, a graphene TBJ device was fabricated using exfoliated graphene with Ni/Au electrodes. The device was observed by AFM to confirm the size and surface states. Then electrical measurements were conducted by semiconductor device parameter analyzer (Agilent B1500A) and digital phosphor oscilloscope (Tektronix DPO 5104) in ambient at room temperature.

6.2 Characterization of graphene channel

Fig. 6-1 shows the AFM phase image of fabricated device. The device cannot be identified under AFM height image considering the surface was heavily covered by PEI and impurities. The length and width of each branch are both 300nm making the total left-right channel length of 900nm.

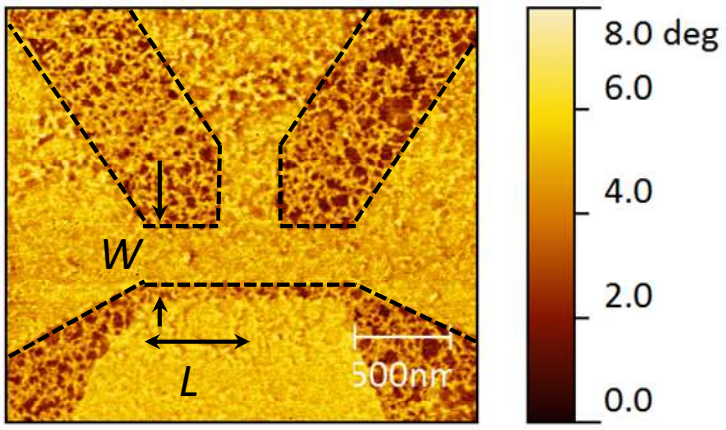

Fig. 6-1 AFM phase image of fabricated graphene TBJ.

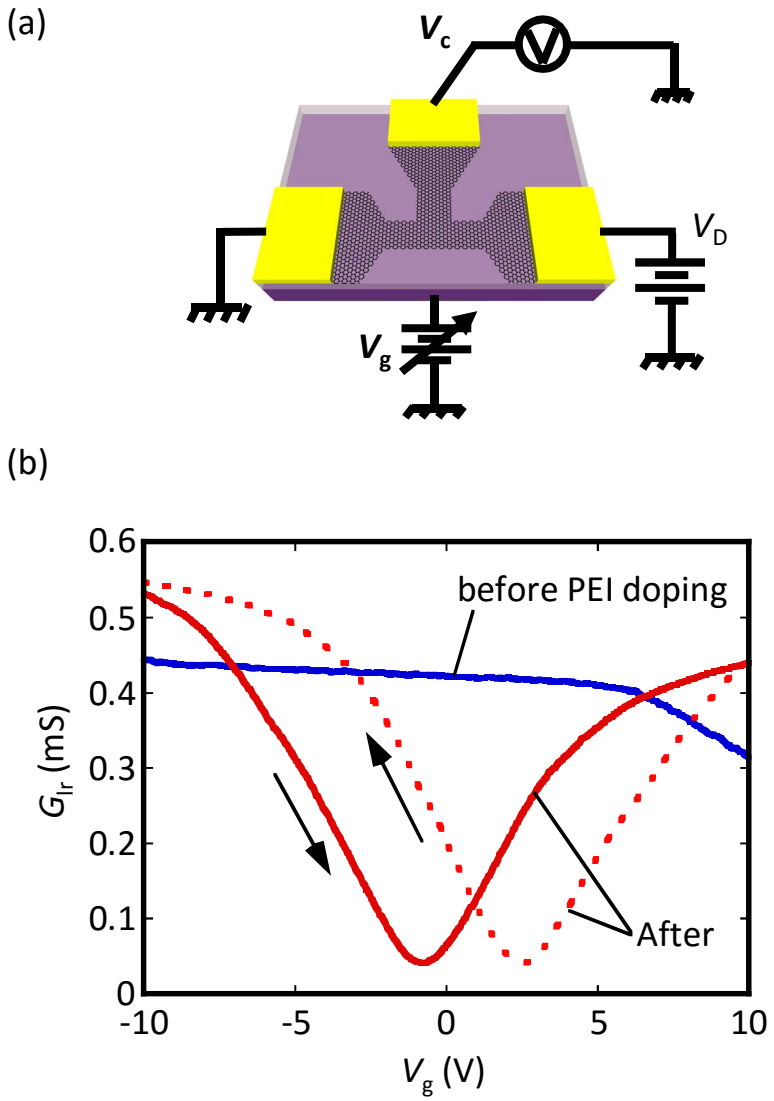

Fig. 6-2 (a) The setup and (b) conductance gate transfer characteristics of fabricated graphene channel

Then the graphene channel was characterized by measuring the current gate voltage transfer characteristic of left-right channel as the setup in Fig. 6-2(a). The left-right channel conductance shown in Fig. 6-2(b) is calculated from measured currents divided by applied drain voltage (0.02 V and 0.1 V for before and after doping data) is shown in Fig. 6-2(b). The charge neutral point was shifted by the PEI from over 10 V to -1 V. After PEI doping, the conductance G_{lr} -gate voltage plot shows ambipolar

characteristic of graphene. A 3 V hysteresis width of G_{lr} - V_g was observed which indicates the existence of charge traps. They may be from PEI, impurity or SiO_2 substrate. For this reason the charge neutral point may be lightly shifting during the measurement. The contact resistance is estimated by the contact resistivity as shown in chapter 5 and the contact area as 50 Ω each. Therefore the current saturation at high V_g may be arose by the graphene sheet resistance under/near electrodes [1] or by the surface/interface charge traps [2]. By fitting the current formula of graphene as Eq. (4.5), $W\mu C_g/L$ = 0.69 $FV^{-1}m^{-1}s^{-1}$, V_{Dirac} = -0.80 V, and β = 0.79 V were achieved. Therefore effective mobility μ of graphene was estimated at 5,625 $cm^2V^{-1}s^{-1}$ for both hole and electron for 90 nm SiO_2 substrate.

6.3 Nonlinear voltage transfer characteristics

The nonlinear voltage transfer characteristics of fabricated graphene TBJ are shown in Fig. 6-3 with the measurement configuration. Under the push-pull fashion biases, the curves showed clear parabolic relation without incline. They were well controlled by V_g. The polarity of the curves was switched between V_g = 1 V and 2 V where the charge neutral point is located. The absolute value of the curvature decreased as the gate voltage departed from the V_{CNP} as predicted in chapter 4.

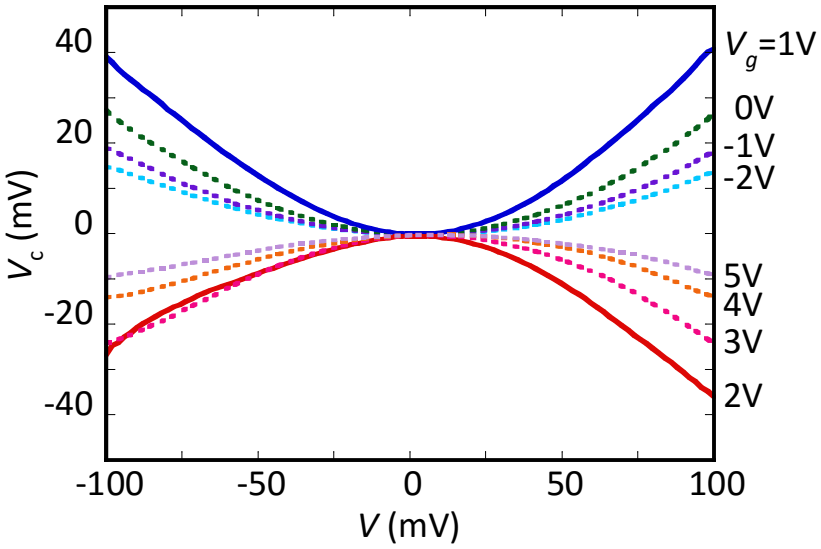

Fig. 6-3 Measured nonlinear voltage transfer characteristics

6.4 AND/OR gate operation

The AND/OR gate operation was examined by inputting logic voltage signals with a 200 mV amplitude to the left and right branches as the schematic shown in Fig. 6-4(a). Fig. 6-4(b) shows the measured inputs and outputs waveforms. The results confirmed that the device was operated as OR gate at V_g = 0.7 V and AND gate at V_g = 0.7 V, each corresponding to hole and electron conductions, respectively. By only changing the back gate voltage, the function of graphene TBJ device was altered between AND gate and OR gate. This confirmed the configurability of graphene TBJ.

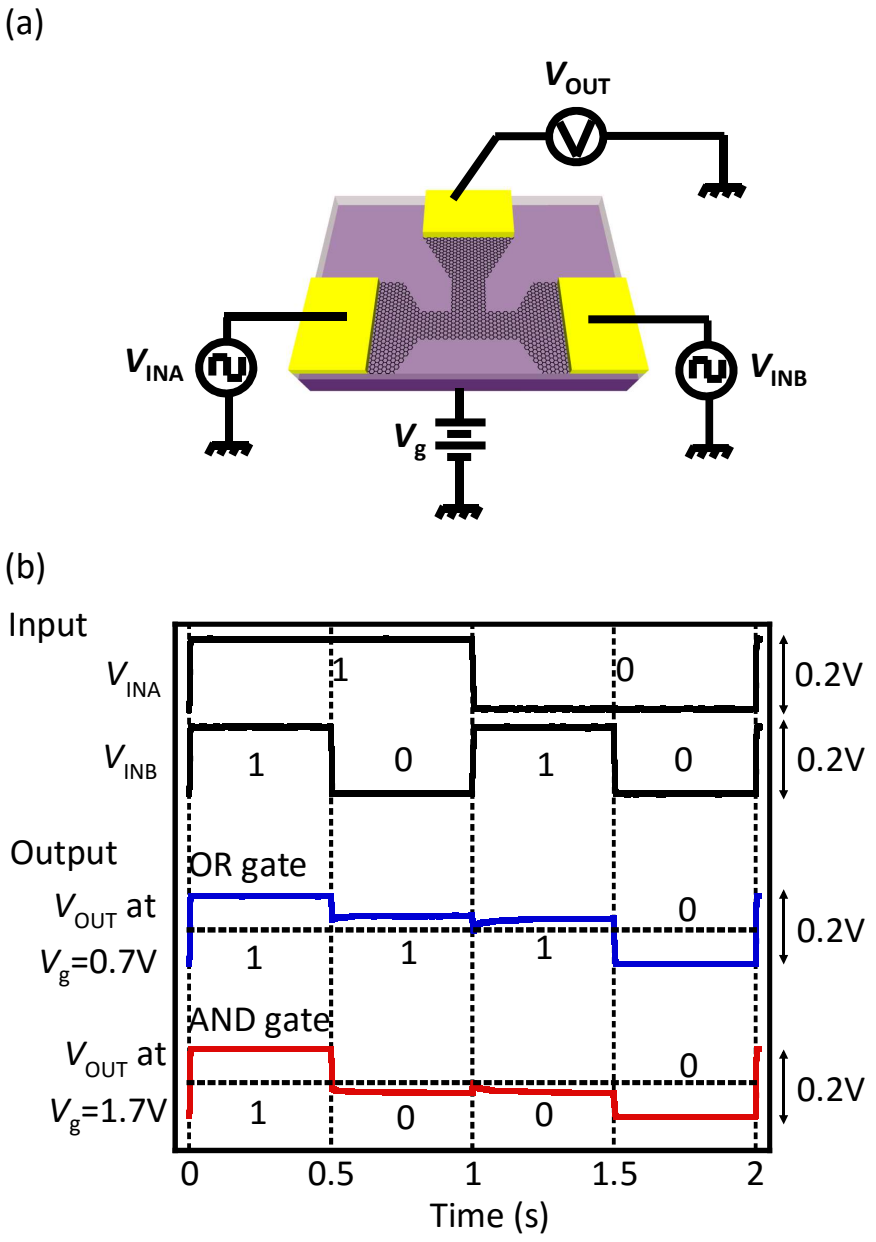

Fig. 6-4 (a) Measurement configuration and (b) waveforms of AND/OR gate in fabricated graphene TBJ

6.5 NOT gate operation

In the measurement mentioned in section 6.2, the simultaneously obtained V_c and its differential to gate voltage are shown in Fig. 6-5(a). The polarity of V_c was inversed when V_g crossed V_{CNP}, consequently achieving minus gain at threshold voltage of -0.65 V which equals to V_{CNP} exactly. This inverter transfer characteristic indicates that graphene TBJ can operate as NOT gate though the maximum gain is -0.036 at V_g = -0.8 V with V_d = 0.1V.

Next a waveform was applied on back gate to demonstrate the NOT gate operation. The input waveform is set 1 V amplitude and -0.8 V offset to match the threshold voltage in inverter characteristic. Fig. 6-5(b) shows the output waveform from V_c comparing to the input of V_g. Through the graphene TBJ the phase of input signal at V_g is shifted 180 degrees at the output. Therefore NOT gate operation was achieved by a single graphene TBJ device.

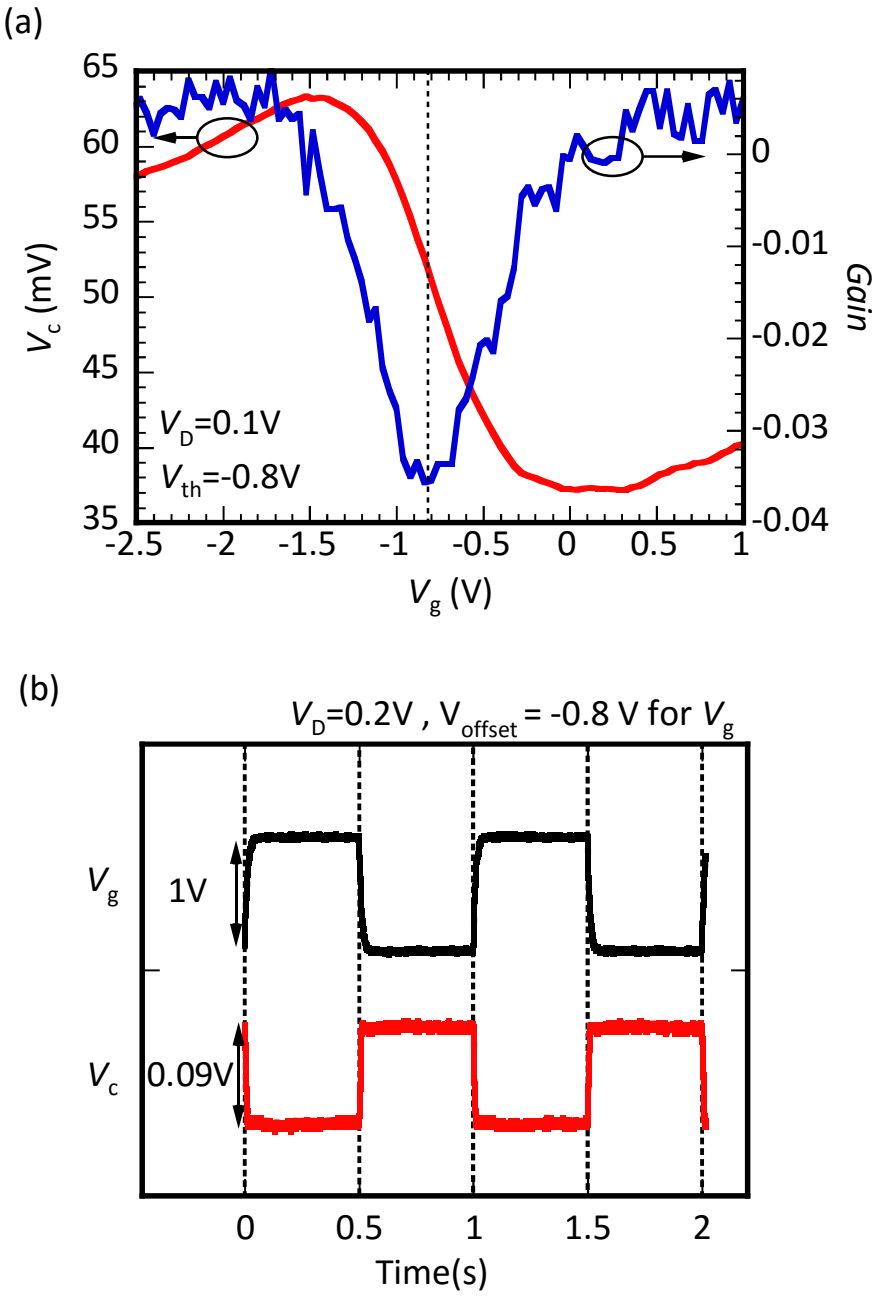

Fig. 6-5 Measured (a) inverter characteristics and (b) waveform of NOT gate operation.

6.6 Discussions

Firstly the symmetry of achieved nonlinear characteristics is evaluated with the asymmetry factor at different gate voltage as Eq. (4.11) in chapter 4. V_c values were chosen at V= -100 mV and 100 mV. The results are shown in Fig. 6-6 for nonlinear characteristics of process optimized device in Fig. 6-3 and unoptimized one in Fig. 4-6(a). The calculated curves from Eq. (4.12) are also shown in Fig. 6-6 which could explain the experimental curves reasonably well. In unoptimized device, Δ was increased as V_g increased and reached as high as 30%. On contrary, Δ from the process optimized contact showed very low value even less than 2% at V_g - V_{CNP} = 4V. It proves that for process optimized device, the contact resistances on left and right side is identical. A slight asymmetry was observed for process optimized device at V_g - V_{CNP} = 1 V in both Fig. 6-3 and Fig. 6-6. The asymmetry appeared only near V_{CNP} fits the profile of Dirac point asymmetry as discussed in chapter 4 and Eq. (4.20). It is

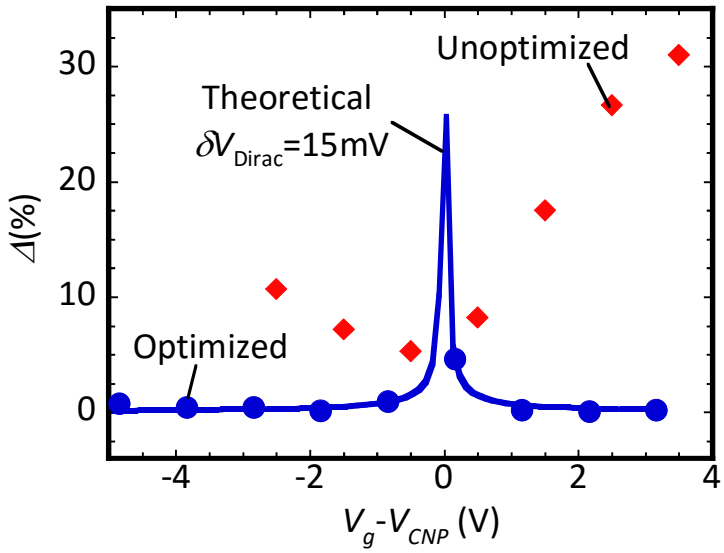

Fig. 6-6 Comparison of asymmetry factors before and after process optimization.

reasonable due to inhomogeneous distribution of PEI and residual charges. Generally ideal nonlinear voltage transfer characteristics were achieved in this highly symmetric graphene TBJ device due to optimization of process.

Next the performance of graphene TBJ is discussed with the gradual channel approximation (GCA) model as introduced in chapter 4. A major issue is that the outputs V_c of nonlinear characteristic, also equaling to the logic output swings of AND/OR gate, were only 40 mV for 100 mV input which is small for applications. The input-output equation as Eq. (4.7) from GCA model indicates that the only term effecting V_c is $\beta = en_0/C_g$ which is interpreted as the gate voltage required for switching between hole and electron. Fig. 6-7 shows the maximum output ratio $r_{max} = V_{c,max}/V \times 100\%$ at proper gate voltage changing with β. It clearly show that the r_{max} increases with reducing β, but saturates at 50% due to coexistence of electron and hole at Dirac point. Meanwhile experimentally obtained r_{max} are also shown in Fig. 6-7. It confirms the effect of reducing β in increasing r_{max}. The experiment result in this work is higher the theoretical one which might be due to the approximation and other neglected elements in the model. This value is the largest r_{max} for now and already close to the max limit. In order to break through this limit, the coexistence of electron and hole has to be eliminated by inducing bandgap in graphene.

Another issue is the low gain of graphene TBJ in NOT gate operation. The theoretical gain can be derived by taking the partial derivative of V_g for Eq. (4.7) and expanding its Taylor series at threshold voltage as

$$Gain = \left(\frac{dV_c}{dV_g}\right)_{max} = 1 - \sqrt{1 + \left(\frac{V_D}{2\beta}\right)^2} \,. \tag{6.1}$$

For a constant power voltage, reducing β will rapidly increase the gain over unity as

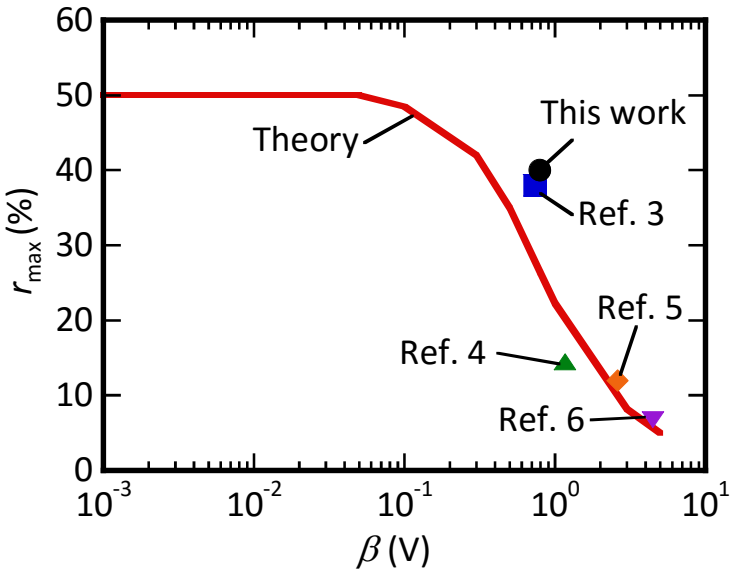

Fig. 6-7 The maximum input-output ratio varies with β.

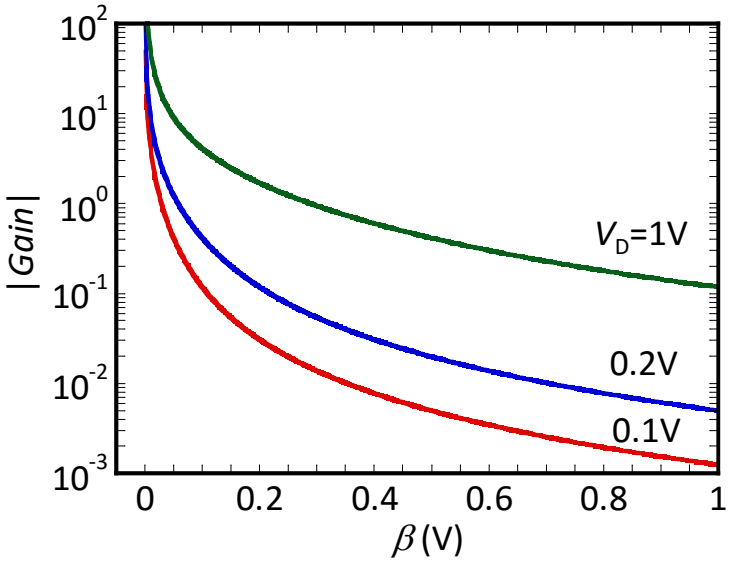

Fig. 6-8 Inverter gain varies with β.

shown in Fig. 6-8. The experimental approach for reducing β can be accomplished by increasing the gate capacitance in a top gate structure, or reducing n_0 in a bandgap graphene channel.

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Chapter 7 Further enhancement in nonlinearity and gate controllability

7.1 Introduction

As discussions in chapter 6, a small bandgap is demanded for improving both output swing of nonlinear characteristic and the gain of inverter operation. The value of this bandgap has to be carefully investigated because there is trade off for other factors. The larger band gap is, the more output and gain of graphene TBJ will be improved meanwhile the more difficult experimental process becomes to achieve such bandgap even less losing the reconfigurability. Therefore a model of bandgap introduced graphene TBJ is needed and investigated to determine the relationship between bandgap and output of nonlinear characteristic. Then a experimental approach is desired to attain such band gap in graphene. In this process, a few fabrication techniques can be further improved.

7.2 Band opening in graphene TBJ

7.2.1 Model and calculation results

A band gap introduced graphene can be considered as other small bandgap materials [1,2]. The symmetry of effective mass and band structure for hole and electron is still valid for such graphene. However the *E*-*k* dispersion should become parabolic as other semiconductors [3]. Then it is reasonably assuming that the intrinsic energy E_i is located in the middle of band gap E_g. The band diagram in a MOS structure is depicted in Fig. 7-1. For gate voltage is positive, the gate potential is dropped on oxide and graphene

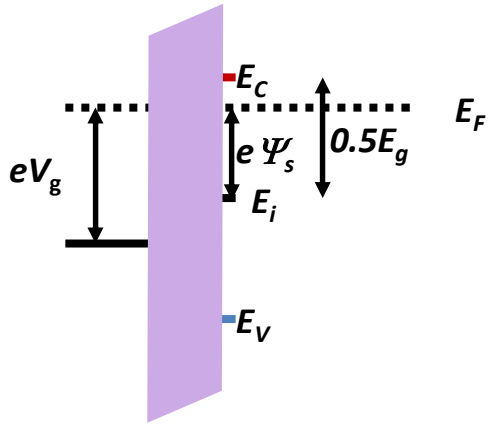

Fig. 7-1 MOS structure of a small bandgap graphene TBJ

channel. The carrier density induced on oxide is given as

$$n_s = C_g\left(V_g - \Psi_s\right)/e, \tag{7.1}$$

where Ψ_s is the surface potential changed by gate voltage. This amount of charges is exactly equal to the charges induced in graphene channel. And the amount of charges for electrons can be approximated for non-degenerate limit (E_C-E_F<3k_BT) as

$$n_s = \int N(E)F(E)dE \approx N_C e^{\frac{E_F - E_c}{k_BT}} = N_C e^{\left(e\Psi_s - 0.5E_g\right)/k_BT}. \tag{7.2}$$

where N_C is effective density of state [3]. By replacing Ψ_s in Eq. (7.2) with Eq. (7.1), the bandgap can be expressed as

$$E_g = 2e\left(V_g - \frac{en_s}{C_g}\right) + 2k_BT\ln\left(\frac{n_s}{N_C}\right). \tag{7.3}$$

Here the threshold voltage is defined as the gate voltage the carrier density is zero. Since the symmetry for electron and hole, the threshold voltages are $V_{th,n} = V_{th}$ and $V_{th,p} = -V_{th}$ ($V_{th} > 0$ V), respectively. As a result, the relation between bandgap E_g and V_{th} can be derived as

$$E_g = 2eV_{th} + 2k_BT. \tag{7.4}$$

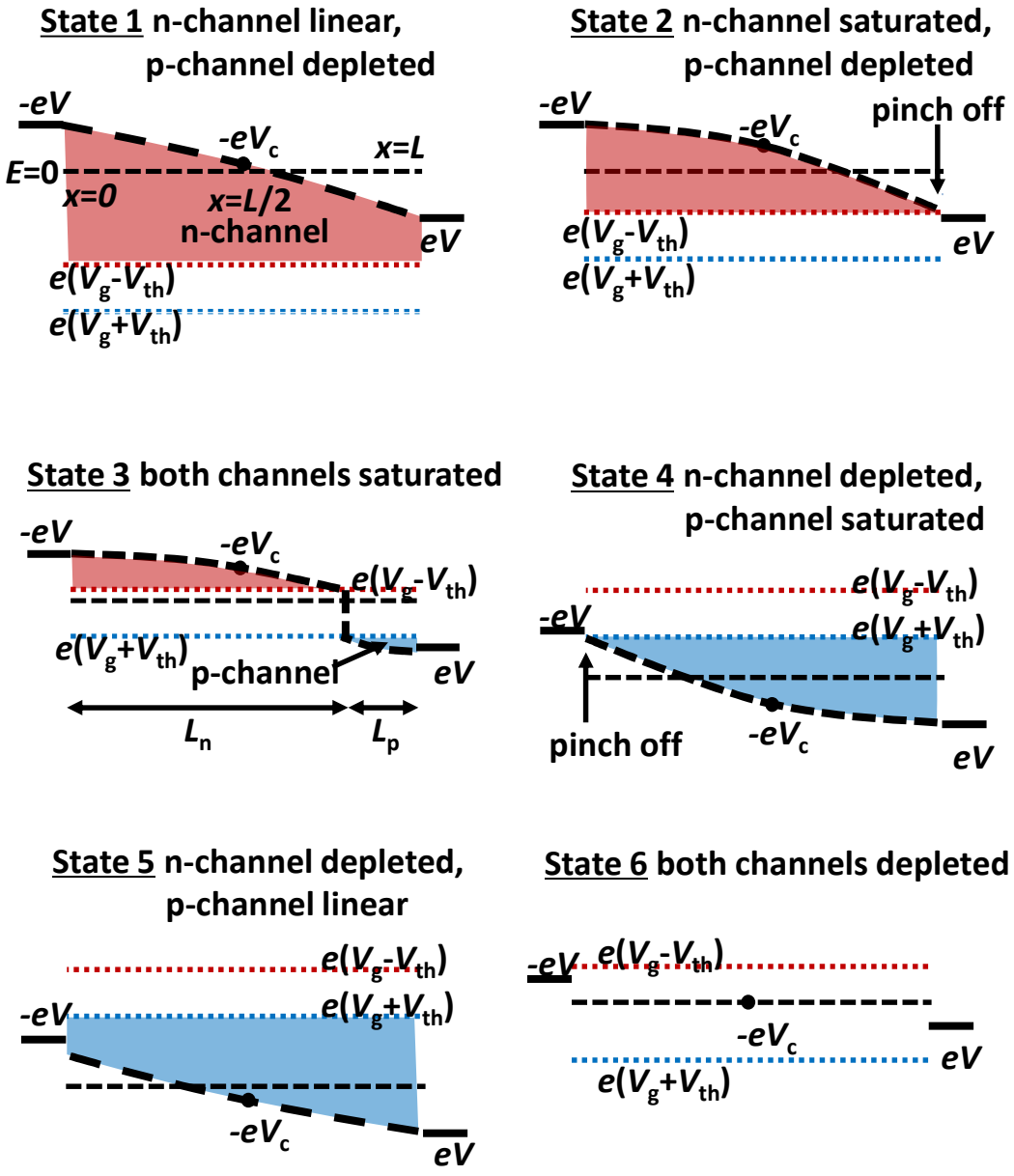

Fig. 7-2 Six states in small bandgap graphene TBJ

Basing on the gradual channel approximation as introduced in chapter 4, bandgap introduced graphene TBJ device is analyzed in six divided states according to operation condition as shown in Fig. 7-2.

State 1: $V < V_g - V_{th}$

In this case, the p-channel is depleted and only electrons contribute to the

current. The current is linearly controlled by applied voltage V. The carrier density is given by the formula as

$$n(V(x)) = C_g\left(V_g - V_{th} - V(x)\right)/e. \tag{7.5}$$

The current is evaluated similarly to Eq. (4.5) as

$$I = \frac{W\mu C_g}{L}\int_{V_l}^{V_r}\left(V_g - V_{th} - V(x)\right)dV(x)$$

$$= \frac{W\mu C_g}{L}\left[\left(V_g - V_{th}\right)\left(V_l - V_r\right) - \frac{1}{2}V_l^2 + \frac{1}{2}V_r^2\right]. \tag{7.6}$$

Current in the push-pull bias operation is evaluated by replacing V_l and V_r with -V and V, respectively. It is given as

$$I = \frac{W\mu C_g}{L}\left(V_g - V_{th}\right)\cdot 2V. \tag{7.7}$$

From Eq. (4.7) together with Eq. (7.6) and Eq. (7.7), V_c becomes

$$V_c = \left(V_g - V_{th}\right) - \sqrt{\left(V_g - V_{th}\right)^2 + V^2}. \tag{7.8}$$

State 2: $-V < V_g - V_{th} \le V < V_g + V_{th}$

In this case, the n-channel current is saturated. The p-channel is again depleted and does not contribute to the current. When the n-channel is saturated, the channel length modulation is ignored and it is assuming that most of the voltage is applied to the pinch off point in the positively biased branch. Then V_c only depends on the voltage in the negatively biased branch. The saturation current in the push-pull bias operation is obtain by substituting $V_r = V_g - V_{th}$ and $V_l = -V$ in Eq. (7.6) as

$$I = \frac{W\mu C_g}{L}\frac{1}{2}\left(V_g - V_{th} + V\right)^2. \tag{7.9}$$

Again V_c is obtained using Eqs. (4.7), (7.6) and (7.9).

$$V_c = \left(V_g - V_{th}\right) - \frac{\sqrt{2}}{2}\left(V_g - V_{th} + V\right). \tag{7.10}$$

This equation has a different from Eq. (7.8).

State 3: $-V \le V_g - V_{th} < V_g + V_{th} \le V$

In this case, both n- and p-channel are in the saturation region. The pinch off point starts to move from the positively biased branch to another branch. The channel is divided by the pinch off point into a n-channel with the length of L_n and a p-channel with the length of L_p. Here the length corresponds to the distance from the branch edge to the pinch off point. The depletion length between n-channel and p-channel is ignored here due to high electric field in long channel. Assume that electron and hole parallel conduction in the p- and n-channel does not take place owing to the bandgap, the current continuity gives the relationship as follows.

$$I_{sat} = \frac{WC_g\mu}{L_n}\frac{1}{2}\left(V_g - V_{th} + V\right)^2 = \frac{WC_g\mu}{L_p}\frac{1}{2}\left(V_g + V_{th} - V\right)^2. \tag{7.11}$$

With the relation of $L = L_n + L_p$, I_{sat} can be rewritten as,

$$I_{sat} = \frac{W\mu C_g}{L}\left[V_g^2 + \left(V_{th} - V\right)^2\right]. \tag{7.12}$$

When $L_n > L_p$, the pinch off point is between the center of the junction and the positively biased branch. V_c is still dominated by the voltage in the negatively biased branch. From Eq. (7.6) and Eq. (7.12), V_c is given as

$$V_c = \left(V_g - V_{th}\right) - \sqrt{2V_g\left(V - V_{th}\right)}. \tag{7.13}$$

When $L_n = L_p$, the pinch off point reaches the center of the junction and the conductance of the left and right branches are in the same. Then $V_c = 0$ V. When $L_n < L_p$, V_c is obtained similarly to the case of $L_n > L_p$ as

$$V_c = \left(V_g + V_{th}\right) + \sqrt{2V_g\left(V_{th} - V\right)}. \tag{7.14}$$

State 4: $V_g - V_{th} < -V < V_g + V_{th} \le V$

In this case the n-channel is depleted and the p-channel is saturated. This situation is similar to State 2. V_c is derived as

$$V_c = \left(V_g + V_{th}\right) - \frac{\sqrt{2}}{2}\left(V_g + V_{th} - V\right). \tag{7.15}$$

State 5: $V_g + V_{th} \leq -V$

In this case the n-channel is depleted and the p-channel is in the linear region. V_c is derived similarly to state 1 as

$$V_c = \left(V_g + V_{th}\right) + \sqrt{\left(V_g + V_{th}\right)^2 + V^2}\ . \tag{7.16}$$

State 6: $V_g - V_{th} < -V$ and $V < V_g + V_{th}$

In this case, both the n-channel and p-channel are depleted. Then no current flows and V_c is floating. In this calculation, V_c is zero.

On the basis the 6 states above, the V_c-V_g curve is calculated and the results are plotted in Fig. 7-3. When V_{th} = 0 V, the curve equals to the maximum V_c of Eq. (4.7). Increasing V_{th} from 0 to 90 mV, the peak of $|V_c|$ is largely increased from 0.5×V to 0.95×V. The peak of $|V_c|$ exists in State 3. By taking the maximum in Eq. (7.13) or Eq. (7.14), we have the optimal gate bias and the maximum value of $V_{c,max}$ such as

$$\begin{aligned} \left|V_g\right| &= 0.5\left|V - V_{th}\right| \\ r = \left|V_{C,\max}/V\right| &= 0.5\left|1 + V_{th}/V\right| \qquad V_{th} < V \end{aligned} \tag{7.17}$$

Eq. (17) reveals that V_c can be increased up to V by adjusting V to V_{th}. However V_{th} cannot be larger than V otherwise the channel is depleted as in State 6..

Nonlinear characteristics of the graphene TBJ with bandgap are plotted in Fig. 7-3(b). The nonlinearity is enhanced by increasing V_{th} from 0 to V. V_c suddenly drops when V_{th} = 0.5 V and 0.9 V. This is caused by insufficient bias to inject the carriers.

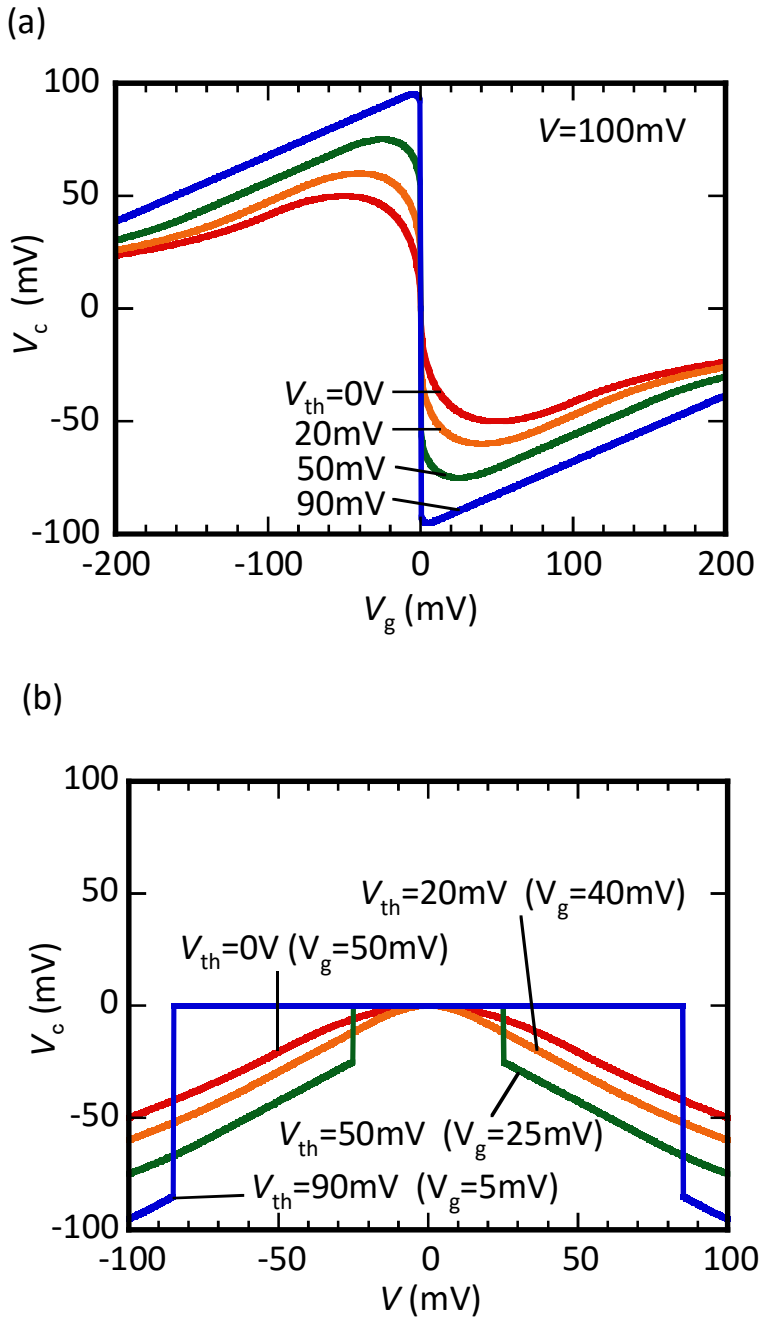

Fig. 7-3 Calculated (a) inverter transfer characteristics and (b) nonlinear transfer characteristics in small bandgap graphene TBJ.

7.2.2 Experimental approach

Eq. (7.4) and Eq. (7.17) suggest that in order to obtain high output ratio *r* as 90% at

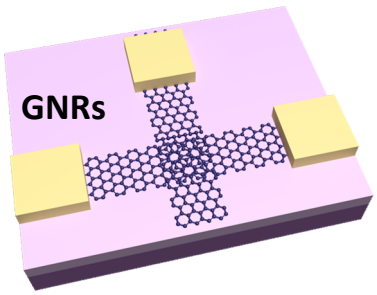

Fig. 7-4 Schematic of proposed graphene TBJ based on GNR crossbar

room temperature, the bandgap should be larger than twice of k_BT = 26meV. Moreover V_{th} needs to be 80% of V. For operating at V = 50 mV, the bandgap should be 100 meV. This value is easily achieved by the use of graphene nanoribbon (GNR). Previous investigations both theoretically and experimentally proved that a bandgap up to 200 meV can be achieved by tuning the width of GNR in ones to tens of nanometers [4-6]. However the carrier mobility was severely decreased in the GNR fabricated by the lithography and etching due to the edge scattering. Another damage-free method for formation of GNR is unzipping carbon nanotube (CNT). This GNR showed ultra-smooth edge and high mobility [6]. Furthermore the GNR exhibits a large bandgap by functionalization by dispersing single molecules [7]. A possible configuration of the graphene TBJ using the GNR is schematically shown in Fig. 7-4, where a GNR crossbar is used as a junction.

7.3 Process improvement

The fabrication of graphene nanoribbon crossbar TBJ is much more challenging than that of normal graphene TBJ. Besides the random distribution and low possibility of existence of GNR crossbar, the most critical issues for such small-scale device are

achieving good metal contact of electrodes and homogeneous surface charge distribution.

To make a good metal contact with GNR, first of all the surface of GNR after electrode patterning require extreme cleanness since the contact width and area is already shrink to tens nano order. Any kind of organic molecular between metal and GNR will further reduce the contact area. Then the contact property of metal and GNR need more thorough investigations including theoretical simulation of 3D-1D material contacting and experimental research of transfer length and so on.

Meanwhile surface potential fluctuation in 1-D material with a bandgap will easily create quantum dots and exhibiting single electron behavior which will bury the intrinsic properties of a GNR crossbar [8]. One of the most common reasons for having such fluctuation is the impurity charges from resist residuals and other organic molecules. Especially the EB resist ZEP520A seems having large Van der Waals force with substrate and graphene that cannot be easily removed. In addition Poly[(m-phenylenevinylene)-co-(2,5-dioctoxy-p-phenylenevinylene)] (PmPV) is added in the solution in order to disperse GNRs. Experiment showed that after casting GNRs on a ZEP520A coated and removed substrate large grains of molecules were observed. It indicated that ZEP520 and PmPV attracted each other to form a large and resistive molecular gathers. These molecules even would not decompose at 600 ºC. It is possible because ZEP520 has phenyl group in the molecules increasing its resistance [9]. An alternative EB resist is Polymethylmethacrylate (PMMA). PMMA is a simple-structure organic molecule which has low melting point of 160 ºC and decomposing temperature as 450 ºC. Further tests are required for PMMA.

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Chapter 8 Conclusion

In this thesis we proposed analysis models for the graphene TBJ device. After process optimization, we fabricated a graphene TBJ. We achieved superior nonlinear voltage transfer characteristics in a graphene TBJ device. Moreover the AND/OR gate and NOT gate logic function have been demonstrated based on the nonlinear behavior and its gate controllability. To further improve the performance of graphene TBJ, experimental results were analyzed and discussed based on the models. A new structure of graphene TBJ using graphene nano-ribbon (GNR) crossbar was discussed.

Chapter 1 introduced the current technology development in information process systems and its trend in the future. It pointed out that a novel device based on new material and mechanism is highly expected. As an candidate, graphene three branch nano-junction was introduced due to its simple structure, possibility of high speed operation and unique nonlinear transfer characteristic which operates as Boolean logic gates. The current status of graphene TBJ has been stated that due to lack of proper fabrication techniques and handy analysis model, an ideal nonlinear characteristic has not been demonstrated yet, not speaking of its logic gate operation. The purpose of this thesis is to fill in the blank of graphene TBJ.

Chapter 2 explained the birth and progress of semiconductor TBJ device and provided the principles of the TBJ nonlinear mechanism and operations for analysis.

Chapter 3 described the basic band and electrical properties of graphene which are beneficial for TBJ. A simple experimental formula for graphene carrier density was introduced which is very convenient in the later models.

Chapter 4 discussed two kinds of analysis model for graphene three-branch

nano-junction device that we proposed. One of them was based on a simple capacitor model of left and right branch in a graphene TBJ and exhibited reasonable result of nonlinear characteristics. Then the asymmetry in contact resistance, geometry and neutral charge point of left and right branches in a graphene TBJ were discussed with acceptable approximations. Results addressed the importance of symmetry and provide valuable judgments in evaluating experimental data. The other model was based on gradual channel approximation model to give qualitative detail and essentials of graphene TBJ. It showed that the gate capacitance and the minimum carrier density of graphene are the key point to the nonlinear characteristic. These models have been proved very useful in examining experimental result and providing device modification principles in later chapters. Then the possibility of a graphene TBJ operating as Boolean logic device was described.

Chapter 5 gave descriptions of fabricating a graphene TBJ device. The details of the fabrication procedure including graphene formation, optimization of electrode fabrication, and Dirac point control were explained.

Chapter 6 exhibited the experimental results of fabricated graphene TBJ. Owing to these analysis and process improvement, we achieved superior nonlinear voltage transfer characteristics in a graphene TBJ device. Moreover the AND/OR gate and NOT gate logic function have been demonstrated based on the nonlinear behavior and its gate controllability. It confirmed the Boolean logic function of graphene TBJ. The output swing and inverter gain were small in fabricated device. By analyzing the models comparing to the experimental results, we clarified that the output swing has almost reached the theoretical limitation of graphene TBJ due to the existence of minimum carrier density in graphene. The small gain was also believed for the same

reason.

Chapter 7 discussed the principle and method of improving performance of graphene TBJ. In order to resolve the issue pointed out in chapter 6, an bandgap introduced graphene TBJ was investigated theoretically. By building its model similar to chapter 4, we confirmed that in a bandgap introduced graphene TBJ both the output swing and inverter gain can be enhanced for proper biases. Then an experimental approach was proposed as graphene TBJ based on graphene nanoribbon crossbar. Also some critical aspects and solutions of fabricating such device was pointed out. These modeling and fabrication technique in this thesis will promote the development not only for graphene TBJ device but also for other devices based on graphene.

List of publications/conferences/awards

Publications

Journals

(1) X. Yin, and S. Kasai: “Graphene-based Three-branch Nano-junction (TBJ) Logic Inverter", Phys. Status Solidi C, Vol. 10, pp.1485-1488, 2013.

(2) X. Yin, M. Sato, and S. Kasai: “Analysis on non-ideal nonlinear characteristics of graphene-based three-branch nano-junction device", IEICE Trans. Electron, Vol.E98-C, 5, pp.434-438, 2015.

Proceedings

(1) X. Yin, and S. Kasai: “Graphene-based Three-branch Nano-junction (TBJ) Logic Inverter”, 40th International Symposium on Compound Semiconductor, MoPC-04-15, Kobe, Japan, May 19-23, 2013.

(2) X. Yin, M. Sato, and Seiya Kasai: “Implementation of A Complete Set of Logic Gates Using A Graphene-based Three-branch Nano-junction Device”, 42nd International Symposium on Compound Semiconductor, Mo4PP-E.19, Santa Barbara, USA, June 28-July 2, 2015.

Journals/proceedings related to this study

(1) M. Sato, X. Yin, and S. Kasai:"Surface Dependence of Nonlinear Characteristic in GaAs-based Three-branch Nanowire Junctions", 2014 IEEE International Nanoelectronics Conference (INEC).

(2) Y. Abe, R. Kuroda, X. Yin, M. Sato, T. Tanaka, and S. Kasai: “Structural parameter

dependence of directed current generation in GaAs nanowire-based electron Brownian ratchet devices", Jpn. J. Appl. Phys., vol. 54, pp.06FG02-1-5, 2015.

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Awards

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