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Study on Characterization of GaAs-based Electron Nanodevices Using Local Conductance and Surface Potential Modulation Techniques

(局所コンダクタンス変調および表面電位変調を用いた

GaAs系電子ナノデバイス評価に関する研究)

Graduate School of Information Science and Technology,
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of the requirements for the degree of Doctor of
Philosophy (Engineering)
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Dissertation Supervisor
Professor Seiya KASAI

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Chapter 1 Introduction

1.1 Background

The recent rapid development of the information communication technology has been achieved by the growth and technical innovation of the semiconductor industry. Complementary metal oxide semiconductor (CMOS) is an important element in the large-scale integrated circuits (LSIs), which are the physical cores of the information communication technology. The CMOS consists of a pair of n- and p-channel metal oxide semiconductor field effect transistors (MOSFETs). The CMOS is suitable for the LSIs because of its high speed switching and ultra-low power consumption capabilities. The integration density of the MOSFETs on a chip has increased following Moore's Law which predicted the number of MOSFETs per chip increase exponentially to improve the performance. International technology roadmap for semiconductors (ITRS) predicted the miniaturization trend of the transistors in logic LSIs [2]. Figure 1-1 shows the timeline of the transistor size. However, miniaturization of the transistor size will be limited by the size of an atom. This situation causes problems of variation and fluctuation in the characteristics of the transistors and gate leakage current due to the tunneling effect through an ultra-thin gate oxide. It is necessary to find an alternative way to further improve the LSI performances without miniaturization. Therefore new device operation principle, material, and architecture have been extensively explored recently.

III-V compound semiconductor devices such as GaAs-based nanowire devices

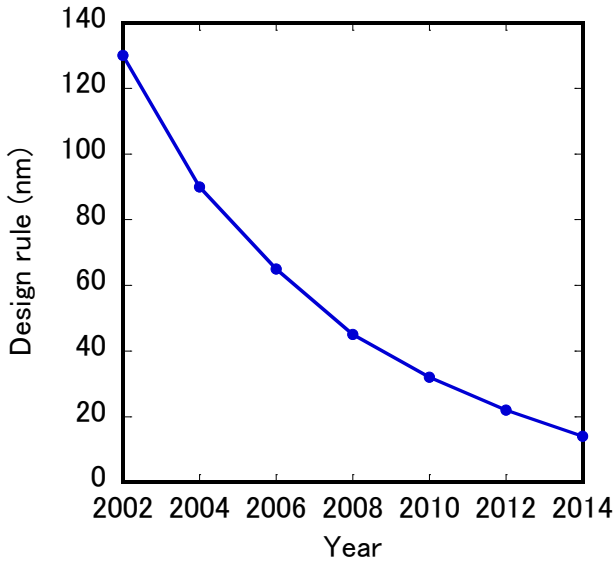

Fig. 1-1 Timeline of design rule of CMOS technology.

are candidate for the future ultra-high performance LSIs. A GaAs-based nanowire three-branch junction (TBJ) device is an important example of such devices. The TBJ device was firstly introduced by H. Q. Xu in 2001 [3]. The TBJ device exhibits unique nonlinear characteristics even with a simple structure. This nonlinearity makes the TBJ to operate as two-input AND logic gate by itself [4] as shown in Fig. 1-2. Various circuits integrating the TBJ devices has been demonstrated so far [5-15]. Originally, ballistic transport was assumed for the mechanism of the nonlinear characteristics in the TBJ [3]. However, the nonlinear characteristics were experimentally observed even at room temperature where the electron transport is in the non-ballistic regime [16-20]. The nonlinear mechanism for such cases has not been clarified yet.

The miniaturization of the semiconductor devices has highlighted the influence of the individual electron traps in the semiconductor surface. The single electron trap that randomly captures and emits an electron gives great influence on the electrical

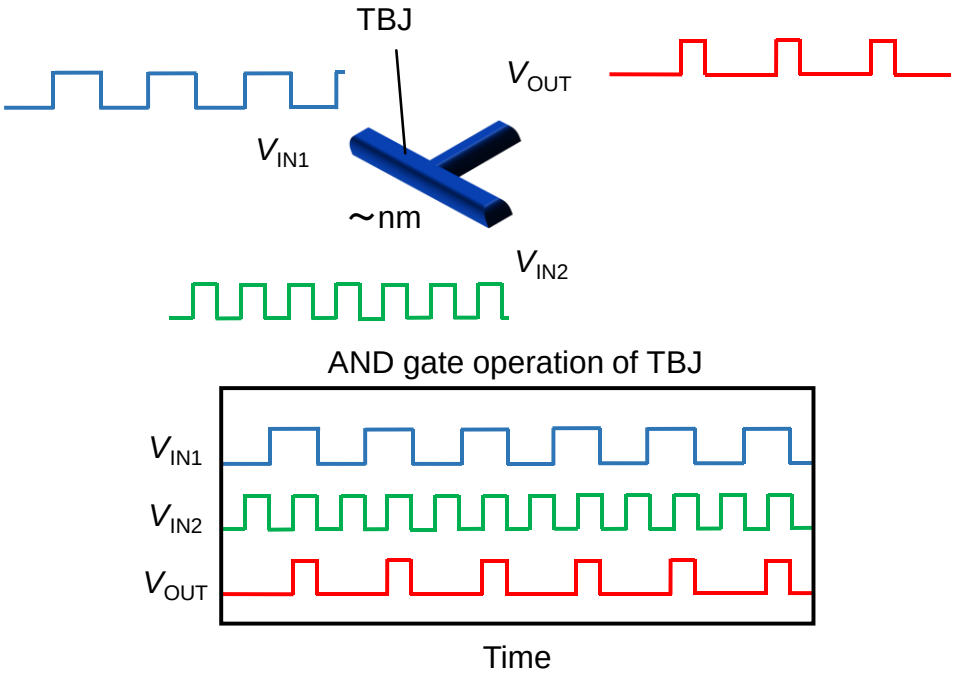

Fig. 1-2 Schematic image of TBJ which is able to use as AND logic gate.

characteristics in the semiconductor nanodevices as shown in Fig. 1-3. Therefore detection and characterization of the single electron trap in the semiconductor surface become an important issue recently. Although various scanning probe microscopy (SPM) techniques have been developed for atomic-scale characterization of the surface [21-42], it is difficult for these techniques to detect the dynamics of the electrical properties of the traps in the semiconductor surface because of the difficulty in high speed and high SNR detection of ultra-small current signal generated by weak interaction between the SPM tip and the surface trap through the SPM tip.

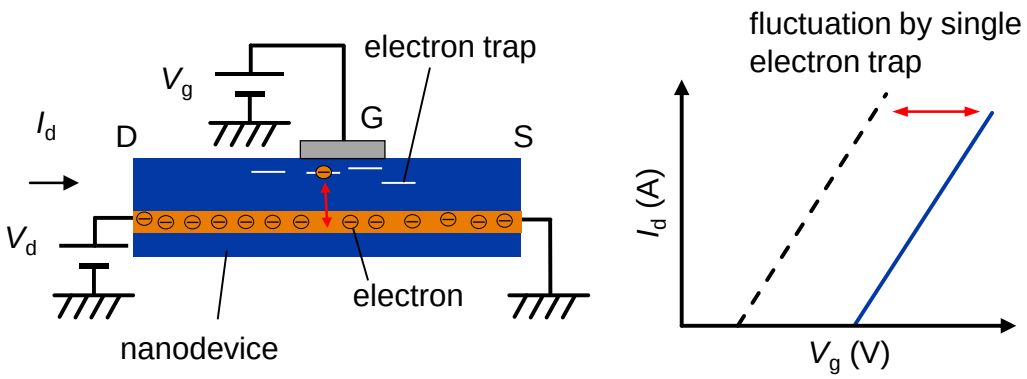

Fig. 1-3 Schematic image of influence of single electron trap on the electrical characteristic in nanodevice.

1.2 Purpose of this work

Considering the backgrounds in the previous section, the objective of this work is to clarify the mechanism of the nonlinear characteristics in the III-V semiconductor TBJ devices at room temperature. The GaAs-based TBJ device was characterized by a local conductance modulation method using focused laser irradiation to understand the nonlinear mechanism. From this study, it is found that the local surface potential in the TBJ is an important factor in the nonlinear characteristics of the TBJ. Here the surface electron trap play key role in the surface potential. Then I introduce a novel detecting technique for the individual electron traps in semiconductor surfaces. Charge dynamics of the electron trap in the semiconductor surface is detected through the current noise in the semiconductor induced by a metal tip. The concept is demonstrated using an atomic force microscope (AFM) system with a metal tip and a small current noise measurement system.

1.3 Synopsis of this thesis

This thesis consists of seven chapters.

Chapter 2 describes the properties of semiconductor nanostructures and surfaces including the electrical properties of the basic GaAs-based devices.

Chapter 3 summarizes the basic concept and techniques of various scanning probe microscopy for the semiconductor nanosturcutures and surfaces.

Chapter 4 introduces a three-branch nanowire junction (TBJ) device and explains its nonlinear electrical characteristics.

Chapter 5 shows and discusses the experimental results of characterization of the GaAs-based TBJ devices using the focused light-induced local conductance modulation method. This method could identify the conductance domain in the device. The effect of the semiconductor surface on the TBJ characteristics was also investigated. I point out that the surface is an important key in understanding its nonlinear characteristics.

Chapter 6 describes the novel detection technique of the discrete electron trap in the GaAs-based nanowire surface through the metal-tip induced surface potential modulation. Random telegraph signal (RTS) was imposed on the nanowire current when the tip was located on an electron trap position. This behavior indicated the capture and emission of an electron between the surface trap and the nanowire channel. From the analysis of the RTS information of electron trap depth and energy could be obtained.

Chapter 7 summarizes and concludes this thesis.

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Chapter 2 Properties of semiconductor nano-structures and surfaces

2.1 Introduction

To improve the performance of electron devices, introducing novel materials and structures is expected. The electrical properties of III-V compound semiconductors are superior to Si as shown in Table 2-1 [1]. GaAs is expected high speed circuit operation because of high electron mobility due to electron effective mass. A nanowire is promising structure for transistors. A Nanowire transistor has excellent gate controllability because of wrapped gate structure and it suppress the short channel effect [2]. Nanostructures such as nanowire are strongly influenced on its surface, therefore, it is important for the device application to understand the physical properties of its surface. In this chapter, basic

Table 2-1 Electrical properties of semiconductors.

	Electron mobility (cm^2/Vs)	Electron effective mass (in units of electron mass)	Saturation velocity (10^7 cm/s)
Si	1400	0.19	1.0
GaAs	8500	0.063	1.2

electrical properties of compound semiconductor materials and nanowire transistors are summarized.

2.2 Electrical properties of AlGaAs/GaAs heterostructure and GaAs-based nanowire

A field effect transistor using AlGaAs/GaAs heterostructure called high-electron mobility transistor (HEMT) was invented by Mimura in 1980 [3]. The band diagram and layer structure of a delta-doped AlGaAs/GaAs heterostructure with a Schottky gate using this work are shown Fig. 2-1. This structure shows a high electron mobility because the two dimensional electron gas (2DEG) layer is isolated from the impurity layer, therefore, electrons in channel are not affected by impurity scattering. In Fig. 2-1, ϕ_B is Schottky barrier height, ΔEc is a band offset between AlGaAs and GaAs, E_F is fermi energy, d_1 is the thickness of AlGaAs barrier layer, and d_2 is the thickness of AlGaAs spacer layer, respectively. The static potential in AlGaAs layer V(z) using Poisson's equation is given by

$$\frac{d^2V(z)}{dz^2} = -\frac{qN(z)}{\varepsilon_{\mathrm{AlGaAs}}}, \tag{2.1}$$

where q is elementary charge, N(z) is the donor density distribution of AlGaAs in the depth direction, and $\varepsilon_{\mathrm{AlGaAs}}$ is the electric permittivity of AlGaAs, respectively. The difference of the electric potential in AlGaAs V_1 using the integration of Eq. (2.1) is given by

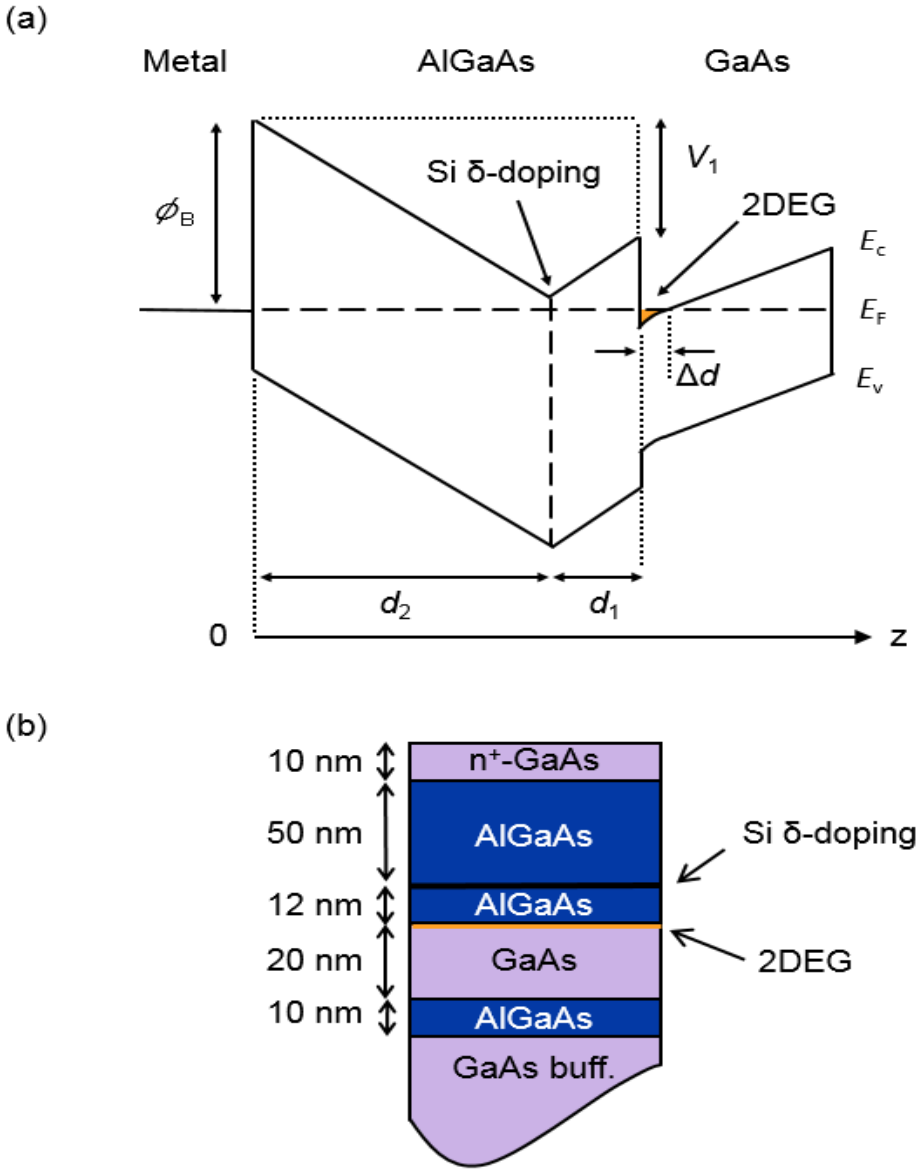

Fig. 2-1 (a) Band diagram and (b) layer structure of a delta-doped AlGaAs/GaAs heterostructure with a Schottky gate using this work.

$$V_1 = F_s(d_1 + d_2) + \frac{qN_d d_2}{\varepsilon_{AlGaAs}}, \tag{2.2}$$

where Fs is the electric field of heterointerface, and N_d is the sheet donor density. The 2DEG density n_s is given by

$$qn_s = \varepsilon_{AlGaAs} F_s . \tag{2.3}$$

The relationship of n_s and gate voltage V_G by using Eq. (2.2) and (2.3) [4] is represented as

$$n_s = \frac{\varepsilon_{AlGaAs}}{q(d_1 + d_2 + \Delta d)}(V_G - V_{th}), \tag{2.4}$$

where V_{th} is threshold voltage, and Δd is the distance between AlGaAs/GaAs heterointerface and 2DEG as shown in Fig. 2-1. Threshold voltage is given by

$$V_{th} = \phi_B - \Delta E_c - E_{F0} - \frac{qN_d d_2}{\varepsilon_{AlGaAs}}, \tag{2.5}$$

where E_{F0} is Fermi level from the conduction band when V_G = 0 V.

Figure 2-2 shows a schematic image of Schottky wrap-gate (WPG) controlled nanowire transistor. The width of the depletion region estimating by the ideal in-plane gate structure [5] is given by

$$W_{dep} = \frac{2\varepsilon_{AlGaAs}}{qn_s}(V_{bi} - V_G), \tag{2.6}$$

where V_{bi} is the built-in potential of the Schottky contact. The effective channel width of nanowire transistor is given by

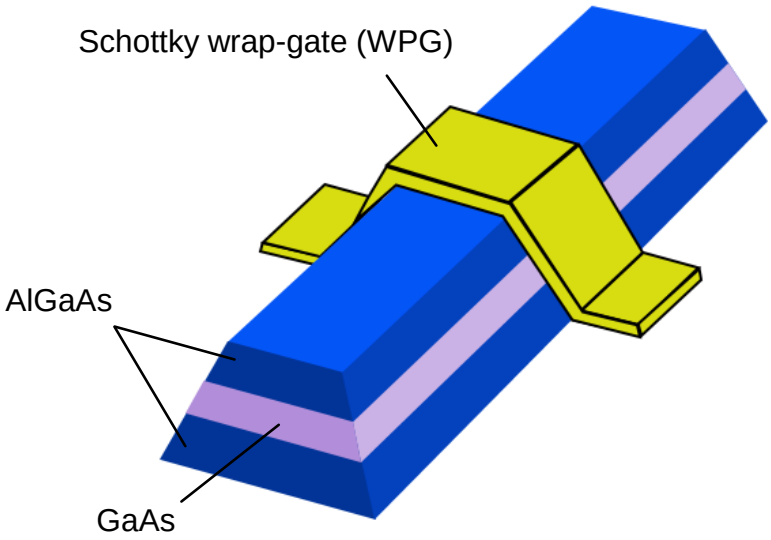

Fig. 2-2 Schematic image of Schottky wrap-gate (WPG) controlled nanowire transistor.

$$W_{\text{eff}} = W_{\text{geo}} - 2W_{\text{dep}}, \tag{2.7}$$

where W_{geo} is the geometrical nanowire width. The effective threshold voltage of the nanowire transistor which defined as $W_{\text{eff}} = 0$ is determined by

$$V_{\text{thWPG}} = V_{\text{bi}} - \frac{qn_{\text{s}}}{4\varepsilon_{\text{AlGaAs}}} W_{\text{geo}}. \tag{2.8}$$

Substituting Eq. (2.4) into Eq. (2.6),

$$V_{\text{thWPG}} = \frac{1}{1+\alpha} V_{\text{bi}} - \frac{1}{1+\alpha} V_{\text{th}}, \tag{2.9}$$

where α is the ratio between the geometrical nanowire width and AlGaAs layer, and

$$\alpha = \frac{W_{\text{geo}}}{4(d_1 + d_2)}. \tag{2.10}$$

In the linear region, when the channel potential is less than saturation electric field E_S, drain current of HEMT is described as

$$I_d = \frac{\varepsilon_{\text{AlGaAs}} \mu W_G}{(d_1 + d_2 + \Delta d)} \left[(V_G - V_{th}) V_d - \frac{V_d^2}{2} \right], \tag{2.11}$$

where μ is the electron mobility, W_G is the width of the gate, and V_d is drain voltage, respectively [4, 6]. In the saturation region, when the electron velocity $v_S = \mu E_S$, saturation drain current is expressed as

$$I_{\text{dsat}} = \frac{\varepsilon_{\text{AlGaAs}} \mu W_G E_S}{(d_1 + d_2 + \Delta d)} \left[\sqrt{(V_G - V_{th})^2 + E_S^2 L_G^2} - E_S L_G \right], \tag{2.12}$$

where L_G is the gate length. If the gate length L_G is much smaller than $(V_G\text{-}V_{th})/E_S$,

$$I_{\text{dsat}} = \frac{\varepsilon_{\text{AlGaAs}} W_G v_S}{(d_1 + d_2 + \Delta d)} (V_G - V_{th}). \tag{2.13}$$

The transconductance is given by

$$g_m = \frac{\varepsilon_{\text{AlGaAs}} W_G v_S}{(d_1 + d_2 + \Delta d)}. \tag{2.14}$$

2.3 Surface and interface states

The electron state at the end of periodic crystal forms surface state and interface state when materials such as metal, amorphous, and other crystal contacts to the surface. The charge of interface state causes potential bending and trap and emission of carriers to the state influences on the carrier transport and transient response. For the application of the semiconductor devices including MOS FETs and heterostructure, control of the interface is an important issue of electrical properties and reliability.

The unified disorder induced gap state (DIGS) model to explain the interface state was proposed by Hasegawa and Ohno in 1986 [7]. Figure 2-3 shows a schematic image of interface state density distribution. In the upper region of bandgap, anti-bonding states succeed to conduction band and it is called accepter-like states. On the other hand, in the lower region of the bandgap, bonding states succeed to valence band and it is called donor-like states. These have the highest density of states near the band edge and minimum value at the charge neutral level E_{HO}. As a result, the density of states shows the U-shaped distribution.

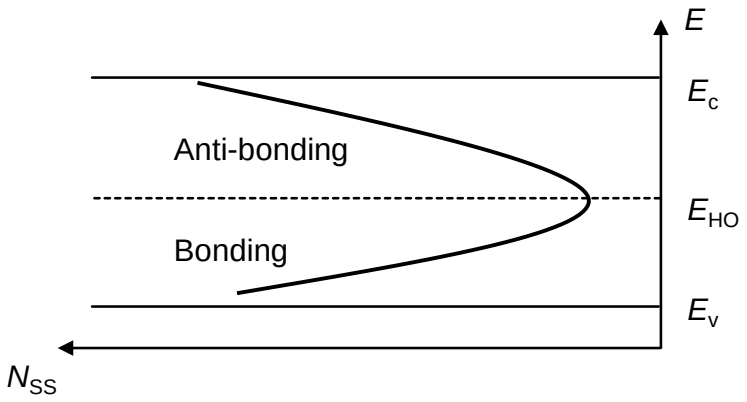

Fig. 2-3 Schematic image of interface state density distribution based on the DIGS model.

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Chapter 3 Scanning probe microscopy

3.1 Introduction

The scanning probe microscopy (SPM) techniques are the methods of obtaining surface images of the specimen surface and information of electrical characteristics. As the first of the SPM technique, Scanning tunneling microscopy (STM) was invented by Binnig and Rohrer in 1982 [1]. Since then, various SPM techniques such as an atomic force microscopy (AFM) utilizing the atomic force between a tip and a sample surface and a kelvin force microscopy (KFM) which is able to characterize the electrical properties of the sample have been developed. In this section, the basic principles of these techniques are summarized.

3.2 Scanning tunneling spectroscopy

Binnig and Rohrer realized the measurement of tunneling current between probe and superconductive material and scanning its distribution. Figure 3-1 shows a schematic image of STM. Tunneling current through the gap between tip and sample changes sensitively and then if the tunneling current is remained constant and the height between the tip and sample is controlled, the tip describes unevenness of sample surface. Here, we consider a one dimension model of metal-vacuum-metal tunnel barrier to understand the tunneling current. The tunneling current gives

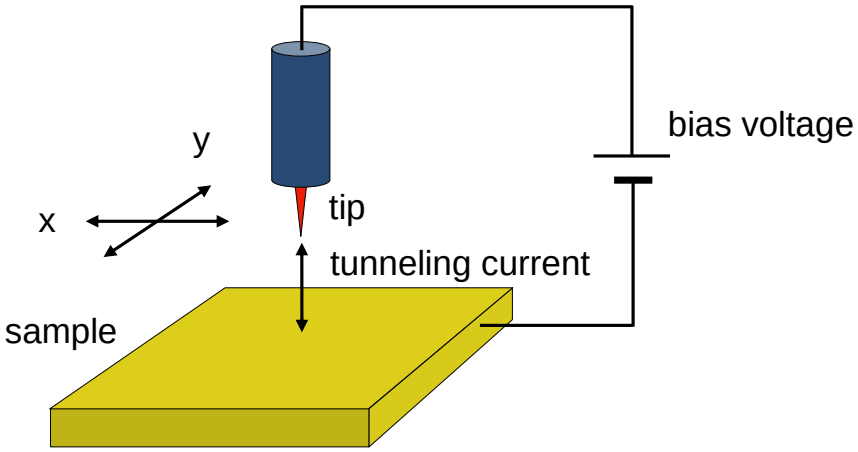

Fig. 3-1 Schematic image of STM.

$$I \propto \exp\left(-2s\sqrt{\frac{2m}{\hbar^2}(<\phi> - \frac{e|V|}{2})} \right) \tag{3.1}$$

where s is a distance between the metal, m is an electron mass, e is an elementary charge, $\hbar$ is a plank constant, φ is a work function of the metal, and V is an applied tip-sample bias between tip and the sample. Note that the tunneling current depends on the electronic density of states of tip and sample. Scanning tunneling spectroscopy (STS) is an experimental technique to obtain the information of local density of electronic states by measuring the local tunneling current versus tip-sample bias [2-5].

3.3 Atomic force microscopy

AFM was invented by Binnig, Quate and Gerber in 1986 [6] and first commercially introduced in 1989. Figure 3-2 shows a schematic image of AFM. The AFM consists of a cantilever which has a nanometer order tip and lever and it is used to scan and obtain

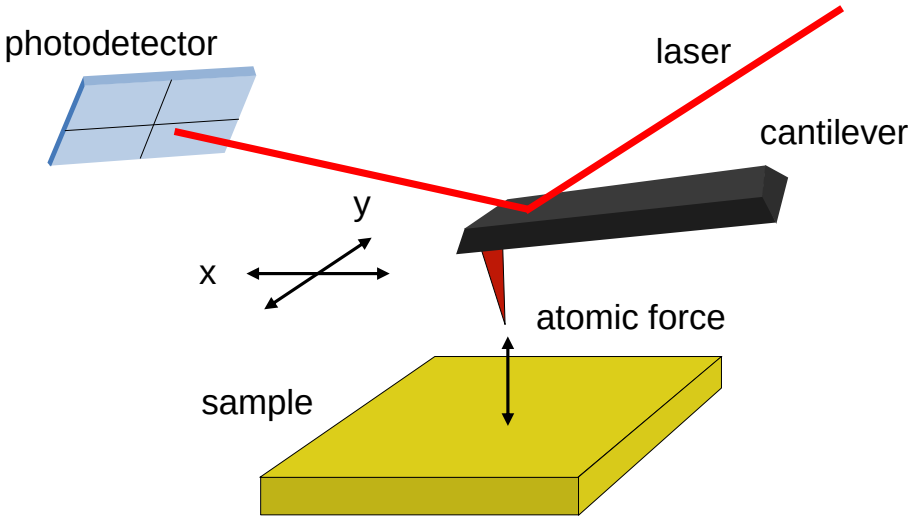

Fig. 3-2 Schematic image of AFM.

an image of a sample surface. The typical material of the cantilever is silicon or silicon nitride. The principle of AFM is based on the force between the tip and the sample. If the chip closes to the surface, forces works between the tip and the sample and it leads to deflection of the cantilever. Detection of the deflection of the cantilever is called the optical lever method. Optical lever method is to detect a deflection of the cantilever irradiating laser to back of the cantilever and detecting its reflection by position sensitive detector. Generally, force between nearby two objects always works so the AFM can be theoretically used to any material. In addition, scanning gate microscopy (SGM) for characterizing the local transport properties of electron devices has been reported [7-18]. In this technique, the biased conducting tip of an atomic force microscope (AFM) modulates electrostatic potential locally in the device and the current passing through the device, which is not influenced by the tip conductance, is measured.

3.3.1 Imaging modes

There are three modes for imaging by AFM describing as follows.

3.3.1.1 Contact mode

In contact mode, the tip directly contacts to the sample. Therefore, this mode can achieve the high resolution imaging. The vertical force of the cantilever is controlled and then pressure to the sample is also limited. However, the tip and the sample are susceptible to damage because of the direct contact.

3.3.1.2 Tapping mode

In the case of a sample observation in liquids, there are problems of damage to the sample and the lateral dragging of the sample. Tapping mode was developed to solve these problems [19]. In the tapping mode, the cantilever is driven close to a resonance frequency and its amplitude is kept constant. The intermittent contacts between the tip and the sample surface give the AFM image in the tapping mode. The tapping mode is often used when a sample is measured in liquids because that can reduce the damage to the tip and lateral movement of the sample.

3.3.1.3 Non-contact mode

In the non-contact mode, the cantilever oscillates at resonance frequency and measuring a shift of its resonance peak [20]. Generally, resonance frequency decreases if the cantilever closes to the sample surface. The short-range force between the tip and the surface is like a covalent bond which is effective around an atomic scale. On the other hand, the long-range force is like van der Waals forces which are effective over several 10 nm. An atomic scale AFM image can

be obtained by the frequency shift caused by these forces in the non-contact mode. Therefore, the cantilever and the sample do not be degrade in the non-contact mode.

3.3.2 Force spectroscopy

In the force spectroscopy, in order to obtain detailed information of the sample, the lateral direction is fixed and the cantilever is moved in the vertical direction, and its deflection is measured. A simple force curve is shown in the Fig. 3-3. The vertical line shows the deflection of the cantilever and the horizontal one the height of the cantilever from the surface. The force is too small to give a deflection of the cantilever when the distance between the cantilever and the sample is long. As the cantilever approaches the surface,

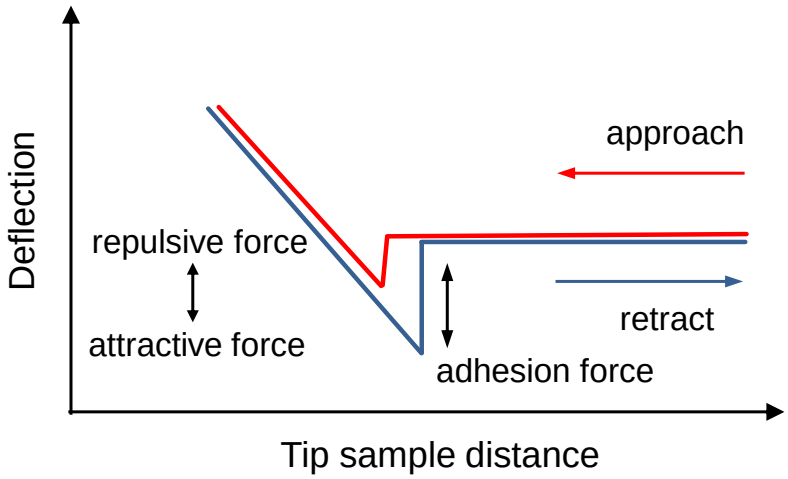

Fig. 3-3 Typical force curve of AFM.

an attractive force works between the surface and the tip, and the tip jumps into contacts with the surface. When the tip is contact with the sample surface, a repulsive force from the sample works to the tip, and it causes opposite deflection.

3.4 Kelvin probe force microscopy

KFM for measuring a contact point difference (CPD) in surface study was proposed in 1991 [21]. The KFM can provide high resolution information of potential or charge distribution and CPD by detecting electrostatic force. The KFM is often used to surface and interface of thin film sample and surface potential of semiconductor material [22-27]. Figure 3-4 shows a schematic image of principle of the KFM. If a conductive tip is not applied DC bias as shown in Fig. 3-4(a), the work function of conductive tip φ_1 and that of the sample φ_2 are given by

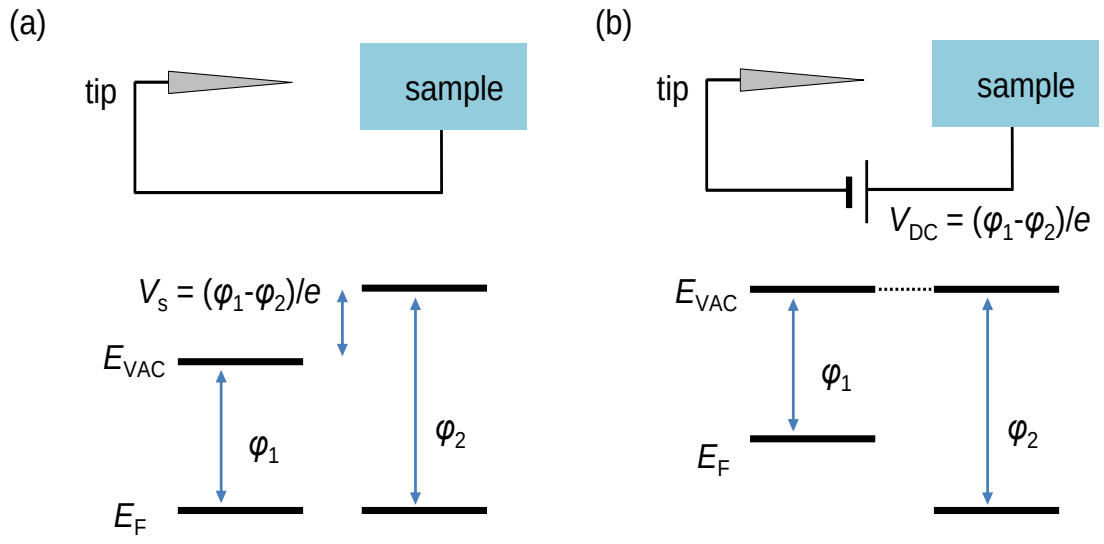

Fig. 3-4 Schematic image of principle of KFM. (a) Tip is not applied DC bias and (b) tip is applied DC bias to cancel out the electrostatic force.

$$\varphi_1 = E_{\mathrm{VAC}} - E_1, \tag{3.2}$$

$$\varphi_2 = E_{\mathrm{VAC}} - E_2, \tag{3.3}$$

where E_{VAC} is vacuum level, E_1 is fermi energy of the conductive tip, and E_2 is fermi energy of the sample, respectively. When the tip contacts to the sample surface, the CPD *V*s between the tip and the sample which is same as the difference of the work function is given by

$$V_{\mathrm{s}} = \frac{\varphi_1 - \varphi_2}{e}. \tag{3.4}$$

When we apply DC voltage to cancel out the electrostatic force as shown in Fig. 3-4(b), we can obtain the value of CPD. The electrostatic force when there are potential difference *V* between the tip and the sample is given by

$$F = \frac{1}{2}\frac{dC}{dz}V^2, \tag{3.5}$$

where *C* is a capacitance, and *z* is a distance between the tip and the sample, respectively. When we apply DC voltage V_{DC} and AC voltage $V_{\mathrm{AC}}\sin\omega t$, this formula is replaced by

$$\begin{aligned} F &= \frac{1}{2}\frac{dC}{dZ}(V_{\mathrm{s}} - V_{\mathrm{DC}} - V_{\mathrm{AC}}\sin\omega t)^2 \\ &= \frac{1}{2}\frac{dC}{dZ}\left\{(V_{\mathrm{s}} - V_{\mathrm{DC}})^2 + \frac{1}{2}{V_{\mathrm{AC}}}^2\right\} - \frac{dC}{dZ}(V_{\mathrm{s}} - V_{\mathrm{DC}})V_{\mathrm{AC}}\sin\omega t - \frac{1}{4}\frac{dC}{dZ}{V_{\mathrm{AC}}}^2\cos 2\omega t. \end{aligned} \tag{3.6}$$

We can obtain the CPD between the tip and the sample if the DC voltage is adjusted to amplitude to be zero because $V_{\mathrm{s}} = V_{\mathrm{DC}}$.

Figure 3-5 shows a schematic image of characterization for surface potential in a semiconductor using the KFM. If an electron trap exists in the semiconductor, its work function increases resulting in the surface potential is smaller than the semiconductor which has no electron trap. Therefore, we can find a disorder in semiconductor by characterizing the CPD using the KFM.

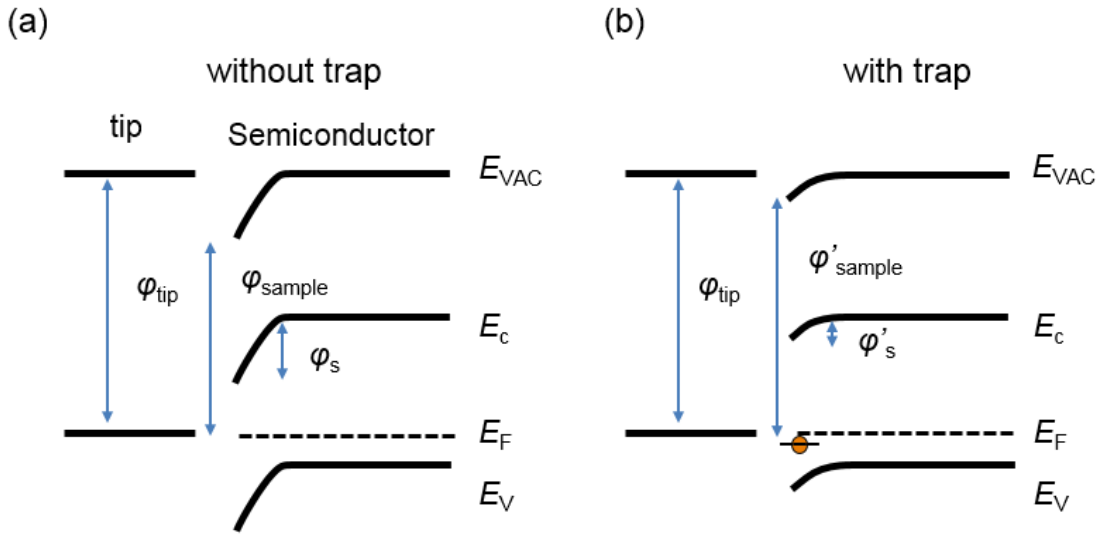

Fig. 3-5 Schematic image of characterization of semiconductor using the KFM (a) with and (b) without electron trap.

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Chapter 4 Three-branch nanowire junction (TBJ) device

4.1 Introduction

The recent development of nanotechnology allows us to create various functional nanodevices. A semiconductor three-branch nano junction (TBJ) device is a typical and important example of such devices. The TBJ exhibits a unique nonlinear voltage transfer characteristic even with a simple structure [1]. Various analog and digital circuits integrating TBJs have been demonstrated thus far, including NOR logic gates [2], NAND logic gates [3-6], frequency mixers [7, 8], half adders [9], rectifiers [10], and flip-flops [11, 12]. The TBJ also has the capability of ultrahigh-speed operation up to THz frequency [13]. For the design and control of the device and circuits, understanding of the mechanism for the nonlinear characteristic is an important issue. A pioneering work by Xu indicates that the nonlinear characteristic appears when the TBJ is operated in the ballistic transport regime [1]. However, experimentally, it is also clearly observed at room temperature (RT) [14-18] where the carrier transport should be in the nonballistic transport regime. The mechanism in such a case has not been clarified yet, although several hypotheses have been introduced, including those regarding the effective mean free path extension [16] and the asymmetric channel depletion due to the surface potential [19-26].

4.2 Nonlinear electric characteristics of TBJ

The TBJ with a typical measurement circuit is shown in Fig. 4-1(a). We consider the device with an n-type semiconductor. An equivalent circuit deduced from the structure is shown in Fig. 4-1(b). When voltage signals are applied to the left and right branches in push-pull fashion ($V_{INL} = -V_{INR}$), the output voltage V_{OUT} in the center branch shows a bell-shaped nonlinear voltage transfer curve, as shown in Fig. 4-1(c). To explain such a nonlinear behavior in terms of the equivalent circuit in Fig. 4-1(b), we consider the formula of V_{OUT} as

$$V_{OUT} = \frac{G_+ - G_-}{G_+ + G_-} V_{IN}, \tag{4.1}$$

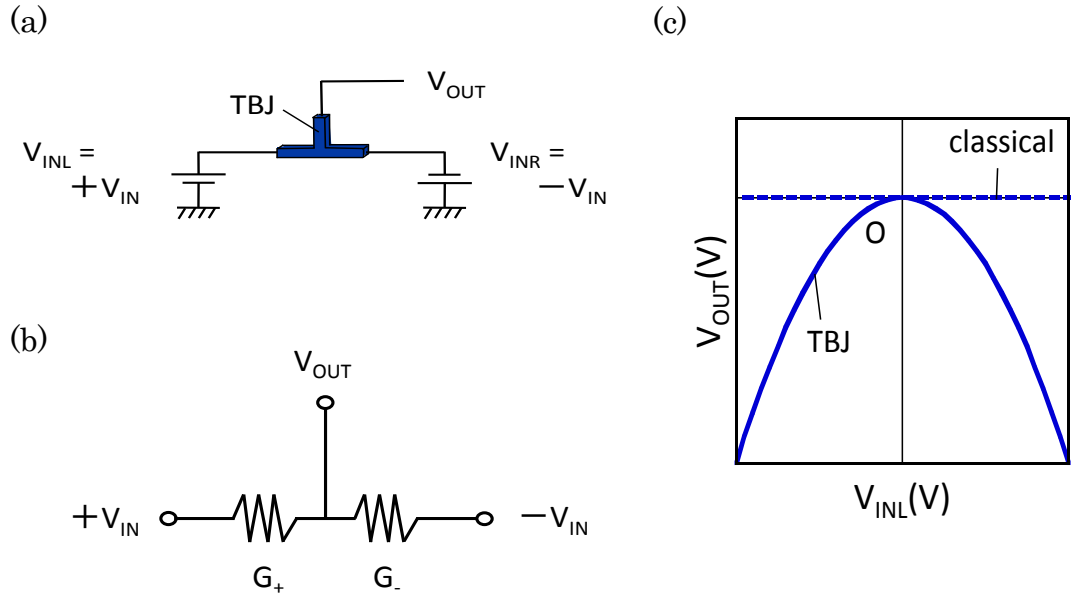


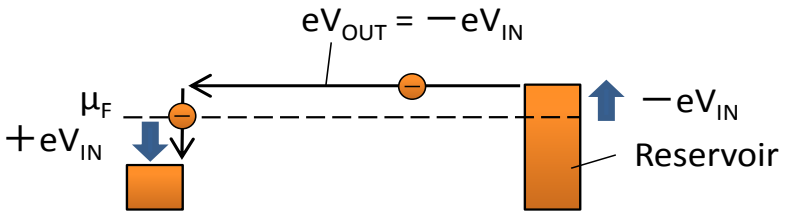
Fig. 4-1 TBJ device: (a) measurement circuit, (b) equivalent circuit of the device, and (c) typical voltage transfer characteristic.

where G_+ and G_- are the input branch conductance values with positive and negative biases, respectively. From the device configuration, the conductance in the input branches is expected to be the same and V_{OUT} is expected to be zero. In turn, to explain the nonlinear curve, we must accept that G_+ is always smaller than G_-.

4.3 Possible models for nonlinear characteristics

The nonlinearity in the TBJ is understood by the asymmetric conductance that depends on the polarity of the input voltage. The original model explains it by the ballistic transport of electrons [1]. In this model, the electrons emitted from the negatively biased branch reach another branch without scattering, as shown in Fig. 4-2(a). As a result, the resistance of the negatively biased branch is zero. Then, the output voltage follows that of the negatively biased branch, namely, $V_{OUT} = -|V_{IN}|$. This model is applicable to the low-temperature operation where the mean free path is longer than the device size. However, the nonlinear characteristic is observed at RT, which cannot be explained using this model. At present, there are two models for such a case. The mean free path extension model indicates that the effective mean free path is extended at a high electric field because the carrier velocity increases while the carrier relaxation time remains constant [16]. On the other hand, the asymmetric channel depletion model indicates that the potential difference between the surface and the biased branch causes asymmetric depletion in the channel, which is similar to the channel pinch off in a field-effect transistor (FET) with large drain bias. In the case of the n-type semiconductor, the channel depletion occurs in the positively biased branch, as shown in Fig. 4-2(b) [19-26]. This means that G_+ is small. The III-V semiconductor nanowire surface is known to behave

(a)



(b)

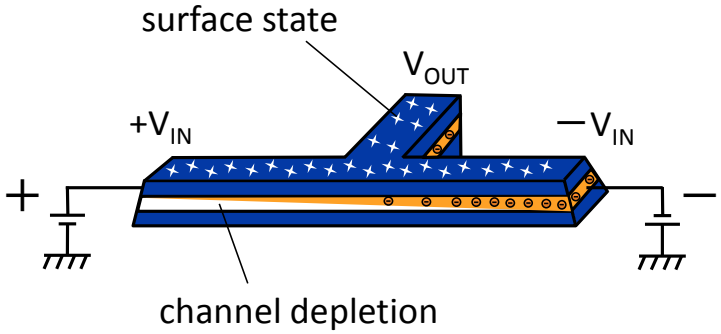


Fig. 4-2 (a) Ballistic transport model and (b) asymmetric channel depletion model.

similarly to a metal gate because high-density surface states fix the surface Fermi level at a certain energy level. From the size dependence of the nonlinear curve [26] and its asymmetric change in the gate-controlled TBJ devices [17, 25], we suppose that this model is applicable to the nonlinear characteristic at RT. To verify the applicability of this model, the identification of the existence of the conductance domain and its portion is necessary. The effect of the surface should also be clarified.

4.4 Applications

The relationship between the output voltage and input voltage of TBJ device is summarized in Table 4-1. The output voltage of TBJ device always follows the lower input voltage. For example, if the one of input voltage is applied 1 V and the other input is applied 0 V, then the output voltage follows the lower input 0 V. If the both input voltage is 0 V or 1 V, the output voltage is as same as the input voltage. This relationship is as same as the AND logic gate. Therefore, TBJ device behaves as AND logic gate itself. In addition, NAND logic gate has been demonstrated combining with TBJ device and TBJ-shaped inverter which can increase gain [6]. Any Boolean logic gate can be implemented by using combination of the TBJ device because NAND logic gate is the universal circuit.

Table 4-1 Truth table of TBJ device logic operation.

V_{INPUT1}	V_{INPUT2}	V_{OUT}
0	0	0
0	1	0
1	0	0
1	1	1

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Chapter 5 Characterization of GaAs-based TBJ devices by light-induced local conductance modulation method

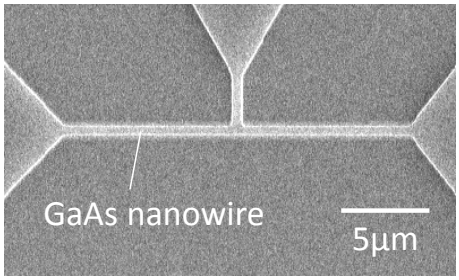
5.1 Experimental Procedure

In this study, to identify the model for the nonlinear mechanism in the TBJ at room temperature, we characterized the GaAs-based TBJ device by local conductance modulation by focused laser light irradiation. This method revealed the conductance domain in the device, which is an important factor for understanding the nonlinear characteristic. We also fabricated and characterized a SiN-deposited TBJ to clarify the effect of the surface potential on the nonlinear characteristic in terms of channel depletion.

GaAs-based TBJ devices were fabricated and characterized. The nanowire channel was formed on an AlGaAs/GaAs heterostructure on a (001) semi-insulating GaAs substrate by EB lithography and wet chemical etching. A Ni/Ge/Au/Ni/Au ohmic contact was formed on each branch. Figure 5-1(a) shows a scanning electron microscopy (SEM) image of a fabricated device. The two-dimensional electron gas (2DEG) density was 7.8×10^{11} cm^2. The 2DEG mobility (μ_e) values were 7,100 $cm^2V^{-1}s^{-1}$ at 300 K and 11,000 $cm^2V^{-1}s^{-1}$ at 77 K. The corresponding mean free paths were 100 nm at 300 K and 1600 nm at 77 K. To identify the conductance domain position distinctly, we designed a relatively large device. The input nanowire length was 20 μm and the output nanowire

length was 2.5 μm. The nanowire directions were <-110> for input branches and <110> for output branches. In the case of the GaAs channel, the electron transport properties including the mobility, mean free path, and density of states do not depend on the nanowire direction, since the Fermi surface of GaAs has a spherical symmetry and the effective mass of the electron is isotropic. The width and cross section of the nanowire

(a)



(b)

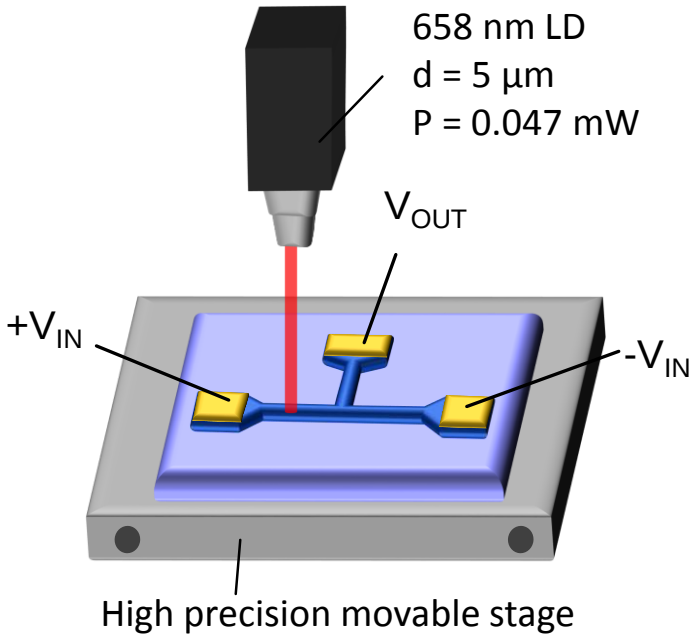


Fig. 5-1 (a) SEM image of a fabricated GaAs TBJ device and (b) a light-induced local conductance modulation measurement system.

mainly affect the conductivity. The nanowire widths were 300 nm for the input branch and 500 nm for the output branch. The nanowire was larger than the mean free path and the device operated in the nonballistic transport regime at RT. To clarify the effect of the surface potential, we also prepared devices with and without a SiN layer on their surface. The SiN layer is known to change the surface potential in GaAs-based materials [1, 2]. The SiN layer was deposited by electron cyclotron resonance chemical vapor deposition (ECR-CVD) at a substrate temperature of 260 °C. The gas flow conditions were a SiH_4 gas flow rate of 30 sccm and a N_2 gas flow rate of 1 sccm. The measured film thickness was 30 nm.

To find the conductance domain and its effect on the nonlinear characteristic, we developed the light-induced local conductance modulation measurement system shown in Fig. 5-1(b). A focused laser light was irradiated on the device. The diameter of the laser spot was 5 μm and the wavelength was 658 nm. The laser light excited carriers and modulated the conductance locally. The sample position could be controlled with a 10 nm resolution in this system. All measurements were performed at RT.

5.2 Results

5.2.1 Effect of focused light irradiation

To confirm the local conductance modulation in the developed system, we measured the *I-V* characteristics of the device in the beginning. Figure 5-2(a) shows the measured *I-V* characteristics under dark and light irradiation conditions. The laser light was irradiated at the end of the left branch. The significant current increase was observed only when the

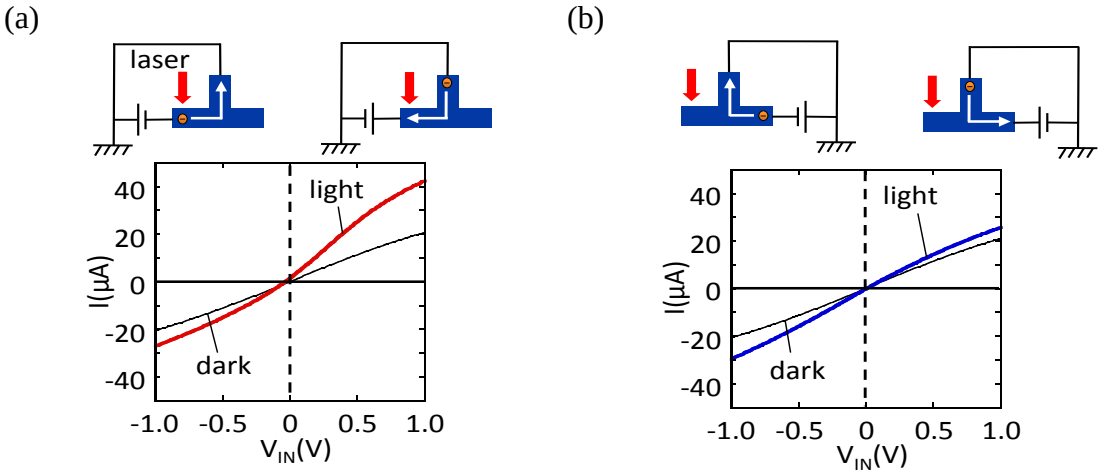


Fig. 5-2 *I* –*V* characteristics with laser light irradiation: (a) irradiation on the current path side and (b) irradiation on the outside of the path.

laser light was irradiated on the positively biased branch. The results confirmed the local conductance modulation in the present system and also indicated the existence of the conductance domain in this portion. A small increase in current was also observed even in the branch without light irradiation, as shown in Fig. 5-2(b). This was because the photogenerated carriers in the laser-irradiated branch diffused to the current channel portion. The increase in conductance was 22 μS. The estimated increase in carrier density, Δn, was 1.9×10^{10} cm^{-2}. Theoretically, in the case of 658 nm light, the number of generated photons was 4.6×10^{19} $cm^{-2}s^{-1}$ considering the reflectance of 0.34 for GaAs and the laser power of 0.102 mW. The increase in carrier density is estimated using

$$\Delta n = \eta \tau f, \tag{5.1}$$

where τ is the carrier lifetime, η is the quantum efficiency, and f is the photon flux density. τ was estimated to be 10 ns [3]. Assuming η = 30%, we obtained $\Delta n = 4.6 \times 10^{11}$ cm^{-2} and the increase in conductance was estimated to be 523 μS. This value is one orders of

magnitude larger than the experimental one. The difference is attributed to the small effective quantum efficiency due to the large surface recombination of the GaAs nanowire [4].

Figure 5-3 shows the measured V_{OUT}-V_{INL} characteristics with and without laser light irradiation. The output voltage increased when the laser light was irradiated on the positively biased branch. In contrast, the output decreased when the laser light was irradiated on the negatively biased branch. The observed behaviors were explained by the increase in conductance in the laser-irradiated branch in terms of Eq. (4.1). The polarity of the output voltage was changed from negative to positive by the light on the positively biased branch. This was because the magnitude relationship between the conductance in the left and right branches was switched and the output branch potential followed the positively biased branch. The increase in conductance from the result was estimated to be

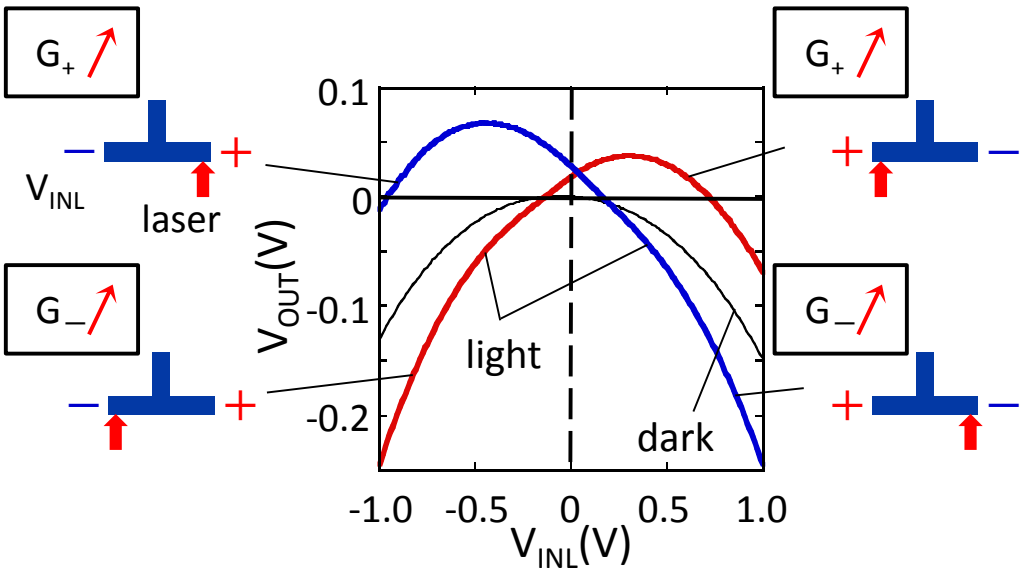


Fig.5-3 V_{OUT}–V_{INL} characteristics with and without the laser light irradiation.

11 μS, which was in agreement with that from the *I-V* characteristics. This result indicates that the asymmetry of the input nanowire conductance caused the nonlinearity in the voltage transfer curve.

To determine the position of the conductance domain and its relationship with the nonlinear curve, the laser light position dependences of the output voltage and the input-branch current I_{IN} were characterized. The measurement system is schematically shown in Fig. 5-4(a). In these measurements, constant positive and negative voltages were applied to the left and right branches, respectively (V_{INL} = +1 V, V_{INR} = -1 V). Figures 5-4(b) and 4(c) show the laser position dependences of V_{OUT} and I_{IN}, respectively. The output voltage increased as the laser position was moved from right (x = 10 μm) to left (x = -10 μm). The current also increased similarly to the output voltage. The highest voltage and current were observed at the end of the positively biased nanowire at x = -10 μm. These results indicate that the lowest conductance portion was the end of the positively biased nanowire. V_{OUT} showed a minimum value at x = 2.5 μm. This was because the conductance in the negatively biased branch, G_-, increased and it enhanced the nonlinearity, as indicated by Eq. (4.1). V_{OUT} increased when the laser position was greater than 2.5 μm, since the light spot gradually left the nanowire and transferred to the wide channel portion, and the situation approached the dark condition.

We estimated the change in conductance in the two input branches as a function of the laser-irradiated position. Input branch conductance is expressed by

$$G_+ = \frac{I_{IN}}{V_{INL} - V_{OUT}} \ , \ G_- = \frac{I_{IN}}{V_{OUT} - V_{INR}} \ . \tag{5.2}$$

The calculated result is shown in Fig. 5-5. Note that the largest conductance change

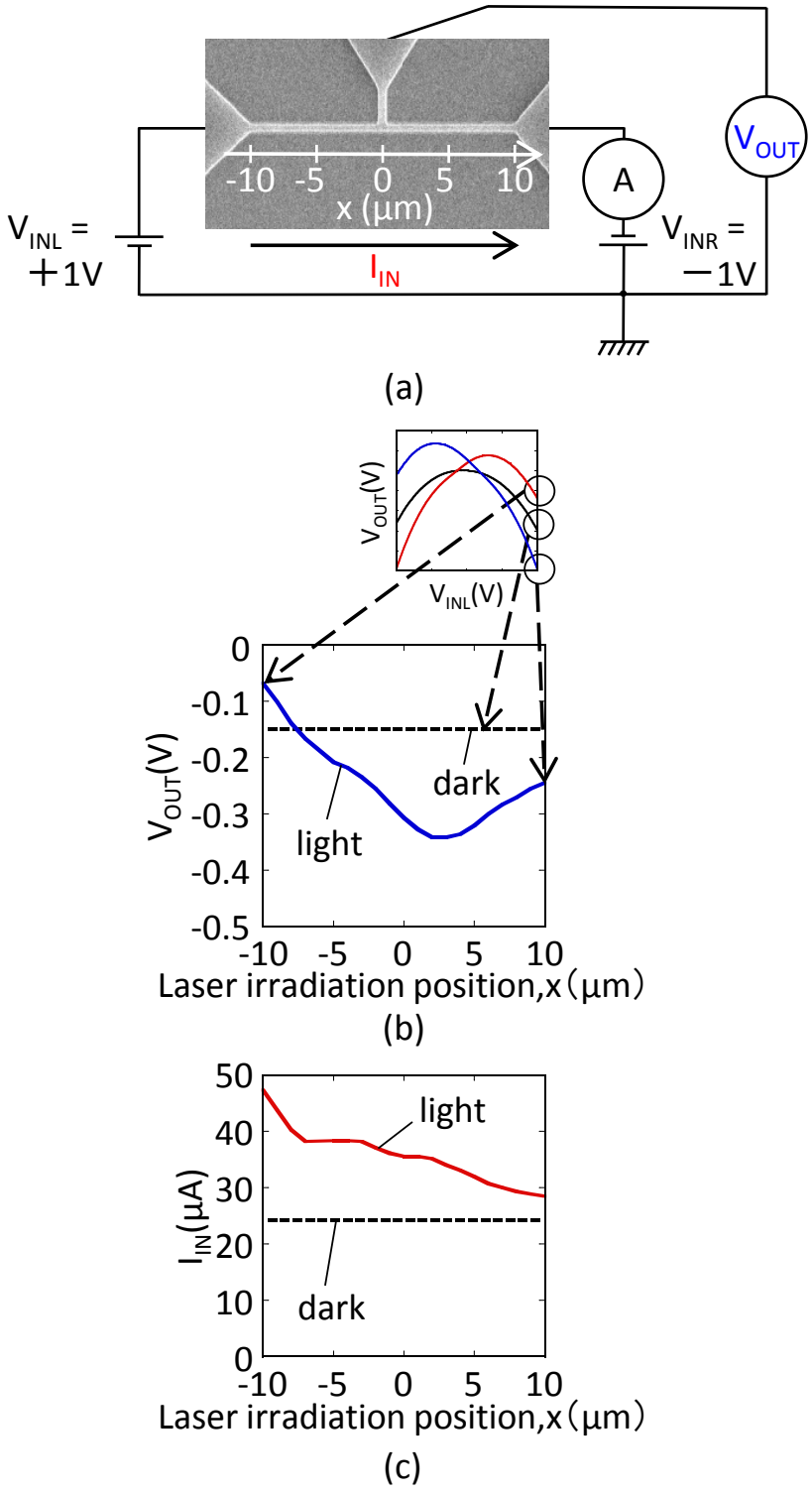


Fig. 5-4 (a) Measurement system for conductance domain identification and (b) laser light positional dependences of V_{OUT} and (c) I_{IN}.

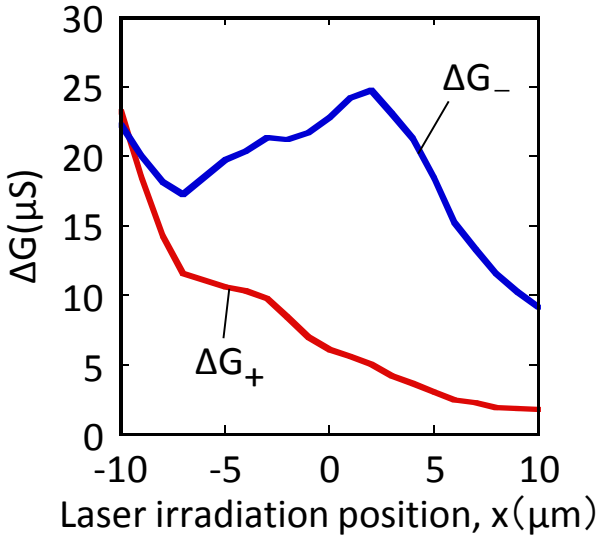


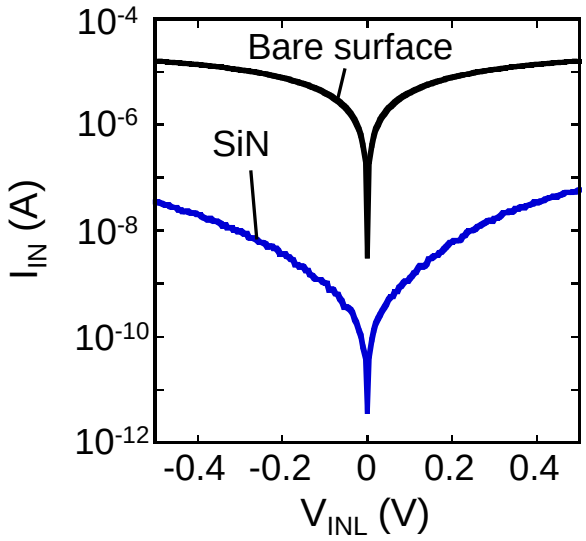
Fig.5-5 Evaluated conductance values in the left and right branches.

occurs when the laser is irradiated on the conductance domain, since the lowest conductance dominates the current. Therefore, we could determine the position of the conductance domain from the plot in Fig. 5-5. The largest change in G_+ was obtained when the laser was irradiated at the end of the positively biased nanowire, x = -10 μm. Thus, the conductance domain existed at the end of the positively biased nanowire.

5.2.2 Surface dependence of nonlinear voltage transfer characteristics

To clarify the mechanism of the formation of the conductance domain, we investigated the effect of the nanowire surface on the electric characteristics in the TBJ. Figure 5-6(a) shows the currents in the nanowire before and after the SiN deposition. The current decreased after the SiN deposition. This showed the increase in surface potential that

(a)



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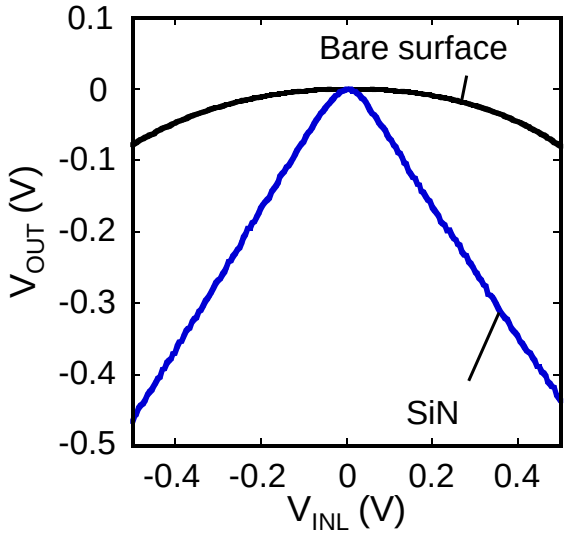

Fig. 5-6 (a) I –V and (b) V_{OUT}–V_{INL} characteristics before and after SiN deposition.

promoted the channel depletion. Figure 5-6(b) shows the voltage transfer curves before and after the SiN deposition. The reinforcement of the nonlinearity was observed in the device after the SiN deposition. Therefore, the surface condition affected the nonlinearity in the TBJ. The study on the electric field concentration in MESFETs [5] showed that the large surface potential of the channel semiconductor shifted the position of the high field

to the drain electrode. In the case of the TBJ, the increased surface potential enhanced the channel depletion in the positively biased branch similar to the drain in a FET and the conduction was decreased and the nonlinearity was reinforced. Considering the position of the conductance domain, the results suggest that the asymmetry channel depletion model is feasible for the nonlinear characteristic of the TBJ in the nonballistic transport regime.

5.3 Discussion

A possible model for the voltage-polarity-dependent conductance in a GaAs-based TBJ is asymmetric channel depletion. This model is based on the fact that the surface potential of the TBJ is almost fixed due to the surface Fermi level pinning on the GaAs and related materials by high-density surface states [6]. Such surface behaves as a metal gate.

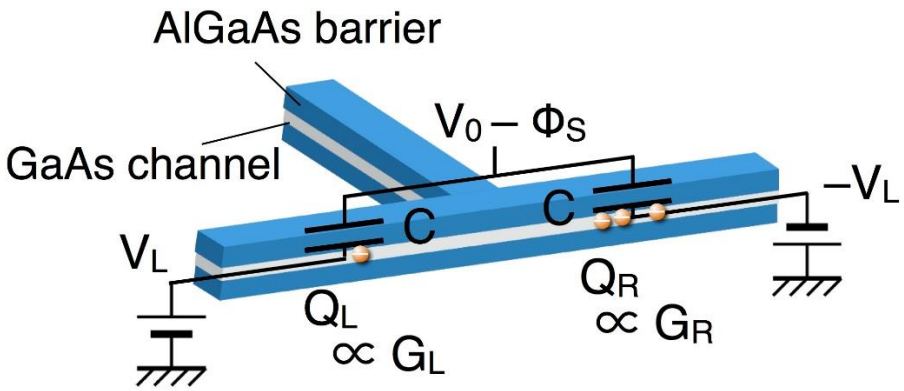

Fig. 5-7 Surface-related model for asymmetric conductance in input branches.

Considering the typical GaAs-based TBJ structure as shown in Fig. 5-7 together with the linear transport approximation similar to the long-channel FET, carrier density of the electrons in the channel n_s is expressed by the capacitance C per unit area of the AlGaAs barrier layer,

$$e \cdot n_S(V) = C(V_0 - \phi_S - V) = \frac{\varepsilon_{AlGaAs}}{d_{AlGaAs}}(V_0 - \phi_S - V), \tag{5.3}$$

where e is an elementary charge, V_0 is an equivalent potential representing the accumulated electrons by doping, ϕ_S is surface potential, ε_{AlGaAs} and d_{AlGaAs} are the permittivity and thickness of the top AlGaAs barrier layer, and V is applied voltage to the input branch. We obtained C = 1.8 mF/m^2 from $\varepsilon_{AlGaAs} = 1.1 \times 10^{-10}$ F/m and d_{AlGaAs} = 60 nm respectively. In terms of charging a capacitance, positive input voltage cancels V_0 and reduces the electrons in the channel. Assuming the linear transport in the branch, $G_L = \mu_e e n_S(V_L) = e\mu_e C(V_0 - \phi_S - V_L)W$ and $G_R = \mu_e e n_S(-V_L) = e\mu_e C(V_0 - \phi_S + V_L)W$ (μ_e is electron mobility and W is nanowire width). We find that the conductance is controlled by the input voltage. Substituting G_L and G_R in Eq. (4.1), we obtain

$$V_C = -\frac{1}{V_0 - \phi_S} V_L^2 . \tag{5.4}$$

This simple equation clearly demonstrates that the bell-shaped curve and the surface potential directly relates to the curvature. As the surface potential increases, the curvature increases and the nonlinear curve becomes abrupt. In addition, considering $en_{S0} = C(V_0 - \phi_S)$ for 2D carrier density at $V_L = 0$, Eq.(5.4) is expressed as follows,

$$V_C = -\frac{C}{en_{S0}} V_L^2 . \tag{5.5}$$

Since n_{S0} is proportional to Fermi energy, E_F, in the case of two-dimensional electron channel, the curvature is proportional to the inverse of E_F. This Fermi energy dependence is similar to that predicted by the ballistic transport model [7]. Eq. (5.5) also indicates that a narrow nanowire with small carrier density shows an abrupt nonlinear curve, which is consistent with our previous result [8].

In addition, we also characterized the wavelength dependence. From *I-V* measurements as shown in Fig. 5-8, the 658 nm light resulted in a large conductance change, while the change by the 405 nm light was small. This was because light penetration length in AlGaAs of the 405 nm light was 17 nm, which was less than the AlGaAs thickness and the light could not excite the carriers in the AlGaAs/GaAs interface. A slight increase in current was also observed even in the branch without light irradiation

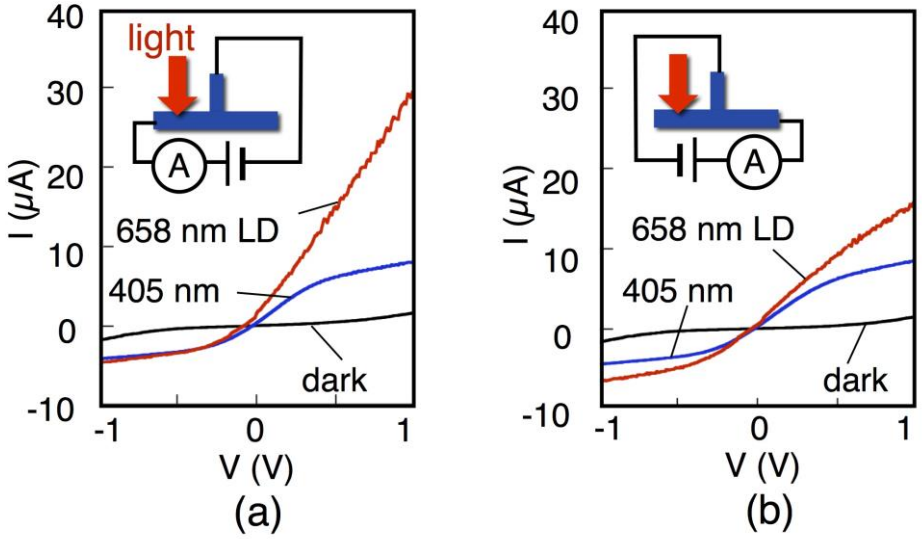

Fig. 5-8 Measured current-voltage characteristics in (a) left branch and (b) right branch with local light irradiation on left branch.

in Fig. 5-8(b), because of the diffusion of the photogenerated carriers in the laser-irradiated branch to the other branches. Measured nonlinear curves with local light irradiation are shown in Fig. 5-9. The LD power was 0.047 mW for both wavelengths. By irradiating the left branch, the curves only in $V_L > 0$ moved upward. Whereas the curve moved upward only in $V_L < 0$, when the right branch was irradiated. Similar to the *I-V* characteristics in Fig. 5-8, the 658 nm light caused larger modification of the curve than the 405 nm light. The top of the convex curve shifted to the left when the right branch was irradiated, while the curve shifted to the right when the left branch was irradiated. The amount of the shift was large when the 658 nm light was irradiated.

Observed behaviors were analyzed by our model. When the light was irradiated on the left branch, only the left branch conductance G_L was modified such as $G_L = e\mu_e C(V_0 + \Delta V_0 - \phi_S - V_L)W$, where ΔV_0 represents the increase of the carriers by the light irradiation. Then Eq. (5.4) is modified as follows,

$$V_C = -\frac{(V_L - \Delta V_0)V_L}{V_0 + \Delta V_0 - \phi_S} = \frac{-(V_L - \Delta V_0/2)^2 + \Delta V_0{}^2/4}{V_0 + \Delta V_0 - \phi_S}. \tag{5.6}$$

The formula suggests that the convex curve shifts to the right and the top moves upward when the left branch is irradiated. Calculated curves with $\Delta V_0 = 0.2$ V and 0.9 V are shown in Fig. 5-10. The value of $V_0 - \phi_S$ in the calculation was estimated from the curve in dark and $V_0 - \phi_S = 2.3$ V was used. The calculated curves reproduce the basic behaviors of the experimental ones in Fig. 5-10. Estimated photo-excited carriers by the 658 nm light with 0.047 mW was 1.5×10^{12} cm^{-2}. Obtained carrier density corresponds to $\Delta V_0 = 1.8$ V at quantum efficiency = 1. Considering the reduction of the effective quantum efficiency by surface recombination [9], estimated ΔV_0 is reasonably in agreement with the assumed

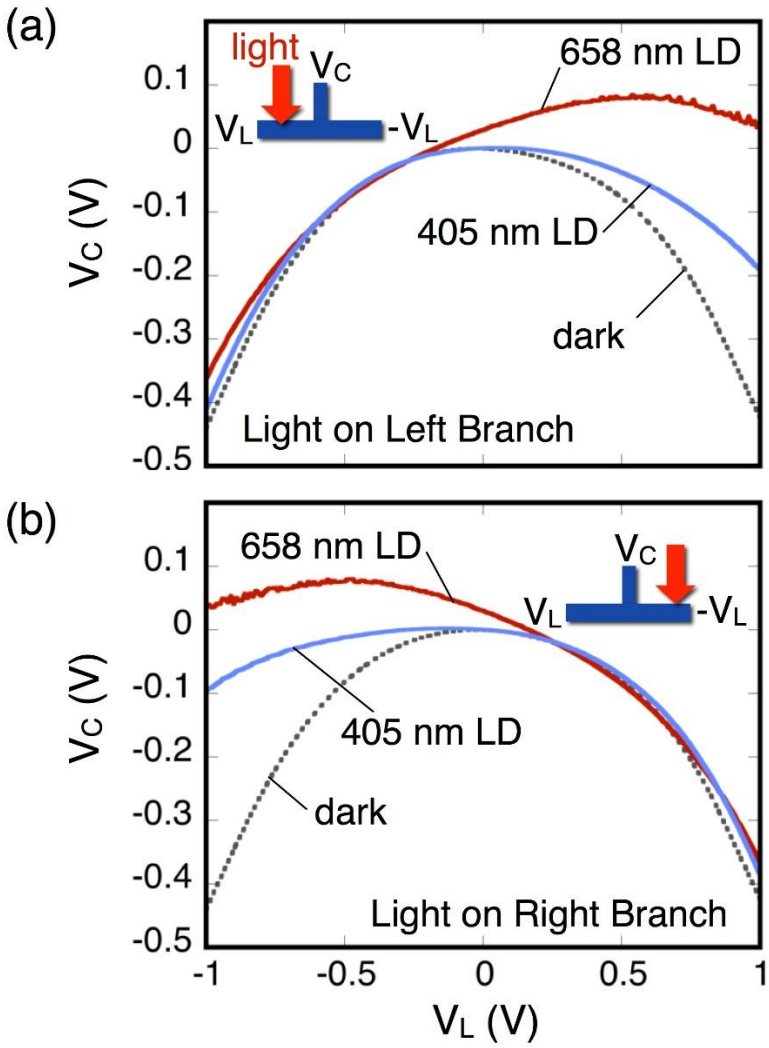

Fig. 5-9 Measured voltage transfer curves with local light irradiation on (a) left branch and (b) right branch.

value for calculation. Curvatures of the calculated curves for $V_L < 0$ V in Fig. 5-10(a) and $V_L > 0$ V in Fig. 5-10(b) was smaller than the experimental ones in Fig. 5-10. This discrepancy suggested the increase of the conductance in non-irradiated branch. It was verified from the measured current in Fig. 5-9. V_0 in Eq. (5.6) increased simultaneously

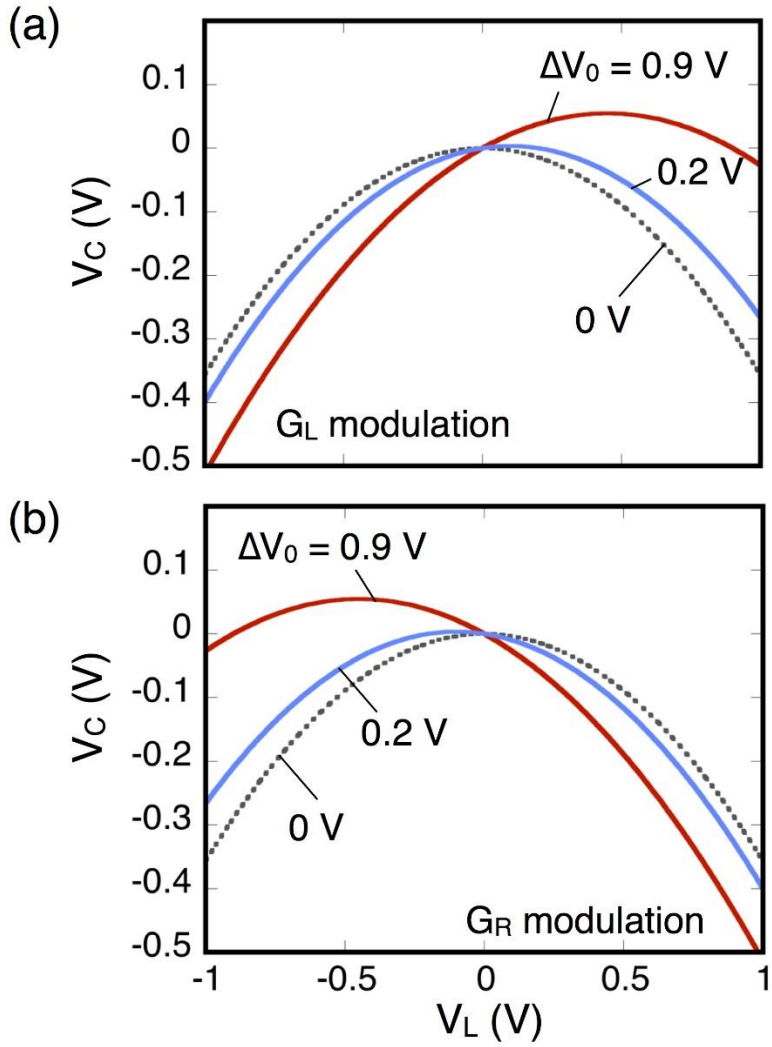

Fig. 5-10 Calculated voltage transfer curves for (a) left branch conductance modulation and (b) right branch conductance modulation.

and the curvature itself decreased. Observed behaviors of the current and nonlinear characteristics in the GaAs-based TBJ were consistently understood by our model.

5.4 Conclusion

Nonlinear voltage transfer characteristics in GaAs-based three-branch nanowire junction (TBJ) devices were investigated by a light-induced local conductance modulation method. The nonlinear transfer curve greatly changed only when the laser was irradiated on the positively biased branch. The conductance domain was found to exist at the end of the positively biased branch of the TBJ. A SiN layer deposited on the TBJ increased the surface potential and reinforced the nonlinearity in the transfer curve. The obtained results indicate that the asymmetric channel depletion model is appropriate for the observed nonlinearity mechanism in the GaAs TBJ at room temperature.

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Chapter 6 Detection of discrete electron trap in a GaAs-based nanowire through metal-tip induced surface potential modulation

6.1 Introduction

Electron traps in a semiconductor significantly influence the electrical characteristics of semiconductor devices. Random charging and discharging of the trap causes temporal fluctuation of the electrostatic potential in the device, which often appears as current or voltage noise and affects various device performances. Because fluctuation becomes obvious as the size of the device decreases [1-3], the characterization and understanding of the charge dynamics of a surface trap has become an important issue in recent years. Although there are various scanning probe techniques that characterize the surface at an atomic scale, such as scanning tunneling spectroscopy (STS) [4-6] and electrostatic force microscopy (EFM) [7-11], they mostly characterize static properties of the surface. The detection of the dynamics of the electric properties is difficult for such systems because the small conductance of the tiny tip contact results in a delay of the electric response. Here, we focus on scanning gate microscopy (SGM) for characterizing the local transport properties of electron devices [12-24]. In this technique, the biased conducting tip of an atomic force microscope (AFM) modulates electrostatic potential locally in the device and the current passing through the device, which is not influenced by the tip conductance,

is measured. We propose and demonstrate the detection of discrete charge dynamics of electron traps in the semiconductor surface through the measurement of current noise induced by contacting a metal tip to the surface. First we describe our concept of detecting charge dynamics in the semiconductor surface. Next the proposed technique is demonstrated using an AFM system with a metal tip. Then we discuss possible approaches to obtaining information on individual traps from the measured noise.

6.2 Concept

The basic concept of detecting discrete charge dynamics of a trap in the semiconductor is shown in Fig. 6-1. We characterize the trap in a semiconductor nanowire. A metal tip comes into contact with the surface of the semiconductor nanowire channel having source and drain electrodes. A biased conducting tip acts as a small movable gate that modulates the electrostatic potential locally in the device. Drain voltage V_D is applied to the channel and drain current I_D is measured in the time domain. When a trap exists in the nanowire, it stochastically captures and emits an electron owing to thermal fluctuation. This process modulates the channel potential and is expected to cause drain current noise having binary states, called random telegraph signal (RTS) noise. We recently found that the metal contact on the surface enhanced such current noise, from the analysis on the current noise in a GaAs-based nanowire FET with single-molecule dispersion [25]. Figure 6-1(b) schematically shows the sample with a metal tip contact together with corresponding equivalent circuit. C_1 is the capacitance between the tip and the trap and C_2 is the tunnel capacitance between the trap and the channel, respectively. The trap is represented by a

node between capacitors C_1 and C_2. Charging and discharging of the trap is assumed to occur through C_2. When the tip touches the surface over the electron trap, the tip capacitively couples with the trap, as shown in Fig. 6-1(b), and the charge in the trap, in turn, influences the electrostatic potential inside the device. Computing the equivalent

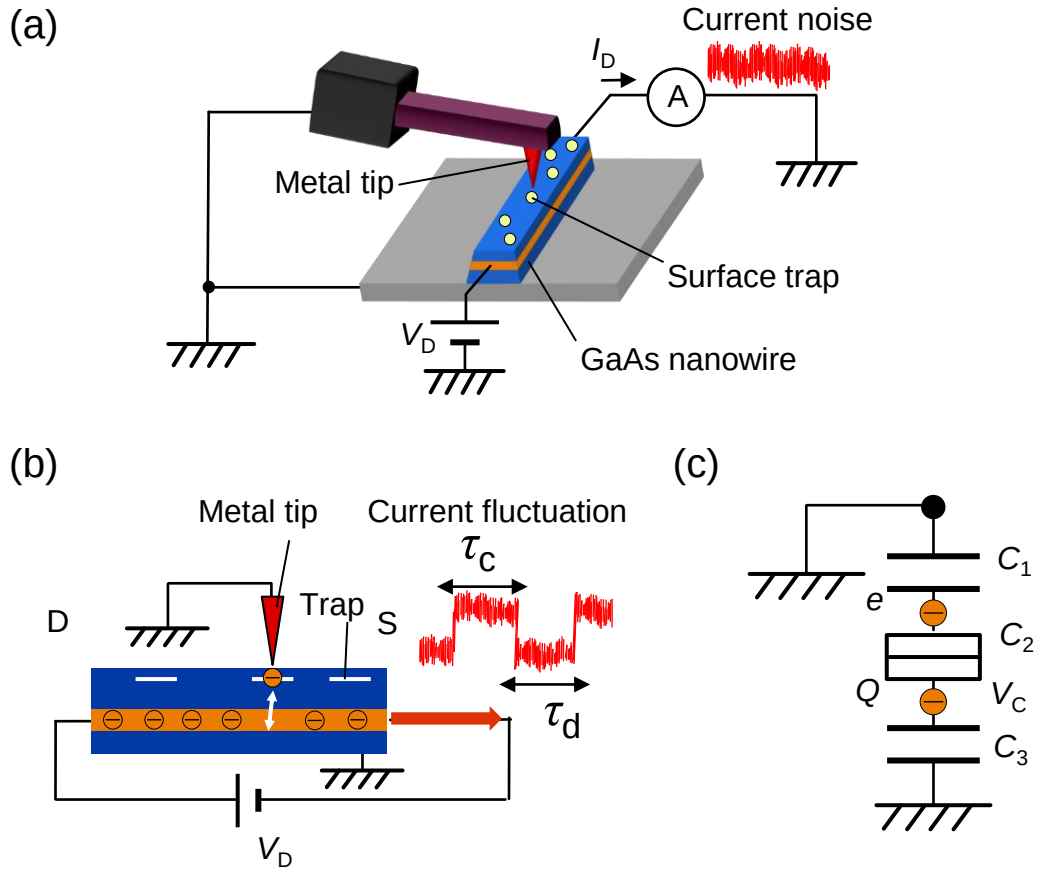


Fig. 6-1 Concept of detection of charge dynamics of trap in semiconductor surface. (a) Detection setup including AFM system with a metal tip together with I_D–V_D measurement system for GaAs-based nanowire sample. (b) Schematic views of the sample are also shown. (c) Equivalent circuits of the system with metal tip contact on the sample.

circuit, the difference of channel potential is given by

$$\Delta V_C = \frac{C_1 e}{C_1 C_2 + C_2 C_3 + C_3 C_1} . \tag{6.1}$$

It is found that V_C depends on e. Therefore, as shown in Fig. 6-1(b), RTS noise appears when a metal tip comes into contact with the surface over a trap, whereas it disappears when the tip is retracted. If there is no trap underneath the tip, RTS noise will not appear even when the tip is in contact with the surface. On the other hand, when the tip is retracted, the drain current will show small noise. In this case, from the analysis of the equivalent circuit, the channel potential V_C is found to be independent of the charge in the trap e because the distance between the tip and the surface is large resulting in C_1 is approximately zero. On the basis of this mechanism, we can detect a discrete trap in the semiconductor surface by observing RTS noise induced by a very small metal tip. In this study, we characterize the trap in the surface of a III–V compound semiconductor nanowire device, since the nanowire current is very sensitive to the surface charge owing to the high surface-area-to-volume ratio and high electron mobility. In an actual case, current in the device often includes $1/f$ noise [26-29], which is generated by a large number of traps distributed uniformly relative to the time constant [30]. Although RTS noise caused by the above mechanism might be small and difficult to distinguish from other noise, it shows a Lorentzian spectrum of $1/f^2$ slope [31, 32]. When the discrete charge dynamics of a trap takes place, the Lorentzian spectrum will be superimposed onto the $1/f$ noise spectrum, which can be detected using a spectrum analyzer having a wide dynamic range. It can be distinguished from other noise by an appropriate spectrum decomposition technique.

6.3 Experimental procedure

To demonstrate the above concept, we prepared the system shown in Fig. 6-1(a) using an atomic force microscopy (AFM) system. An etched GaAs-based nanowire was used for the device under test. The conductive AFM tip was covered with PtIr. The radius of the tip was 30 nm. In this system, the current in the nanowire was simultaneously measured with a contacting tip on the nanowire surface. The GaAs-based nanowire was fabricated on the modulation-doped AlGaAs/GaAs heterostructure having two-dimensional electron gas (2DEG) by electron beam lithography and wet chemical etching using a H_2SO_4-based etchant. The heterostructure consisted of a 10 nm n^+-GaAs cap layer, 50 nm undoped AlGaAs top barrier, Si delta-doping layer, 12 nm undoped AlGaAs spacer, 20 nm undoped GaAs channel, 100-nm AlGaAs bottom barrier, and undoped GaAs buffer on a semi-insulating (001) GaAs substrate. The sheet density of the 2DEG was 7.8×10^{11} cm^{-2} and the mobility was 7,100 cm^2V^{-1} s^{-1} at 300 K. The direction of the nanowire was <110>. Ni/Ge/Au/Ni/Au ohmic contacts were formed for the source and drain electrodes. The drain current was once amplified and converted to voltage using a low-noise amplifier whose amplification gain was 10 kV/A. We characterized the drain current in the nanowire using a voltage monitor or a spectrum analyzer. Drain voltage V_D was set at 0.85 V, where the current noise in the fabricated device sufficiently exceeded the noise floor of the measurement system of 10^{-23} A^2/Hz. All the measurements were carried out at room temperature.

6.4 Results and discussions

6.4.1 Drain current noise in time domain

Figure 6-2 shows measured drain currents with tip contact at three different surface positions, together with an AFM image of the fabricated sample. When the tip was located at position 1, the drain current showed small noise, as shown in Fig. 6-2(a). However, when the tip was located at positions 2 and 3, RTS noise was clearly superimposed, as shown in Figs. 2(b) and 2(c). The obtained results suggested that the traps existed in the surface region under positions 2 and 3. These RTS noise waveforms had different intensities and time constants. Such differences indicated that we detected different discrete traps. The RTS waveform at position 2 provided a charging time constant τ_c of

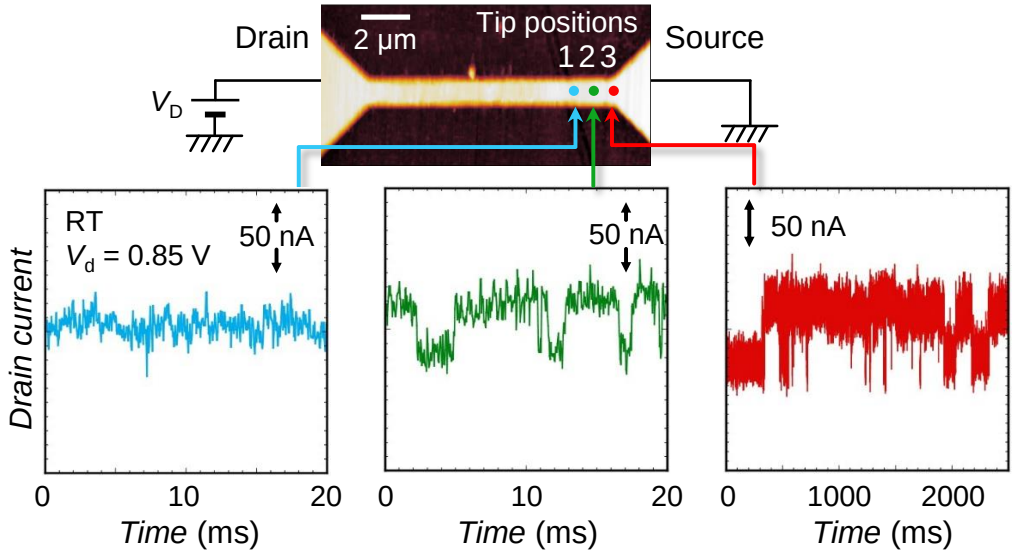


Fig. 6-2 Measured drain currents with metal tip contact at three different surface positions together with AFM image of the fabricated sample: (a) position 1, (b) position 2, and (c) position 3.

2.4 ms and discharging time constant τ_d of 8.2 ms. Here τ_c and τ_d are defined as shown in Fig. 6-1(b). We also evaluated the average time constant τ_0 from $\tau_c\tau_d/(\tau_c + \tau_d)$ and τ_0 = 1.9 ms was obtained. Similarly, the charging and discharging time constants for the RTS at position 3 were τ_c = 710 ms and τ_d = 2130 ms, respectively, and τ_0 = 530 ms was obtained. Figure 6-3 shows the tip position dependence of noise intensity at V_D = 0.85 V. The noise intensity was measured as the variance of the measured noise amplitude when the tip was in contact with the surface. The interval between measured positions was approximately 1 μm. The intensity of noise with the tip contact depended on the tip position. The noise intensity increased as the tip position became close to the source electrode, as shown in Fig. 6-3. Such dependence disappeared when the tip was retracted. This tendency could be explained by difference in potential of source and drain. High potential of source side decreased discharging time constant, therefore, RTS could be observed in source side.

Figure 6-4 shows histograms of the drain current with the tip contact at positions 2 and 3.

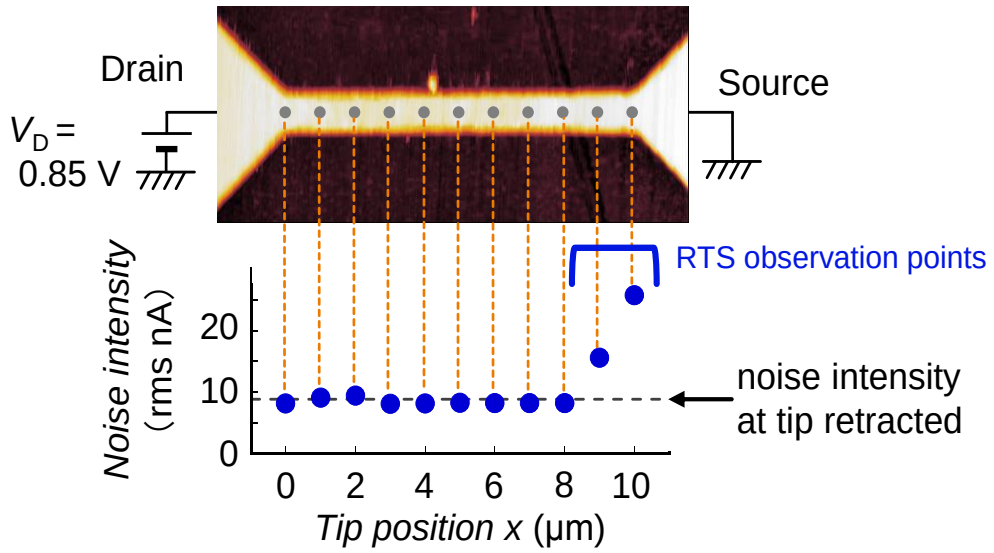
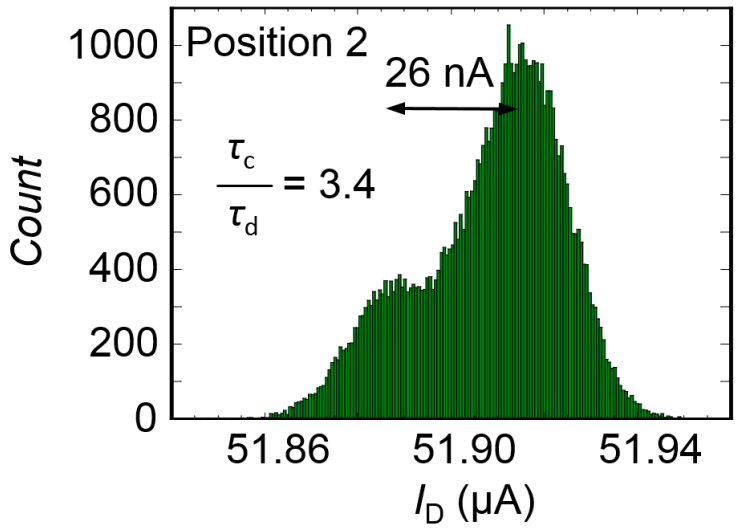


Fig. 6-3 Drain current noise intensity as a function of lateral tip contact position along the nanowire direction.

The histograms exhibited two clear peaks corresponding to binary states in the potential inside. This again indicated discrete charge dynamics. The intervals of the current peaks in Figs. 6-4(a) and 6-4(b) were 26 and 52 nA, respectively, which were equal to the average amplitudes of the RTS in Fig. 6-2. The obtained histograms also showed different

(a)



(b)

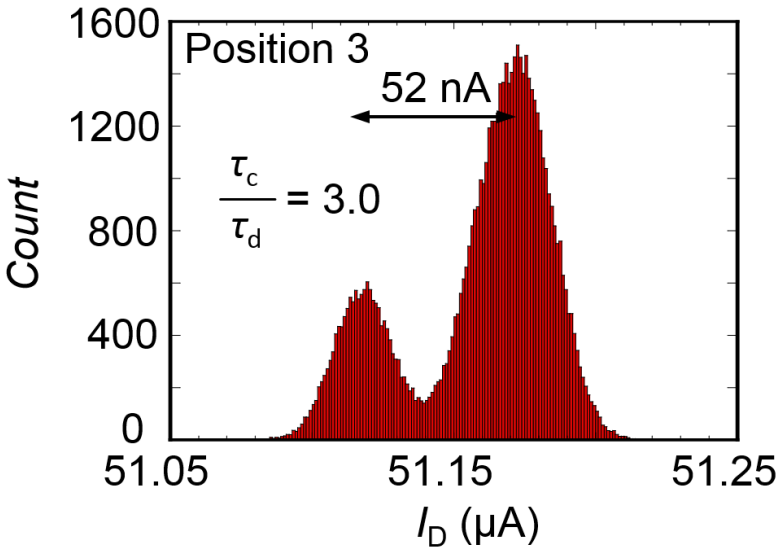


Fig.6-4 Histograms of drain current noise with metal tip contact at (a) position 2 and (b) position 3.

peak intensities between the two peaks. The ratio of the two peak intensities corresponds to the ratio of the charging and discharging time constants, τ_c/τ_d, which was evaluated to be 3.4 and 3.0 for the RTS with tip contacts at positions 2 and 3, respectively. The values were in reasonable agreement with the ratios from the time constants directly evaluated from the RTS waveforms in Fig. 6-2. The differences in the amplitudes of RTS and the ratios of the charging and discharging time constants of RTS are expected to include physical information on the trap.

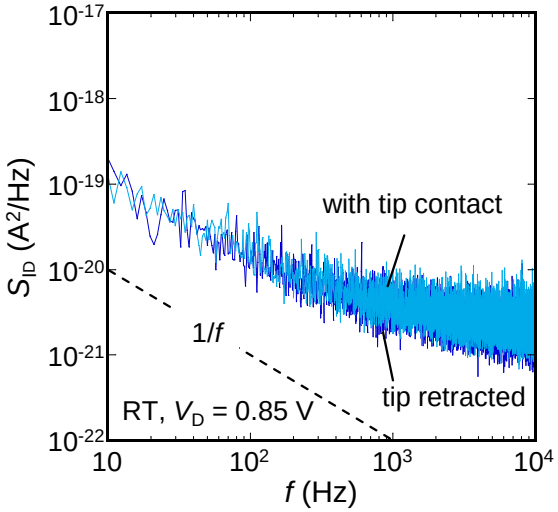
6.4.2 Drain current noise spectra

Figure 6-5 shows measured drain current noise spectra. When the tip was retracted from the surface, the 1/*f* noise was dominant. When the tip was brought into contact with the surface at position 1, a similar 1/*f* noise was again observed, as shown in Fig. 6-5(a). The noise power was also the same. On the other hand, when the tip came into contact with the surface at positions 2 and 3, the noise was increased and the configuration of the spectrum was changed. The results indicated that the tip affected the noise spectrum only when a trap existed underneath the tip. The spectrum could be well fitted by the combination of 1/*f* and Lorentzian components,

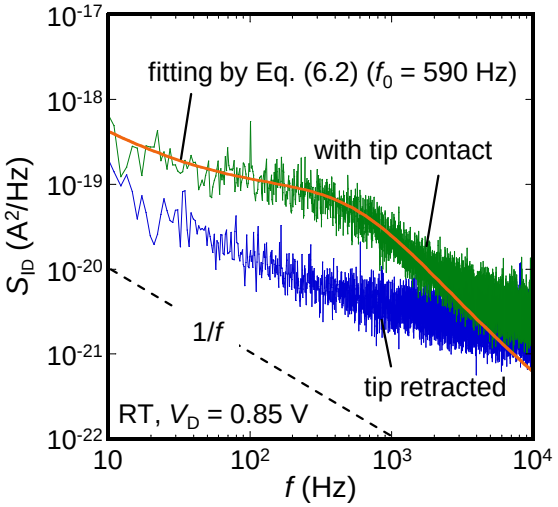
$$S_{I_D} = a\frac{1}{f} + b\frac{1}{1+\left(f/f_0\right)^2}, \tag{6.2}$$

where f_0 is a corner frequency of the Lorentzian spectrum and *a*, *b*, and f_0 are fitting parameters. From the fitting, corner frequencies of f_0 = 590 and 1.8 Hz were obtained for RTS noise at positions 2 and 3, respectively. The relationship between the corner

(a)



(b)



(c)

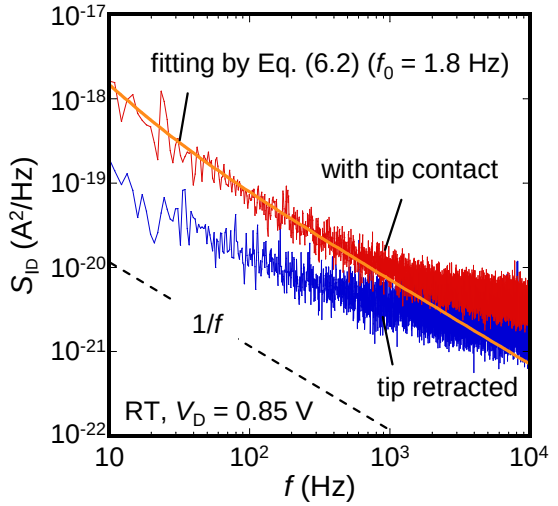


Fig. 6-5 Measured noise spectra with tip contact at (a) position 1, (b) position 2, and (c) position 3. Noise spectrum at which tip was retracted is also shown.

frequency and the average time constant τ_0 is given by $2\pi f_0 = 1/\tau_0$. The estimated f_0 from τ_0 = 0.27 ms in RTS at position 2 was 253 Hz, which was in reasonably good agreement with the corner frequency of 590 Hz from the noise spectrum. Similarly, τ_0 = 530 ms from RTS at position 3 corresponded to f_0 = 0.3 Hz, which was again reasonably in agreement with the f_0 = 1.8 Hz from the noise spectrum at position 3. The reason of differences in evaluated value were accuracy of analysis and short time characterization. Therefore, the origin of the superimposed Lorentzian spectrum at positions 2 and 3 was the same to that for the generation of the RTS in Fig. 6-2. The difference in the corner frequency was reflected in the information of the trap energy and the depth position.

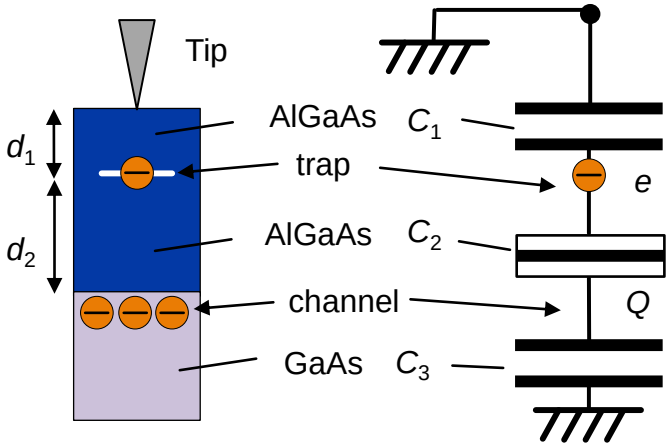
First we verify that the observed RTS arose from the charge dynamics of a single trap. For verification, we estimated the possible current change ΔI_D owing to charging and discharging of an electron in a trap. In the case of the fieldeffect transistor (FET), ΔI_D is given by $g_m\, e/C_G$, where g_m is the transconductance and C_G is the gate capacitance of the FET [31]. The value of e/C_G corresponds to the effective gate voltage ΔV_G induced by charging or discharging an electron to the gate capacitance. In our case, effective gate voltage is estimated from Eq. (6.1) instead of e/C_G. Then ΔI_D is given by

$$\Delta I_D = g_m \frac{C_1 e}{C_1 C_2 + C_2 C_3 + C_3 C_1}, \tag{6.3}$$

where $C_1 = \varepsilon_{AlGaAs} S/d_1 + \varepsilon_0 S/d_{gap}$, $C_2 = \varepsilon_{AlGaAs} S/d_2$, $C_3 = \varepsilon_{GaAs} S/d_3$, ε_{AlGaAs} is the permittivity of AlGaAs, ε_{GaAs} is the permittivity of GaAs, d_1 is the gap between the tip and the trap, d_2 is the distance between the surface trap and the channel, and d_3 is a thickness of the layer under the 2DEG channel. The effective tip area in contact with the surface S was

estimated to be 2.6×10^3 nm^2 from the tip geometry [33]. We obtained g_m of 18.8 mS/mm from the material parameters and the device geometry. Because the depth position of the trap was unknown, we calculated ΔI_D and plot the result in Fig. 6-6 as a function of d_1. The calculated ΔI_D varies in the range of 0 to 100 nA depending on the depth position of

(a)



(b)

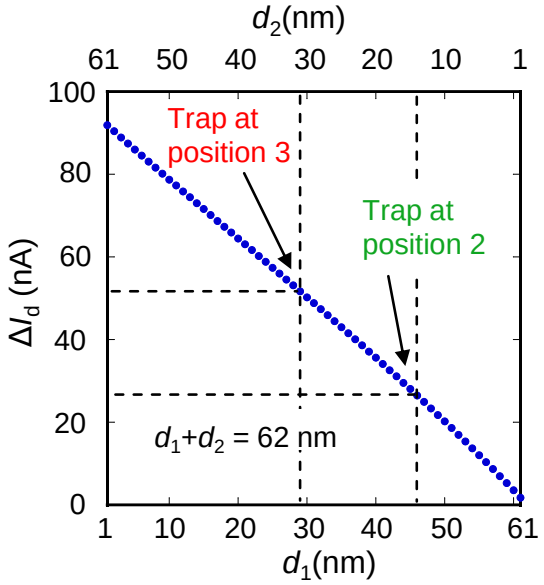


Fig. 6-6 (a) Schematic view and equivalent circuit of the sample including a trap and (b) calculated RTS amplitude ΔI_D as a function of depth position of a trap d_1.

the trap. The experimentally observed ΔI_D of 26 and 52 nA for tip contact at positions 2 and 3 can be explained by assuming d_1 = 46 and 29 nm, respectively. Although the depth position of the trap was not just at the surface at an atomic level, it was reasonable to consider that the observed RTS was caused by charging and discharging of a single trap between the surface and the channel. Charging and discharging time constants also include information on the depth position. A thick barrier between the channel and the trap should prolong the charging and discharging time constants even with the same τ_c/τ_d. Finally we discuss the energy level of the trap. Information on the trap energy E_T can be obtained from

$$\frac{\tau_c}{\tau_d} = \exp\left(\frac{E_T - E_F}{kT}\right), \tag{6.4}$$

where E_F is the Fermi energy, k is the Boltzmann constant, and T is the temperature. The evaluated $E_T - E_F$ of the traps at positions 2 and 3 were 32and 28 meV, respectively. Almost the same energy was obtained for the two positions, since the values of τ_c/τ_d were similar to each other. The evaluated trap energy was rather shallow compared with the well-known deep trap in AlGaAs, that is, DX center with an activation energy of around 0.4 eV [34]. Considering the band bending in the AlGaAs/GaAs modulation doped structure with a large surface potential of around 0.8 eV in GaAs [35], the trap energy could be aligned to the Fermi level of the 2DEG channel when the trap depth position was around 25 nm from the surface. Bringing a metal tip into contact with the surface also affected the surface potential, which would influence the trap energy estimation.

6.4.3 Tip position dependence of drain current

It is known that the surface trap density of the GaAs-based material is often as high as 10^{12} cm^{-2}, indicating that traps exist at approximately 10 nm intervals. To obtain the actual spatial distribution of the individual traps, it is necessary to measure current by changing the tip position with intervals of less than 10 nm. Figure 6-7 shows the tip position dependence of drain current. In this work, the nanowire length and width were 2 μm and 400 nm respectively. The movement of the tip was at intervals of 10 nm and V_{tip} = -3 V as in Fig. 6-7(a). RTS noise was superimposed on the drain current when the tip was at position 2 while the drain current showed the small noise when the tip contacted to the other position. This behavior indicated that the electron trap existed at position 2. The properties of drain current was obviously changed even though the intervals of tip

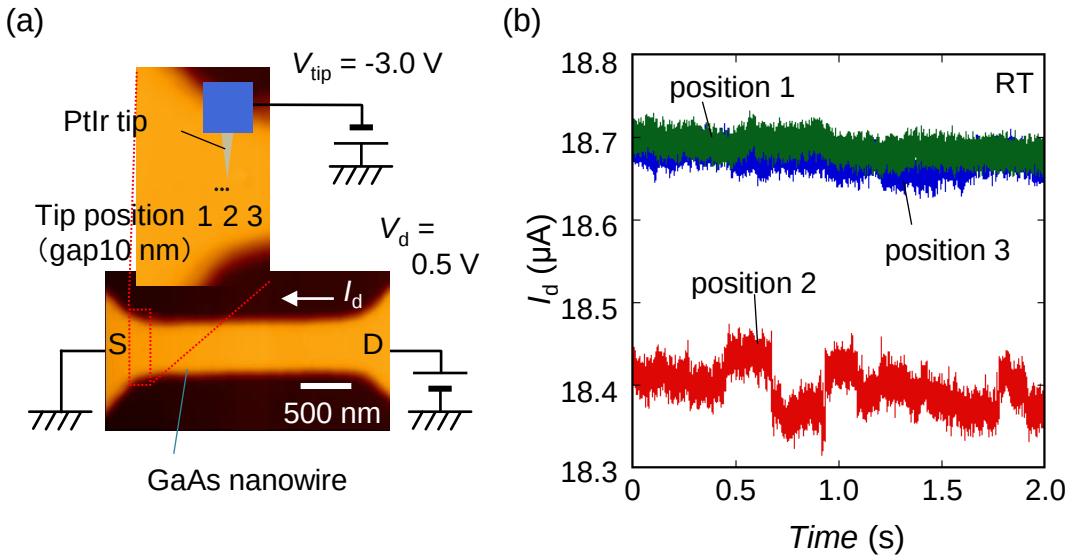


Fig. 6-7 (a) Measured drain currents with metal tip contact at three different surface positions at intervals of 10 nm. (b)Tip position dependence of the drain current.

movement was 10 nm. Therefore, detected trap might have existed near the surface. As the experimental result, this measurement system showed the potential of characterization for GaAs-based materials whose traps exist at intervals of 10 nm.

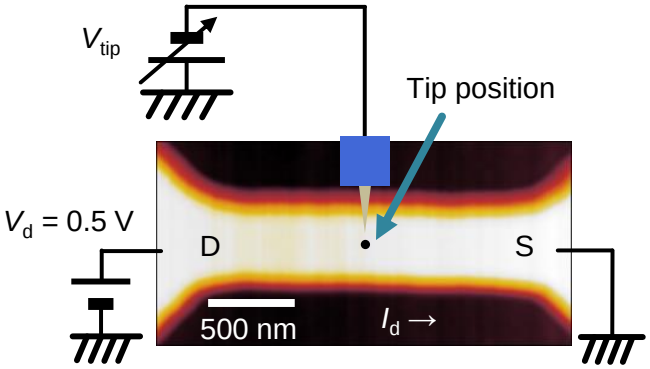
6.4.4 Tip bias dependence of drain current

To obtain the further information of the trap energy, it will be useful to characterize the tip-bias dependence of the charging and discharging time constants. If the tip bias can achieve the flat band condition, activation energy from conduction band will be evaluated using Eq. (6.4). The bias dependence of the time constants should change depending on the trap depth position, which also provides information on depth position. Such comprehensive analysis of the RTS time constants, amplitude, and their tip bias dependence in our technique will reveal the physical properties of the individual trap.

First, we confirmed the tip bias dependence of drain current as shown in Fig. 6-8. Figure 6-8(a) shows the AFM image of the fabricated device with tip position and measurement circuit and the tip bias dependence of drain current was summarized in Fig. 6-8(b). The vertical distance between the tip and nanowire surface was 20 nm in this measurement. The drain current was systematically controlled by the tip bias. This experimental result showed the metal tip certainly worked as a small gate.

Figure 6-9 shows the tip bias dependence of drain current when the tip contact on another position. The position of the tip is indicated as shown Fig. 6-9(a). When the tip is applied -3.0 V and -3.1 V, RTS noise was observed as shown in Fig 9(c) and 9(d). On the other hand, RTS noise could not be observed when the tip is applied -2.9 V as shown in Fig. 6-9(b). Moreover, capture and emission time constants are different between V_{tip} = -

(a)



(b)

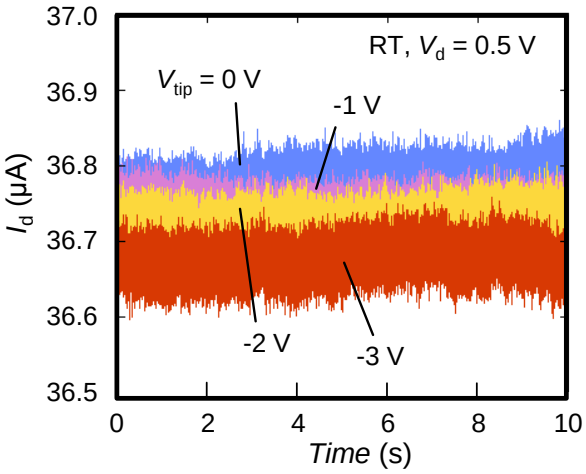


Fig. 6-8 (a) AFM image of the fabricated device with tip position and measurement circuit and (b) the tip bias dependence of drain current.

3.0 V and V_{tip} = -3.1 V. In the case of this measurement, RTS could be observed in drain side, even though RTS observed only in source side when the V_{tip} = 0 V as shown in Fig. 6-2. This was because tip bias and high source potential decreased discharging time constant in source side and it became smaller than the measurement time resolution. Figure 6-10 shows the tip bias dependence of the drain current noise spectra. When the

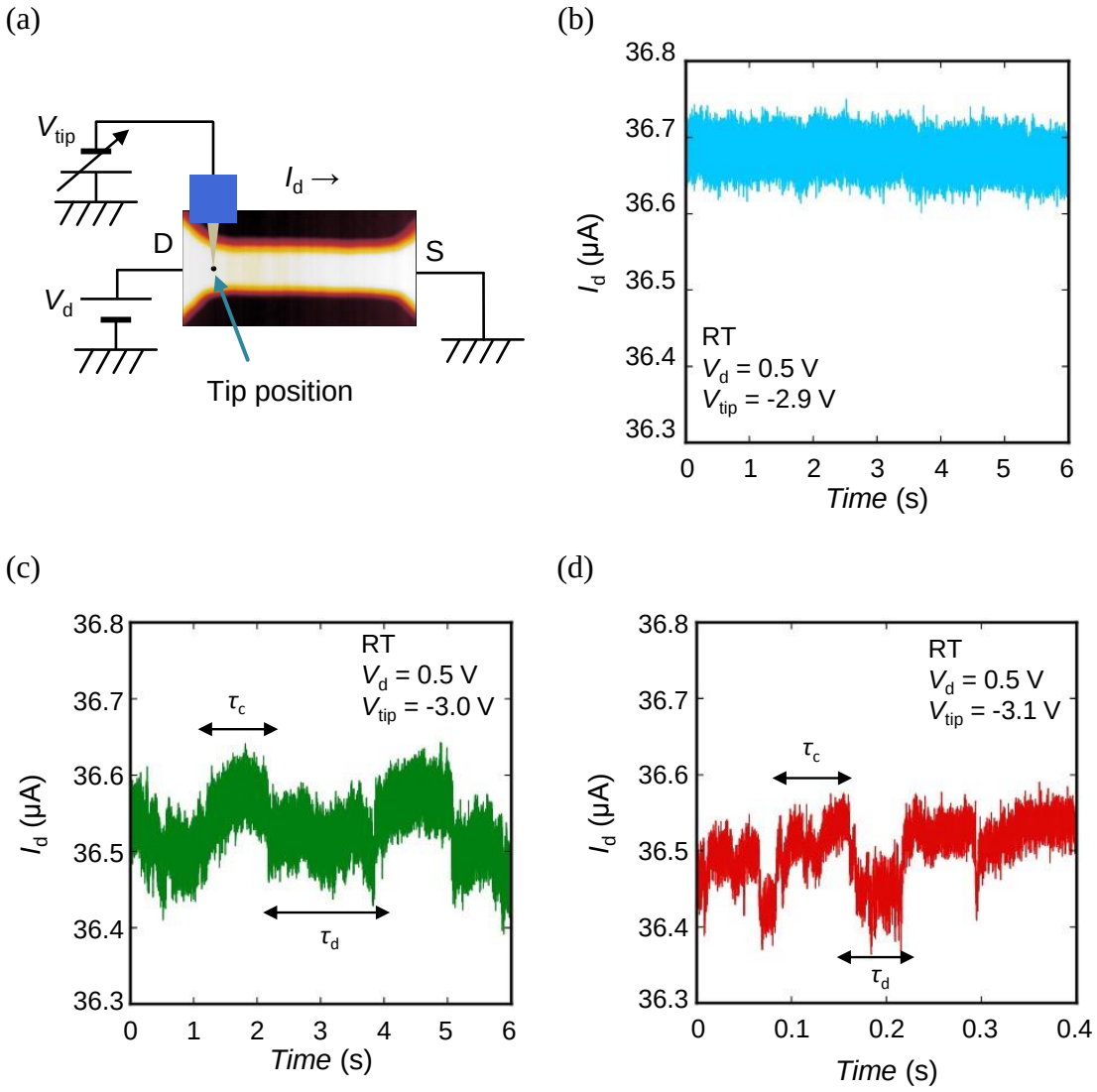


Fig. 6-9 (a) AFM image of the fabricated device with tip position and the tip bias dependence of drain current when (b) V_{tip} = -2.9 V, (c) -3.0 V, and (d) -3.1 V.

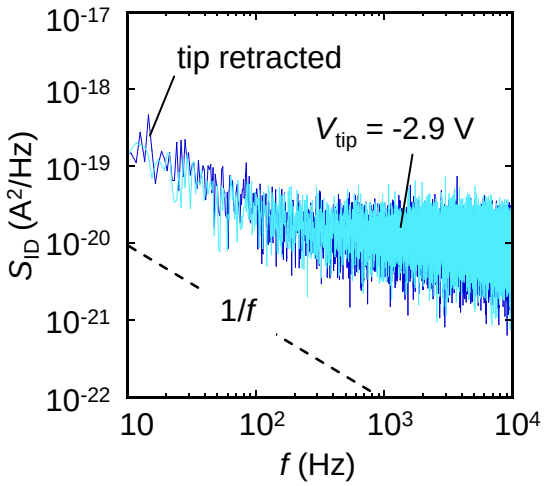
V_{tip} = -2.9 V, 1/f noise similar to the noise when the tip was retracted from the surface was dominant as shown in Fig. 6-10(a). When the V_{tip} = -3.0 V and 3.1 V, noise intensity increased and these spectrum included Lorentzian component and were well fitted by

$$S_{I_D} = a\frac{1}{f} + b\frac{1}{1+(f/f_0)^2} + c, \tag{6.5}$$

where c is a constant of thermal noise component. We detected the same trap when the V_{tip} = -3.0 V and 3.1 V because these noise intensity were same.

In order to understand these behavior of drain current noise, we consider the relationship of trap energy level and time constants. These results were summarized in Table 6-1. Trap energy were calculated by Eq. (6.4). Time constant ratio and trap energy increased when the tip bias decreased. The band diagrams of this situation is described in Fig. 6-11. Negatively biased tip raised up the surface potential and deeper trap energy level and it promoted the capture and emission of charge between the channel and trap. As a result, this caused increase of time constant ratio and it was reflected in the drain current.

(a)



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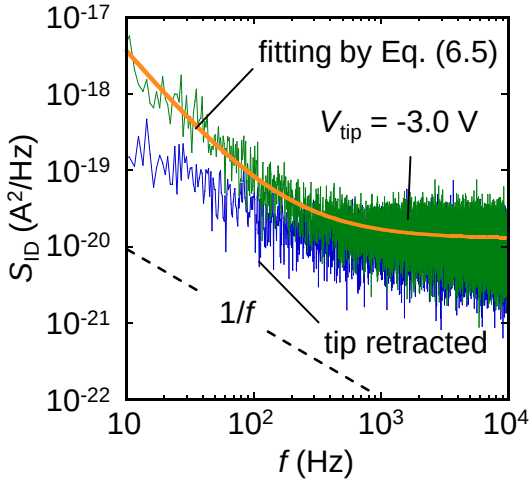

(c)

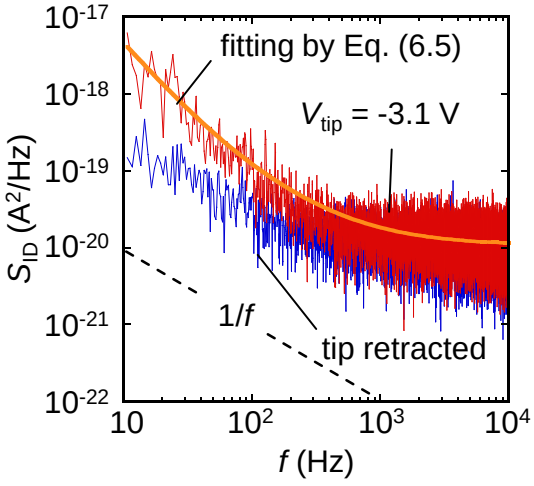

Fig. 6-10 Measured noise spectra with tip contact when (a) V_{tip} = -2.9 V, (b) -3.0 V, and (c) -3.1 V. Noise spectrum at which tip was retracted is also shown.

Table 6-1 Relationship of time constants and trap energy.

	τ_c (s)	τ_d (s)	τ_c/τ_d	$E_T - E_F$ (meV)
V_{tip} = -3.0 V	0.50	0.46	1.1	2.5
V_{tip} = -3.1 V	0.37	0.12	3.2	30

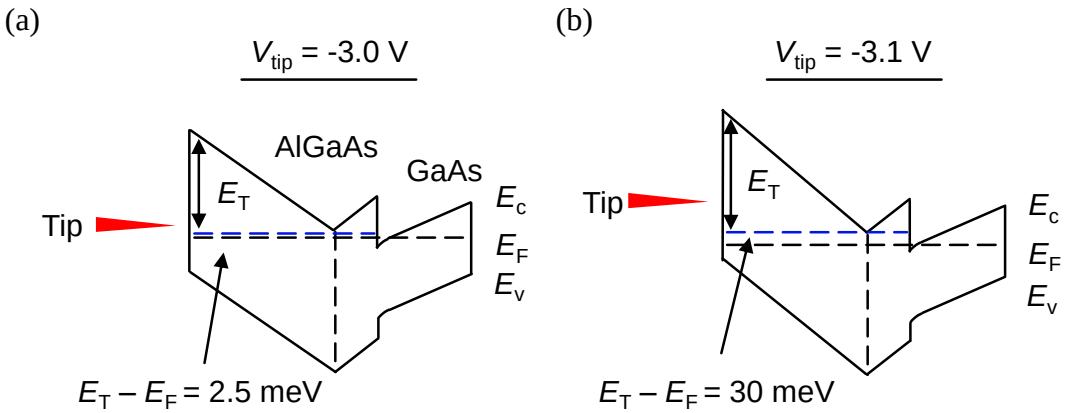

Fig. 6-11 Band diagrams of tip bias dependence measurement when (a) V_{tip} = -3.0 V and (b) -3.1 V.

6.5 Conclusion

We proposed and demonstrated a novel detection technique of discrete charge dynamics of a trap in a GaAs-based nanowire surface using current fluctuation induced by a metal tip. A simple equivalent circuit model indicated that the random telegraph signal (RTS) noise was imposed in the drain current when the metal tip came into contact with the surface. The concept was successfully demonstrated by measuring current noise in a GaAs-based nanowire set in an atomic force microscope (AFM) system with a metal tip, where RTS noise with a Lorentzian spectrum was superimposed when the metal tip came

into contact with the nanowire surface at specific positions. From the intensity and time constant of the RTS noise, we could obtain information on the energy and position of the discrete trap. The obtained results showed the possibility of detecting charge dynamics of the individual surface traps in semiconductor devices.

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Chapter 7 Conclusion

In this thesis we summarized characterization of GaAs-based TBJ devices by light-induced local conductance modulation method and detection technique of discrete electron trap in GaAs-based nanowire through metal-tip induced surface potential modulation.

Chapter 1 introduced the background and purpose of this work. We showed three-branch nanowire junction (TBJ) devices are expected for a part of the future logic circuit element but its mechanism is not clarified. And then, we also explained the novel detection technique of discrete charge dynamics of a trap in semiconductor material is needed for the advanced technology of semiconductor devices.

Chapter 2 described the basic electrical and physical properties of semiconductor nanostructure and surfaces.

Chapter 3 summarized the various scanning probe microscopy techniques and these principle.

Chapter 4 explained the electrical nonlinear characteristics in TBJ and its application. We showed the two possible model for the nonlinear characteristics in TBJ. One of them is ballistic transport model, and the other is asymmetric channel depletion model.

In chapter 5, nonlinear voltage transfer characteristics in GaAs-based TBJ devices were investigated by a light-induced local conductance modulation method.

Using this method, the nonlinear transfer curve of TBJ greatly changed only when the laser was irradiated on the positively biased branch, and we found the conductance domain existed at the end of the positively biased branch of the TBJ. We also characterized the influence of the surface on the nonlinear characteristics of TBJ using a SiN layer. The SiN layer deposited on the TBJ increased the surface potential and reinforced the nonlinearity in the transfer curve. The obtained results indicate that the asymmetric channel depletion model is appropriate for the observed nonlinearity mechanism in the GaAs-based TBJ at room temperature.

In chapter 6, we proposed and demonstrated a novel detection technique of discrete charge dynamics of a trap in a GaAs-based nanowire surface using current fluctuation induced by a metal tip. We showed a simple equivalent circuit model indicated that the random telegraph signal (RTS) noise was imposed in the drain current when the metal tip came into contact with the surface. The concept was successfully demonstrated by measuring current noise in a GaAs-based nanowire set in an atomic force microscope (AFM) system with a metal tip, where RTS noise with a Lorentzian spectrum was superimposed when the metal tip came into contact with the nanowire surface at specific positions. We could obtain information on the energy and position of the discrete trap from the intensity and time constant of the RTS noise. The obtained results showed the possibility of detecting charge dynamics of the individual surface traps in semiconductor devices.

List of publications/conferences/awards

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1. Publications related to this work

[1] 佐藤将来、村松徹、葛西誠也、「光照射局所コンダクタンス変調法を用いたGaAsナノワイヤ3分岐接合デバイスの非線形伝達特性評価と動作機構の検討」、電子情報通信学会技術研究報告 ED2011-158 (2012) pp. 95-99

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[7] 佐々木健太郎、黒田亮太、殷翔、佐藤将来、葛西誠也、「微小電荷空間分布検出半導体デバイスの基礎的検討」、2015 年電子情報通信学会ソサイエティ大会、東北大学、2015 年 9 月

5. Awards

[1] 平成24年度電子情報通信学会北海道支部学生員奨励賞（2013年3月）

[2] 新学術領域研究分子アーキテクトニクス第3回領域会議学生ポスター賞（2014年6月）

[3] International Microprocesses and Nanotechnology Conference MNC2013 Outstanding Paper Award（2014年11月）