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GaAs-Based Nanowire Devices with Multiple Asymmetric Gates for Electrical Brownian Ratchets

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GaAs-based nanowire devices having multiple asymmetric gates for electrical Brownian ratchets were fabricated and characterized. From three-dimensional potential simulation results and current-voltage characteristics, we confirmed the formation of the asymmetric potential in our device design. Direct current was generated at room temperature by repeatedly switching the potential in a multiple-asymmetric-gate device on and off. Such current was not observed in either a single-asymmetric-gate device or a multiple-symmetric-gate device. The current direction and input frequency dependences of the net current indicated that the observed current was generated by the flashing-ratchet mechanism.

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1. Introduction

Biological systems are of interest to electronics engineers because natural selection has yielded various functions characterized by high energy efficiency, low power consumption, and robustness against fluctuation.[1,2] Recent advanced semiconductor integrated logic circuit technology is facing problems achieving those characteristics[3]. An interesting example of an efficient and robust biological function is that of a molecular motor, which converts chemical energy to mechanical motion.[4] Although its input energy is as small as thermal energy, it can produce coherent force.[5] The high conversion efficiency of molecular motors suggests that they favor thermal energy.[6–8] A Brownian ratchet is a possible mechanism for molecular motors.[5,9] It rectifies a particle's random motion (Brownian motion) by using a periodic but asymmetric potential.[10–16] The rectification does not break the second law of thermodynamics if the system is not adiabatic. Several experimental studies on electrical implementations of Brownian ratchets using semiconductors have been reported,[17–22] but the operation of such ratchets at room temperature has not been achieved. The purpose of the work reported here is to demonstrate that a GaAs-based nanowire device with appropriately designed multiple asymmetric gates can function as an electrical Brownian ratchet.

2. Basic Concept and Device Design

An electrical Brownian ratchet device generates direct current from fluctuating electron motions. It uses an asymmetric potential that works as a ratchet, skewing the distribution of the carrier motion to one direction. The periodic arrangement of asymmetric potentials, as shown in Fig. 1(a), is expected to enhance the coherency of

the electron motion. There are two typical operation modes used to generate directional current: the *flashing ratchet*, in which an asymmetric potential is built and diminished repeatedly by a zero-average external signal,[12–16,22] and the *rocking ratchet*, in which an asymmetric potential is rocked by an external force.[10,11,17,18] In this study, we investigate the flashing ratchet, the basic concept of which is shown schematically in Fig. 1(a). A narrow channel has a periodic asymmetric potential that can be turned on and off. When the potential is first turned on, Brownian particles are trapped in potential valleys. When the potential is turned off, they diffuse forward and backward along the channel. When the potential is turned on again, some of the diffusing particles move to the next valley, as shown at the bottom of Fig. 1(a), whereas the others are trapped in the same valley. Repeating this process generates a directed particle flow. If the particles are charge carriers, direct current flows in the channel.

The design of the device in this study is shown in Fig. 1(b). A GaAs-based nanowire was used for the channel to limit the electron motion in one direction[23–25] and to obtain the obvious skew of the carrier distribution. Electrons in this material system have a high mobility and a large diffusion coefficient. Asymmetric Schottky wrap gates (WPGs) produce periodically arranged asymmetric potentials. Each gate has a notch on top of the nanowire. To confirm the formation of the asymmetric potential in this structure, we carried out potential simulation by numerically solving the three-dimensional Poisson equation. The result is shown in Fig. 2, where one sees that an asymmetric potential forms at the center of the channel and that the potential barrier height depends on the gate voltage.

3. Experimental Procedure

The GaAs-based nanowire was formed in the <-110> direction on modulation-doped AlGaAs/GaAs heterostructure on a (001) GaAs substrate by EB lithography and wet chemical etching using a H_2SO_4-based etchant. The mobility and carrier concentration of two-dimensional electron gas (2DEG) were respectively 7,100 $cm^2 V^{-1} s^{-1}$ and 7.8×10^{11} cm^{-2} at room temperature (RT), and 110,000 $cm^2 V^{-1} s^{-1}$ and 7.8×10^{11} cm^{-2} at 77 K. In the modulation-doped AlGaA/GaAs system, the mobility at temperatures between 300 and 77 K is controlled by polar optical phonon scattering.[26)] Since this scattering decreases as temperature decreases, the mobility increases as temperature decreases.[26, 27)] Electrons in the GaAs channel are generated by Si donors selectively doped into the AlGaAs layer and the thermal activation of the donors makes the 2DEG concentration temperature-dependent. Because the activation energy of the Si donor into the AlGaAs layer is 10-20 meV,[28)] the carrier concentration does not change significantly at temperatures between 77 and 300 K. The mean free path was estimated to be 100 nm at RT and 1,600 nm at 77 K. After Ni/Ge/Au/Ni/Au Ohmic source and drain electrodes were formed by vacuum deposition. 20 asymmetric WPGs were formed by EB lithography and PtPd deposition. A scanning electron microscopy (SEM) image of the device is shown in **Fig. 3**. The nanowire width W, gate length L_G, and distance D between the gates were 300, 300, and 150 nm, respectively. Each potential barrier along the nanowire direction, $L_G + D$, was longer than the electron mean free path at RT, which was necessary to cause the drift motion of the electrons along the potential slope. The number of gates we used was chosen because it is similar to that in the device reported by Rousselet *et al.*[15)] The number of gates affects the amount of current generated,[22)] and the relationship between current and gate number is an interesting subject. For comparison, we also fabricated other devices with either multiple

symmetric gates, a single asymmetric gate, or a single symmetric gate. The device dimensions are summarized in Table I.

We characterized the potential configuration in the fabricated device by drain current-gate voltage (I_D-V_G) and drain current-drain voltage (I_D-V_D) measurements. Then, we characterized the flashing-ratchet operation by measuring the drain current without drain voltage at RT.

4. Characterization of Potential Asymmetry

To confirm the asymmetric potential configuration in the fabricated devices, we measured I_D-V_G characteristics in single-gate devices and then measured them again after exchanging the source and drain electrodes. For comparison, we also measured these characteristics in a single-symmetric-gate device. A device with either an asymmetric or symmetric gate operated as a conventional field–effect transistor (FET) (Fig. 4) and, at RT, no difference was observed when the source and drain electrodes were exchanged. The results obtained when we measured I_D-V_G characteristics at 10 K are shown in Fig. 5. As shown in Fig. 5(a), in the asymmetric-gate device, a threshold voltage shift ΔV_{th} of 150 mV was observed when the source and drain electrodes were exchanged. A similar shift was observed in the other asymmetric-gate devices. As shown in **Fig. 5(b)**, however, no threshold voltage shift was observed in the symmetric-gate device. These results suggest that the observed ΔV_{th} was due to the asymmetric potential in the channel.

The relationship between the asymmetric potential and the threshold voltage shift could be due to a mechanism similar to the drain-induced barrier lowering (DIBL) in the FET.[29] That is, the potential barrier under the gate is pulled down by the drain

bias. The amount of the potential barrier lowering on the drain side is larger than that on the source side connected to the ground. When the gate length is small, this effect extends to the source side and the potential barrier height decreases. The amount of potential barrier lowering is large when the position of the potential top is close to the drain. This possibly results in the observed threshold voltage shift. The DIBL in the FET occurs when the gate length is in the submicron range.[30] Considering that the basic operation of the present device is the same as that of the FET, together with the gate length of 400 nm, the DIBL would occur in the fabricated device. If a 400-nm-long asymmetric gate were equivalent to the combination of a 250-nm-long uniform gate and a 150-nm-long ungated portion, the theory in Ref. 30 would predict a ΔV_{th} of about 100 mV, close to the observed ΔV_{th} = 150 mV.

We evaluated the difference in barrier height, $\Delta\varphi$, between the two measurement circuit configurations from the drain current difference. In the subthreshold region of the FET transfer characteristic, where $\log(I_D)$ changes linearly with V_G, I_D is proportional to $\exp[(\alpha V_G - \Delta E)/kT]$. α is a V_G-to-energy scaling factor ($\alpha = \Delta E/\Delta V_G$) and ΔE is the potential barrier height. From the two curves in Fig. 5(a), $\Delta\varphi$ at each gate voltage is calculated using the following equation without α:

$$\Delta\varphi = \Delta E_2 - \Delta E_1 = kT \ln\left[\frac{I_{D1}(V_G)}{I_{D2}(V_G)}\right], \qquad (1)$$

where ΔE_1 and ΔE_2 are the barrier heights in the measurement circuit with the exchanged source and drain electrodes. The evaluated $\Delta\varphi$ is plotted against V_G in Fig. 6(b). We obtained a barrier height difference of 5 meV at $V_G = -1.2$ V. Since this value was much smaller than the thermal energy at RT, it was difficult to see the potential difference at RT. Note that $\Delta\varphi$ smaller than kT does not mean that there is no

asymmetric potential. The consistency between the obtained ΔV_{th} and $\Delta\varphi$ can be examined using the relation $\Delta\varphi = \alpha \Delta V_{th}$. α can be evaluated from the slope of the linear part of the log(I_D)-vs-V_G plot, and the left and right curves in Fig. 5(a) yield α values of 0.06 and 0.04, respectively. Using the average value of 0.05 for simplicity, the $\Delta\varphi$ of 5 meV results in a ΔV_{th} of 100 mV. This value is reasonably close to the observed ΔV_{th} of 150 mV. The result suggests that the DIBL model is appropriate for the observed threshold voltage shift.

Next, we evaluated the temperature dependence of the potential barrier height by considering the temperature dependence of the I_D-V_D characteristics. Here, the gate voltage was biased at −1.3 V. A plot of log|I_D| against V_D showed a linear curve and the slope became steep as temperature decreased. We assumed thermionic emission over the potential barrier and evaluated the saturation current I_0 at V_D = 0 V by extrapolating the linear region of the log|I_D|-V_D curves. Assuming Arrhenius-type current activation, I_0 is expressed by the following equation

$$I_0 \propto \exp\left(-\frac{\Delta E}{kT}\right). \qquad (2)$$

We estimated ΔE from the Arrhenius plot of I_0. The result is shown in Fig. 7. The barrier height at V_G = −1.3 V was estimated to be 12 meV. This value is much smaller than the thermal energy at RT. It is noted that, as seen in the results of the potential simulation in Fig. 2, the barrier height could be adjusted by changing the gate voltage. A higher potential barrier could be obtained by further decreasing the gate voltage.

5. Flashing-Ratchet Operation

The measurement circuit for flashing-ratchet operation is shown in Fig. 8(a). All the gates were biased at the threshold voltage and a square wave with a

peak-to-peak voltage V_{PP} of 1 V was applied to them. Then, the DC net current in the drain, $I_{NET,}$ was measured. Note that a drain voltage was not applied. For comparison, we characterized devices with multiple symmetric gates and a single asymmetric gate (Table I). The threshold voltages of these devices were different from each other. Therefore, the gate voltage in each device was biased at its threshold value, and then −0.5 V was added as the ON potential and +0.5 V was added as the OFF potential. The threshold voltage of both the multiple-asymmetric-gate and multiple-symmetric-gate devices was 0 V, whereas that of the single-asymmetric-gate device was −0.8 V. The difference was attributed to the difference in nanowire surface condition. It is known that there are high-density surface states on III-V compound semiconductors and they make the threshold voltage unstable.[31)] This instability also often causes the threshold voltage to be temperature-dependent. When −0.5 V was added to the gate, the drain current was in the subthreshold region, and from $\Delta E = \alpha(V_G - V_{th})$, it was expected that a potential barrier 50 meV high would be formed. Figure 8(b) shows the result of the flashing-ratchet operation. The measurement was carried out at RT. A negative current was observed in the multiple-asymmetric-gate device at a flashing frequency f of more than 1 MHz, and its amount increased with f. On the other hand, no obvious current was seen in other devices.

To verify whether the observed current is actually generated by the flashing Brownian ratchet mechanism, we examined the direction and magnitude of the current. In a flashing-ratchet device, the current direction is determined by the direction of the skew of the potential barrier. As shown in Fig. 2, the position is highest where the metal wrapping of the nanowire is narrowest. When the potential barriers are flashing, electrons move from the steep-slope side to the gentle-slope side as shown in Fig. 1(a).

According to this behavior, in Fig. 8(a), electrons move from the drain side to the source side. Thus, the I_{NET} generated by the flashing-ratchet mechanism must be negative. The observed current direction was consistent with this, indicating that the present device operated as a flashing ratchet. The frequency dependence of the DC current excluded the possibility of simple rectification of the input signal through the Schottky gate.

We next compared the experimental I_{NET}-vs- f curve with the theoretical current estimated using the simple model expressed by

$$I_{Theory} = e \cdot n_s \cdot \beta \cdot (D + L_G) \cdot f \cdot W, \qquad (3)$$

where e is the electron charge, n_s is the 2DEG sheet carrier concentration, β is the carrier transfer rate (the fraction of carriers moving to the next potential), and W is the nanowire channel width. This equation was deduced from the average velocity v in Ref. 15 ($v = \beta L f$, where L is the length of each potential). Then, we obtained $I_{NET} = e\, n_s\, v\, W$. β was evaluated from the potential asymmetry, size, and carrier diffusion length (the product of the diffusion constant of the carrier and the potential-OFF time).[15] The β for the present device design and material was approximately 0.5. The theoretical curve is shown in Fig. 8(b) with a broken line. It reproduced the trend of the experimental curve. The amount of current was of the same order as the experimental one but smaller. A possible explanation for the difference is the accumulation of carriers in the channel when a positive gate voltage was applied for the potential-OFF. At V_G = +0.5 V + V_{th} in the multiple-asymmetric-gate device, the carrier concentration underneath the gate increased as compared with that at V_G = 0 V.

We also characterized the pulse regularity dependence of I_{NET}. A pseudo-random pulse train was used for flashing the potential, and the results were compared with those obtained when a regular pulse train was used. If the flashing

period is irregular, the net current is expected to decrease because the correlation time decreases.[32,33] In this measurement the average ON and OFF times were equal to each other; thus, the power of the random pulse train was the same as that of the regular pulse train. The results obtained are shown in Fig. 9. The net current was found to depend on the regularity of the input pulse train. The ratio of the I_{NET} generated by the regular and random pulse trains was evaluated and is plotted in Fig. 9. 50% electron transfer loss was observed in the random flashing. A possible reason for this loss is the longer effective flashing cycle of the random pulse train. The net current is determined by the number of ON-OFF transitions of the potential per unit time. In the case of the regular pulse train, the transition occurs in every period defined by the flashing frequency. In the case of the random pulse train, on the other hand, the transition occurs stochastically with a probability of 0.5 in every clock cycle. This indicates that the transfer of carriers occurs with 50% probability. Thus, the I_{NET} generated with the random pulse train is half that with the regular pulse train.

6. Conclusions

GaAs-based nanowire devices with multiple asymmetric gates for electrical Brownian ratchets were fabricated and characterized. Three-dimensional potential simulation results and current-voltage characteristics confirmed the formation of asymmetric potentials. Direct current was generated at room temperature by flashing-ratchet operation in a device with multiple asymmetric gates but not in one with a single asymmetric gate or multiple symmetric gates. The direction of the current and the flashing-frequency dependence of the net current indicated that the observed current was generated by the flashing-ratchet mechanism.

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Figure captions

Figure 1. (a) Schematic illustration of flashing-ratchet operation. Particles trapped in the potential valleys diffuse forward and backward when the potential barriers disappear (OFF). When the potential barriers are built up again (ON), the fraction of particles in the next valley on the forward side is greater than that in the adjacent valley on the backward side. Repeating this process produces a directed particle flow. (b) GaAs-based nanowire device with multiple asymmetric Schottky wrap gates (WPGs).

Figure 2. Cross-sectional channel potentials in the asymmetric-gate device (calculated in three-dimensional potential simulations at various gate voltages). The inset shows the contour plot of the potential at $V_G = -1.5$ V.

Figure 3. SEM image of multiple-asymmetric-gate device. The nanowire was formed by etching an AlGaAs/GaAs heterostructure. The nanowire width W was 300 nm. The gate length of the longest portion, L_G, was 300 nm. The distance between the gates, D, was 150 nm.

Figure 4. I_D-V_D characteristics in the single-asymmetric gate device measured at room temperature.

Figure 5. I_D-V_G characteristics measured at 10 K in (a) the asymmetric gate device and (b) the symmetric gate device.

Figure 6. (a) Model for the threshold voltage shift. The potential on the drain side is pulled down by the drain bias. When the potential is asymmetric, the barrier height measured from the source potential changes when the source and drain terminals are exchanged. (b) Estimated barrier height difference plotted against drain currents measured as shown in **Fig 6(a)**. The 5 meV difference indicates the existence of the asymmetric potential.

Figure 7. Arrhenius plot of the drain current I_D at $V_G = -1.3$ V. I_0 was obtained by extrapolating the linear part of the $\log(I_D)$-V_D curve to $V_D = 0$.

Figure 8. (a) Flashing-ratchet measurement circuit. The potential was flashed out using a regular rectangular wave with a duty ratio of 50%. The DC net current I_{NET} was measured at the drain. The top of each potential barrier skews to the source side. (b) Measured I_{NET} in flashing-ratchet operation at RT. Currents from a multiple-asymmetric-gate device, a single-asymmetric gate device, and a multiple-symmetric-gate device are plotted as a function of flashing frequency. Current was generated only in the multiple-asymmetric-gate device. The dotted line is the theoretical curve calculated using Eq. (3).

Figure 9. Measured DC net current in the multiple-asymmetric-gate device operated with a pseudo-random pulse train. The generated current was half that generated using a regular pulse train with the same amplitude.

Table I. Device dimensions. *W* is nanowire width, L_G is gate length, and *D* is gate distance.

Device	Gate shape	Number of gates	W (nm)	L_G (nm)	D (nm)
	Asymmetric	20	300	300	150
	Symmetric	20	300	300	150
	Asymmetric	1	300	400	
	Symmetric	1	300	300	

Table I Takayuki Tanaka et al.

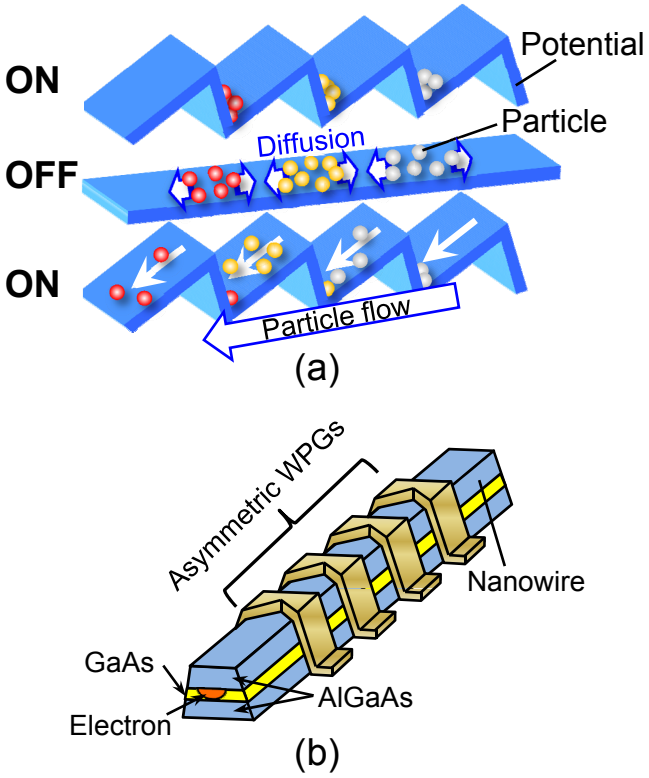


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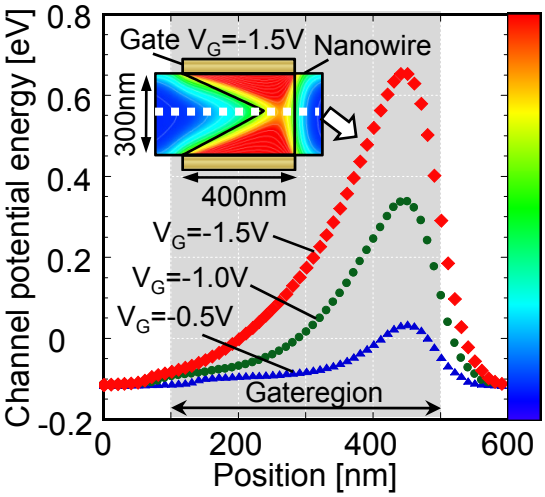


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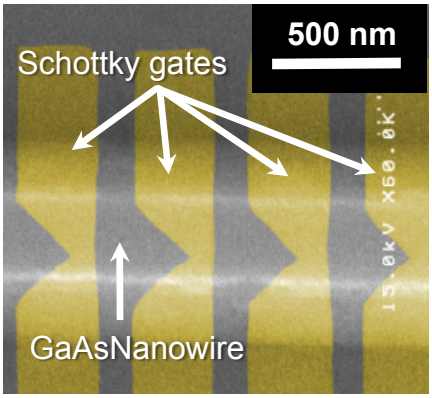


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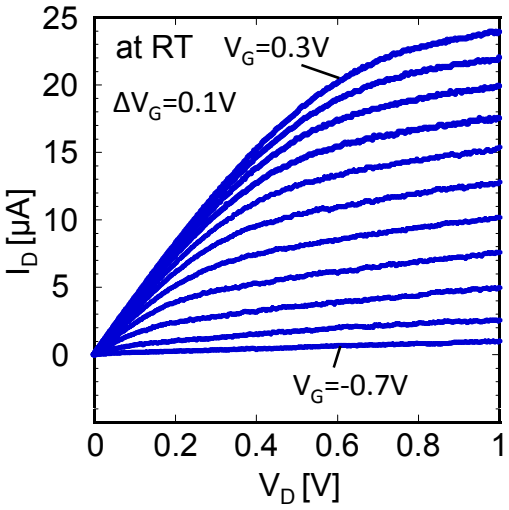


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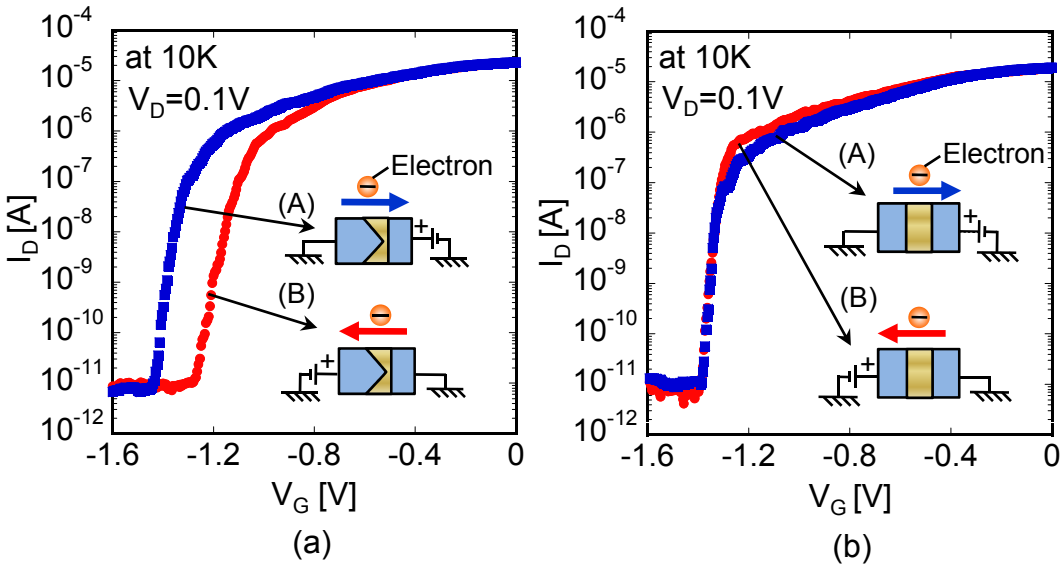


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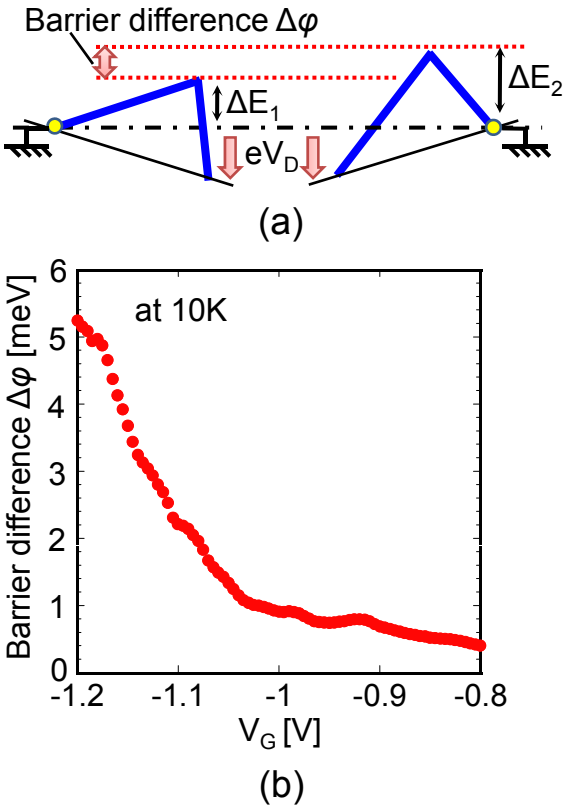


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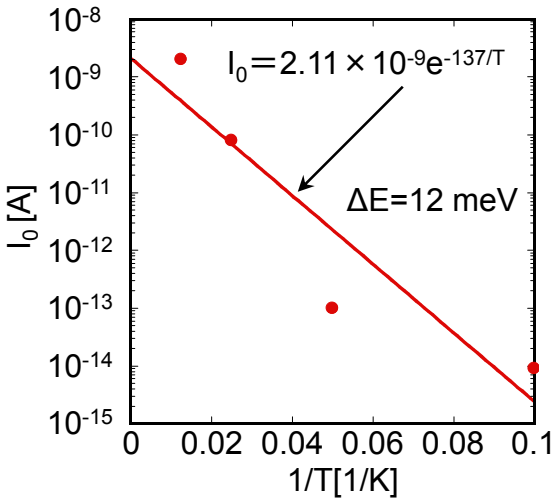


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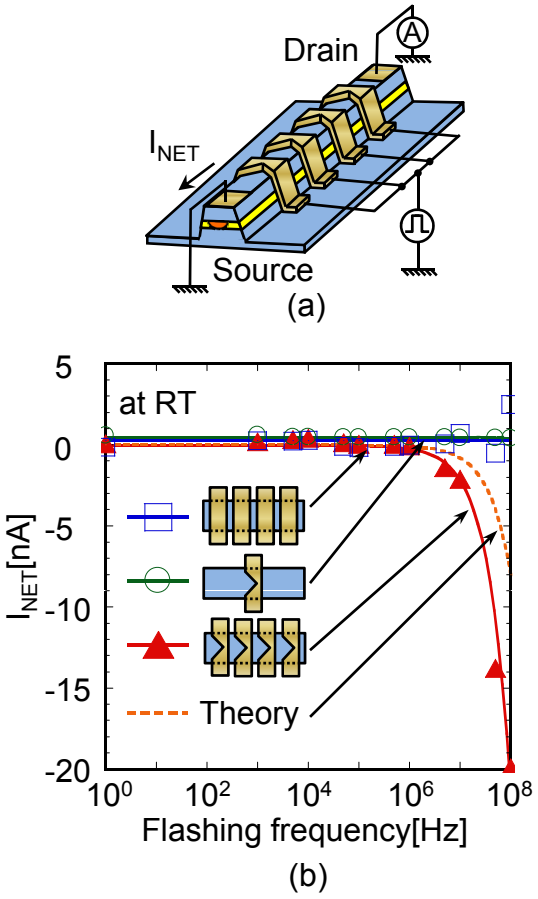


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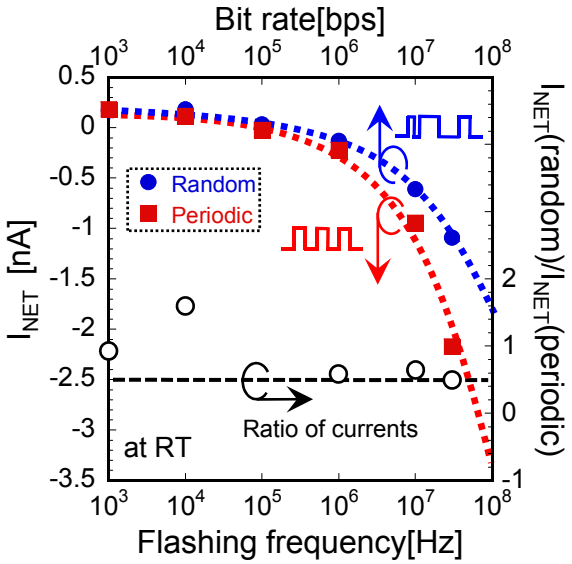


Fig. 9 Takayuki Tanaka et al.