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State of the art on gate insulation and surface passivation for GaN-based power HEMTs

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ABSTRACT

In this article, we review recent progress on AlGaN/GaN and InAlN/GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) using Al-based oxides, nitride dielectrics, SiO_2 and high-k dielectrics. Although GaN MIS-HEMTs have been suffering from the instability of threshold voltage (V_{TH}), recent interface technologies using in-situ SiN_x and surface oxidation of (Al)GaN achieved excellent DC and dynamic performances of GaN MIS-HEMTs with stable V_{TH}. Furthermore, a new design of the gate dielectric such as a nano-laminate structure has been applied to GaN HEMTs. GaN-based MIS-HEMTs sometimes showed sudden current saturation at forward gate bias, and we discuss effects of electronic states at insulator-semiconductor interfaces on current linearity of GaN MIS-HEMTs. Finally, we present effective surface passivation schemes in conjunction with field-plate structures and emerging device structures utilizing multi nanochannels under the gate region.

1. Introduction

For GaN-based high electron mobility transistors (HEMTs), great efforts have been devoted to improve device performance and operation stability/reliability. In particular, AlGaN/GaN HEMTs have been making steady progress in high-frequency and high-power performances [1–7]. By using GaN HEMTs with breakdown voltages up to 600 V, highly efficient and high-frequency switching systems with compact size have been demonstrated [5,7,8]. In addition, GaN HEMTs are well-suited for high power radio frequency (RF) applications owing to electron saturation velocity as high as 2×10^7 cm/s and high 2D electron gas (2DEG) density of over 1×10^{13} cm^{-2}, originating from spontaneous and piezoelectric polarization fields as well as from large conduction band offset. By downscaling of the gate length to sub-100 nm regime in conjunction with state-of-the-art technologies, Shinohara and co-workers [1,9] have recently achieved ultrahigh-speed operation with record-high maximum current gain cutoff frequency f_T of 454 GHz with accompanying power gain cutoff frequency (f_{max}) of 444 GHz on a 20 nm gate HEMT. These are fairly desirable for the 5th generation (5G) communication system where the W-band (75–110 GHz) and the E-band (60–90 GHz) frequency ranges will be used for wireless backhaul of mobile communications.

For reduced power consumption as well as failure protection, normally-off operation is highly preferred, in particular for power switching devices. Obviously, normally-off devices require a positive gate voltage to be turned on, which leads to exceedingly high leakage current levels in Schottky-gate (SG) devices. Thus, a metal-insulator-semiconductor (MIS) gate is absolutely necessary for normally-off power switching transistors. In RF application, the 5G wireless system also requires higher efficiency and linearity for RF power transistors. Power amplifiers using SG GaN HEMTs suffer from reduced gain and efficiency with increasing input RF power due to significant gate leakage currents caused by a large input swing that may drive the devices deep into the forward bias regime [10]. Such high leakage currents seriously affect the operation stability and large signal linearity of power amplifiers. Moreover, a suitable surface passivation scheme is absolutely necessary for stable and reliable operation of power devices.

A metal-insulator-semiconductor (MIS) structure is very effective to overcome such problems related to SG structure. For example, a gate-stack technology from the perspectives of interface engineering, barrier-layer engineering and gate dielectric technique have been employed to normally-off GaN HEMTs for power switching devices [5,7,11,12]. As for RF devices, Kanamura et al. [10] demonstrated that gate leakage current was sufficiently controlled in the AlGaN/GaN MIS-HEMT even under high input power operation. Thus, a MIS-HEMT can accommodate a wider range of input signal sweep, resulting in higher maximum output power. In addition, the MIS structure will be necessary for InAlN/GaN HEMTs. It is known that GaN HEMTs using an

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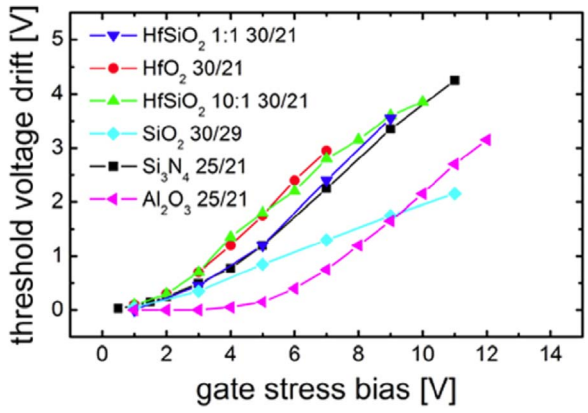

Fig. 1. Comparison of gate-stress induced V_{TH} drift of AlGaN/GaN MIS-HEMTs for different dielectrics with different insulator and AlGaN thicknesses. (Reprinted from [20], copyright 2014 with permission from AIP Publishing.).

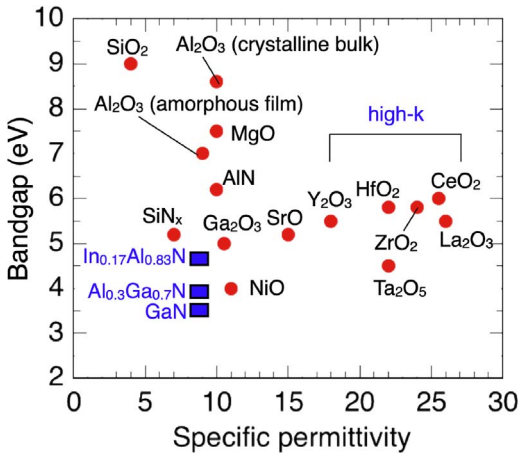

Fig. 2. Relationship between bandgap and permittivity for major insulators and GaN-based materials.

InAlN electron-supplying layer are promising because of their high spontaneous polarization and high band offset at the conduction band, for enhancing 2DEG density [13]. In fact, Makiyama et al. [14] demonstrated an output power density of 3 W/mm at 96 GHz in the GaN HEMT using quaternary InAlGaN barrier layers. However, large gate leakage current in InAlN/GaN HEMTs often limits their operations. Appropriately, the MIS structure is well-suited for addressing the leakage current issue and therefore promoting the performance of InAlN/GaN HEMTs.

Since the semiconductor/insulator interfacial quality significantly affects the transistor performance, a chemically stable MIS structure with low interface state densities should be developed for practical device application [11,15,16]. In this regard, various kinds of insulators have been applied to achieve excellent performance of GaN MIS HEMTs. However, several problems remain unsolved [16]. The instability of threshold voltage (V_{TH}) is one of the most serious problems. Some groups reported that the V_{TH} shift appears at different gate bias conditions in MIS-HEMTs [17–20], as shown in Fig. 1. The charging state of the interface traps varies with the gate bias, and excess interface charges particularly at deeper electronic states are responsible for such V_{TH} fluctuation. Another problem is an unexpected degradation of current linearity in GaN-based MIS HEMTs. Although a dynamic range of input signal sweeping is one of advantages in MIS HEMTs, some groups reported on the sudden current saturation at forward bias [21,22]. It is likely that a high density of electronic states at the insulator/barrier interface, in particular near the conduction band edge, screens the gate electric field and causes a limited control of surface potential of the barrier layer. This prevents further increase in the 2DEG density, leading to pronounced current saturation at forward gate bias. Such degradation of current linearity can be responsible for gain loss and degradation of large signal linearity in power amplifiers.

Accordingly, this paper reviews state of the art on gate insulation and surface passivation for GaN-based power HEMTs. First, we present the recent progress of GaN MIS-HEMTs using Al-based oxides, nitride dielectrics, SiO_2 and high-k dielectrics. Next, we discuss effects of electronic states at insulator-semiconductor interfaces on current linearity of GaN MIS-HEMTs. Finally, we present surface passivation schemes in conjunction with field-plate structures and emerging device structures utilizing multi nanochannels under the gate region.

2. AlGaN/GaN and InAlN/GaN MIS-HEMTs

For designing of a MIS gate or a surface passivation structure applicable to GaN-based HEMTs, it is important to consider bandgap, permittivity, breakdown field and chemical stability of insulators. In addition, insulator/semiconductor band offsets and interface state densities are responsible for performance and stability of MIS-HEMTs, as mentioned above. Fig. 2 shows a relationship between bandgap and permittivity for major insulators, clearly indicating the trade off between them. For a sufficient suppression of the gate leakage current even at forward bias, we need a large bandgap as well as large band offsets for a gate insulator. This is indispensable for a robust operation of power switching transistors applicable to power conversion systems. On the other hand, high-k oxides such as HfO_2, ZrO_2, CeO_2, La_2O_3, etc. are desirable for fabrication of a MIS-HEMT with high transconductance (g_m), leading to high f_T and f_{max} in RF amplifier devices. In addition, the barrier thickness including AlGaN (InAlN) and insulator layers is directly related to the g_m characteristics in MIS-HEMTs, indicating that the thinner barrier thickness results in the higher g_m and the smaller gate bias swing up to the maximum drain current. Therefore, it is necessary to adopt a suitable gate insulator according to a type of device applications. In these circumstances, we review the recent progress of GaN MIS-HEMTs using Al-based oxides, nitride dielectrics, SiO_2 and high-k dielectrics.

2.1. AlGaN/GaN MOS-HEMTs using Al-based oxides

Al_2O_3 is very attractive for a gate insulator in power MIS devices because it possesses large bandgap, relatively high dielectric constant (~ 9), and high breakdown field (~ 10 MV/cm). Note that the bandgap of Al_2O_3 obtained experimentally from amorphous films ranges from 6.7 to 7.0 eV [23,24], which is lower than that of the bulk. The band offset of 1.8 eV at the conduction band was reported for the Al_2O_3/$Al_{0.25}Ga_{0.75}N$ interface [25]. Hashizume et al. [26,27] first demonstrated that an Al_2O_3 dielectric for both insulated gate and surface passivation schemes was effective in controlling current collapse in the $Al_{0.3}Ga_{0.7}N$/GaN HEMT. For Al_2O_3 formation on the AlGaN surface, they carried out molecular beam deposition of thin Al film and in-situ plasma oxidation of Al. In addition, a technological progress in the atomic layer deposition (ALD) has enabled us to apply a high-quality Al_2O_3 to gate and passivation structures in GaN transistors. Park et al. [28] and Ye et al. [29] reported excellent electrical characteristics, such as low gate leakage current, high drain current, high g_m and high channel mobility, in ALD-Al_2O_3-gate AlGaN/GaN HEMTs. Yatabe e al. [15,16] revealed from precise capacitance-voltage (C-V) analysis and photo-assisted C-V method that the ALD-Al_2O_3/AlGaN interface showed relatively low state densities less than $1 \times 10^{12}\,cm^{-2}eV^{-1}$.

However, Al_2O_3/AlGaN/GaN HEMTs often suffer from fluctuation of threshold voltage (V_{TH}) under different bias conditions. Lu et al. [17] reported from the pulsed V_G-I_D measurement that higher gate-bias stress caused the larger V_{TH} shift toward the forward bias direction in their Al_2O_3-gate AlGaN/GaN HEMTs. Tapajna et al. [18] discussed the effect of interface states on the V_{TH} shift in Al_2O_3-gate AlGaN/GaN

HEMTs. Many papers pointed out that high densities of electronic states still exist at the insulators/AlGaN interfaces. The charging state of the interface traps varies with the gate bias (surface potential), and deeper electronic states with long time constants for electron emission contribute to a slow V_{TH} fluctuation. Fixed charges in insulator films [30,31] and border traps in insulator films near the insulators/AlGaN interfaces [32,33] are also involved in the V_{TH} shift mechanism. To control the V_{TH}, Yang et al. [12] applied a monolayer AlN as an interfacial layer to AlGaN/GaN MOS HEMTs with an ALD-Al_2O_3 gate, and demonstrated small frequency dispersion in C-V characteristics of Al_2O_3/AlN/AlGaN/GaN MOS diodes and a small V_{TH} shift in AlGaN/GaN MOS HEMTs. Van Hove et al. [34] reported that AlGaN/GaN HEMTs with stable V_{TH} and weak current collapse were achieved using an in-situ MOCVD-SiN_x/ALD-Al_2O_3 bilayer gates.

A limited process temperature should be considered for the use of Al_2O_3 as a gate dielectric. Hori et al. [35] observed that the as-deposited ALD-Al_2O_3 layer has an amorphous-phase structure and that the Al_2O_3/GaN interface is uniformly flat. However, annealing at 800 °C, a typical temperature for the formation of ohmic electrodes in AlGaN/GaN HEMTs, generated a large number of microcrystallized regions in the Al_2O_3 layer, causing a marked increase in the leakage current of the Al_2O_3/GaN structure, as shown Fig. 3. Toyoda et al. [36] also reported that annealing procedures at 800 °C resulted in the phase transformation of Al_2O_3 films from amorphous to crystalline. To overcome this issue, Asahara et al. [37] proposed an application of aluminum oxynitride (AlON) to a gate dielectric in AlGaN/GaN MOS-HEMTs. They revealed from TEM observation that an atomically abrupt interface between the amorphous AlON and the AlGaN layers remained even after post-deposition annealing at 800 °C. In addition, they observed excellent C-V curves with a typical two-step behavior and negligible frequency dispersion, as shown Fig. 4, indicating low densities of electronic states at the AlON/AlGaN interface. To achieve the larger bandgap and the higher process temperature of a gate oxide than those of Al_2O_3, Kikuta et al. [38] very recently developed the deposition of Al_2O_3/SiO_2 nanolaminate, equivalently corresponding to $Al_{1-x}Si_xO_y$, on GaN using ALD. The Al_2O_3/SiO_2 composition ratio, the relative permittivity and the total thickness of the nanolaminate oxide were precisely controlled by the ALD cycle numbers for the Al_2O_3 and SiO_2 deposition processes, respectively. As compared to Al_2O_3, they reported the higher breakdown field and the better oxide reliability for Al_2O_3/SiO_2 nanolaminate with the equivalent SiO_2 composition from 0.21 to 0.69. These results indicate that Al_2O_3/SiO_2 nanolaminate is a promising gate oxide applicable to GaN-based MOS-HEMTs.

From the time-dependent dielectric breakdown (TDDB) measurement, Kachi [4] pointed out that the TDDB lifetime of ALD Al_2O_3 at the electric field of 3 MV cm^{-1} is more than 20 years at RT, and hence it is applicable to power devices for automotive applications. At high temperatures, however, the TDDB lifetime significantly decreased.

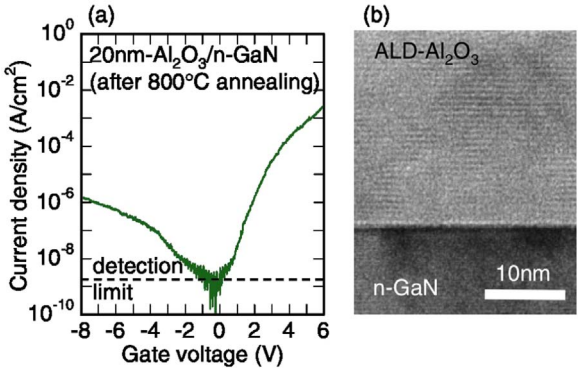

Fig. 3. (a) I–V characteristics and (b) TEM image of the ALD-Al_2O_3/n-GaN structure after annealing at 800 °C in N_2. (Reprinted with permission from [35], copyright 2010 by the Japan Society of Applied Physics.).

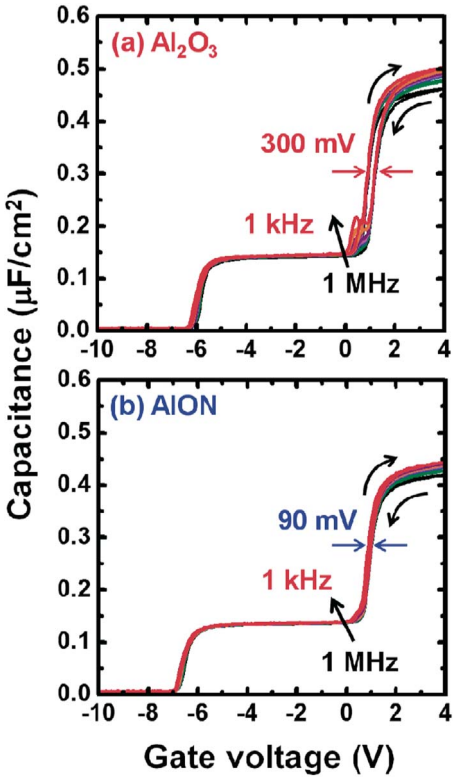

Fig. 4. C–V curves of AlGaN/GaN MOS capacitors with (a) Al_2O_3 and (b) AlON gate dielectrics. Multifrequency measurements ranging from 1 kHz to 1 MHz were carried out at room temperature. (Reprinted with permission from [37], copyright 2016 by the Japan Society of Applied Physics.).

Meneghesso et al. [39] also measured the TDDB characteristics of AlGaN/GaN MOS HEMTs with Al_2O_3. Since time to failure of devices indicated a Weibull distribution with slopes larger than 1.0, they demonstrated high robustness for ALD Al_2O_3.

2.2. AlGaN/GaN MIS-HEMTs using nitride dielectrics

SiN_x gate was also applied to AlGaN/GaN MIS HEMTs [40–42], from which significant reduction of current collapse was achieved. However, relatively high gate leakage current, in particular at forward bias, was observed in SiN_x-gate HEMTs [26,41,42], due to the small conduction band offset (ΔE_C) between SiN_x and (Al)GaN [26]. The in-situ deposition of SiN_x by MOCVD is a promising process in terms of interface control, because the AlGaN surface is never subjected to air, hence passivating dangling bonds at the AlGaN surface without oxidation and contamination. Derluyn et al. [43] reported excellent I-V characteristics of AlGaN/GaN MIS-HEMTs using an in-situ SiN_x gate layer with a thickness of 3.5 nm. The in-situ process realized an oxide-free SiN_x/AlGaN interface [44]. A structural analysis using the high-resolution transmission electron microscopy (HR-TEM) showed that the in-situ SiN_x has a single crystalline structure [45]. Van Hove et al. [34] demonstrated that an in-situ SiN_x/Al_2O_3 bilayer gate achieved an AlGaN/GaN MIS-HEMT with a stable threshold voltage and a low current collapse.

Jiang et al. [46] very recently performed systematic characterization of AlGaN/GaN MIS diodes and MIS-HEMTs using in-situ SiN_x with thicknesses from 7 to 28 nm. For all MIS diodes, they observed good C-V characteristics with a typical two-step behavior, and successfully determined the value of 7.0 for the relative permittivity of in-situ SiN_x. They also demonstrated good DC transfer characteristics, small subthreshold slope of 75 mV/dec and the V_{TH} stability under bias-stress and high-temperature conditions in the MIS-HEMT using SiN_x with a thickness of 14 nm. In conjunction with the PECVD SiN_x to form a

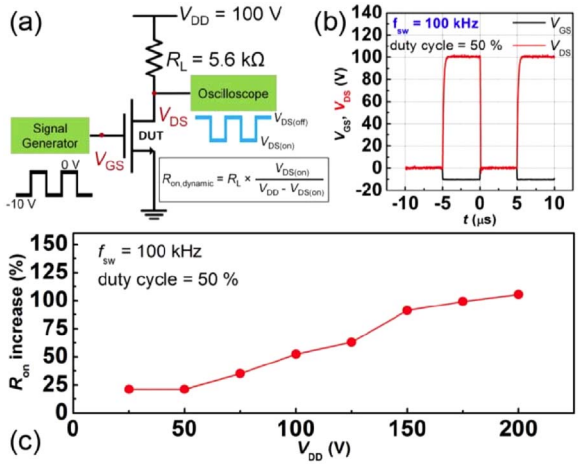

Fig. 5. (a) Schematic of resistive load hard switching test for AlGaN/GaN MIS-HEMTs using in-situ SiN_x. (b) Switching waveforms of input gate signal and output drain voltage. The switching frequency is 100 kHz and the duty cycle is 50%. (c) Percentage increase of the dynamic R_{ON} over the static R_{ON} versus V_{DD}. (Reprinted with permission from [46], copyright 2017 IEEE.).

bilayer passivation scheme, the MIS-HEMT effectively suppressed current collapse and showed an excellent dynamic performance with a low dynamic/static ratio of on-state resistance (R_{ON}), as shown in Fig. 5. Hua et al. [47] recently proposed a crystalline oxidation interlayer between a gate SiN_x and an etched GaN surface in a recessed gate AlGaN/GaN HEMT. The etched GaN surface was subjected to O_2 plasma treatment in an inductively coupled plasma (ICP) system with a low ICP/RF power of 5/10 W, and subsequently annealed at 780 °C for 20 min in NH_3 atmosphere. Form XPS and TEM analyses, they concluded that crystalline GaN oxide with several monolayers was formed at the interface between the GaN surface and SiN_x deposited by low-pressure CVD (LPCVD). The SiN_x-gate MIS-HEMT with a crystalline oxide interlayer showed small subthreshold slope of 82 mV/dec and excellent V_{TH} stability at temperatures up to 200 °C, as shown in Fig. 6.

Hua et al. [48] carried out the TDDB measurement on AlGaN/GaN MIS HEMTs with SiN_x deposited by LPCVD. They reported that time to failure of devices showed the Weibull distribution with a slope of 2.4 and that the maximum forward bias for ten-year lifetime was extracted as 9.8 V at the failure level of 63%. Jauss et al. [49] also measured TDDB characteristics of AlGaN/GaN MIS HEMTs with the LPCVD SiN_x, including dependence of the dielectric breakdown on temperature, the process flow, the thickness of the dielectric (12–20 nm) and the area scaling. They observed Weibull distributions with slopes larger than 2 for time to failure of devices, resulting in a 20-years 100 ppm lifetime at 130 °C for the gate voltage of 9.4 V.

2.3. AlGaN/GaN MOS-HEMTs using SiO_2 and high-k dielectrics

Khan and co-workers [50] first applied SiO_2 to the AlGaN/GaN MOS-HEMT to control gate leakage current and to improve gate-voltage swing capability. Kambayashi et al. [51] reported over 100-A operation in AlGaN/GaN hybrid HEMT using the PECVD-SiO_2 gate with post-deposition annealing at 700 °C. In addition, the hybrid HEMT using the Al_2O_3/SiO_2 bilayer gate demonstrated a channel mobility of 192 cm^2/Vs [52]. Recently, Lee et al. [53] applied a high-quality PECVD SiO_2 to a recessed AlGaN/GaN MOS-HEMT. The optimal PECVD process for SiO_2 deposition realized the breakdown filed over 11 MV/cm and a wide forward gate voltage swing range with a low leakage current level. The PECVD SiO_2/AlGaN/GaN MOS-HEMT showed good transfer characteristics and a slight increase in dynamic on-state resistance under high drain voltage operation. Some groups have tried to deposit SiO_2 on GaN and AlGaN by ALD using 3-aminopropyltriethoxysilane [54] or tris (dimethyl-amino)silane [38,55,56] as Si sources. The bandgap and the breakdown field of ALD-SiO_2 were estimated to be 8.8–9.0 eV [54,57] and 9.9 MV/cm [38], respectively, similar to those of standard SiO_2 deposited by PECVD or thermally grown on Si. However, Kirkpatrick et al. [54] and Kikuta et al. [38] pointed out that relatively high leakage currents were observed at forward bias in the SiO_2/AlGaN/GaN MOS-HEMT and the SiO_2/GaN diode, indicating that further investigation on starting materials and process conditions is needed for ALD-SiO_2. Although SiO_2 film has a low permittivity (3.9), it remains attractive for MOS HEMT applications because of its large bandgap and chemical stability.

High-κ insulators are attractive for achieving high g_m in MIS transistors. Various kinds of high-k dielectrics (HfO_2, ZrO_2, Ta_2O_5 , La_2O_3, $LaLuO_3$, NiO, TiO_2, CeO_2, etc.) have been applied to AlGaN/GaN MOS-HEMTs [58–66]. As expected, high g_m values were observed in high-k-gate MOS-HEMTs. Yang et al. [60] demonstrated $LaLuO_3$-gate AlGaN/GaN HEMTs showing good electrical performance such as high g_m, low gate leakage, small V_{TH} fluctuation and small current collapse. However, high leakage currents were observed at forward bias for MOS HEMTs [59,63], probably due to insufficient bandgaps against AlGaN [16]. In addition, Deen et al. [59] and Hayashi et al. [67] reported severe V_{th} fluctuations from HEMTs with HfO_2-gate dielectric materials while Stoklas et al. [68] described similar instability issues in HEMTs with ZrO_2-gate dielectric materials. Therefore, further investigation is necessary to gain better understanding of high-κ insulators/(Al)GaN interfaces.

2.4. InAlN/GaN MIS-HEMTs

It is known that GaN HEMTs using an InAlN electron-supplying layer are promising [13] because of their high spontaneous polarization

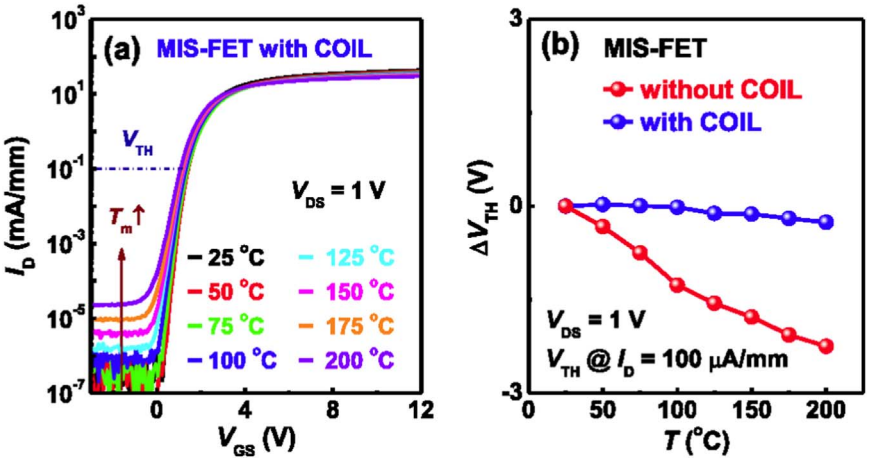

Fig. 6. (a) Temperature-dependent transfer characteristics of the recessed gate AlGaN/GaN MIS-HEMT with LPCVD-SiN_x gate and crystalline oxidation interlayer (COIL). (b) V_{TH} temperature dependence of MIS-HEMTs with and without COIL. (Reprinted with permission from [47], copyright 2017 IEEE.).

[69] and high band offset at the conduction band [70], for enhancing 2DEG density. Kotani et al. [71] investigated leakage characteristics of Ni/Au Schottky diodes on InAlN/GaN structures grown on GaN and sapphire substrates. They achieved a low dislocation density of $1.8 \times 10^4\,cm^{-2}$ for the HEMT grown on a GaN substrate while $1.2 \times 10^9\,cm^{-2}$ for the HEMT grown on a sapphire substrate. They observed a reduction of leakage current at low gate bias for the Schottky diode on a GaN substrate. However, no significant difference was observed at high reverse bias between two Schottky diodes. They pointed out that remarkable leakage currents in the high reverse bias region originate from an intrinsic field emission due to the large internal electric field in the InAlN barrier layer [72].

Pozzovivo et al. [73] applied the Al_2O_3 gate to the InAlN/GaN HEMT. A 12-nm amorphous Al_2O_3 layer was deposited by MOCVD. As compared to the Schottky-gate HEMT, they reported significant reduction of gate leakage current, increase in g_m and increase in a maximal drain current for the MOS-HEMTs. Hu et al. [74] and Freedsman et al. [75] fabricated MOS-HEMTs with an ALD Al_2O_3 as a gate dielectric. They showed good DC I-V characteristics, high current on/off ratios and negligible current collapse [74]. Very recently, Ozaki et al. [76] reported effects of air annealing on DC characteristics of ALD-Al_2O_3/InAlN/GaN MOS HEMTs. They observed the improvement of current linearity, subthreshold slope and V_{TH} stability in the MOS-HEMT after air annealing at 300 °C, indicating effective reduction of interface states at Al_2O_3/InAlN interface. In addition, the reduction of oxygen-vacancy-related defects in Al_2O_3 and the increase in mass density of Al_2O_3 were revealed after air annealing, from cathodoluminescence (CL) and Rutherford backscattering spectrometry (RBS), respectively. The latter led to the enhancement of tensile stress of Al_2O_3 (piezoelectric polarization), resulting in the increase in the 2DEG density.

Lachab et al. [77] demonstrated that the thickness of the AlInN barrier could be reduced below 5 nm without degradation of device performance in SiO_2/InAlN/GaN MOS-HEMTs. However, their C-V and pulsed I-V characterization indicated high densities of electronic states at the SiO_2/InAlN interface. Kotani and co-workers [78] recently investigated in-situ AlN cap layers (3–7 nm) grown on InAlN/GaN structures. They found that a low-temperature (LT) growth (430 °C) achieved an amorphous AlN layer, resulting in a significant reduction of the Schottky-gate leakage current by 4–5 orders of magnitudes compared to the InAlN/GaN structure without the AlN cap layer. From structural analyses (TEM and XRD) and one-dimensional simulation based on Poisson and Schrödinger equations, they explained that the reduced polarization field in the LT-AlN cap modified a band profile, as shown in Fig. 7, suppressing the penetration of 2DEG into the InAlN barrier layer. Further investigation will improve operation performance and stability of InAlN/GaN HEMTs with a suitable insulated gate structure.

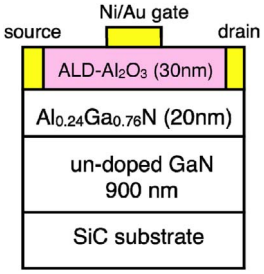

Fig. 8. Schematic illustration of Al_2O_3-gate MOS-HEMTs without and with a bias annealing in air at 300 °C.

3. Current linearity in GaN-based MIS-HEMTs

Although a dynamic range of input signal sweeping is one of advantages in MIS HEMTs, some groups reported on sudden current saturation at forward gate bias [21,22]. It is likely that a high density of electronic states at the insulator/barrier interface, in particular near the conduction band edge, screens the gate electric field and causes a limited control of surface potential of the barrier layer. To investigate current linearity and operation stability of AlGaN/GaN MOS-HEMTs, we have fabricated and characterized the Al_2O_3-gate MOS-HEMTs without and with a bias annealing in air at 300 °C.

The cross-section of MOS-HEMT device is shown in Fig. 8. The 2DEG density and mobility of the AlGaN/GaN heterostructure were $9.0 \times 10^{12}\,cm^{-2}$ and $1740\,cm^2/Vs$, respectively. An Al_2O_3 layer with a nominal thickness of 30 nm was then deposited on the AlGaN surface using an ALD system (SUGA-SAL1500) at 300 °C. In the deposition process, water vapor and trimethylaluminum (TMA) were introduced into a reactor in alternate pulse forms. The gate length, gate width, and gate-drain distance were 5, 100, and 10 μm, respectively. After the fabrication, the devices were subjected to a bias annealing in air for 3 h at 300 °C under a reverse voltage. Kaneki et al. [79] recently reported that the reverse-bias annealing reduces the state densities at the Al_2O_3/GaN interface, probably due to the relaxation of dangling bonds and/or reduction of point defects on the GaN surface (Al_2O_3/GaN interface). They also demonstrated small shifts of flat-band voltage and stable C-V behavior at 200 °C for bias annealed Al_2O_3/GaN diode. We expected similar effects of bias annealing on AlGaN/GaN MOS HEMTs.

The transfer characteristics of MOS-HEMTs without and with the bias annealing are shown in Fig. 9**(a)**. For comparison, their transfer curves as a function of gate overdrive voltage (V_G–V_{TH}) are replotted in Fig. 9**(b)**. The bias-annealing process effectively improved the current linearity, particularly in forward bias, resulting in a broader g_m plateau and increased maximum drain current. This effect is important for the MOS-HEMT in terms of the input dynamic range at forward bias.

To investigate interface properties of the Al_2O_3/AlGaN gate structures, C–V characterization was performed on MOS diodes fabricated on

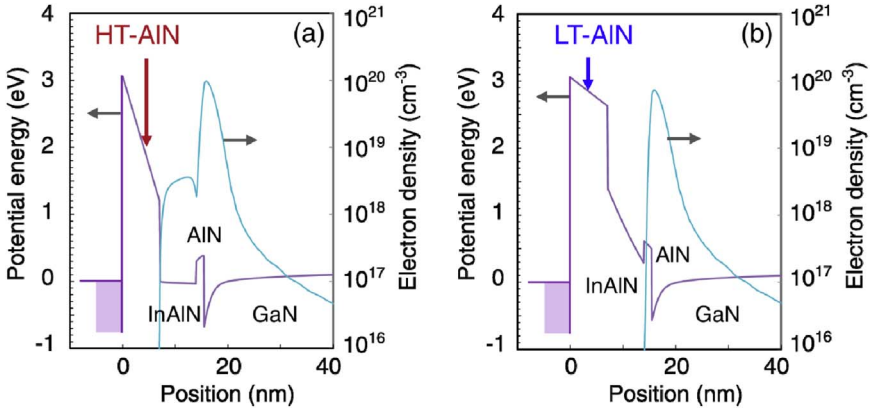

Fig. 7. Calculated band profiles and electron distributions for high-temperature (HT) and low-temperature (LT) AlN capped InAlN/AlN/GaN HEMT structures. (Reprinted from [78], copyright 2017 with permission from AIP Publishing.).

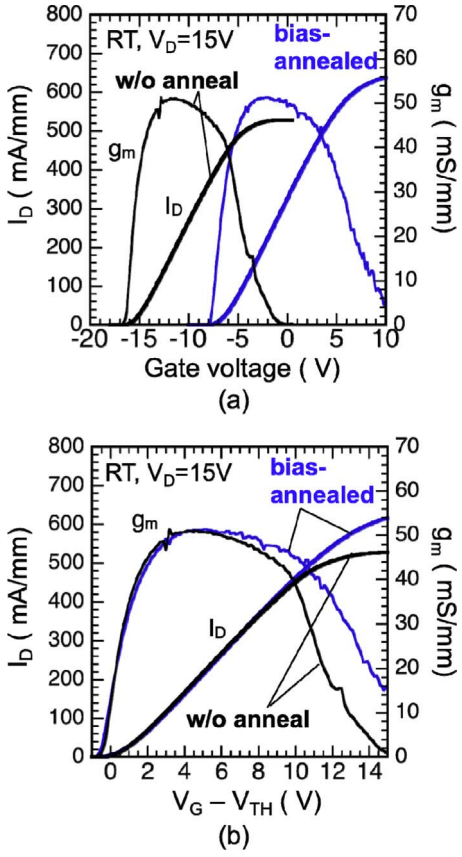

Fig. 9. (a) Transfer characteristics of Al_2O_3/AlGaN/GaN MOS HEMTs without and with the bias annealing process. (b) The data were replotted with respect to V_G-V_{TH}.

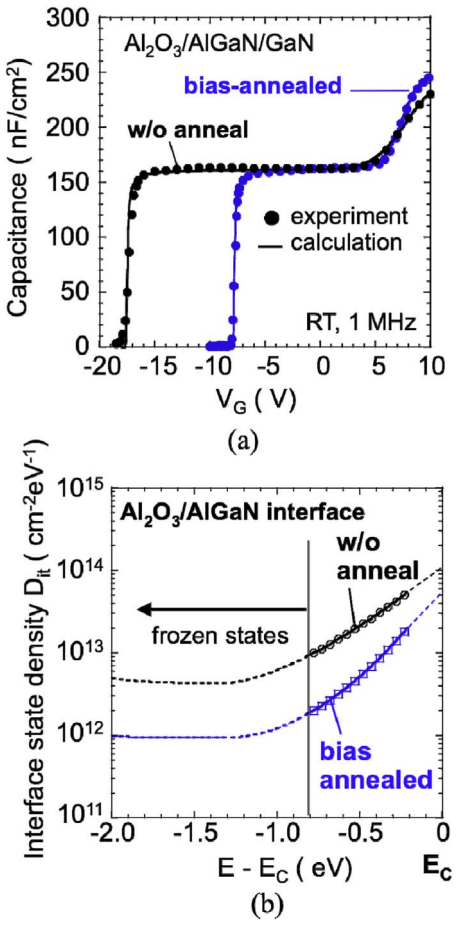

Fig. 10. (a) C-V characteristics of the Al_2O_3/AlGaN/GaN MOS diodes. The solid line indicates calculated curves. (b) Interface state density distributions (D_{it}) determined by the fitting of C-V curves.

the same AlGaN/GaN heterostructures. A circular gate with a diameter of 200 μm was prepared for the MOS diodes. C–V curves obtained using a signal frequency of 1 MHz at RT are shown in Fig. 10**(a)**. Both diodes without and with the bias annealing showed the two-step behavior typically observed in HEMT MOS structures [15,16]. To evaluate the effects of interface states on the C-V characteristics, one-dimensional simulation including self-consistent Poisson-Schrödinger calculations was carried out for the Al_2O_3/AlGaN/GaN structure, taking into account a state density distribution [D_{it} (E)] consisting of acceptor- and donor-like states separated by the charge neutrality level E_{CNL} [80–82]. Along the insulator-semiconductor interface, the crystalline periodicity of the semiconductor is terminated. In addition, disorder in atomic-bond arrangement can be induced at the semiconductor surface. In this case, the separation of conduction and valence bands becomes insufficient, resulting in the penetration of bonding and anti-bonding states into the forbidden band (bandgap) from valence and conduction bands, respectively [83,84]. Namely, a negative charge appears in the conduction band if a state is occupied by an electron (acceptor-like character), while valence band state is positively charged when unoccupied (donor-like character). This model is often used as a density distribution of interface states [85–87]. In addition, we can estimate electron emission time constant τ from interface states to the conduction band using Shockley-Read-Hall (SRH) statistics:

$$\tau = \frac{1}{v_{TH}\sigma_{TH}N_C} exp\left(\frac{E_T}{k_B T}\right) \quad (1)$$

where v_{TH}, σ_{TH}, N_C and E_T are electron thermal velocity, capture cross section of interface states, density of state at the conduction band, and interface state energy, respectively.

The calculated C–V curves are shown by solid lines in Fig. 10**(a)**. Using the D_{it} distributions shown in Fig. 10**(b)**, the calculation well reproduced the experimental C-V data. According to Eq. (1), time constants of electron emission from interface states near midgap or deeper are too long at RT that electrons once captured at such deep interface states remain trapped even when large negative bias is applied to the gate electrode. This makes the interface states act as “frozen” charges. At RT, it is estimated that interface states at energies below E_C – 0.8 eV are “frozen states”. Thus only the states in the energy range indicated by symbols in Fig. 10**(b)** can change their charge state accordingly with the gate voltage sweep at RT. In addition, there is a possibility that interface states at energies close to the conduction band edge can respond to the measurement AC signal (1 MHz), thereby making accurate estimate of capacitance difficult. Therefore, state densities at the energies above E_C – 0.2 eV were not taken into account in the present C-V analysis.

As shown in Fig. 10**(b)**, the bias annealing process effectively decreased the state densities, leading to the steeper C-V slope in forward bias shown in Fig. 10**(a)**. The calculated V_{TH} corresponding to the first step in the C-V curve was − 7.5 V, very close to that of the MOS-HEMT subjected to bias annealing. On the other hand, the sample without the annealing showed a V_{FB} shift toward the negative bias direction, probably due to excess positive charges arising from donor-type interface states and/or defect levels in the bulk Al_2O_3. A possible candidate for a defect level in Al_2O_3 is an oxygen-vacancy related defect [88,89]. The bias- annealing process decreased such levels, resulting in the V_{FB} recovery toward the expected value. To gain a better insight into the relationship between interface states and gate controllability of the MOS-HEMT, we calculated the 2DEG density as a function of gate overdrive, taking into account D_{it} distributions obtained from the C-V analysis (Fig. 10(b)). For the 2DEG density calculation, we used the

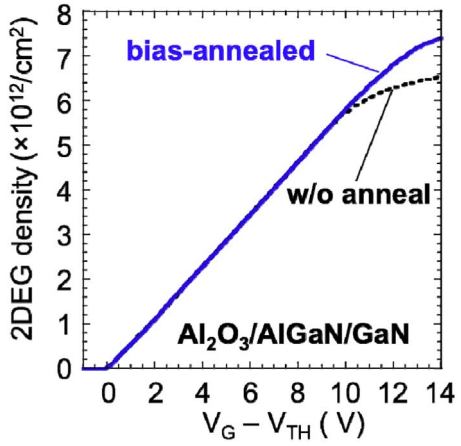

Fig. 11. Calculated 2DEG densities as a function of V_G-V_{TH} for the MOS-HEMTs without and with the bias annealing.

following equation [90,91]:

$$D_{2DEGi} = \frac{m_e k_B T}{\pi \hbar^2} ln\left[1 + exp\left(\frac{E_i - E_f}{k_B T}\right)\right] \quad (2)$$

where m_e is the effective electron mass, k_B is Boltzman's constant, T is the temperature, and i indicates the i_{th} discrete excited level at the AlGaN/GaN interface.

Fig. 11 shows the calculated 2DEG density as a function of gate overdrive for the MOS-HEMTs without and with the bias annealing. Beyond V_G–V_{TH} = 10 V, acceptor states shown in Fig. 10(b) are active accordingly with the gate voltage sweeping, and the ionized acceptor charges screen the gate electric field. Thus high-density states prevent the potential modulation (poor potential control) for the MOS-HEMT without the bias annealing. Thus the limited increase in the 2DEG density with V_G is clearly observed for the MOS-HEMT without the bias annealing. On the other hand, the MOS-HEMT with annealing shows relatively good control of 2DEG by V_G. The calculated results shown in Fig. 11 are similar to the measured I_D–V_G curves of MOS-HEMTs shown in Fig. 9(b), indicating that the effective reduction of interface states is responsible for the improved linearity in MOS-HEMT with bias annealing.

It should be mentioned that some papers reported poor current linearity in MIS-type Al- GaN/GaN HEMTs. To investigate current linearity behavior, we tried to plot the full width at half maxima (FWHM) of g_m–V_{GS} profiles as a function of the equivalent oxide thickness (EOT) including insulator and AlGaN barrier layers. Fig. 12 shows comparison of FWHM of g_m for AlGaN/GaN MIS-HMETs using SiO_2 [50,92,93], Al_2O_3 [29,94–97], SiN_x [21,22,46,98], HfO_2 [99,100], Ga_2O_3 [101], TiO_2 [66], and CeO_2 [64] dielectric materials. Our data are also included in Fig. 12. The insulator permittivity and the barrier thickness including AlGaN and insulator layers are directly related to the g_m characteristics in MIS-HEMTs, indicating that the thinner barrier thickness (EOT) results in the smaller gate bias swing up to the maximum drain current. Therefore, it is expected that the FWHM of g_m increases with EOT, and experimental data generally showed this tendency. However, there is a wide scattering of data, indicating that interface properties of insulator/AlGaN structures are not dependent on the insulator material used but on the bond disorder and/or surface defects on the AlGaN surface, probably related to fabrication process conditions including deposition methods [16,102–104]. The broken line is a guide to the eye for the better results reported [46,93,95,101]. Our device with the bias annealing showed high FWHM value, demonstrating excellent current linearity in our AlGaN/GaN MOS-HEMT.

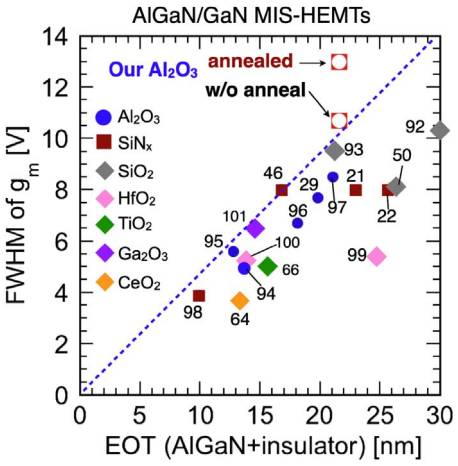

Fig. 12. Plots of FWHM in the g_m spectrum as a function of the equivalent oxide thickness (EOT) including insulator and AlGaN barrier layers for AlGaN/GaN MIS-HEMTs. The numbers indicate literatures cited.

4. Surface passivation and emerging device structures

A surface passivation scheme is absolutely necessary for improving long-term operation stability and controlling current collapse in GaN-based HEMTs. Green et al. [105] first reported noteworthy passivation effects on performance of AlGaN/GaN HEMTs. They applied the PECVD SiN_x passivation to an access region of the AlGaN/GaN HEMT, and demonstrated significant improvement of microwave output power owing to the mitigation of current collapse. It can be considered that nitrogen radicals generated during the PECVD process control the formation of surface defects related to nitrogen vacancy [102,103], leading to low-density electronic states at the SiN_x/AlGaN interface. Tsurumi et al. [106] demonstrated the fabrication of AlGaN/GaN HEMTs with a polycrystalline AlN surface passivation layer, taking advantage of the low thermal resistance of the AlN. They reported that the AlN-passivated HEMT showed a 30% higher drain current and a 66% lower R_{ON} compared with those of HEMTs with SiN surface passivation.

In GaN-based HEMTs, a field-plate (FP) structure [107–110] is very effective in decreasing the concentration of electric field at the gate edge on the drain side, hence enhancing device breakdown voltage. In addition, the reduction of electric field at the gate edge can also mitigate the electron injection from the metal gate into surface states at the AlGaN surface. Thus the FP structure is effective to control current collapse phenomena, thereby suppressing the increase in R_{ON} even under high drain voltage. Ando et al. [108] demonstrated that the gate FP significantly reduced current collapse, leading to high-efficiency RF power performance of AlGaN/GaN HEMTs under high voltage operation. Saito et al. [110] reported that the dual-FP structure, a combination of gate FP and source FP, was effective in suppressing the R_{ON} increase due to better uniform distribution of electric field than the single gate FP.

Recently various types of FPs have been applied to GaN-based HEMTs. Dora et al. [111] and Pei at al. [112] developed a “slant” FP, which is angled with respect to the semiconductor surface, on AlGaN/GaN HEMTs by controlling an etching process of SiN_x for FP. They achieved a kilovolt breakdown voltage and an excellent millimeter-wave power density with a high efficiency at 30 GHz. By controlling the deposition condition of SiCN in PECVD process, Kobayashi et al. [113] successfully fabricated slant FPs on AlGaN/GaN HEMTs. They reported that HEMTs with the SiCN slant FP exhibited 66% higher off-state breakdown voltage (BV_{OFF}) and a $f_T \times BV_{OFF}$ value four times larger than the corresponding values for HEMTs with conventional field plates. Wong et al. [114] very recently reported an excellent SiN_x slant-FP on AlGaN/GaN HEMTs by using the surface tension property of

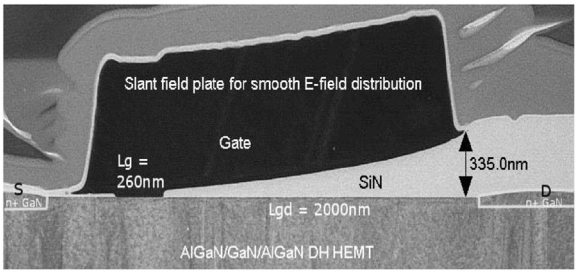

Fig. 13. TEM cross-section of the AlGaN/GaN HEMT using a SiN_x slant-FP with slope of 6° at the drain-side gate corner. (Reprinted with permission from [114], copyright 2017 IEEE.).

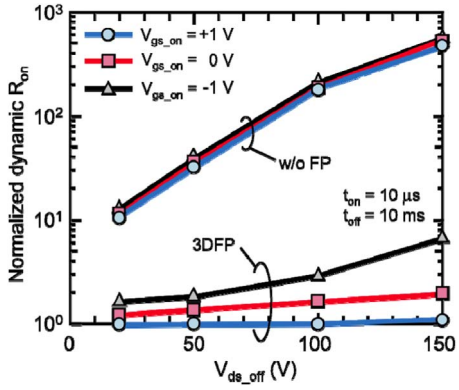

Fig. 14. Normalized dynamic R_{ON} as a function of off-state drain bias voltage (V_{ds_off}) of reference (without FP) and 3D-FP AlGaN/GaN HEMTs with varying on-state gate voltage (V_{gs_on}). (Reprinted with permission from [115], copyright 2016 by the Japan Society of Applied Physics.).

hydrogen silsesquioxane (HSQ) on a pre-patterned PECVD SiN_x dielectric and specially tuned dry-etching process for SiN_x, as shown in Fig. 13. The HEMTs with an optimized slant FP demonstrated a low dynamic R_{ON} as well as good high-frequency performance with f_T/f_{MAX} = 41/100 GHz. Kuzuhara and co-workers [115] have proposed and developed a unique FP structure, 3-D FP or a multi-groove FP. In AlGaN/GaN HEMTs with such 3-D FPs, they observed a very limited increase in dynamic R_{ON}, almost collapse-free operation even under high drain voltage, as shown in Fig. 14. They explained that the side-wall structures in the FP area also induced the lateral gate control of field, resulting in the enhanced emission of electrons trapped at the AlGaN surface during the on-state operation.

To improve gate controllability of GaN HEMTs, new device structures including 3-D multi nanochannels have extensively been studied. Ohi and Hashizume [116,117] proposed and characterized multi-mesa-channel (MMC) AlGaN/GaN HEMTs, as schematically illustrated in Fig. 15. Through forming periodic trenches by dry etching, the HEMT has parallel mesa-shaped channels with 2DEG surrounded by the gate electrode, realizing the gate control with a combination of vertical and lateral field effects. The MMC HEMTs thus showed a positive threshold voltage shift and the better subthreshold slope compared with conventional planar transistors, leading to a better suppression of short-channel effects in devices with downscaled gate length. This feature was also observed in similar 3D nanochannel devices such as nanochannel array and tri-gate AlGaN/GaN HEMTs [118,119]. Ohi and Hashizume [117,120] also found a limited increase of R_{ON} in the MMC HEMT even after applying high drain bias stress. They proposed that the MMC HEMT is less susceptible to current collapse because of the higher resistance of each nanochannel compared with that of the drain access region.

Several groups reported unique characteristics for GaN HEMTs with 3D nanochannel structures. Lee et al. [121] and Jo et al. [122] reported

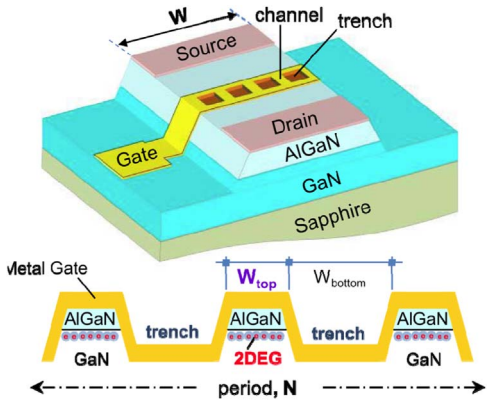

Fig. 15. Schematic illustration of the multi-mesa-channel (MMC) HEMT showing the periodic trench structure under the gate electrode. W_{top} is the width of the mesa channel. (Reprinted with permission from [117], copyright 2013 IEEE.).

excellent current linearity (g_m linearity) in tri-gate InAlN/GaN HEMTs and Al_2O_3/AlGaN/GaN MOS FinFETs. Lee et al. [123] pointed out that the suppression of the increase in source access resistance in the tri-gate HEMTs provides a flat g_m profile at high drain current. On the other hand, Jo et al. [122] demonstrated that side-wall channels in addition to the 2DEG channel could be formed at the Al_2O_3/side-wall GaN interfaces, contributing to an effective increase of drain current at forward bias. A high linearity of f_T, very attractive for millimeter-wave applications, was also observed in tri-gate InAlGaN/GaN HEMTs [121,123] and AlGaN/GaN FinFETs [124], as shown in Fig. 16**(a)** and **(b)**, respectively. In addition, Alsharef et al. [125] proposed from the device simulation that optimal design of tri-gate structure can minimize parasitic gate capacitance, leading to the improvement of RF performance, i.e., higher f_T and f_{MAX} for the tri-gate HEMT compared with its planar counterpart.

5. Summary

For practical transistor applications, low leakage current, effective current control with high linearity, stable threshold voltage, high g_m and wide dynamic range of input voltage are required for GaN-based MIS-HEMTs. In view of these points, various MIS-HEMTs using Al-based oxides, nitride dielectrics, SiO_2 and high-k dielectrics were reviewed and discussed.

AlGaN/GaN MIS-HEMTs using ALD-Al_2O_3 are promising for both RF and power switching applications. In particular, the interface control layers such as a monolayer AlN and an in-situ SiN_x were effective in achieving stable V_{TH}. To improve a process temperature range and interface properties, AlON and Al_2O_3/SiO_2 nanolaminate were successfully applied to AlGaN/GaN MIS-HEMTs. The MIS-HEMT using in-situ SiN_x in conjunction with the PECVD SiN_x effectively suppressed current collapse and showed an excellent dynamic performance with a low dynamic/static R_{ON} ratio. The LPCVD SiN_x gate with a crystalline oxidation interlayer also demonstrated excellent V_{TH} stability at temperatures up to 200 °C. Although SiO_2 film has a low permittivity (3.9), it remains attractive for MOS HEMT applications because of its large bandgap and chemical stability. Various types of high-k insulators have also been applied to the gate structures of GaN transistors. However, further investigation on chemical stability and interface properties of high-k/GaN structures is still needed. An insulated gate structure achieved significant suppression of gate leakage current and increase in a maximal drain current in InAlN/GaN HEMTs. In addition, it was proposed that the low-temperature grown AlN cap layer reduced polarization field and modified a band profile in the InAlN barrier layer. It will be promising for an interface control layer in combination with a stable gate dielectric such as Al_2O_3.

GaN-based MIS-HEMTs sometimes showed sudden current

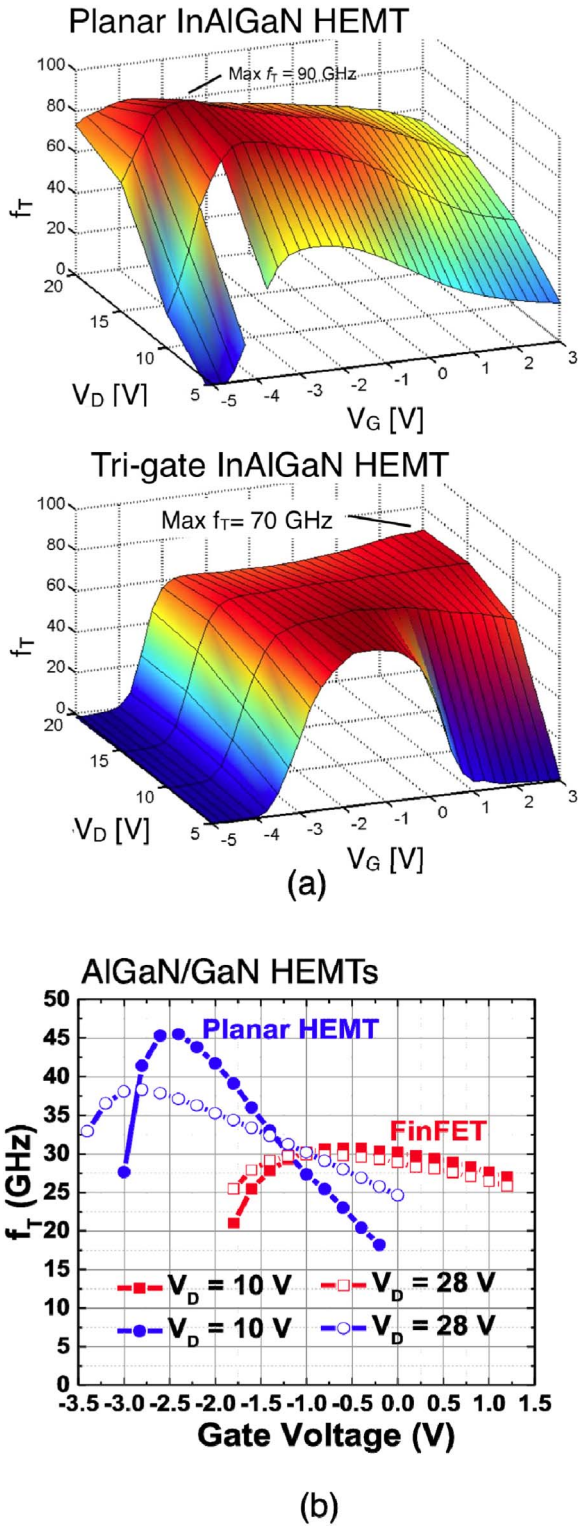

Fig. 16. (a) Intrinsic current-gain cut-off frequency (f_T) of the planar and Tri-gate InAlGaN HEMTs as a function of gate (V_G) and drain (V_D) bias. (b) f_T as a function of gate voltages at V_D = 10 V and 28 V for the planar and Fin AlGaN/GaN HEMTs. (Reprinted with permission from [123,124], copyright 2016 and 2017 IEEE.).

saturation at forward gate bias, and we investigated effects of electronic states at insulator-semiconductor interfaces on current linearity of GaN MIS-HEMTs. From precise C-V analysis and the Poisson-Schrödinger calculation for Al_2O_3/AlGaN/GaN HEMTs, it was found that the ionization of interface states screen the gate electric field and prevent the potential modulation of AlGaN at forward bias. This dominantly causes the limited increase in the 2DEG density with V_G, thereby resulting in current saturation at forward gate bias. The control of electronic states at insulator/semiconductor interfaces will improve current linearity in GaN-based MIS-HEMTs. A suitable surface passivation scheme in conjunction with a FP structure is very important for improving long-term operation stability and controlling current collapse in GaN-based HEMTs. Recent studies showed that slant FP and 3-D FP structures are effective in achieving higher off-state breakdown voltage and low dynamic R_{ON}. To improve gate controllability of GaN HEMTs, various types of device structures utilizing 3-D multi nanochannels have extensively been studied. The resulting structures can modulate 2DEG not only through the top but also through the sidewalls, leading to a better suppression of short-channel effects in devices with downscaled gate length. In addition, the multi-nanochannel structure is promising for achieving high linearity of g_m and f_T, very attractive for millimeter-wave applications.

GaN MIS-HEMT structures have been making steady progress in terms of interface control technology, gate dielectric and gate stack engineering, barrier layer engineering and surface passivation technology. We believe that this will push the frontier of nitride-based device technology and will achieve high performance and operation reliability in GaN-based MIS-HEMTs.

Acknowledgments

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