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Studies on Anisotropic Electrodeposition of Copper with Organic Additives

(有機添加剤を用いた銅の異方的電気化学析出に関する研究)

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Chapter 1

General Introduction

1.1 Copper deposition in industrial applications

1.1.1 Technological trends for electronic devices

Electronic devices such as mobile phones and computers must have their sizes reduced and their performance improved year by year as information-oriented society progresses. Therefore, high integration is required for the components of semiconductor devices like large-scale integration (LSI) chips and printed circuit boards (PCBs). The demand for interconnects with characteristics such as reduced size, shape control, and low resistance has thus been increasing year by year. LSI refers to integrated circuits containing devices such as transistors, resistors, and capacitors on a semiconductor chip. Most electronically controlled products such as computers, smartphones, home appliances, and vehicles use LSI technology. It should be possible to achieve high performance and low cost for these products through continued progress in downsizing and high integration of LSI devices. Figure 1.1 shows the increase in the number of transistors in an LSI circuit over time, a relationship known as Moore's law. According to Moore's law [1], the density of LSI circuits doubles about every 18 to 24 months. Until the year 2000, the LSI was reduced to about 70% in processing size, and about 50% in chip area in 3 years. LSI technology has thus kept up with Moore's Law for about 40 years, although the pace of advancement has slowed since 2000. As a result, the minimum pitch of a metal interconnect was 36 nm in 2018 [2].

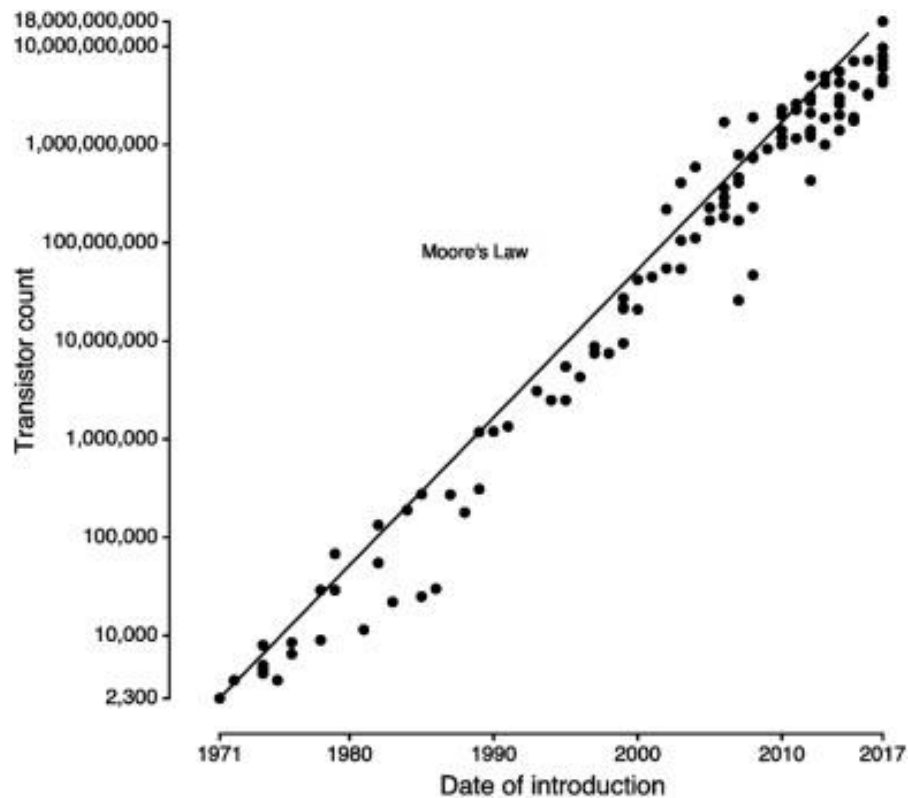


Fig. 1.1 Graphical representation of Moore's law [1].

Packaging technology for connecting highly integrated electronic devices is also important for developing high-performance products while downsizing LSI devices. Production of highly integrated packaging requires downsizing the wiring pitch of PCBs. Figure 1.2 shows examples of electronic components and interconnects. These components use various sizes of interconnects in LSI devices, capacitors, interposers, and PCBs.

1.1.2 Copper electrodeposition for electronic applications

Copper is used as a wiring material in many electronic components such as LSI devices and PCBs. Table 1.1 lists the main properties and price of each metal used in such wiring. Copper is widely used because its electrical conductivity is second only to that of silver, and because it is inexpensive compared to gold and silver, which have high electrical

conductivity, excellent thermal conductivity, and high corrosion resistance. Copper is also easy to process chemically and mechanically.

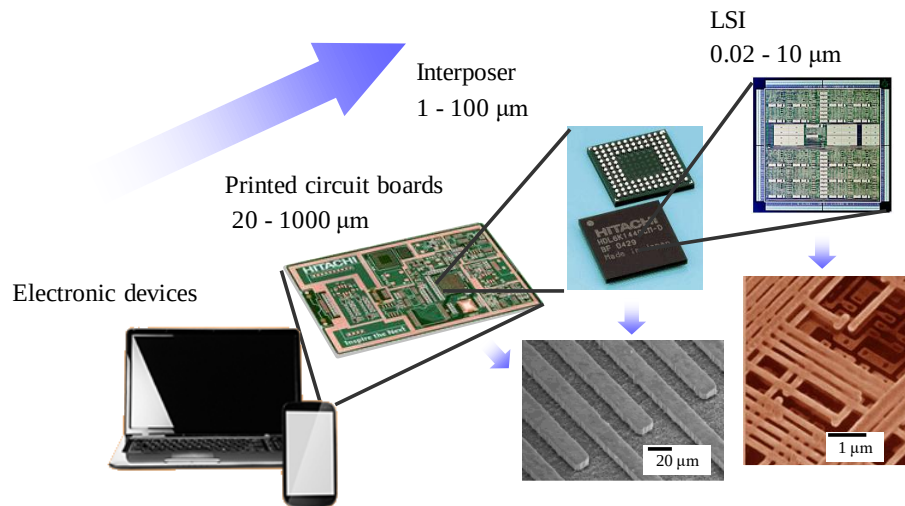


Fig. 1.2 Metal interconnects in various electronic devices.

Table 1.1 Properties and price of various metals for industrial applications.

Metal	Resistivity [$\times 10^{-8} \Omega \text{m}$]	Thermal conductivity @300K [$\text{Wm}^{-1}\text{K}^{-1}$]	Density [g/cm^3]	Price* [USD/g]
Copper	1.68	401	8.94	0.0063
Gold	2.44	318	19.32	43.2
Silver	1.59	429	10.49	0.51
Nickel	6.99	90.9	8.908	0.011
Aluminum	2.82	237	2.70	0.0019

* London Metal Exchange price on November 22, 2018

In the copper wiring technology used for manufacturing electronic components, electrochemical copper deposition plays an important role. Table 1.2 compares copper deposition methods. Electrochemical deposition is an essential technology for manufacturing processes requiring high throughput, because it has a high deposition rate at room temperature and atmospheric pressure. Furthermore, characteristics like the grain size,

conductivity, and surface roughness can be controlled by adjusting the plating conditions, such as the current density, stirring conditions, electrolyte composition, and use of additives in the electrolyte solution.

Table 1.2 Methods and typical conditions for copper deposition.

Method	Temperature [°C]	Pressure [Pa]	Deposition rate [$\mu\text{m}/\text{min}$]
Electrodeposition	20 - 80	Atmospheric pressure	0.1-10
Electroless deposition	40 - 90	Atmospheric pressure	0.01-0.1
Physical vapor deposition	20 - 500	10^{-8} - 10^{-3}	10^{-3} -0.1
Chemical vapor deposition	20 - 500	10^{-1} - 10^2	10^{-5} - 10^{-3}

Generally, the deposition and dissolution reactions in wet processes proceed isotropically. A photoresist mask is required for etching or plating to make wiring at a specific part of an LSI device or PCB. Figure 1.3 shows three process issues in making fine-pitch copper wiring. The process of masking with photoresist is costly and has a large environmental impact. Therefore, methods such as printing of fine metal particles have been studied as novel wiring techniques. It is difficult, however, to make copper wiring with a high aspect ratio by printing with metal inks because of their low viscosity. In contrast, a printing method using copper plating is a promising process for making thick copper wiring. As mentioned before, the plating process is isotropic, so it is difficult to maintain the spaces between lines. Hence, if it is possible to deposit copper anisotropically, it is expected that fine-pitch wiring can be made.

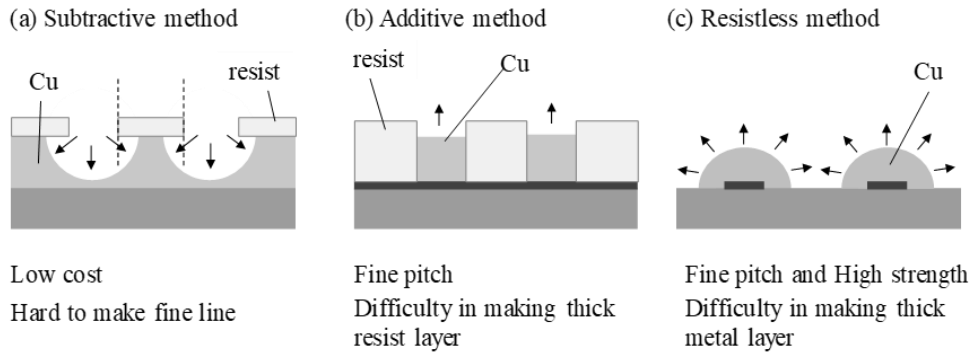


Fig. 1.3 Process issues for fine-pitch copper wiring.

1.1.3 LSI manufacturing process

The importance of the wiring techniques in LSI fabrication processes has increased with the shrinking sizes of LSI devices, because the signal delay of the interconnects cannot be ignored [3]. When the cross-sectional areas of interconnects decrease because of miniaturization, the performance of an LSI device is limited by the signal transmission delay due to the increase in electrical resistance. In addition, as the current density increases, breakage of interconnects due to electromigration occurs, which degrades their reliability. Electromigration is a phenomenon in which metal atoms move because of interactions with electrons flowing through interconnects. The number of moving atoms increases with the current, eventually leading to disconnection. To solve this problem, copper has been used for LSI interconnection, because it has higher electromigration resistance as compared to conventional interconnects using aluminum and its alloys [4].

Copper-based LSI interconnection technology using an electrochemical deposition process was developed by IBM in 1998 [4, 5]. Figure 1.4 shows overhead and cross-sectional scanning electron microscopy (SEM) images of interconnects made with this process [6]. The copper electroplating technique is a method of growing copper anisotropically from the bottoms of trenches and vias to a groove pattern width of under 1 μm on the substrate surface. This enables formation of reliable interconnects with no defects by

anisotropic growth of copper. There are many studies on the copper LSI interconnection process, including analyses of its mechanism.

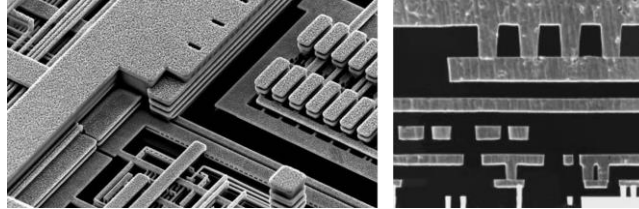


Fig. 1.4 SEM images of copper interconnects [6].

Copper LSI interconnection techniques are divided into two methods: (a) the etching method, in which metal is etched to form interconnects and insulating material is then embedded between lines; and (b) the damascene method, in which trenches or vias are formed in an insulating layer, the resulting features are filled with metal, and the excess metal is finally removed by chemical-mechanical polishing (CMP) to isolate lines. The etching method is used for Al-alloy interconnects, while the damascene method is used for copper interconnects. Figure 1.5 shows schematic diagrams of each interconnection process. The etching method cannot be used with copper, because it has a low vapor pressure with respect to the halide produced during etching, making it difficult to form copper interconnects by a dry etching process [7, 8]. Meanwhile, the damascene method is a much newer process but has advantages. First, it is advantageous for multi-layer interconnection, because the surface is flat after the CMP process. Second, it can make trenches and vias of copper simultaneously. The specific process called the dual damascene process can reduce the number of process steps, so it has become the mainstream approach for copper interconnection technology.

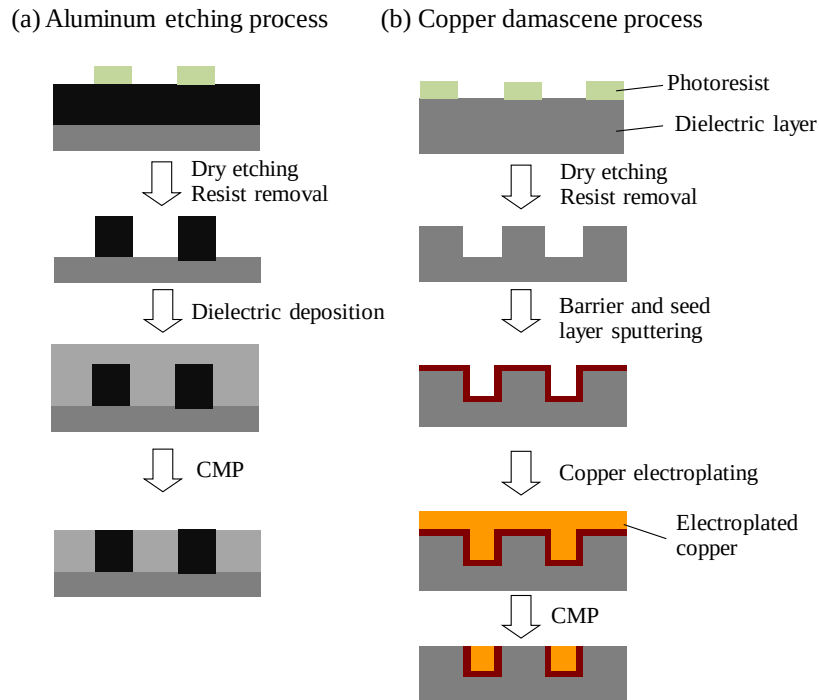


Fig. 1.5 Metal interconnection process flows for (a) Al etching and (b) Cu damascene.

In the damascene process, it is important to fill features without creating defects. Figure 1.6 shows the shape changes of electrodeposited copper under different conditions. As shown in the figure, when copper is deposited uniformly, a void or seam remains inside the feature. It is thus necessary for deposited copper to grow preferentially from the bottom of a feature.

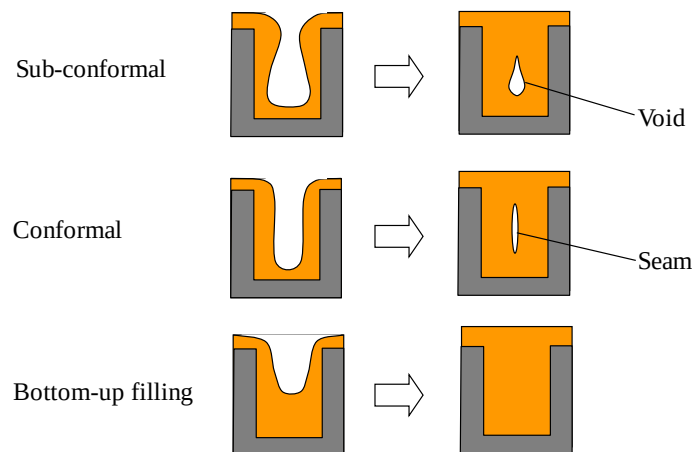


Fig. 1.6 Shape changes of deposited copper.

There are various methods for filling features with copper: (a) sputter-reflow, in which copper is sputtered and then annealed to cause it to flow into features; (b) chemical vapor deposition (CVD), in which copper is deposited directly into features by using an organometallic gas; and (c) electrochemical deposition, in which copper is sputtered onto the surface to form a seed layer and then electrochemically deposited by a solution. The sputter-reflow process uses the same sputtering process that is widely and conventionally used in LSI fabrication. The process is relatively simple and can make films with high purity. Also, it is advantageous in terms of cost, as existing facilities can be used. Unfortunately, it is difficult to fill features with high aspect ratios by using the sputter-reflow process. In contrast, the CVD process has better filling capability, but the costs of the apparatus and reagents are high, and the deposition rate is slow [9, 10]. Compared to these dry metallization processes, the electrochemical deposition process can be operated at room temperature and pressure, which is also advantageous in terms of cost. Copper electrodeposition is also advantageous for its filling capability and process controllability. Therefore, a damascene process using copper electrodeposition has been used for mass LSI production.

The copper damascene process needs a barrier layer, which prevents diffusion of copper atoms into transistors, and a sputtered copper seed layer with a thickness of several hundred nanometers, which is necessary for electrochemical deposition. Copper easily diffuses into insulating layers of SiO_2 or low-k dielectric materials. When it diffuses into a transistor from interconnects, it reduces the performance and reliability because of degradation of the insulating layer and leakage from the transistor junction. A barrier layer to prevent diffusion of copper is thus essential at the interface with the insulating layer. The materials used for the barrier layer, like Ta, TaN, and TiN, have higher electrical resistance and easily form an oxide layer on the surface, however, which makes it difficult to deposit

copper directly onto the barrier layer surface by electrochemical deposition. Therefore, it is also necessary to form a metal seed layer with low resistance as a power-supply layer by ionization sputtering. As seed layer materials, noble metals such as Ru have been studied [11]. A copper seed layer made by electroless copper plating has also been reported [12].

1.1.4 PCB manufacturing process

A PCB is a part that supports and electronically connects components such as LSI devices, resistors, and capacitors. PCBs are classified into three types. The first is a rigid substrate made of hard, insulating resin. The second is a flexible printed circuit (FPC), which uses a thin, flexible resin film as an insulating material. The third type is a “rigid-flexible” substrate, which combines a rigid substrate and a flexible substrate. The key characteristic of an FPC is that it can be embedded in a narrow space because of its high flexibility. Therefore, FPCs are used in small, thin electronic devices such as mobile phones, hard disk drives, and flat-panel displays.

In general, the structure of a PCB consists of either a single-sided board, with wiring on one side of an insulating substrate; a double-sided substrate with wiring on both sides; or a multilayer substrate with multilayer wiring implemented by stacking insulating and wiring layers [13]. A build-up substrate, which is one type of multilayer substrate, is manufactured by repeated formation of an insulating layer, interlayer connections, and copper wiring. As with LSI technology, PCBs require downsizing, and processes for finer metal wiring have thus been studied. Figure 1.7 shows a comparison of typical PCB wiring processes, which are classified into six methods: the (a) subtractive method, (b) semi-additive method, (c) full-additive method, (d) printing method, (e) imprinting method, and (f) anisotropic plating method.

The subtractive method is the most commonly used copper wiring manufacturing method for PCBs. In the subtractive method, circuits are patterned with an etching resist by photolithography to form the desired wiring pattern on a copper foil on the substrate, and then the copper is etched to fabricate the circuit pattern. The challenge in making fine-pitch wiring by the subtractive method is to inhibit side etching. Because the dissolution reaction of copper by the etching solution progresses isotropically, the wiring cross sections become trapezoidal under the photoresist, as shown in Fig. 1.7(a). This side etching decreases the cross-sectional area of the copper. Suppression of side etching is thus one of the most important issues in the subtractive method. The width of the copper pattern is determined not only by the size of the resist but also by variations in the thickness of the copper foil and the flow velocity distribution of the etching solution.

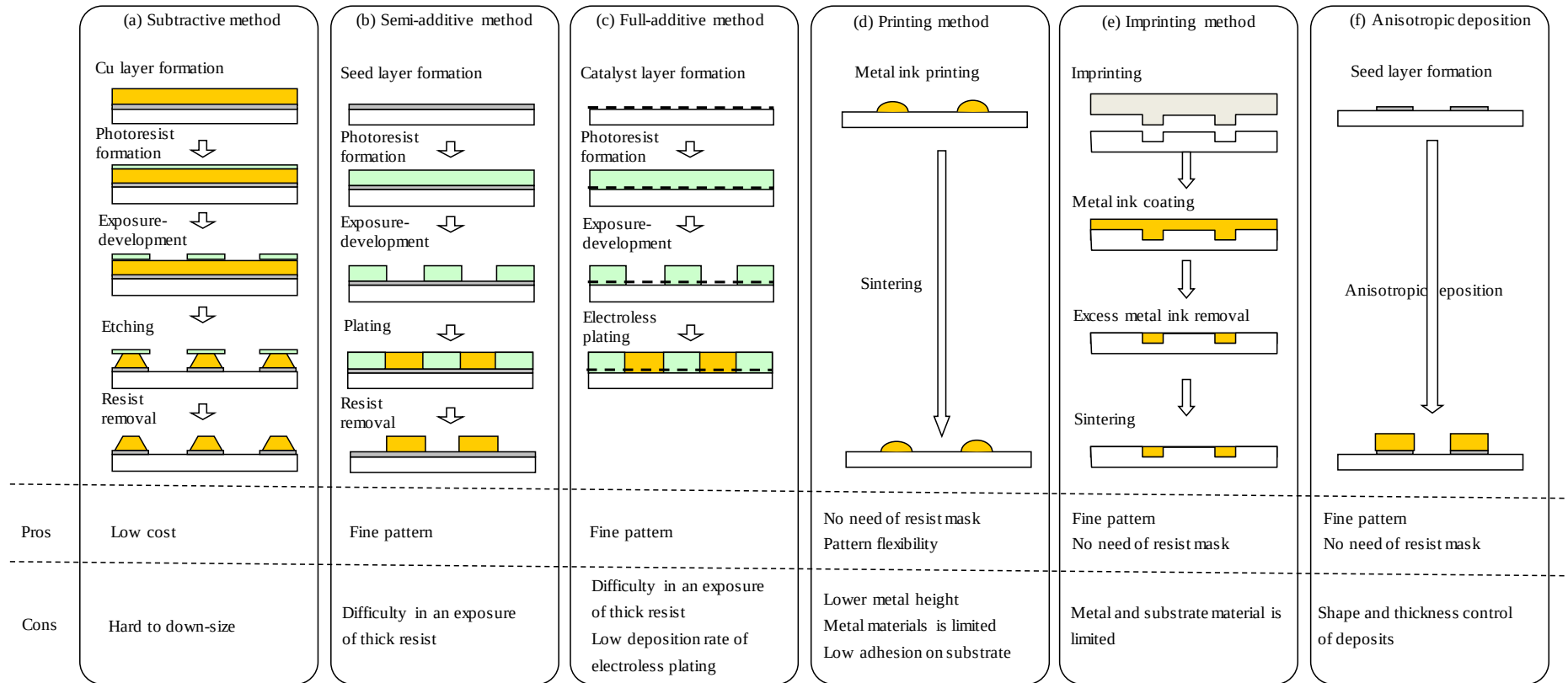


Fig. 1.7 Process flows for manufacturing wiring on a PCB.

In contrast, additive methods first apply resist for plating on the insulating substrate and then deposit copper after exposing the resist. There are two types of additive methods, the semi-additive method and the full-additive method. In the semi-additive method, a thin metal layer is formed as a conductive seed layer over the surface of the substrate, resist for plating is patterned by photolithography, and copper is deposited and filled into the patterned area, as shown in Fig. 1.7(b). After plating, the resist is peeled off and the underlying seed layer is removed by etching to make the final wiring pattern. Although the semi-additive method is a somewhat more complicated process, it can take advantage of copper electrodeposition, with its high deposition rate. The challenge in making fine-pitch wiring by the semi-additive method is to diminish variations in the thickness of the deposited copper, which are due to the influence of the local pattern density of the resist. In addition, because the seed layer is removed by etching, the underlying film is as thin as possible and requires using a material that can be selectively etched with respect to copper. In the full-additive method, shown in Fig. 1.7(c), after pattern formation by a photoresist film without forming a seed layer, copper is deposited by electroless deposition only in areas of the wiring pattern. The full-additive method uses fewer materials for processing and is simple. The issue is that it is difficult to form copper with superior physical properties and good adhesion by thick electroless copper plating.

For formation of fine-pitch wiring, an additive process is theoretically better than the subtractive method. The subtractive method is influenced by the precision of resist formation, etching variation, and side etching, whereas the additive method is affected only by the precision of resist formation. When a photoresist is used, the shape of the resist film can be largely rectangular, and the copper then grows according to this shape, so that copper wiring with a rectangular cross section can be obtained. It is difficult, however, to expose the resist by photolithography, because a thick resist film of the same thickness as the wiring is

necessary, as shown in Fig. 1.7(b). In addition, as wiring becomes finer, it is expected to become more difficult to remove the resist between wires. Furthermore, when the photolithography method is used, the exposure apparatus necessary for forming finer patterns is expensive, and it is becoming difficult to reduce the cost of this process. On the other hand, the thinner the resist film is, the easier fine processing becomes. In a typical plating process, however, the portion of the plating film beyond the thickness of the resist film grows isotropically, not only perpendicular but also parallel to the surface. This makes the space between wires narrower, so it is difficult to reduce the thickness of the resist.

To solve these issues of wiring processes using photolithography, new wiring processes without photolithography have been studied. The metal ink printing method, shown in Fig. 1.7(d), is one such promising technology. In the printing method, an ink with fine metal particles is printed to the substrate surface by screen or inkjet printing, and then the printed pattern is sintered to convert the metal ink into metal wiring. By using the printing method, it is possible to directly form wiring on an insulating substrate without a resist, and the method is suitable for producing small quantities of various kinds of wiring. Because of some issues in wiring processes using the printing method, however, its applications for mass production are quite limited. One issue is that the metal for printing is limited to silver, which has low electromigration resistance. Although copper is preferable from the viewpoints of reliability and cost, it is difficult to make stable copper ink because of the difficulty in suppressing the oxidation of fine copper particles. Nevertheless, copper inks have been developed, and some have been commercialized. Another issue is a tradeoff between the ink viscosity and wiring thickness. Reducing the viscosity of the ink makes printing easier but reduces the wiring thickness after sintering. On the other hand, increasing the ink viscosity makes the wiring thicker, but it becomes more difficult to print because of

problems like nozzle clogging. Furthermore, wiring formed by printing methods has low adhesion to the substrate.

An alternative printing method using ink with fine metal particles is the imprinting method shown in Fig. 1.7(e). In this method, features corresponding to a wiring pattern are formed on the substrate, and the ink is then filled into the pattern and sintered to form wiring. If a pattern with a high aspect ratio was formed, it would be possible to make thick wiring. Unfortunately, the available insulating resins for patterning such high-aspect-ratio features are limited.

As another potential approach, if it was possible to anisotropically deposit metal only in the direction perpendicular to the substrate, as shown in Fig. 1.7(f), then wiring could be formed with a thin resist film or even without resist. This would make it possible to decrease the width of the wiring by using a fine-pitch seed layer. As mentioned above, however, wet processes such as plating and etching generally involve isotropic reactions. Therefore, it is difficult to make a specific structure such as a copper wire on a PCB without masking by using a resist film. Because the photolithography step in resist formation is a major factor determining both the limit of miniaturization and the cost, if plating growth could be controlled entirely in the substrate-depth direction without using a resist mask, it would be advantageous for both downsizing wiring and achieving a low-cost process. Figure 1.8 shows wiring processes with their major applications and ranges of wiring widths.

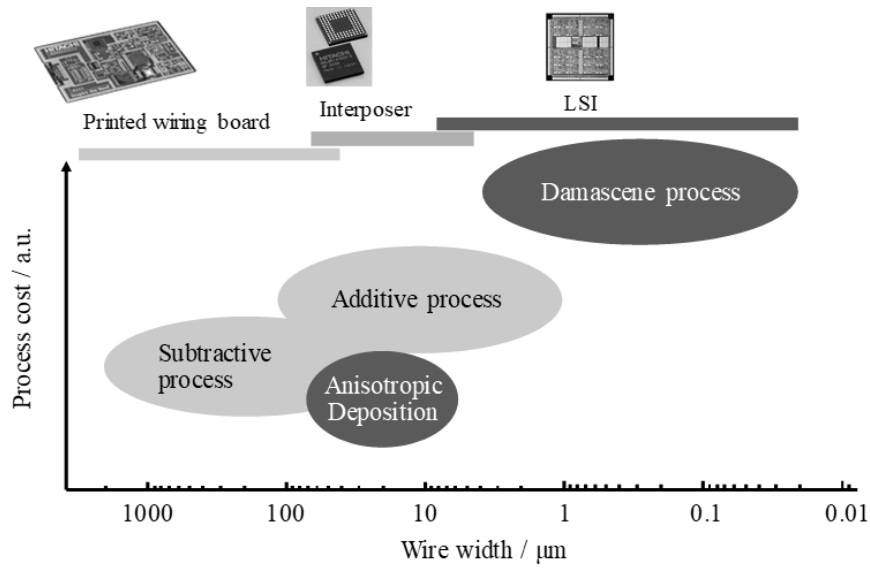


Fig. 1.8 Wiring processes and their applications for electronic devices.

1.2 Electrochemical metal deposition

1.2.1 Surface reactions

The surface reactions in electrochemical deposition of metals in solution were studied from the 1950s to the 1970s. The reactions of single-metal deposition have already been studied systematically [14-17]. Figure 1.9 shows the growth process of the metal layer, which consists of three steps: (1) movement of metal ions to the surface, (2) adsorption of atoms, and (3) surface diffusion of the adsorbed atoms and subsequent crystallization.

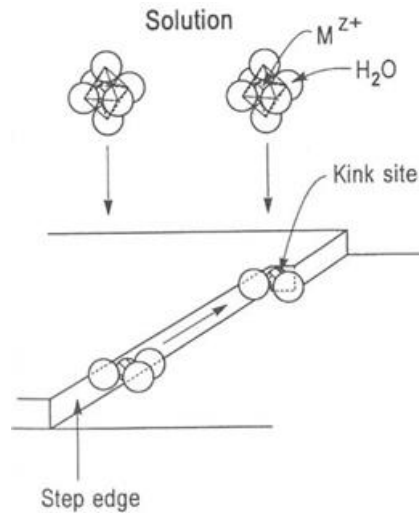


Fig. 1.9 Surface reaction model for electrochemical single-metal deposition [14].

The metal surface has linear defects called steps and point defects called kinks. When the overvoltage in the deposition process is low, the adsorbed atoms diffuse along the step, and the crystal grows at the kink site. The crystal grows epitaxially because it reflects the crystal structure of the underlayer. In this process, when impurities are adsorbed at the step, the crystal growth parallel to the surface is inhibited, but the growth rate perpendicular to the surface becomes faster. As shown in Fig. 1.10, the deposited metal can have a variety of shapes, such as dendrites, triangular pyramids, or spirals, according to the effects of epitaxial growth and preferential growth on specific crystal planes [18]. The shape thus changes depending on the deposition conditions as well as the composition of the solution, including additives.

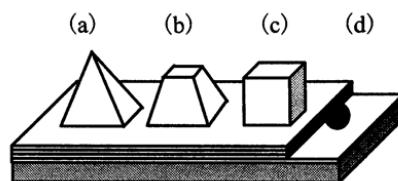


Fig. 1.10 Electrodeposition forms appearing in growth: a (a) pyramid, (b) burning pyramid, (c) cubic crystal, and (d) layered crystal, where the symbol ● represents adsorbed impurities [18].

In contrast, when the overvoltage is high, adsorbed atoms combine with each other to form crystal nuclei, which become sites for crystal growth. For deposition from an aqueous sulfuric acid solution containing CuSO_4 , Fig. 1.11 shows the shapes of the deposited Cu as a function of the overpotential.

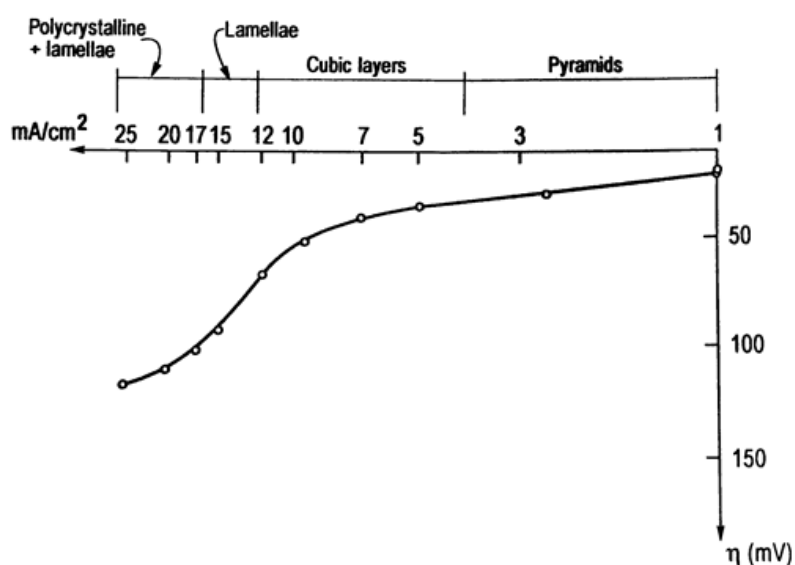


Fig. 1.11 Current-potential curve showing the correlation between overpotential and the growth forms of electrodeposited Cu from CuSO_4 and H_2SO_4 at 25°C [14].

It is necessary to investigate the reaction at the atomic scale to understand the elementary process at the initial stage of metal deposition. For that purpose, it is useful to study the reaction on a single crystal whose surface structure is well known. Before the 1980s, preparation of a clean, single-crystal electrode required an ultra-high vacuum environment, and it was difficult to fabricate a single-crystal electrode that could be used in solution. By the method developed by Clavilier et al. in 1980, however, single crystals of noble metals such as Pt, Au, Pd, Ir, and Rh could easily be prepared [20, 21]. By using this technique, a single crystal with a size of several millimeters can be produced by heating and melting a noble metal wire in a hydrogen-oxygen flame. By cooling this single crystal with

ultrapure water while heating it, it is then possible to obtain a clean, single-crystal surface covered with water. Also, Cu is easily oxidized, but a single-crystal Cu surface can be prepared by electrolytic polishing [22-24]. Studies of electrode surface reactions at the atomic or molecular level with single crystals have been reported [25]. To understand these electrode reactions, however, it is also important to understand the roles of ions, solutions, and organic molecules adsorbed on the surface, in addition to the electrode structure.

Scanning probe microscopy (SPM) techniques, such as scanning tunneling microscopy (STM) and atomic force microscopy (AFM), are widely used to observe metal deposition processes and surface adsorption species at the atomic level [26]. SPM was developed in the 1980s and is a powerful technique that can investigate the atomic-level structure of atoms and molecules adsorbed on a solid surface in solution as well as in ultra-high vacuum. At the early stage of SPM development, reaction analysis at the atomic level was performed for underpotential deposition (UPD) of metals on the surface of a single crystal of a noble metal such as Au or Pt. The Cu electrodeposition reaction has been examined on single-crystal surfaces of Pd, Au [27, 28], Pt [29, 30], and Rh [30].

In addition, a study of the adsorption structures of anions and organic molecules on Cu single-crystal electrodes has been reported [31]. Other studies have examined the adsorption structures of halide ions such as Cl^- , Br^- , and I^- [23, 32, 33] and of organic molecules [34], including simple aromatic molecules such as benzene [35] and benzotriazoles [36]. Regarding the adsorption of additive molecules on Cu in a sulfate solution, Sugimasa et al. reported on the adsorption of phenanthroline [37], and Bae et al. reported on the structures of additive molecules adsorbed on Cu (100), as shown in Fig. 1.12 [38].

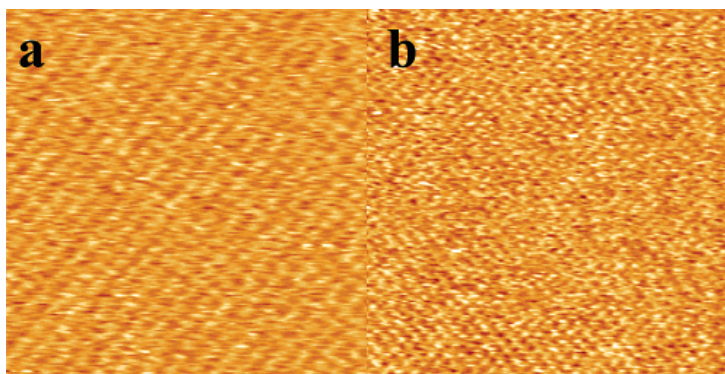


Fig. 1.12 In situ electrochemical STM images of a Cu (100) surface obtained at -0.30 V in ca. 0.4 M SPS + 0.1 M HClO_4 solution. The images were obtained 120 s (a) and 6576 s (b) after addition of bis (3-sulfopropyl) disulfide (SPS). The image sizes are 5 nm $\times$ 5 nm (a) and 8 nm $\times$ 8 nm (b). The respective tip potentials and tunneling currents were -0.29 V and 44 nA (a) and -0.28 V and 40 nA (b) [38].

As another measurement tool, a quartz crystal microbalance (QCM) can quantitatively measure metal deposition and molecular adsorption on an electrode surface. An electrochemical quartz crystal microbalance (EQCM) is specifically applied to study the mass change of an electrode and obtain current-potential curves at the same time. An EQCM can thus be applied to investigate the underpotential deposition of metals and the reactions of adsorbed molecules on the surface. While SPM and EQCM measurements are essential experimental methods for electrode surface analysis in a solution, however, it is still difficult to identify surface species.

On the other hand, spectroscopy is a suitable method for identifying surface-adsorbed species. Spectroscopy techniques for in situ observation of electrode surface reactions include ultraviolet-visible (UV-vis) spectroscopy, ellipsometry, infrared spectroscopy, and Raman spectroscopy. Other spectroscopic techniques use nonlinear optical phenomena, namely, second-harmonic generation and sum-frequency generation [39]. These spectroscopy techniques can observe an electrode surface and the molecules adsorbed on it by using light transmitted through the solution.

1.2.2 Kinetics and mechanisms

Electrochemical deposition of metals involves complicated reactions, because the state of the electrode varies with the progress of deposition, while in the solution, various ions and additive molecules influence each other. Therefore, analysis of the actual reaction system is difficult. On the other hand, the reaction mechanisms used for practical applications such as Cu electroplating have been widely studied in terms of the shapes of deposited Cu and the adsorption and consumption of additives [40, 41].

Figure 1.13 shows general cathodic polarization curves in an aqueous solution containing metal ions. As the overpotential increases, the current for metal deposition begins to flow. At this time, the current density is determined by the activation reaction and increases in proportion to the exponential of the overpotential. When the overpotential becomes higher than a certain level, the diffusion of metal ions to the surface becomes the rate-limiting step, and the current density becomes constant regardless of the overpotential. When the overvoltage is further increased, hydrogen is generated by electrolysis of water.

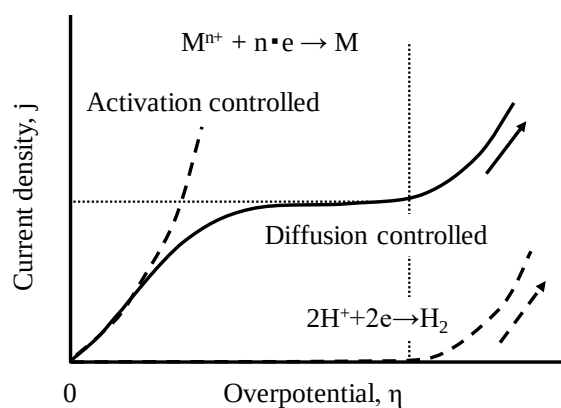
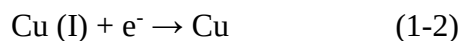
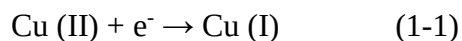


Fig. 1.13 General current-overpotential relationship in a solution containing metal ions.

The Cu deposition reaction in a solution containing CuSO₄ proceeds in the two steps shown below [42, 43, 44].



The former reaction (1-1) is relatively slow and becomes the rate-determining step [42]. Cu (I) can also be formed from Cu (II) by the following disproportionation reaction.



The equilibrium constant of this reaction is 5.6×10^{-7} at 25 °C, and hardly any Cu (I) exists in the solution [45]. When Cl⁻ or thiourea is present, however, Cu (I) forms a complex with these ions or molecules and thus exists in a monovalent state [46, 47].

Higher current density is desirable for industrial applications of Cu plating. As mentioned above, the reaction is greatly affected by diffusion in the solution when the overpotential is increased. In particular, when irregularities are present or a specific resist pattern is formed on the surface, the diffusion layer near these irregularities or patterns changes. Figure 1.14 shows the time-dependent change of the diffusion layer for electrodes having different surface morphologies [18]. In Fig. 1.14(b), the diffusion of ions to the protrusion becomes faster, leading to a faster deposition rate. On the other hand, in Fig. 1.14(c), the difference in deposition rates between the convex and flat portions is small. The deposition shape change due to the surface morphology becomes remarkable when the surface roughness of the electrode is equal to or larger than the thickness of the diffusion layer. Therefore, it is necessary to determine the deposition conditions according to the roughness of the electrode surface.

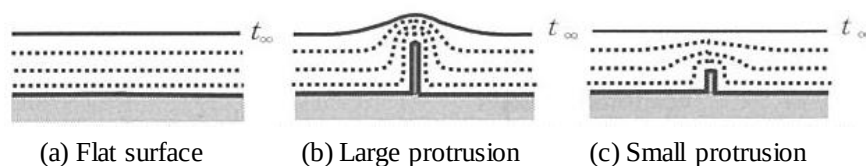


Fig. 1.14 Change over time of non-steady-state diffusion layers on different electrode surface morphologies. The solid lines denoted by "t" show the Nernst layer after a long time [18].

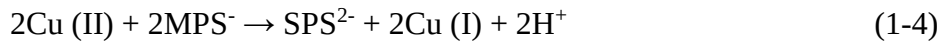
1.2.3 Additives for copper electroplating

A Cu plating solution usually contains one or more additives in addition to the Cu ions and electrolyte. The additives are compounds added in small amounts in the plating solution to obtain desired characteristics such as specific shapes and physical properties of the deposited Cu. These additives adsorb and react on the surface, affecting the deposition rate, crystal growth, and surface shape of the deposited metal [14]. To obtain the desired properties, it is important to appropriately select the deposition conditions and control the additives.

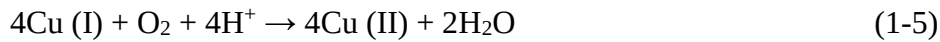
Various organic compounds and inorganic ions have been used as additives for a CuSO_4 plating solution, including gelatin [48], thiourea [49, 50, 51, 52, 53], benzotriazole [54], and chloride ions (Cl^-) [55, 56]. The additive currently used widely in practice is a combination of chloride ions and two or three kinds of organic compounds [57]. Because the specific compositions of additives on the market have not been disclosed, each additive is frequently described by its expected effect, such as an accelerator, a suppressor, or a leveler. Despite this classification by the effect of the additive, note that an additive may have multiple effects and be composed of multiple compounds, and additives with the same effect may be described differently. This section describes four representative additives for a CuSO_4 plating solution: the suppressor, accelerator, leveler, and Cl^- .

A suppressor is an additive that suppresses the plating reaction by adsorbing on the Cu surface. In other contexts, it is called a polymer, inhibitor, or lubricant. Two well-known suppressor compounds are polyethylene glycol and polypropylene glycol [58, 59, 60, 61].

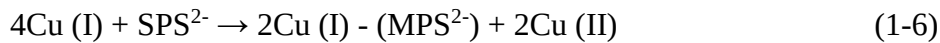
An accelerator is an additive that enhances the Cu plating reaction in the presence of suppressors. In other contexts, it is called a catalyst or brightener. Widely known accelerator compounds include bis (3-sulfopropyl) disulfide (SPS) and 3-mercapto-1-propane sulfonate (MPS) [62, 63]. SPS is a dimer to which the thiol group of MPS is bound. Moffat et al. reported mutual change between SPS and MPS in a CuSO₄ plating solution [64]. MPS changes to SPS through oxidation by the following reaction.



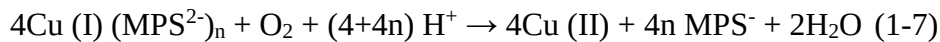
The resulting Cu (I) is immediately oxidized by dissolved oxygen through the following reaction.



On the other hand, for the case of a Cu anode, it has been proposed that Cu (I) forms on the surface of the anode, and that MPS and Cu (I) then form a complex [62].



This complex is oxidized to MPS by the following reaction.



When Nafion film is placed between the substrate (cathode) and the anode to prevent the movement of additives in a plating solution, the oxidation from SPS to MPS does not occur. Therefore, if Cu metal is not present in the plating solution, reaction (1-5) proceeds rapidly as reaction (1-4) becomes dominant.

A leveler is an additive that has a leveling effect to smooth surface roughness. It works by adsorbing more to convex areas by diffusion and increasing the overpotential of those areas to suppress plating deposition. Known levelers include some dyes such as Janus

Green B, cationic surfactants, and alkyl ammonium salts. Zheng et al. reported the result of calculating the adsorption energy on the Cu surface of Janus Green B and 1-vinyl imidazole by using density functional theory (DFT) [65]. Both of these molecules have a nitrogen-containing aromatic ring, and the adsorption on the Cu surface is considered to mainly involve nitrogen atoms [66]. Molecules with large adsorption energies are expected to have structures such as adsorbable polar groups and planar structures with π -conjugated rings. This information can be considered as a guide for selecting additives to suppress the Cu deposition reaction.

Lastly among the four additive types considered here, Cl^- affects the deposition reaction of Cu by adsorbing on the surface. It is particularly effective in combination with organic compounds such as thiourea [51].

These additives are believed to react in a composite manner, and their specific roles and reaction mechanisms are not understood well. To meet various requirements for Cu plating, it is important to understand the roles of additives and the Cu deposition process in detail, and to clarify the reaction mechanisms. In addition, it should be possible to develop a new Cu wiring process based on these mechanisms.

1.2.4 Structure and properties of deposited copper

The physical properties of electrochemically deposited copper depend greatly on the plating conditions. The strength of the deposited film can be improved by refining the crystal grains. As described in section 1.2.1, by increasing the overpotential to promote nucleation, crystal grains can be miniaturized. The overpotential can be increased by using an additive that inhibits the crystallization reaction, making it possible to refine the crystal grains. On the other hand, additives can become impurities in the deposited film, which may lead to an increase in electrical resistance and a decrease in ductility [67, 68, 69].

1.2.5 Electroless copper deposition

Electroless copper deposition is a method of reducing copper ions chemically with a reducing agent in a plating solution to deposit copper on a substrate [70]. Although the copper ions and reducing agent coexist in the solution, they do not directly react with each other. By selecting proper compounds and conditions to allow reaction only on a copper surface, copper can be deposited only on the substrate. The greatest advantage of electroless copper plating is that it enables deposition on an insulating substrate without an external power supply. Another advantage is that copper can be deposited with uniform thickness even on a substrate having a complicated shape, because there is no influence from the current density distribution, which is one issue in electrochemical deposition. The disadvantage of electroless copper plating is that the deposition rate is slow, at several micrometers per hour, versus several micrometers per minute for electrochemical deposition. Other disadvantages are that it is difficult to maintain the solution conditions and that the solution contains formaldehyde, a harmful compound, as a reducing agent. To solve these issues, a solution with a deposition rate of over 5 $\mu\text{m/h}$ has been developed [71], while other reducing agents, including dimethylamine borane [72], hypophosphite [73], glyoxylic acid [74, 75], and a Co (II) compound [76], have been investigated as substitutes for formaldehyde.

1.3 Anisotropic metal deposition

1.3.1 Metal deposition for trench filling

There are two types of anisotropic deposition at a macroscopic scale: preferential growth from the bottom in a recess, and formation of a convex shape from a flat area on the

substrate. The former type of deposition is known as a leveling effect. In 1957, Watson et al. reported a phenomenon in which the thickness of electroplated nickel in a recess becomes thicker than in flat portions of the substrate surface [77]. Figure 1.15 shows a cross-sectional optical image of a substrate after electrodeposition of nickel in a solution containing thiourea as a leveler. The surface roughness is reduced by nickel electroplating, thus smoothing the substrate surface and improving its appearance.

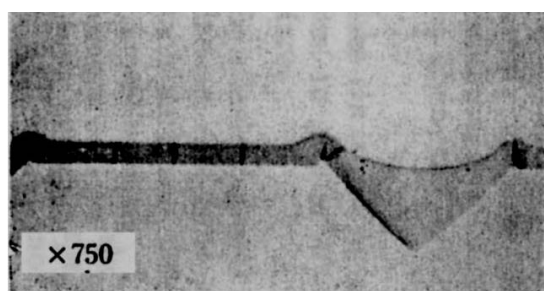


Fig. 1.15 Optical image of nickel deposited on a substrate from a nickel plating solution containing thiourea [77].

A similar leveling effect is also obtained by using additives in electrolytic copper plating. Figure 1.16 shows cross-sectional SEM images of a copper-plated substrate under changing deposition conditions in a solution containing Janus Green B as a leveler [78]. The thickness ratio between the recesses and convex areas is changed by the plating conditions. Assuming that the leveler reacts on the substrate surface and its concentration decreases, the deposition rate in the recesses varies depending on the balance between consumption and diffusion of the leveler because of its deposition-inhibiting effect.

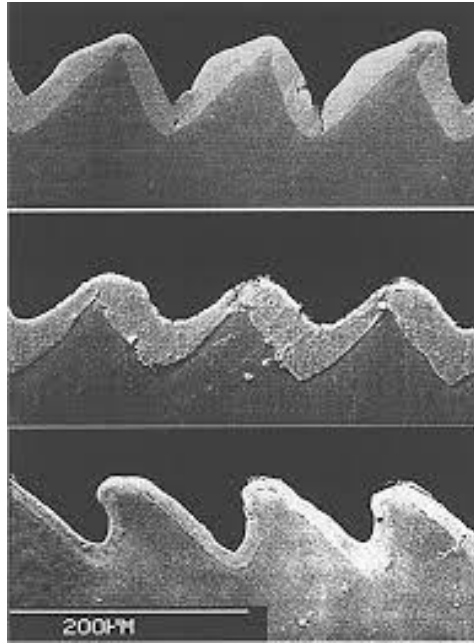


Fig. 1.16 Cross-sectional SEM images of deposited copper from a solution of 0.24 M $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ + 1.8 M H_2SO_4 + 300 mg/L PEG3350 +50 mg/L Cl^- + 1 mg/L SPS + 1 mg/L Janus Green B [78].

Preferential growth from the bottom of a recessed feature, which includes trenches and vias, is applicable to the damascene process in LSI copper interconnections. To fill features completely, it is important to balance the suppressor and the accelerator for preferential growth from the bottoms. Two models of preferential growth using additives have been reported. In one model, an accelerating additive is concentrated in the bottoms of features as the deposition process proceeds. In the other model, a suppressing additive is consumed on the surface, causing the concentration in the bottoms to decrease. In both models, however, the phenomenon by which the additive is concentrated or the concentration decreases cannot be directly observed, and the reaction mechanism is not clear.

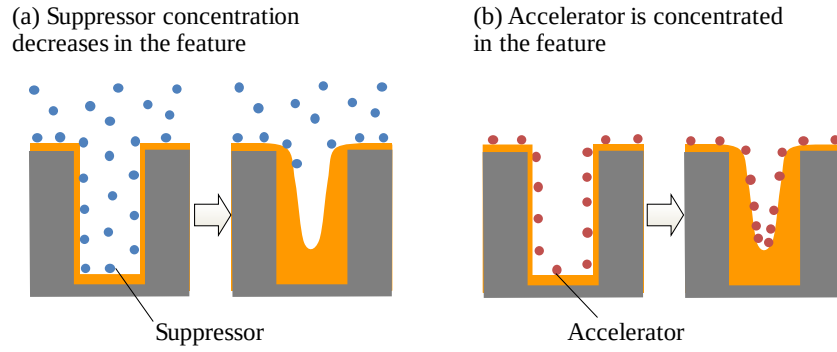


Fig. 1.17 Trench and via filling mechanisms with additives in the damascene process.

Electrochemical deposition of copper is used for the damascene process because an accelerator and suppressor in a copper sulfate solution can play the role described above to promote preferential deposition from the bottoms of features. This type of preferential deposition is called "superfilling" or "bottom-up filling." Figure 1.17 shows the difference in the growth of deposited copper in a feature because of a suppressor or an accelerator. In a conventional copper plating solution, the deposited copper grows almost uniformly in a feature, and defects called voids or seams remain in the center of the feature, as described previously. On the other hand, in the bottom-up filling process, the inside of the feature is filled with copper without defects, because the deposition rate is faster at the bottom than on the sides. Figure 1.18 shows cross-sectional SEM micrographs of fine-pitch trench patterns deposited from a sulfuric acid solution with a suppressor and an accelerator [79]. It can be seen that the copper grew preferentially from the bottoms of the trenches for widths ranging from 0.2 to 1.7 μm .

These results lead to a proposed model, represented by the formula below, of an accelerator concentrated on the surfaces inside a trench. Here, A is the local surface area, t is the time, k_1 is a rate constant, Θ_{sps} is the surface coverage of the accelerator, and $\Theta_{\text{sps, eq}}$ is the equilibrium surface coverage of the accelerator.

$$\frac{d(A\theta_{\text{SPS}})}{dt} = -k_1 A(\theta_{\text{SPS}} - \theta_{\text{SPS,eq}}) \quad (1-8)$$

From this model, Fig. 1.19 shows the calculated results for the growth process of the deposited copper in a trench. The results shown in Figs. 1.18 and 1.19 are in good agreement.

In addition, when electrochemical copper deposition continues after filling is complete by using a solution containing an accelerator, the phenomenon called overgrowth or overplating is observed. In this phenomenon, the metal deposited on filled features becomes thicker than that in flat areas. This occurs because the accelerator is concentrated on the patterned feature just after filling. Because the overgrowth increases the surface roughness, this is disadvantageous to planarization during the subsequent CMP process. Thus, the copper damascene process requires as much prevention of overgrowth as possible. A leveler is useful for inhibiting the overgrowth. Figure 1.20 shows cross-sectional SEM images of features obtained from solutions with and without dodecyltrimethylammonium chloride (DTAC) as a leveler [80]. Without DTAC, the deposited metal on the patterned features became thick, but the overgrowth was suppressed with DTAC.

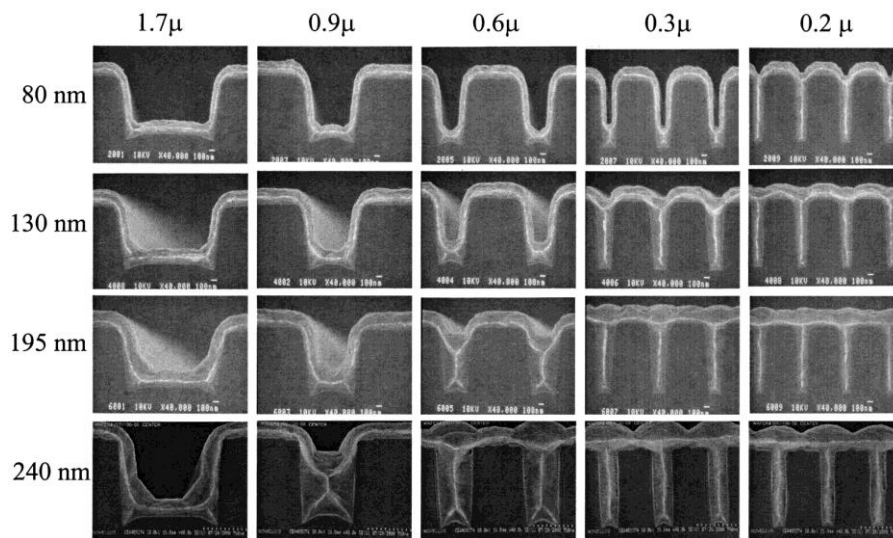


Fig. 1.18 Cross-sectional SEM images showing the results of fill experiments for five widths of trenches with nominal thicknesses of 80, 130, 195, and 240 nm [79].

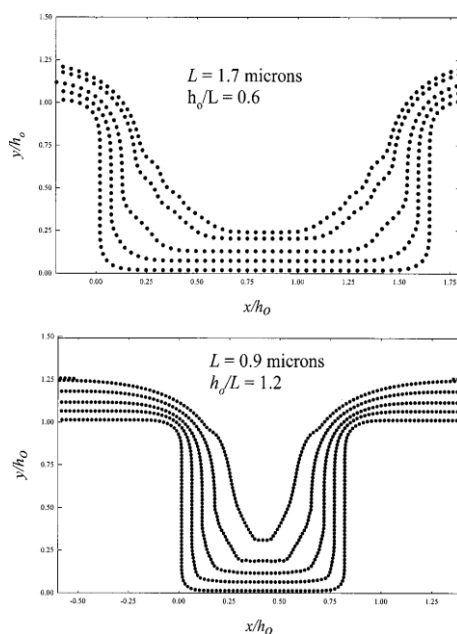


Fig. 1.19 Simulated fill results for two larger trenches. The bottommost lines show the approximate shapes of the original features, and the lines above correspond to deposited thicknesses of 80, 130, 195, and 240 nm [79].

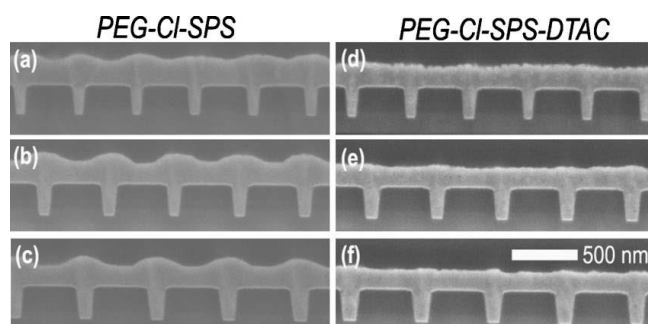


Fig. 1.20 Cross-sectional SEM images of copper deposited at -0.250 V vs. SCE for 30 s from an electrolyte of 0.16 mol/L CuSO_4 + 1.8 mol/L H_2SO_4 + 88 $\mu\text{mol/L}$ PEG + 1 mmol/L NaCl + 50 $\mu\text{mol/L}$ SPS + 60 $\mu\text{mol/L}$ DTAC [80].

1.3.2 Anisotropic metal deposition

The formation of a convex shape from a flat area on a substrate by anisotropic deposition perpendicular to the surface has hardly been reported, as it is difficult to deposit metal patterns without any defined structure. Nevertheless, Putten et al. made a square pyramidal structure by electroless nickel deposition [81]. Figure 1.21 shows an SEM image of deposited nickel (Ni-P) on an Al pad. As illustrated in Fig. 1.22, the mechanism of the anisotropic growth of such deposited nickel is considered to be the diffusion of inhibiting additives. The electroless reaction takes place on the catalyzed surface, while at the same time, the inhibiting additive is incorporated into the film or consumed. At this time, the supply of the inhibiting additive by diffusion is faster at the edges of the pattern than in flat portions. Therefore, the reaction at the edges is suppressed, and the plated film becomes thin there. Lin et al. also investigated anisotropic growth using electroless nickel plating with lead acetate as an additive [82]. They proposed that lead acetate acts as an inhibitor to suppress the reaction at the edges of the pattern.

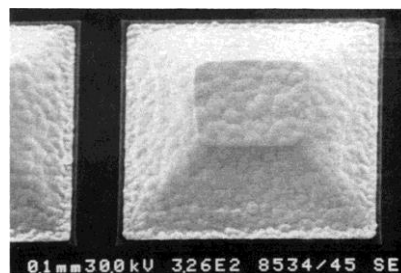


Fig. 1.21 Practical achievement of bevel plating: SEM image of a NiP pyramid deposited onto an Al bond pad of an IC [81].

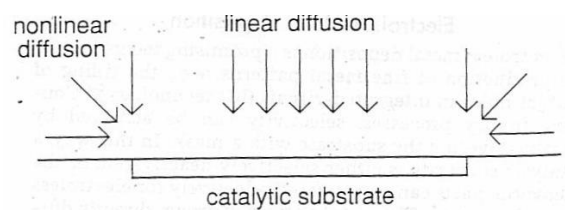


Fig. 1.22 Comparison of mass transport at the edges and to the center of a substrate [81].

1.4 Objectives and outline of this dissertation

The objectives of this work are to clarify the influence of additives on the shapes and properties of deposited copper in an anisotropic electrodeposition reaction and to develop a novel copper wiring method based on this anisotropic growth. The dissertation investigates two anisotropic growth methods for copper deposition: (1) anisotropic deposition from the bottom of a feature in a sub-micrometer pattern on the substrate surface, and (2) anisotropic deposition for the formation of a micrometer-scale convex shape on the surface by using a difference in surface roughness. This work then considers the application of electrolytic copper plating in the manufacturing processes of semiconductor devices and PCBs used in various electronic devices. The dissertation also provides detailed discussions of the proposed method to deposit copper anisotropically by using additives in solution, and of the reaction mechanism of the anisotropic deposition, including the role of additives.

Chapter 1 has described manufacturing processes using copper plating for electronic components and the reaction mechanism of copper deposition with additives. It has also described anisotropic deposition of metals from a solution and models of this phenomenon.

Next, chapter 2 describes the details of the materials, substrate preparation method, electrochemical measurements, spectroscopic measurements, and simulation method used in this work.

Chapter 3 then describes anisotropic deposition of copper from the bottoms of trenches and vias on the surface, which are used for manufacturing copper wiring in LSI devices. The mechanisms of preferential copper growth from the bottom of a feature are proposed by using the results of electrochemical measurements, observations of the shapes of deposited copper, and simulations of the reaction, including additives. The characteristics of deposited copper on fine features under changing deposition conditions are also described.

Chapter 4 describes the feasibility of forming a convex shape with a width of several tens of micrometers for copper wiring on a PCB by using the surface reaction of additives in the copper plating solution and the surface roughness of the substrate. It was found that convex shapes of copper could be formed in areas with fine-pitch trench patterns by selecting proper deposition conditions and a solution with inhibiting additives. Under these conditions, copper was anisotropically grown perpendicular to the surface. In addition, a mechanism is proposed for the effect on the reaction of the concentration gradient of additives in the solution.

Then, chapter 5 proposes a reaction mechanism for anisotropic copper deposition using additives, according to the results of electrochemical measurements and in situ surface-enhanced Raman spectroscopy (SERS). The SERS measurements showed that the additive adsorbs on the electrode surface, and cathodic potential scans by voltammetry found that the copper deposition rate increases. These results indicate that the additive desorbs or decomposes on the surface during copper electrodeposition. Therefore, the concentration of inhibiting additive decreases more on the patterned area than on the flat area. This inhomogeneity of concentration leads to preferential growth of copper on the patterned area.

Finally, chapter 6 summarizes the results of this work and describes future prospects.

References

- [1] John N. Randall, James H.G. Owen, Ehud Fuchs, Joseph Lake, James R. Von Ehr, Josh Ballard, and Erik Henriksen, *Micro and Nano Engineering*, vol. 1, p. 1-14, 2018.
- [2] C. Auth et al., 2017 IEEE International Electron Devices Meeting (IEDM), p. 29.1.1
- [3] A. Bhatnagar et al., *Solid State Technology*, vol. 52, no. 10, p. 16, 2009.
- [4] P.C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, *IBM J. Res. Dev.*, vol. 42, p. 567, 1998.
- [5] D. Edelstein et al., In *Technical Digest, IEEE International Electron Devices Meeting*, p. 773, 1997.
- [6] Panos C. Andricacos, *Interface*, Spring 1999.
- [7] B.J. Howard and C. Steinbruchel, *Appl. Phys. Lett.*, vol. 59, p. 914, 1991.
- [8] K. Ohno, M. Sato, and Y. Arita, *Jpn. J. Appl. Phys. Lett.*, vol. 28, p. L1070, 1989.
- [9] D. Josell, S. Kim, D. Wheeler, T.P. Moffat, and S. G. Pyo, *J. Electrochem. Soc.*, vol. 150, no. 5, p. C368, 2003.
- [10] Z. W. Li, A. Rahtu, and R. G. Gordon, *J. Electrochem. Soc.*, vol. 153, no. 11, p. C787, 2006.
- [11] D. Jeong, H. Inoue, Y. Ohno, K. Namba, and H. Shinriki, *Proceedings of the 2009 IEEE International Interconnect Technology Conference*, p. 95, 2009.
- [12] J. -H. Lin et al., *J. Vac. Sci. Technol. B*, vol. 20, no. 2, p. 561, 2002.
- [13] Clyde F. Coombs Jr. and Happy Holden, *Printed Circuits Handbook, Seventh Edition 7th Edition*, 2016.
- [14] M. Paunovic and M. Schlesinger, *Fundamentals of Electrochemical Deposition*. New York: John Wiley & Sons, 1998.
- [15] J. O'M. Bockris and S. U. M. Khan, *Surface Electrochemistry*. New York: Plenum Press, 1993.
- [16] J. O'M. Bockris and A. K. N. Reddy, *Modern Electrochemistry*. New York: Plenum Press, 1970.
- [17] J. Clavilier, *J. Electroanal. Chem.*, vol. 107, p. 211, 1980.
- [18] S. Haruyama, *Electrochemistry for engineers of the surface finishing (2006)*. (表面技術者のための電気化学 in Japanese)
- [20] J. Clavilier, R. Faure, G. Guinet, and R. Durand, *J. Electroanal. Chem.*, vol. 107, p. 205, 1980.
- [21] K. Itaya, *Prog. Surf. Sci.*, vol. 58, p. 121, 1998.

- [22] J. Inukai, Y. Osawa, and K. Itaya, *J. Phys. Chem., B*, vol. 102, p. 10034, 1998.
- [23] Junji Inukai and Kingo Itaya, *J. Surface Finish. Soc. Jpn.*, vol. 53, no. 12, p. 828, 2002.
(in Japanese)
- [24] S. Ye et al., *Electrochemistry*, vol. 77, no. 1, p. 2, 2009.
- [25] S. Ye and K. Uosaki, *DENKI KAGAKU*, vol. 66, no. 2, p. 145, 1998.
- [26] S. Manne, P. K. Hansma, J. Massie, V. B. Elings, and A. A. Gewirth, *Science*, no. 251, p. 183, 1991.
- [27] K. Ikemiya, S. Miyaoka, and S. Hara, *Surf. Sci. Lett.*, no. 311, p. 641, 1994.
- [28] K. Sashikata, N. Furuya, and K. Itaya, *J. Electroanal. Chem.*, no. 316, p. 361, 1991.
- [29] Z. -L. Wu, Z. -H. Zang, and S. -L. Yau, *Langmuir*, no. 16, p. 3522, 2000.
- [30] J. Inukai and K. Itaya, *J. Surface Finish. Soc. Jpn.*, vol. 53, no. 12, p. 828, 2002.
- [31] D. W. Saggs and A. J. Bard, *J. Phys. Chem.*, vol. 99, p. 8349, 1995.
- [32] L. -J. Wan and K. Itaya, *J. Electroanal. Chem.*, vol. 473, p. 10, 1999.
- [33] J. Inukai et al., *J. Phys. Chem. B*, vol. 102, p. 3498, 1998.
- [34] R. J. Nicols, W. Beckmann, H. Mayer, N. Batina, and D. M. Kolb, *J. Electroanal. Chem.*, vol. 330, p. 381, 1992.
- [35] L. -J. Wan and K. Itaya, *Langmuir*, vol. 13, p. 7173, 1997.
- [36] M. Sugimasa, J. Inukai, and K. Itaya, *J. Electrochem. Soc.*, vol. 149, p. E367, 2002.
- [37] M. Sugimasa, J. Inukai, and K. Itaya, *J. Electrochem. Soc.*, vol. 150, no. 5, p. E266, 2003.
- [38] S. -E. Bae and A. A. Gewirth, *Langmuir*, vol. 22, no. 25, p. 10315, 2006.
- [39] Shen Ye and Osawa Masatoshi, "Molecular Structures on Solid Substrates Probed by Sum Frequency Generation (SFG) Vibration Spectroscopy," *Chem. Lett.*, vol. 38, p. 386, 2009.
- [40] E. D. Eliadis, R. G. Nuzzo, A. A. Gewirth, and R. C. Alkire, *J. Electrochem. Soc.*, vol. 144, p. 96, 1997.
- [41] Kazuo Kondo, *J. Surface Finish. Soc. Jpn.*, vol. 60, no. 12, p. 754, 2009.
- [42] E. Mattson and J. O'M. Bockris, *Trans. Faraday Soc.*, vol. 55, p. 1586, 1959.
- [43] J. O'M. Bockris and M. Enyo, *Trans. Faraday Soc.*, vol. 58, p. 1187, 1962.
- [44] H. Kita and J. O'M. Bockris, *J. Electrochem. Soc.*, vol. 109, p. 928, 1962.
- [45] S. Bruckenstein and G. W. Tindall, *Analyt. Chem.*, vol. 40, p. 1402, 1968.
- [46] M. Yokoi, S. Konishi, and T. Hayashi, *DENKI KAGAKU*, vol. 52, p. 218, 1984.
- [47] A. E. Bolzan, I. B. Wakenge, R. C. V. Piatti, R. C. Salvarezza, and A. J. Arvia, *J. Electroanal. Chem.*, vol. 501, p. 241, 2001.

- [48] N. Koura, Y. Ejiri, M. Mamiya, Y. Idemoto, and F. Matsumoto, *Hyomen Gijutsu*, vol. 51, no. 9, p. 938, 2000.
- [49] L. Fairman, *Metal Finishing*, vol. 68, p. 45, 1970.
- [50] A. E. Bolzan, I. B. Wakenge, R. C. V. Piatti, R. C. Salvarezza, and A. J. Arvia, *J. Electroanal. Chem.*, vol. 501, p. 241, 2001.
- [51] N. Tantavichet, S. Damronglerd, and O. Chailapakul, *Electrochim. Acta.*, vol. 55, p. 240, 2009.
- [52] A. Szymaszek, J. Biernat, and L. Pajdowski, *Electrochimica Acta*, vol. 22, p. 359, 1977.
- [53] S. Yoon, M. Schwartz CEF, and K. Nobe, *Plating and surface finishing*, vol. 81, no. 12, p. 65, 1995.
- [54] T. Y. B. Leung, M. Kang, B. F. Corry, and A. A. Gewirth, *J. Electrochem. Soc.*, vol. 147, no. 9, p. 3326, 2000.
- [55] N. Pradhan, P. G. Krishna, and S. C. Das, *Plating & Surface Finishing*, vol. 83, no. 3, p. 56, 1996.
- [56] Z. Nagy, J. P. Blaudeau, N. C. Hung, L. A. Curtis, and D. J. Zurawski, *J. Electrochem. Soc.*, vol. 142, no. 6, p. L87, 1995.
- [57] P. M. Vereecken, R. A. Binstead, H. Deligianni, and P.C. Andricacos, *IBM J. Res. Dev.*, vol. 49, no. 1, p. 3, 2005.
- [58] R Manu, S. Jayakrishnan, *Bulletin of Materials Science*, vol. 34, Issue 2, p. 347–356, 2011
- [59] D. Stoychev and C. Tsvetanov, *J. Appl. Electrochem.*, vol. 26, Issue 7, p. 741–74, 1996
- [60] James J. Kelly and Alan C. West, *J. Electrochem. Soc.*, vol. 145, issue 10, p. 3472-3476, 1998
- [61] M.R.H.Hill and G.T.Rogers, *J. Electroanal. Chem. Interfacial Electrochem.* vol. 86, Issue 1, p. 179-188, 1978
- [62] J. P. Healy, D. Pletcher, and M. Goodenough, *J. Electroanal. Chem.*, vol. 338, p. 167, 1992.
- [63] Z. D. Schultz, Z. V. Feng, M. E. Biggin, and A. A. Gewirth, *J. Electrochem. Soc.*, vol. 153, no. 2, p. C97, 2006.
- [64] T. P. Moffat, B. Baker, D. Wheeler, and D. Josell, *Electrochem. Solid-State Lett.*, vol. 6, no. 4, p. C59, 2003.
- [65] L. Zheng et al., *Electrochim. Acta*, vol. 283, p. 560-567, 2018.
- [66] Z. Lai et al., *Electrochim. Acta*, vol. 273, p. 318-326, 2018.

- [67] S. H. Brongersma, E. Kerr, I. Vervoort, A. Saerens and K. Maex, J. Materials Res., vol. 17, Issue 3, p. 582-589, 2002.
- [68] M. Stangl, J. Acker, S. Oswald, M. Uhlemann, T. Gemming, S. Baunack and K. Wetzig, Microelectronic Engineering, vol. 84, Issue 1, p. 54-59, 2007.
- [69] W. Zhanga, S. H. Brongersma, N. Heylen, G. Beyer, W. Vandervorst and K. Maex, J. Electrochem. Soc., vol. 152, issue 12, C832-C837, 2005.
- [70] T. Fujinami, Hyomen Gijutsu, vol. 50, no. 2, p. 129, 1999.
- [71] H. Akahoshi, IEEE Trans. CPMT, Part A, vol. 18, p. 127, 1995.
- [72] R. Jagannathan and M. Krishnan, IBM J. Res. Develop., vol. 37, no. 2, p. 117, 1993.
- [73] A. Hung and K. -M. Chen, J. Electrochem. Soc., vol. 136, p. 72, 1989.
- [74] J. Darken, Trans. Inst. Metal Finishing, vol. 69, p. 66, 1991.
- [75] Y. Shacham-Diamond, Electrochem. Solid-State Lett. , vol. 3, no. 6, p. 279, 2000.
- [76] A. Vaškelis, I. Stankevičiene, A. Jagminiene, L.T. Tamašiunaite, and E. Norkus, J. Electroanal. Chem., vol. 622, no. 2, p. 136, 2009.
- [77] S. A. Watson, Trans. Inst. Met. Finishing, vol. 34, p.185, 1957.
- [78] J.J. Kelly et al., J. Electrochem. Soc., vol. 146, no. 7, p. 2540-2545, 1999
- [79] Alan C. West et al., Electrochemical and Solid-State Letters, vol. 4, no. 7, p. C50-C53, 2001
- [80] S.-K. Kim et al., J. Electrochem. Soc., vol. 153, no. 12, p. C826-C833, 2006
- [81] A. M. T. van der Putten and J. W. G. de Bakker, J. Electrochem. Soc., vol. 140, p. 2229, 1993.
- [82] Kwang-Lung Lin et al., J. Electrochem. Soc. vol. 150, no. 5, p. C273-C276, 2003.

Chapter 2

Experimental

2.1 Materials

The chemicals, involving copper sulfate pentahydrate ($\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$), sulfuric acid (H_2SO_4 , 98%), hydrochloric acid (HCl, 36%) are all from Wako Pure Chemical Industries, Ltd., Japan. The additives for an electrodeposition were Janus Green B (Aldrich), Basic Blue 3 (Aldrich), Basic Red 12 (Hodogaya Chemical), NK-3212 (2-[(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-methyl]-1,3,3-trimethyl-3H-indolium perchlorate), NK-529 (2-[5-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1,3-pentadienyl]-1,3,3-trimethyl-3H-indolium iodide), NK-125 (2-[7-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1,3,5-heptatrienyl]-1,3,3-trimethyl-3H-indolium iodide) (Hayashibara Biochemical Laboratories Inc.) .

Structures of additives are shown in Fig. 2.1.

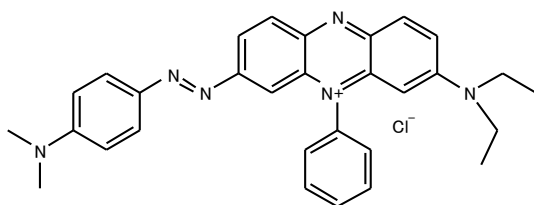
All the chemicals were used without further purifying, and all the solutions used in the experiments were prepared with 18 M Ω cm deionized water.

2.2 Electrochemical measurements

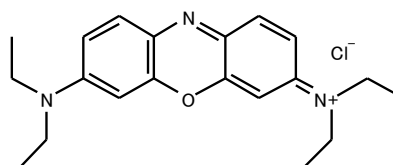
In section 3.2, the electrochemical measurement system (Model 100W type, BAS Inc.) and rotating disk electrode equipment (AFMSR type, PINE INSTRUMENT) shown in Fig. 2.2 were used. The working electrode was a platinum rotating disk electrode (ϕ 5 mm) for polarization curve measurements. It was plated with copper at 1.0 A/dm² for 2 min (about 400 nm thick) in the electrolyte before each measurement. A glassy carbon disk electrode (ϕ 3 mm) was used for cyclic-voltammetry of additive reactions. A platinum microelectrode (ϕ 15

μm) was used to determine the diffusion rate and the reaction rate of additives. The reference electrode was Ag/AgCl (saturated KCl) and the counter electrode was a platinum wire. The basic electrolyte composition included 0.30 mol/L CuSO_4 (Wako Chemical) and 1.8 mol/L H_2SO_4 (Wako Chemical) and 1.7×10^{-3} mol/L HCl (Wako Chemical). Janus Green B (Aldrich) and Basic Blue 3 (Aldrich) were used for additives. The electrolyte and experimental conditions are shown in Table 2.1.

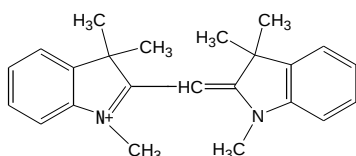
(a) Janus Green B



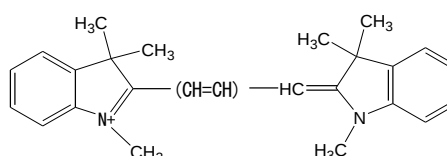
(b) Basic Blue 3



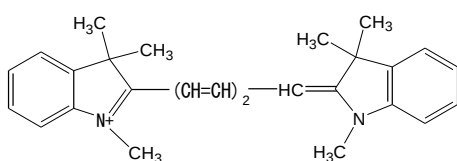
(c) NK-3212



(d) NK-529



(e) Basic Red 12



(f) NK-125

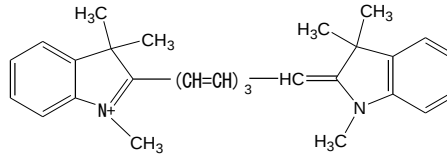


Fig. 2.1 Molecular formulas of additives.

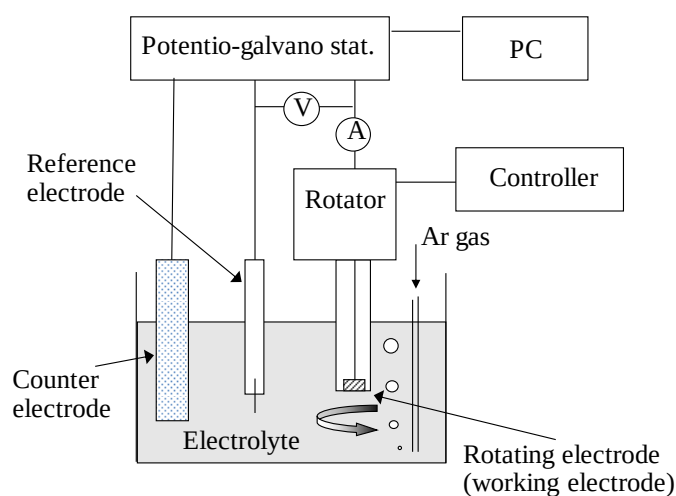


Fig. 2.2 Electrochemical measurement system.

Table 2.1 Electrodes and composition of electrolytes.

Working electrode		Cu ($\phi 5.0$ mm)	Glassy Carbon ($\phi 3.0$ mm)	Platinum ($\phi 15$ μ m)
Reference electrode		Ag AgCl satd. KCl		
Counter electrode		Platinum		
Concentration, $C / \text{mol L}^{-1}$	Copper sulfate	0.30	0	0
	Sulfuric acid	1.8	1.8	1.8
	Chloride ion	1.7×10^{-3}	0	0
	Additive	10 mg/L	2×10^{-3}	2×10^{-3}
Temperature, $T / ^\circ\text{C}$		24		
Scan rate, $v / \text{mV s}^{-1}$		0.5 or 2	10	10

An electrochemical measurement system (Model 100W type, BAS Inc.) and rotating disk electrode equipment (AFMSR type, PINE INSTRUMENT) were used for measuring the electrochemical characteristics of organic additives in a plating bath. The working electrode was a platinum rotating disk electrode ($\phi 5$ mm) for polarization curve measurements. It was plated with copper at 1.0 A/dm^2 for 2 min (about 400 nm thick) before each measurement.

The reference electrode was Ag/AgCl (saturated KCl) and the counter electrode was a platinum wire.

In chapter 5, electrochemical measurements were performed by using an electrochemical measurement system (Model 100W, BAS). Working electrode was polycrystalline Cu and Au disks ($\phi 1.6$ mm). A Ag/AgCl (saturated KCl) electrode and a Cu wire were used as a reference and a counter electrode, respectively.

2.3 Filling experiment

2.3.1 Substrate preparation

In section 3.2, a $\phi 200$ mm Si wafer with 1 μ m thick SiO₂ on which the trenches were formed was used for the substrate. A tantalum barrier layer was first deposited on the substrate to 50 nm thickness and then 150 nm thick Cu seed layer was deposited by sputtering.

Figure 2.3 (a) is a cross-sectional schematic representation of the type of trench used for this investigation in section 3.3. Trenches were fabricated in a SiO₂ dielectric layer by electron beam lithography and reactive ion etching (RIE). They were from 80 to 220 nm wide and 500 nm high. The Ta/TaN barrier and Cu seed layers were 10/10 and 60 nm thick, respectively. These layers were sputter deposited by long-throw sputtering in the same chamber. Figure 2.3 (b) is an SEM image of a trench with 80 nm width and 500 nm height before electroplating.

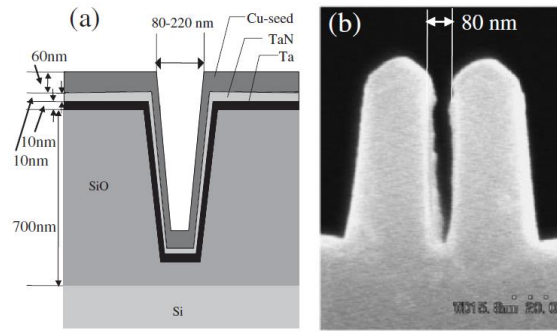


Fig. 2.3 Cross-sectional schematic representation of trench and SEM image of trench with 80nm width.

In section 3.4, trenches in a four-point probe geometry of 50-, 60-, 70-, 80-, 100-, 180- and 280-nm width and 300-nm height were patterned in silicon dioxide dielectric films using electron beam lithography and reactive ion etching. Figure 2.4 shows 50-nm and 80-nm-wide damascene trenches after ultrathin TaN/Ta (TaN: 7.5 nm; Ta: 7.5 nm) barriers and a 55-nm-thick Cu seed layer were sputter-deposited on trenches in that order. The thickness of the TaN/Ta barrier layer was estimated from the TEM images and was reduced to 5–8 nm (nominal 15 nm) due to sidewall shadowing during deposition in the Cu trenches.

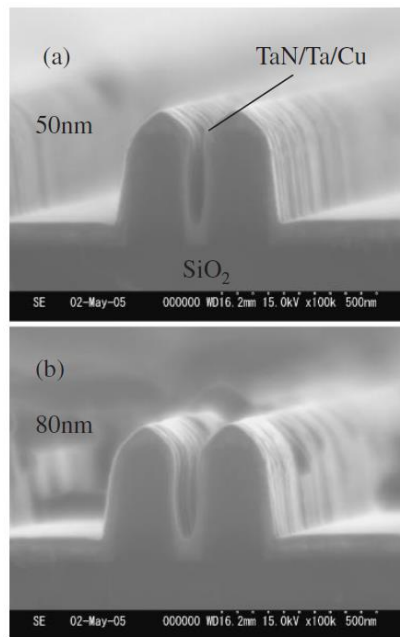


Fig. 2.4 SEM images of as-etched 50-nm and 80-nm-wide damascene trenches after ultrathin TaN/Ta (TaN: 7.5 nm; Ta: 7.5 nm) barriers and a 55-nm-thick Cu seed layer were sputter-deposited into trenches prior to electroplating.

In section 3.5, trenches in a four-point probe geometry of 50, 80, 100, 180, and 280 nm width with 180, 300, and 500 nm height were patterned in silicon dioxide dielectric films using electron-beam lithography and reactive ion etching. Ultrathin TaN/Ta (TaN: 10 nm; Ta: 10 nm) barriers and 60 nm thick Cu seed layer were sputter-deposited into trenches in that order.

In chapter 4, before electroplating, Ta/TaN layers up to 20 nm thick were deposited on the patterned wafer, and then a 150 nm Cu seed layer was deposited by physical vapor deposition. Fig. 2.5 schematically shows the patterned wafers that had a trench pattern 0.25 μm wide and 0.5 μm deep at a 0.5 μm pitch. The pattern regions are 100 μm wide and are separated by 5- μm -wide flat regions. The pattern regions consist of 0.25- μm -wide trenches. The Cu thickness at the sidewall of the pattern is about 20 nm due to the step coverage. The wafer was covered with masking tape to define a plated area of 10 mm x 20 mm. Current density was calculated by this plated area. The patterned area accounted for 91 % of the total plated area.

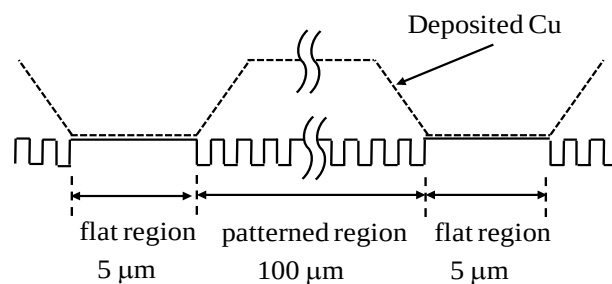


Fig. 2.5 Schematic representation of patterned wafer. Pattern region was 100 μm wide and had a series of 0.25 μm wide trenches. Cu thickness was measured at patterned region and flat region.

2.3.2 Electrochemical deposition conditions

In section 3.2, the substrate was plated at a constant current density 1.0 A/dm^2 for 20 seconds during which time the growth process of Cu in the trench in the solutions of $0.30 \text{ mol/dm}^3 \text{ CuSO}_4$, $1.8 \text{ mol/dm}^3 \text{ H}_2\text{SO}_4$ and $1.7 \times 10^{-3} \text{ mol/dm}^3 \text{ HCl}$ and additives. The additives, $20 \times 10^{-6} \text{ mol/dm}^3$ Janus Green B, $25 \times 10^{-6} \text{ mol/dm}^3$ Basic Red 12, $12 \times 10^{-6} \text{ mol/dm}^3 \text{ NK-3212}$, $12 \times 10^{-6} \text{ mol/dm}^3 \text{ NK-529}$, and $12 \times 10^{-6} \text{ mol/dm}^3 \text{ NK-125}$ were added in the electrolyte. A commercial additive for printed circuit boards (CC-1220, Japan Energy) is added to improve the Cu surface morphology. Copper which contained phosphorous was used for the anode.

In section 3.3, DC and pulse waves were used for Cu electroplating. The electrolyte used was Enthone's viaform. The electrolyte includes additives that have some inhibition effects before applying a voltage, and during plating, it is consumed in the plating reaction, leading to the loss of the inhibition effect [1]. Figure 2.6 shows pulse electroplating and DC electroplating conditions. DC density was fixed at 15 mA/cm^2 . In the case of the pulse wave, the application time of the peak current density (current-on) was fixed as 3 ms. The interval (current off) time and the peak current density were varied, as shown by the open circles in the table of Fig. 2.6 (b). During electroplating, the specimen was set on a rotating electrode, which moved at 1000 rpm.

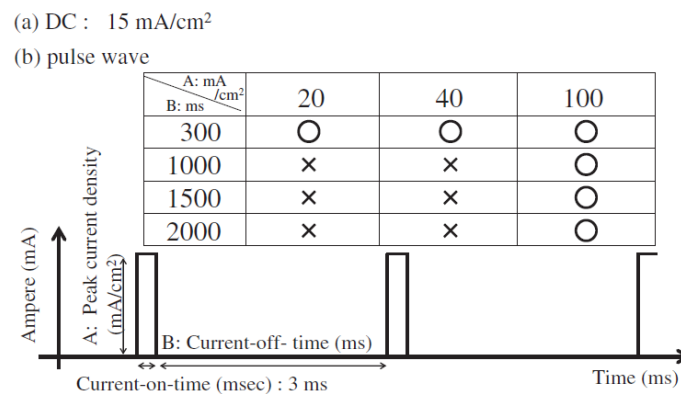


Fig. 2.6 DC electroplating and pulse electroplating conditions.

In section 3.4, the Cu interconnects were made by the DC electroplating process using a pure Cu electrolyte at room temperature with a current density of 5 mA/cm^2 . The bath compositions were composed of commercial $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$, HCl and H_2SO_4 solution with additives. After DC electroplating, the resulting fine-grained Cu film deposition was found to be under a high degree of intrinsic stress due to an excess of vacancies and dislocations [2]. This condition is unstable and this strain energy can only be remedied by recrystallisation. Thus, to expedite recrystallization of the electroplated Cu, these substrates were annealed at 400°C for 0.5 h in pure H_2 ambient and then subjected to chemical mechanical polishing (CMP) to remove excess Cu film from the trenches. The substrate-annealed pre-CMP had an overburden of Cu film with a thickness of 300 nm, i.e., the line height of the Cu trenches. The as-deposited Cu interconnects had a smaller grain size and a higher resistivity than those that were annealed. Thus, coarsening the grain size in the narrow Cu interconnects is very important to reducing the resistivity. After annealing, the grains are larger and the grain boundary scattering is smaller, reducing the resistivity of the Cu interconnects. However, the coarsening of the Cu grains may be restricted by the sidewalls of very narrow trenches [3].

In section 3.5, the Cu interconnects were made by the DC electroplating process using a pure Cu electrolyte at room temperature with a current density of $1\text{--}5 \text{ mA/cm}^2$. The bath compositions were consisted of $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$, HCl, and H_2SO_4 solution with additives. After DC electroplating, the substrates were annealed at 400°C for 0.5 h in H_2 ambient, followed by a chemical mechanical polishing (CMP) to remove the excess Cu and Ta/TaN layers from the trenches. The substrates annealed pre-CMP consisted of an overburden Cu film with a thickness as same as the line height of the Cu trenches. The electrical resistance in the Cu interconnects were measured by the four-probe method.

In chapter 4, Cu was deposited at the current density range 0.5-1.5 A/dm² for 6.7-20 min. All experiments were performed at no solution agitation. The specimens were immersed for 1 min. in the electrolyte before electroplating. It was found that the immersion time affected the shapes of deposited Cu. Sufficient immersion time over 1 min. was needed to obtain reproducible results. The conditions of agitation during plating and immersion before plating were constant and are not discussed in detail. Cu plate was used for the anode. HCl was added to improve Cu anode dissolution and form a uniform and adherent anode film [4].

2.4 Characterization of deposits

In section 3.2, Cross-sectioned Cu images were taken with a scanning electron microscope (S-900, Hitachi).

In section 3.3, the cross-sectional microstructures of Cu in the trenches after electroplating were evaluated using a scanning electron microscope (SEM) and a transmission electron microscope (TEM). Samples for the TEM observation were fabricated using a focused ion beam (FIB) system.

In section 3.4, To clarify the grain sizes and their distributions inside the Cu interconnects with line widths of 50 nm, the cross-sectional microstructures in the longitudinal direction of the Cu wires was investigated using a focused ion beam (FIB) instrument (Hitachi FB-2000A) [5]. Before FIB milling, 100- nm-thick carbon films were evaporated onto the samples to protect the Cu wires from damage during milling. Ga ion beams accelerated at 30 kV were rastered long the Cu wires to cut holes on both sides precisely at the object portion. The resulting freestanding Cu films were placed into a field emission transmission electron microscope (FETEM) to observe the longitudinal

microstructures. The observed Cu interconnect wires were about 4- μm long with a thickness of approximately 40 - 50 nm.

In section 3.5, As-deposited Cu interconnects have a smaller grain size and a higher resistivity. After annealing, the grain size grows and the effect of grain boundary scattering on the resistivity is reduced, resulting in the reduction of the resistivity of Cu interconnects. However, the coarsening of the Cu grains may be restricted by the sidewall of a very narrow trench. In order to clarify the actual grain sizes and their distributions inside the Cu interconnects for line widths less than 100 nm, it was necessary to investigate the cross-sectional microstructures in the longitudinal direction of the Cu wires by using a FIB instrument (Hitachi FB-2000A) [5]. Before FIB milling, 100 nm thick carbon films were evaporated onto the samples to protect the Cu lines from damage during milling. Ga ion beams accelerated at 30 kV were rastered along the Cu lines to cut holes on both sides at the precise object portion. The resulting free-standing Cu films were placed into an FETEM to observe the longitudinal microstructures.

In chapter 4, Plated Cu was evaluated with a scanning electron micrograph (SEM). Cu thickness was measured as a distance between flat surface and the top of the plated Cu in the cross-sectioned images.

2.5 Simulation method

The Laplace equation for potential in the Cu electroplating bath was coupled with the diffusion equation for both the concentration of cupric ion ($=C$) and the concentration of an additive ($=G$) as shown in Fig. 2.7. These were solved by the boundary element method. Then the current density distribution on the Cu surface was calculated and the form of the Cu film was predicted. The boundary moves according to the current distribution given by a

string model. The boundary condition of G in the diffusion equation of the additive on the Cu surface is

$$D \frac{dG}{dn} = k \Theta G \quad (2-1)$$

where D , n , k , and Θ are the diffusion coefficient of the additive, position vector normal to the surface, the consumption rate constant of additive on the Cu surface, and the surface coverage of the additive, respectively. This equation is balanced between the incident flux of an additive and the consumption rate over the unit area. The D/k value determines the distribution of an additive concentration in the trench. Therefore, the D/k value influences the bottom-up filling profile. All the parameters used in the present method were determined by electrochemical measurements.

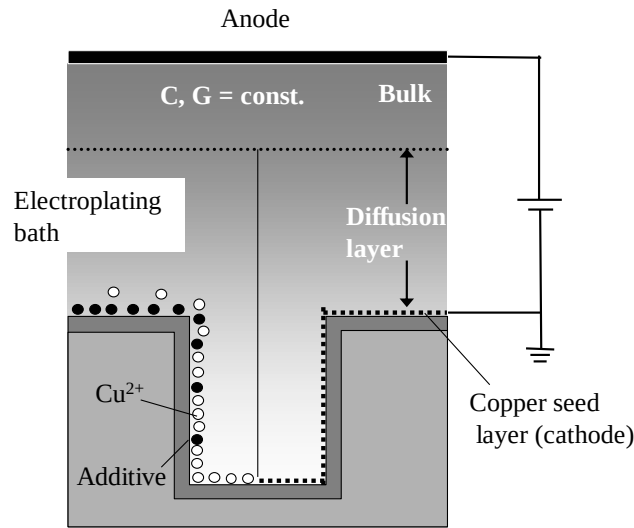


Fig. 2.7 Model of bottom-up filling: additives adsorb on Cu surface and inhibit crystal growth (Ψ , potential; C , Cu^{2+} concentration; G , additive concentration)

List of Symbols

D	diffusion coefficient of the additive, m^2/s
$\mathbf{n}$	position vector normal to the surface
k	reaction rate of additive on the Cu surface
k_0	reaction rate of additive on the Cu surface at standard condition
θ	additive coverage on the Cu surface
G	additive concentration, mol/m^3
C	Cu concentration, mol/m^3
i	current, A
F	Faraday's constant, C/mol
A	electrode area, m^2
ϕ	overpotential, V
b	constant
n	electrons transferred
i_{lim}	diffusion limiting current, A
a	electrode radius of microelectrode, m

2.6 In situ SERS measurements

The Cu-working electrode for SERS measurement was prepared by electrodepositing Cu in a 0.3 M CuSO_4 solution at -0.3 V for 100 s on a polycrystalline Au electrode, which was electrochemically roughened by oxidation/reduction cycles between -0.75 and + 1.05 V with the scan rate of 1 V/s in a 0.1 M KCl solution for 2 hr. A Pt wire was used as a counter electrode in the in situ SERS measurement. A home-built inverted Raman microscope system was used to observe Raman signals [6]. The working electrode was illuminated through an objective lens (40x, 0.6 N.A.) by 632.8 nm radiation from a He-Ne laser (0.02 mW), and backscattered Raman signals were collected with the same objective lens and monitored by a CCD-polychromator system (PIXIS 400B, Princeton Instruments) after Rayleigh scattering light was filtered by an edge filter (LP02-633-RU, Semrock). Potential dependent SERS spectra were obtained with the acquisition time of 10 s during the continuous potential sweep

with a scan rate of 1 mV/s. The observed Raman spectra were compared with the results of density functional calculations using GAUSSIAN 03 Revision E01 at the B3LYP level with 6-31G** basis set.

References

- [1] T. Haba, T. Itabashi, H. Akahoshi, A. Sano, K. Kobayashi and H. Miyazaki: Mater. Trans., JIM vol. 43 p. 1593, 2002
- [2] T. Ritzdorf, L. Graham, S. Jin, C. Mu and D. Fraser: IEEE Proc. Int'l Interconnect Tech. Conf., p. 106–108, 1998.
- [3] K. P. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, T. Tobita, M. Chiba, T. Saito and K. Ishikawa: Advanced Metallization Conference, Tokyo, September (2006) 58.
- [4] M. Lefebvre, G. Allardyce, M. Seita, H. Tsuchida, M. Kusaka, and S. Hayashi, Circuit World, vol. 29(2), p. 9, 2003.
- [5] K. P. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, T. Tobita M. Chiba, T. Saito and K. Ishikawa: Jpn. J. Appl. Phys. Vol. 45, L852–L853, 2006
- [6] K. Ikeda, N. Fujimoto, H. Uehara, K. Uosaki, Chem. Phys. Lett. Vol. 460 p. 205, 2008.

Chapter 3

Anisotropic Deposition of Copper to Fill Trenches and Vias

3.1 Introduction

The damascene process developed by IBM Corporation in 1998 enabled application of copper interconnection in LSI devices. In the damascene process, it is necessary to fill trenches and vias formed in the substrate with copper. Electrochemical copper deposition is a powerful technique that can grow copper preferentially from the bottom of a feature. As the demand for downsizing LSI technology increases year by year, finer interconnection is also required with copper deposition technology. For such interconnects with a width below 100 nm, the crystal size of copper is limited to the line width, and there is a possibility of increased electrical resistance.

This chapter investigates the mechanism of copper anisotropic growth in fine features and the characteristics of the deposited copper. Specifically, section 3.2 examines the mechanism of anisotropic copper deposition in features by using an inhibiting additive. Then, section 3.3 explains the proposed filling method for a trench with a width of 100 nm or less, which works by controlling the current waveform in a solution containing the additive. The characteristics of the deposited copper are also evaluated. Finally, section 3.4 investigates the grain size in a 50-nm-wide copper interconnect formed by electrodeposition.

3.2 Trench filling mechanisms in the copper damascene electroplating process

Electroplating offers an excellent filling capability and is the most attractive process for copper wiring. Typically, copper electroplating baths which were sulfuric acid-based contain some additives to facilitate filling of sub-micrometer trenches and to improve deposit properties. There are various classes of additives, brighteners (or accelerators), carriers (or suppressors or polymers), and levelers. Typical acid-based copper electroplating baths contain two or three organic additive components. They are accelerators (or brighteners), suppressors (or carriers or polymers), and levelers (or weak suppressors). A typical accelerator is bis (3-sulfopropyl) disulfide. A typical suppressor is polyethylene glycol or polypropylene glycol. The proper concentration of each additive optimizing the plating conditions results in a higher deposition rate at the bottom of the feature, which is called “bottom-up filling”. The bottom-up filling effect requires the use of at least two organic additive components such as accelerators and suppressors [1]. Curvature enhanced accelerator coverage model developed by Moffat and Josell have been accepted to explain the bottom-up filling mechanism [2, 3, 4]. The typical third component of additives is a leveler. The leveler is a weak suppressor. The main role of the leveler is to mitigate momentum plating after the trench is filled. On the other hand, some substances used as the leveler effect the trench filling profile [5, 6, 7, 8]. Andricacos et al. propose the bottom-up filling model by additives [9]. This model is due to depletion of inhibitor at the bottom of the trench. The filling capability of the plating bath is important in fabricating copper interconnects without voids. The minimum wiring pitch continues to scale to ever finer dimensions in the coming generation. It is becoming more difficult to fill trenches without voids. So it is important to find organic additives that have a good filling capability. Finding a new leveler substance for improving a filling capability is one of the methods to fill fine features.

In this section, the bottom-up filling model which was confirmed using experimental and numerical simulation results was proposed. Then, the electrochemical characteristics and trench filling profiles of some organic molecules was investigated to find new additives suitable for the Cu damascene electroplating process.

Some models for bottom-up filling have been reported [10, 11, 12, 13, 14]. They can be divided into two types. In one type, the additive has a promotional effect on copper deposition and it is concentrated in the bottom of the trench. In the other, the additive has an inhibition effect on copper deposition and deposition reaction is diffusion-controlled. If additives react electrochemically on the copper surface, the diffusion coefficient and the reaction rate constant of the additives can be evaluated by using electrochemical measurements. When the additive is consumed on the copper surface, a concentration gradient of the additive due to its diffusion is formed. If this concentration gradient is maintained steadily, the concentration of additives at the bottom of the trench drops. This leads to a decrease in the inhibition effect on copper deposition at the bottom of the trench. Therefore, the deposition rate at the bottom of the trench becomes higher than that at the top and bottom-up filling is realized.

3.2.1 Electrochemical Characteristics of Additives

Based on our model, additives must have some characteristics to realize bottom-up filling. 1) It must have an inhibition effect of the plating reaction. It must be adsorbed on a copper surface and include atoms, such as sulfur, nitrogen and so on. 2) It must be consumed in the plating reaction which means the inhibition effect is lost. Two candidate additives, Janus Green B which was to have an effect on bottom-up filling was selected [15, 16] and Basic Blue 3. It has some functional groups that are the same as Janus Green B.

(1) Inhibition effect on the plating reaction

Figure 3.1 shows the current-potential curves for the electroplating bath with and without additives. When potential was scanned from the rest potential in the negative direction, reduction current due to the copper deposition began to flow. In the positive potential region from -100 mV, reduction current in the plating bath that contained Basic Blue 3 or Janus Green B was small compared to the value when the bath contained no additive. These compounds inhibited a deposition of copper in this potential region. There was a difference in the inhibition effect between Basic Blue 3 and Janus Green B. It was thought that the inhibition effect reflected the adsorption condition and the amount of adsorption of each additive.

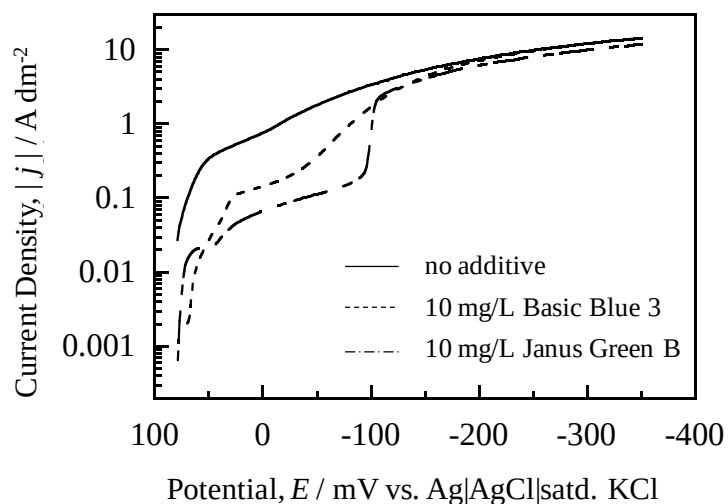


Fig. 3.1 Polarization curves for the electroplating bath with and without additives: 24 °C, scan rate 0.5 mV/s, 1000 rpm.

(2) Consumption on the Cu surface

Consumption of the additive on the copper surface was evaluated by an electrochemical method. It was assumed that additives lost their inhibition effect on the plating reaction when they were electrochemically reduced. Figure 3.2 shows cyclic voltammograms measured in sulfuric acid that contained Basic Blue 3 or Janus Green B. A one-step reduction peak was observed for the Basic Blue 3 containing solution and a two-step peak was observed for the Janus Green B one. This meant that Basic Blue 3 and Janus Green B were reduced electrochemically in acidic solution.

Basic Blue 3 and Janus Green B both had an inhibition effect on the plating reaction and they were consumed on the copper surface. Therefore, both Basic Blue 3 and Janus Green B were thought to possibly have the characteristics required for bottom-up filling.

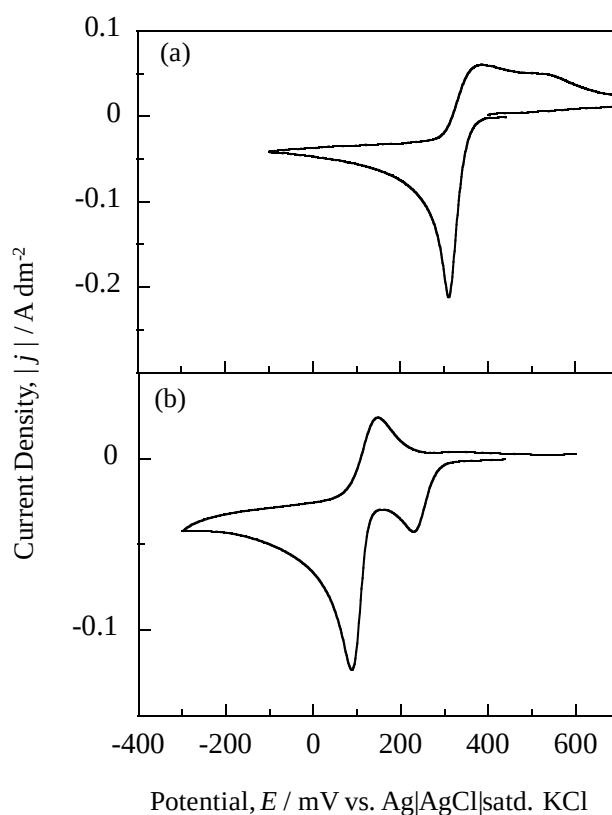


Fig. 3.2 Cyclic voltammograms of 1.8 mol/L sulfuric acid on the glassy carbon electrode (a) with 2×10^{-3} mol/L Basic Blue 3 (b) 2×10^{-3} mol/L Janus Green B: scan rate 50 mV/s.

3.2.2 Filling capability

Figure 3.3 shows cross-sectional SEM images of partially filled 0.25 μm wide trenches prepared in baths containing no additive, Basic Blue 3 and Janus Green B. Copper grew uniformly using the baths with no additive and Basic Blue 3. On the other hand, copper grew preferentially from the bottom of the trench using the bath containing Janus Green B. Janus Green B resulted in bottom-up filling. Bottom-up filling was expected for both additives from characteristics discussed above. However, conformal growth was observed for addition of Basic Blue 3 under the present plating conditions. It was thought this might be explained as follows. Each additive had the required characteristics qualitatively. The difference in filling capability depended on whether the concentration gradient of the additive was maintained properly in the trench. The balance between the supply of the additive by diffusion and the consumption of the additive by the reaction on the copper surface was inappropriate in the bath which contained Basic Blue 3.

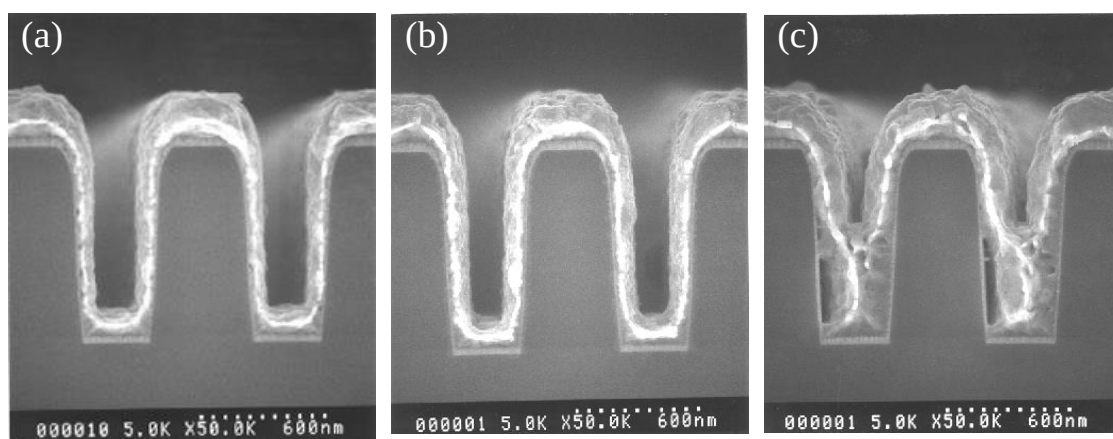


Fig. 3.3 SEM cross-sectional views showing the effect of additives (a) no additive (b) 10 mg/L Basic Blue 3 (c) 10 mg/L Janus Green B.

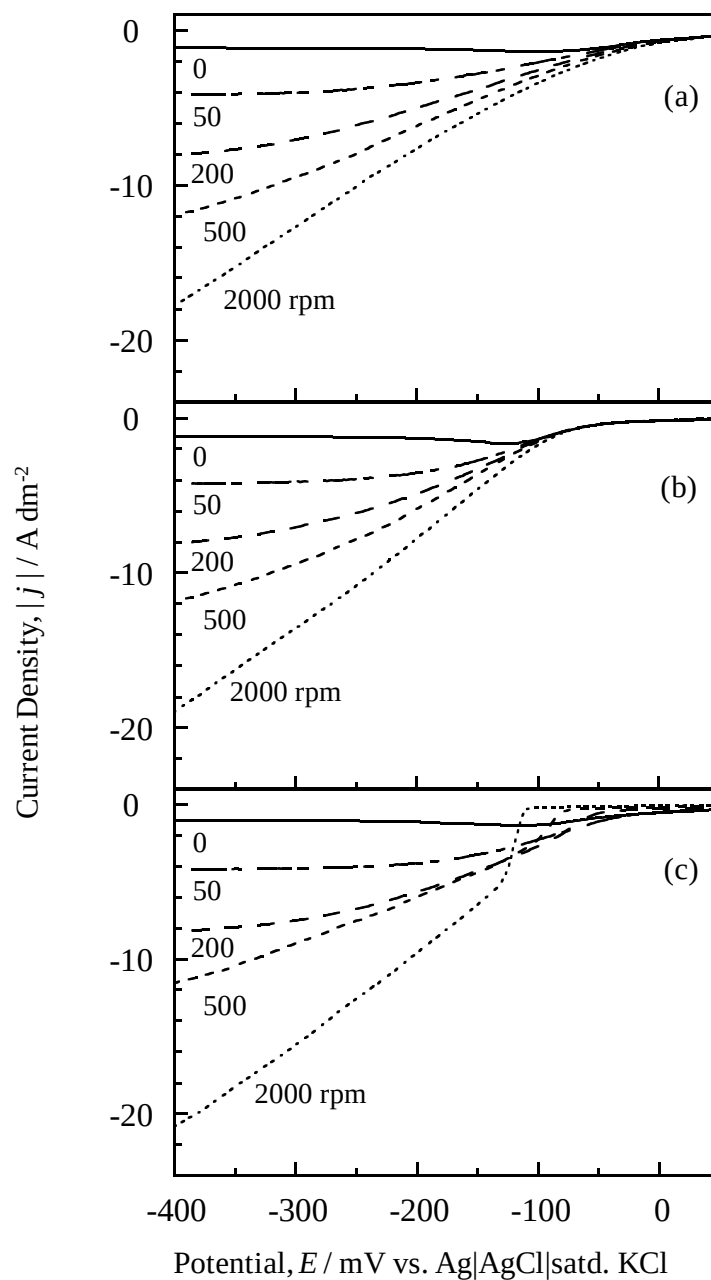


Fig. 3.4 Polarization curves for the electroplating bath (a) no additive (b) with 10 mg/L Basic Blue 3 (c) with 10 mg/L Janus Green B: 24 °C, scan rate 2 mV/s.

The diffusion of additives in plating baths was investigated using a rotating disk electrode. Figure 3.4 shows the current-potential curves of the copper deposition while changing the rotation speed of the electrode from 0 rpm to 2000 rpm. The deposition current

increased with the increase in the rotation speed of the electrode in the bath that contained no additive. When the diffusion layer on the surface of the electrode became thin, the supply rate of cupric ion to the copper surface increased. The deposition current in the bath containing Basic Blue 3 also increased with the increase of rotation speed. On the other hand, in the plating bath containing Janus Green B, the deposition current decreased with the increase of rotation speed in the potential range from 100 mV to -120 mV. This was because the decrease in the current due to the inhibition effect of additives became larger than the increase in the current due to the increase in the supply rate of cupric ion. The inhibition effect of each additive was different though they had the same functional groups and similar characteristics would be expected.

3.2.3 Simulations

The model was confirmed by the comparison with results from experiments and numerical simulations and the difference between Basic Blue 3 and Janus Green B was explained quantitatively. The concentration distribution of the additive in the trench was influenced by a balance between the diffusion coefficient, D and the reaction rate constant, k . As mentioned above, D and k are important parameters for bottom-up filling. These parameters were determined by electrochemical methods.

3.2.3.1 Experimental determinations of the parameters for simulations

(a) Reaction rate constant of additives, k

The current-potential curves of additives in sulfuric acid were measured using the microelectrode. The reaction rate constant of additives on the copper surface k was calculated

from the slope of the current-potential curves. If the charge transfer reaction is the rate determining step, the current against the overpotential ϕ is given by [17]

$$i = n F G A k = n F G A k_0 \exp(\phi/b) \quad (3-1)$$

where i , current; F , Faraday constant; A , electrode area; k_0 , standard rate constant of additive on the copper surface.

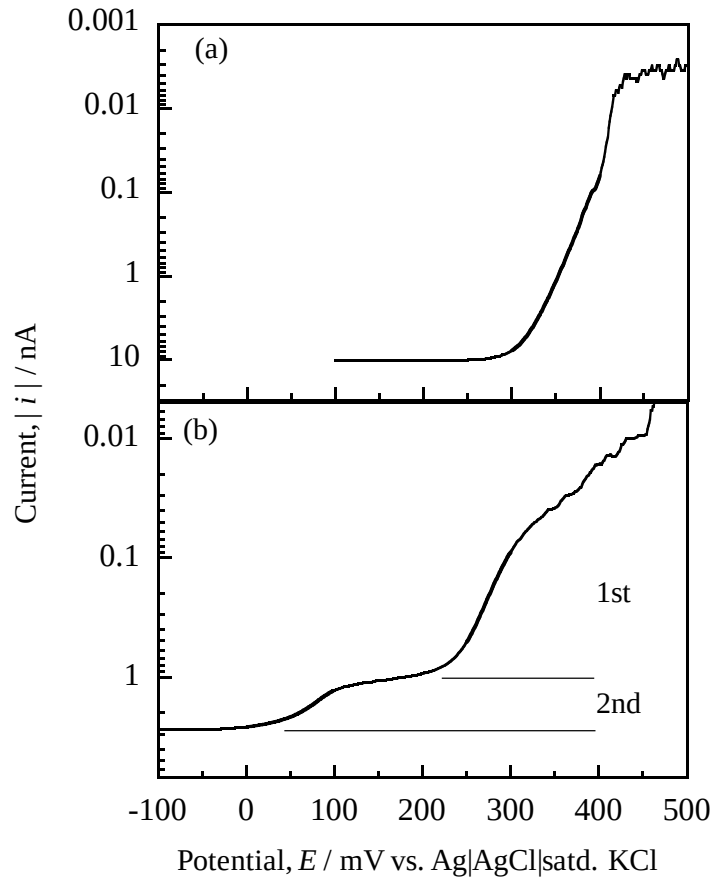


Fig. 3.5 Polarization curves for 1.8 mol/L sulfuric acid on the platinum microelectrode (a) with 2×10^{-3} mol/L Basic Blue 3 (b) 2×10^{-3} mol/L Janus Green B.

Figure 3.5(a) shows the current-potential curve of Basic Blue 3 in the sulfuric acid solution. The slope of the straight part of the curve gave, $i = 8.8 \times 10^{-1} \exp(-59 \phi)$. When $G = 2 \text{ mol m}^{-3}$ and $A = 1.8 \times 10^{-10} \text{ m}^2$ was substituted in Eq. 2 and $n = 1$ was assumed; k_0 for Basic Blue 3 was $2.6 \times 10^4 \text{ m/s}$. The overpotential ϕ was $-8.1 \times 10^{-2} \text{ V}$ from Fig. 3.4 when the plating current density was 1.0 A/dm^2 . The reaction rate constant of Basic Blue 3 k_a was $3.1 \times 10^6 \text{ m/s}$.

Figure 3.5(b) shows the current-potential curve of Janus Green B. Janus Green B reacted in two steps. The second step was considered the rate determining step from the slope of the curve. The k value was calculated for the second step and at 1.0 A/dm^2 , k_b was $1.8 \times 10^{-4} \text{ m/s}$.

(b) Diffusion coefficient of additives: D

The diffusion coefficient of additives was calculated from the diffusion limiting current of current-potential curves. The diffusion coefficient D is given by [18]

$$D = i_{lim} / (4 n F G a) \quad (3-2)$$

where i_{lim} , the diffusion limiting current, a , electrode radius.

The diffusion limiting currents are also shown in Fig. 3.5. The diffusion limiting current in the Basic Blue 3 containing solution was $1.0 \times 10^{-8} \text{ A}$. The diffusion limiting current in the Janus Green B containing solution was $1.7 \times 10^{-9} \text{ A}$ for the second-step reaction. Therefore, the diffusion coefficient of Basic Blue 3 and Janus Green B were $1.7 \times 10^{-9} \text{ m}^2/\text{s}$ and $2.9 \times 10^{-10} \text{ m}^2/\text{s}$ respectively.

3.2.3.2 Comparison of experimental and simulation results

Figure 3.6 shows trench filling profiles obtained by simulations and experiments. The experimental profiles were in good agreement with calculated profiles. For Basic Blue 3, copper thickness was equal at all points of the trench for both experiment and simulation. For Janus Green B, copper grew preferentially at the bottom of the trench. This suggested our model was reasonable.

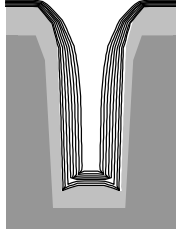
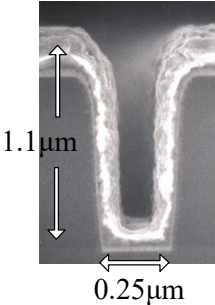
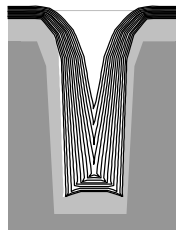
simulation	experiment	additive
		Basic Blue 3 <i>Conformal</i>
		Janus Green B <i>Bottom-up filling</i>

Fig. 3.6 Comparison of filling profiles between experiments and simulations.

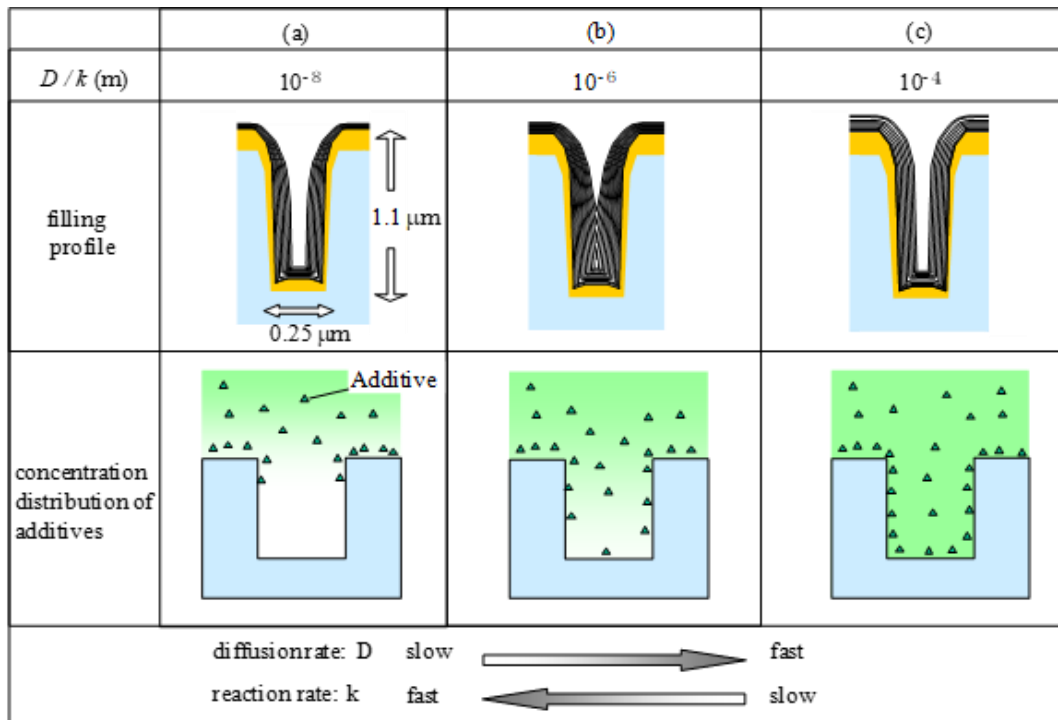


Fig. 3.7 Predicted filling profiles and the concentration distribution of additives in the trench against D/k .

Figure 3.7 shows the predicted filling profiles and the distribution of the additives in a trench against D/k value. Filling profiles changed with D/k value.

Case (a) The D/k value was too small for bottom-up filling. The distribution of the additive concentration was uniform. This was because the reaction rate of additive was so fast relative to the diffusion rate of additive that almost all additives were consumed around the top of a trench. The filling profile of the bath without additive was the same as that with additive.

Case (b) D/k value was suitable for bottom-up filling. The diffusion rate and the reaction rate of the additive were in the appropriate range. In this case, the reaction of additives was diffusion-controlled and the concentration gradient of additives along the trench was formed. The concentration of the additive decreased toward the bottom of the

trench, and because of this decreases, the inhibition effect on the copper deposition at the bottom dropped. Therefore, preferential growth from the bottom of the trench was realized.

Case (c) D/k value was too large for bottom-up filling. A large D/k value meant that the reaction rate of additives was slow and the diffusion rate was fast. In this situation, the concentration of additives in the trench was high and had less concentration gradient. Therefore, the filling profile was conformal.

The D/k values for Basic Blue 3 and Janus Green B was 1.8×10^{-16} and 1.8×10^{-6} , respectively. Thus, Janus Green B fit case (b) and had a suitable D/k value for bottom-up filling. Basic Blue 3 fit case (a) and its D/k value was too small. We concluded for bottom-up filling to occur, the diffusion rate and the reaction rate of the additive must be in appropriate ranges. The filling profiles of the trench would be predicted by calculating the D/k value.

3.2.4 New leveler materials for improving a filling capability

Some dyes, Basic Red 12, NK-3212, NK-529, NK-125 were selected for the leveler that were expected to inhibit copper deposition. These levelers were investigated by electrochemical and filling experiments. According to the filling model with a leveler, the leveler is required to have an inhibiting effect on the copper deposition reaction, simultaneous with consuming properties. The balance between the supply rate to the surface by diffusion and the consumption rate on the surface of the levelers is important to the filling property.

First, we investigated the inhibition effect of the levelers on the plating reaction using the polarization measurements. Figure 3.8 shows the current-potential curves for the electroplating bath with Basic Blue 3, Janus Green B, Basic Red 12 and no levelers. The negative current associated with copper deposition was observed. The negative current in the plating bath that contained levelers was small compared to the current in the bath with no

leveler. This means these levelers inhibit the deposition of copper. There was a difference in the inhibition effect of Basic Blue 3, Janus Green B and Basic Red 12. Basic Red 12 had a strongest inhibition effect. The current in the bath with Basic Red 12 at -100 mV was ten-thousandth part of that in the bath without leveler. This difference reflects the adsorption condition and the amount of adsorption of each leveler.

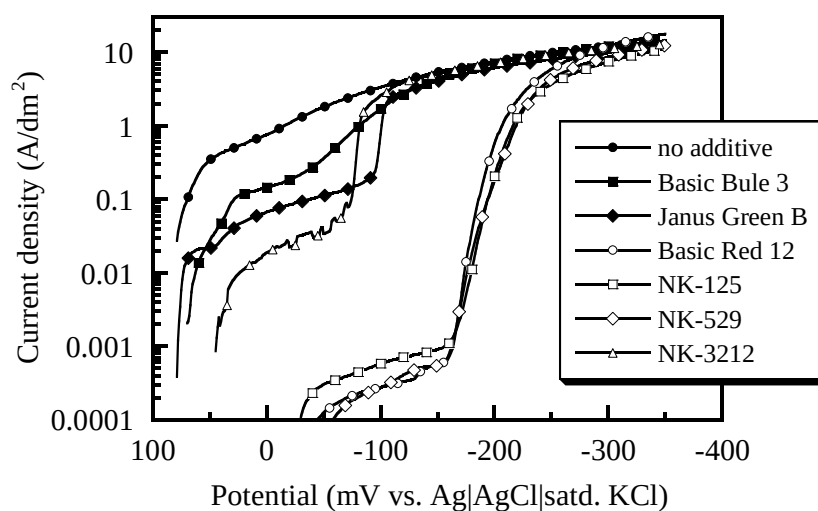


Fig. 3.8 Polarization curves for the electroplating bath: scan rate of 0.5 mV/s, rotation speed of 1000 rpm (a) no additive (b) Basic Blue 3 (c) Janus Green B (d) Basic Red 12.

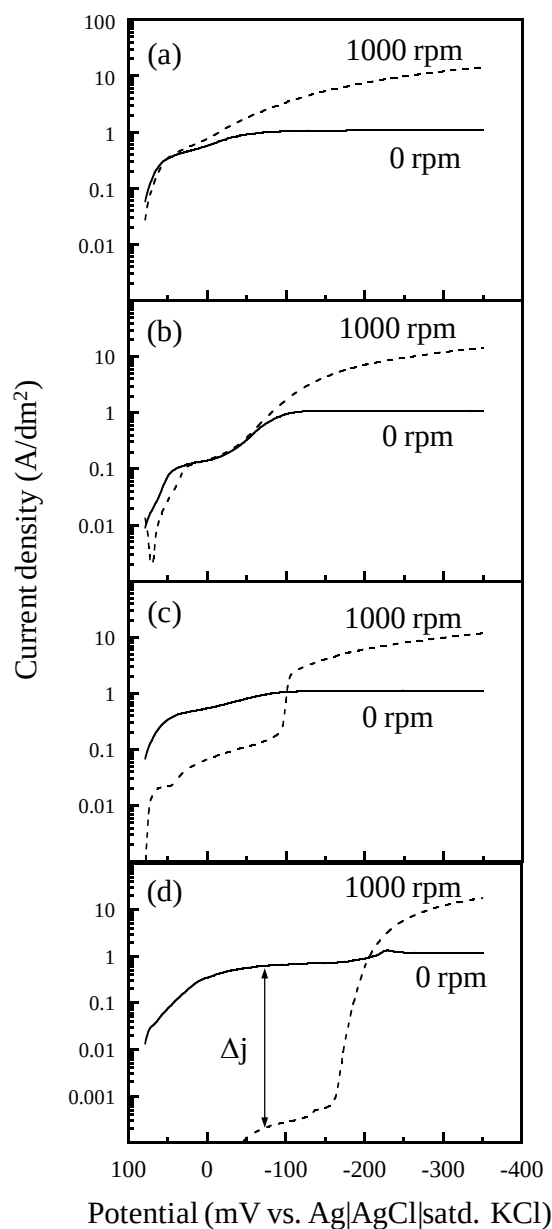


Fig. 3.9 Polarization curves for the electroplating bath: temperature 24 °C, scan rate of 0.5 mV/s, rotation speed of 1000 rpm.

Secondly, we investigated the effect of supply rate of the levelers to the copper surface with electrochemical measurements using the rotating disk electrode. The rotating disk electrode is one of the best methods for controlling the supply rate of materials on the electrode surface. Figure 3.9 shows the polarization curves of the copper deposition while changing the rotation speed of the electrode from 0 rpm and 1000 rpm with and without

levelers. The copper deposition current increased with the increase in the electrode rotation speed in the plating baths that contained Basic Blue 3 and no levelers. In contrast, the deposition current decreased with the increase in rotation speed over the specific potential range in the plating baths containing Janus Green B and Basic Red 12. This was because the current decrease due to the inhibition effect of levelers became larger than the current increase due to the increase in the supply rate of Cu^{2+} to the electrode surface. It showed that the inhibition effect of Janus Green B and Basic Red 12 changed according to the amount supplied to the electrode surface.

The trench filling profiles for each leveler were investigated. Figure 3.10 shows the cross-sectional SEM images of the partially filled 500 nm-wide trenches after electroplating at 1.0 A/dm^2 for 20 seconds. The copper grew uniformly using baths that contained commercial additive without levelers. In this plating condition, the commercial additive doesn't improve the filling capability. In the bath that contained Basic Blue 3, copper grew uniformly as in the case of that without levelers. However, it grew preferentially from the bottom of the trench using baths that contained Janus Green B or Basic Red 12.

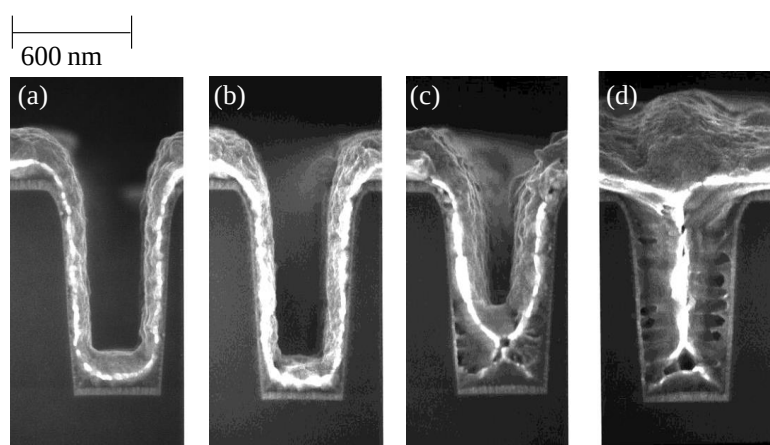


Fig. 3.10 SEM cross-sectional views showing the effect of additives for filling profiles: (a) without leveler (b) Basic Blue 3 (c) Janus Green B (d) Basic Red 12.

Figure 3.11 shows the correlation between the current density ratio R_i and the plated Cu thickness ratio R_t using levelers in the plating baths. R_i is the current density ratio at the potential at which Δj becomes the biggest. Δj is the difference of current density in the polarization curves between 0 rpm and 1000 rpm. R_t is the ratio of the plated copper thickness at the bottom of the trench against the sidewall. Preferential growth rate of copper from the bottom of the trench increased as R_t increased. Levelers that had a large R_i value were suitable for trench filling. This indicates that the electrochemical characteristics of the levelers affected the filling capability. The capability of improving bottom-up filling for the leveler relate to the current decrease with the increasing the supply rate of the leveler to the surface. Strong inhibition effect change of leveler is effective in improving the filling capability in the presence of accelerator and suppressor. This shows that some leveler has a possibility to improve the filling capability of the bath by adding those to a general two additive components.

3.2.5 Conclusions

The role of additives in the copper electroplating bath and the effects of the electrochemical characteristic of additives to improve the trench filling capability in the damascene process has been investigated. We proposed a bottom-up filling model with leveler additives. Filling profiles change with characteristics of additives. The continuous concentration gradient of the additive in the sub-micron trench was necessary to achieve bottom-up filling. There was a suitable balance between the diffusion rate and the reaction rate of the additive on the copper surface. We estimated the filling profile by numerical simulation using parameters that were electrochemically determined. The predicted filling profiles agreed very well with the experimental results. This suggested that the diffusion

coefficient and reaction rate constant of an additive played important roles in bottom-up filling and that our model was reasonable. An electrochemical measurement with a rotating disk electrode is an effective tool for evaluating the filling capability of additives. Using some substances, we observed that the Cu deposition current decreased with increasing rotation speed of electrode over a specific potential range. The quantity of the current decrease is closely related to the trench filling capability. This electrochemical behavior of the additives could be a useful guideline when searching for new levelers to improve the filling capability.

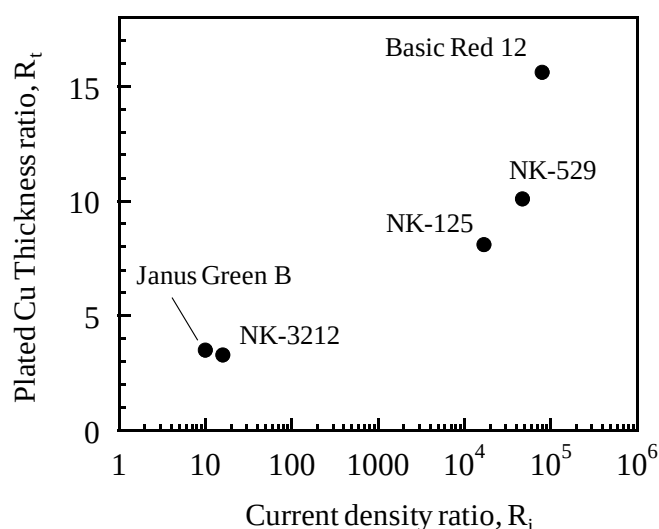


Fig. 3.11 Correlation between electrochemical characteristics and filling profiles, where R_i is the current density ratio at the potential at which Δj becomes the biggest; Δj is the difference of current density in the current-potential curves between 0 rpm and 1000 rpm; R_t is the ratio of the plated copper thickness at the bottom of the trench versus that on the sidewall.

3.3 Trench filling with high-aspect-ratio trench using pulse wave Cu electroplating

Cu is used as an interconnect material for high-performance ultra-large scale integration (ULSI) circuits. Cu offers advantages of low electrical resistivity and high reliability [19]. The dual damascene process is widely used for Cu wiring. In this process, Cu wiring is fabricated by repeatedly burying Cu in narrow trenches followed by chemical mechanical polishing (CMP). Electroplating is a mainstream method of fabricating Cu interconnections in trenches [20]. Electroplating, in comparison with electroless plating, can provide a higher deposition as well as enable the use of electroplating solutions for copper deposition that is more stable and easier to control.

However, unexpected phenomena have occurred in Cu interconnects of less than 100 nm. The resistivity of Cu wires increases substantially with decreasing wiring width. This is attributed to the wiring width being comparable to the mean free path of an electron (39 nm), which causes electron scattering to increase at the surface, sidewall, and grain boundaries of the Cu wires. In addition, the effect of high resistivity barrier metals on the resistance increase of wires multiplies as their size is reduced [21, 22]. Electromigration (EM) and stress-induced migration (SM) resistances in Cu wires are also degraded with reduced wiring size. There are two reasons for this: voids are very difficult to avoid when dealing with very narrow trenches with high aspect ratios, and also, grains in the trenches are very fine. Hence, the development of processes for Cu filling with no voids and with a larger grain size by electroplating is, therefore, essential for producing Cu wiring with a low resistivity and high reliability [23-24].

Furthermore, the quality of Cu wires made by electroplating is strongly dependent on additives in the plating bath and on electric current conditions.

In this section, we investigated the influence of electroplating-conditions when using pulse waves on the bottom-up filling of high-aspect-ratio trenches of 80 nm width. Then, we

investigated trench microstructures to compare the quality of these Cu wires with Cu wires formed by conventional DC plating.

3.3.1 Filling capability with a direct current plating and a pulse wave plating

Figure 3.12 shows cross-sectional SEM images of partially filled 200-nm-wide trenches prepared by (a) DC electroplating and (b) pulse electroplating. For DC electroplating, Cu grew uniformly in the trench, as shown in Fig. 3.12 (a). On the other hand, Cu grew from the bottom of the trench preferentially during pulse wave electroplating, as shown in Fig. 3.12 (b). We see that pulse wave electroplating is more efficient for bottom-up filling than DC plating. Hence, we investigated the influence of pulse wave plating conditions on Cu-filling characteristics in the trench.

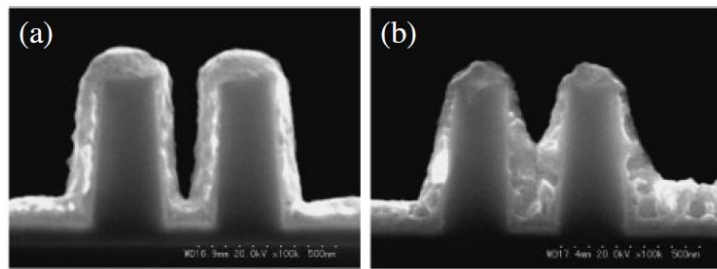


Fig. 3.12 Cross-sectional SEM images of partially filled 200-nm-wide trenches prepared by (a) DC electroplating (15 mA/cm^2) and (b) pulse electroplating (100 mA/cm^2).

We defined the bottom-up rate using a partially filled trench, as shown in Fig. 3.13, to evaluate the effect of pulse wave conditions on the bottom-up filling characteristics quantitatively. A line along the trench and a line along the surface of the Cu film were drawn, and the angle between them was measured as a function of the Cu line width. This value was defined as the bottom-up rate. Hence the bottom-up rate is almost zero when Cu is plated almost uniformly in the trench and, it becomes high when the bottom-up preferential growth becomes dominant.

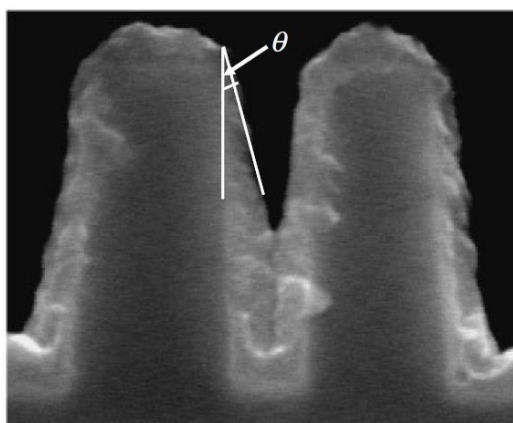


Fig. 3.13 The bottom-up filling rate definition.

Figure 3.14 shows cross-sectional SEM images of trenches partially filled by pulse wave electroplating with different peak current densities. The current-on time was 3ms and current-off time was 300 ms for all samples. We see that Cu grows preferentially from the bottom of the trench for all samples. However, bottom-up rates differ among samples, i.e., the bottom-up rates at 100 mA/cm² are higher than those at 20 mA/cm².

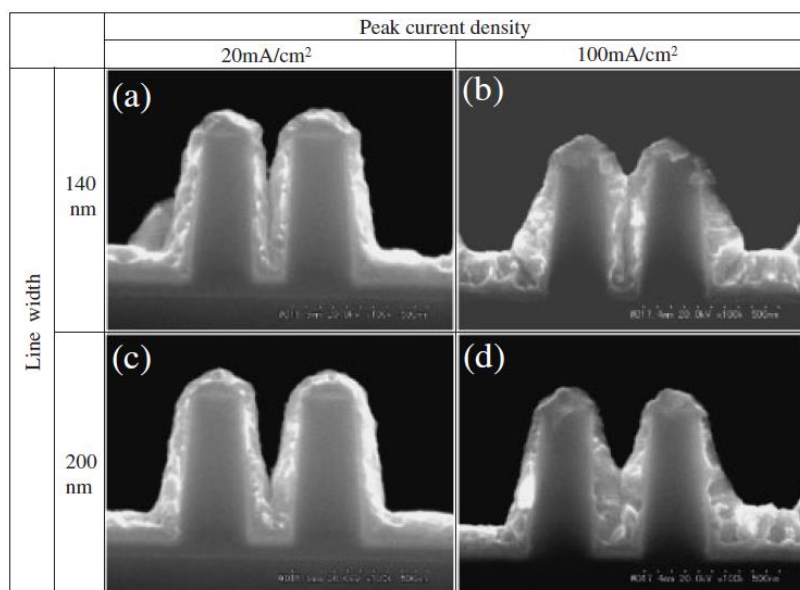


Fig. 3.14 Cross-sectional SEM images of partially filled trenches plated at different peak current densities.

Figure 3.15 shows plots the bottom-up rates of trenches of 140, 160, 180, 200, and 220 nm width against peak current density. The bottom-up rates of the trench at each width were measured for two trenches. It is clear that the bottom-up rate increases with peak current density from 20 to 100 mA/cm². Hence, we adopted the 100 mA/cm² peak current density for filling the trenches.

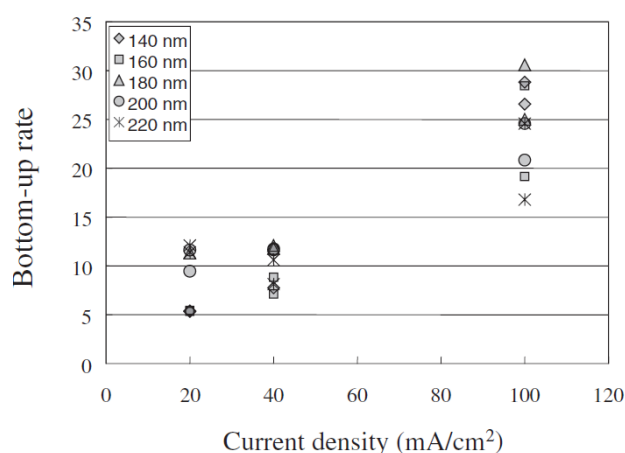


Fig. 3.15 Bottom-up rates for trenches with widths from 140 to 220 nm as a function of peak current density.

Figure 3.16 shows cross-sectional SEM images of 140 nm wide trenches partially filled by pulse wave electroplating when the current-off time was varied. Current-on time and peak current density were fixed at 3 ms and 100 mA/cm², respectively, for all samples. Cu grows preferentially from the bottom of the trench for each sample. However, the bottom-up rate also varies with current-off time, i.e., the bottom-up rate decreases with increasing current-off time.

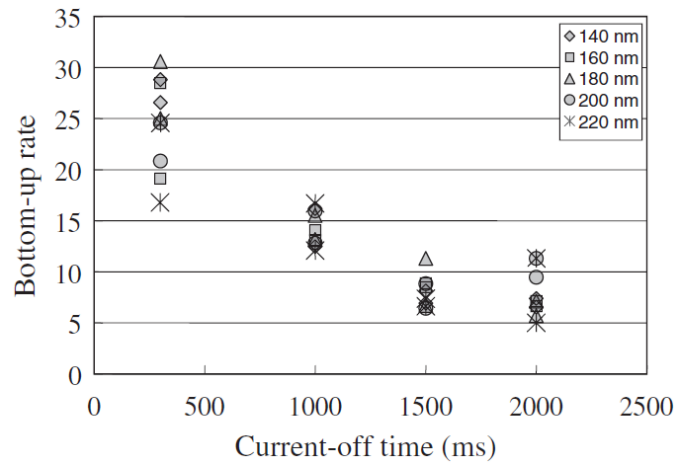


Fig. 3.16 Cross-sectional SEM images of partially filled 140-nm-wide trenches plated with 100 mA/cm² and using different current-off times; (a) 300 ms, (b) 1000 ms, (c) 2000 ms.

Figure 3.17 shows the bottom-up rate of trenches of 140, 160, 180, 200, and 220 nm width against the current-off time. The bottom-up rate of the trench of each width was measured for two trenches. We see the bottom-up rate increases with decreasing current-off time.

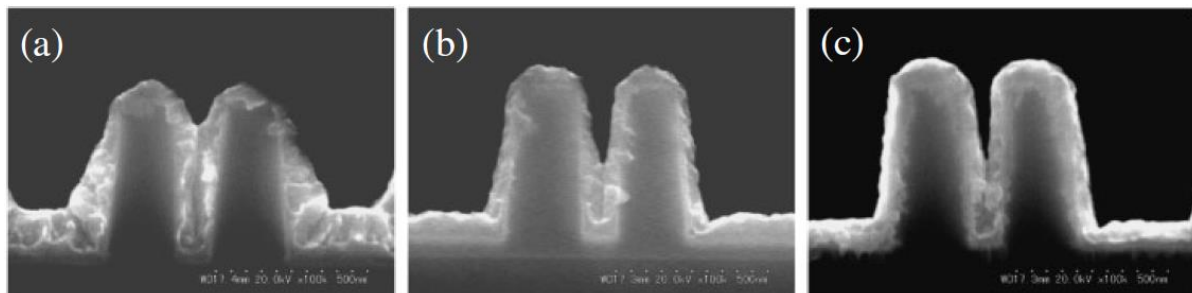


Fig. 3.17 Bottom-up rates for trenches from 140 to 220 nm width as a function of current-off time.

3.3.2 Filling mechanisms of a direct current plating and a pulse wave plating

We considered the bottom-up filling mechanism when using pulse waves of different current densities and frequencies. Figure 3.18 shows schematic cross-sectional representations of the change with time in the filling process for plating with (a) low current density and long current-off time, and plating with (b) high current density and short current-

off time. For the high-current-density application with short current-off time, additives in the bottom part of the trench are consumed and compensation does not occur, leading to bottom-up filling, as shown in Fig. 3.18 (b). This is because current-off time is short, and hence, additive supply from outside the trench through diffusion is not expected. For the low current- density application with long current-off time, a small amount of additives in the bottom part of the trench are consumed and their distribution is uniform in the trench owing to the long current-off time allowing diffusion. As a result, the bottom-up rate decreases.

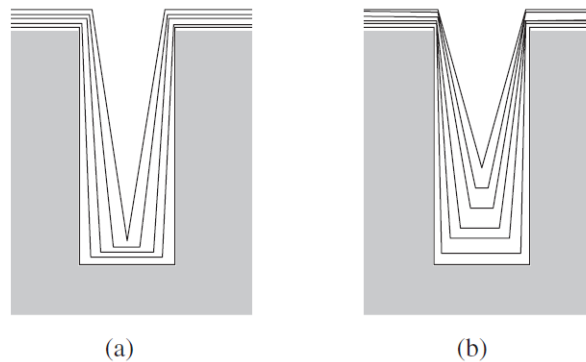


Fig. 3.18 Schematic cross-sectional representations of change in filling processes with time for plating with (a) low current density and long current-off time, and plating with (b) high current density and short current-off time.

3.3.3 Copper microstructures deposited with direct current plating and a pulse wave plating

We compared the microstructures of 80-nm-wide and 500-nm-deep trenches after pulse wave plating (density: 100 mA/cm², current-off time: 100 ms) with those after for DC plating. Figure 3.19 shows cross-sectional microstructures of 80- nm-wide and 500-nm-high Cu trenches after (a) DC and (b) pulse wave plating before annealing. The trench is completely filled with Cu deposited by pulse wave plating, whereas voids are seen in the trench deposited by DC plating. This is due to the fact that Cu grows uniformly in the trenches during DC plating, as expected from Fig. 3.18 (a). On the other hand, we found that

the average grain sizes are 42 nm for DC plating and 38 nm for pulse wave plating. The resistivity of Cu interconnects strongly depends on the grain size. Hence, we investigated the grain size coarsening upon annealing for two samples made by DC and pulse wave plating.

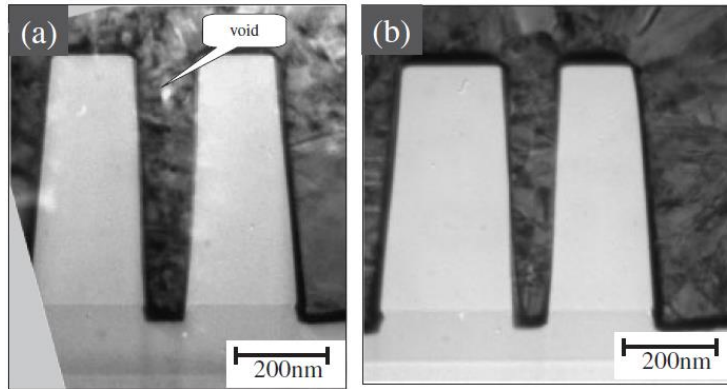


Fig. 3.19 Cross-sectional TEM images of 80-nm-wide trenches after (a) DC electroplating and (b) pulse electroplating.

Figure 3.20 shows TEM images of trenches after (a) DC and (b) pulse wave plating after annealing at 673 K for 30 min in H_2 . After annealing, the grain size of both samples grow, and grains cross the trench width. Seams in the trench formed by DC plating disappear. Furthermore, the average grain size formed by pulse wave plating is 96 nm, i.e., approximately the same level as that for DC plating (101 nm). Pulse wave electroplating is, therefore, promising as a step in the dual damascene process for fabricating very narrow high-aspect-ratio Cu wiring.

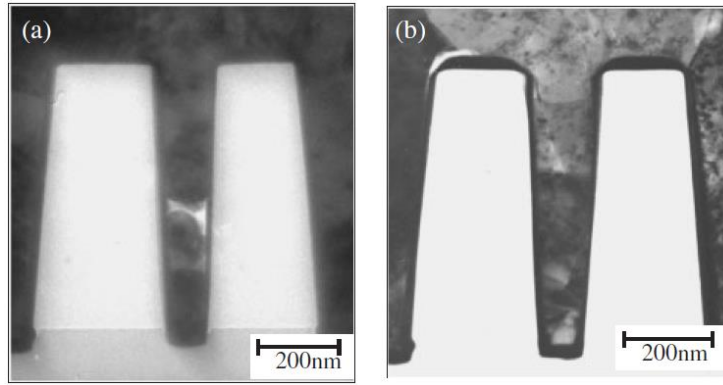


Fig. 3.20 Cross-sectional TEM images of 80-nm-wide trenches after (a) DC electroplating and (b) pulse electroplating after annealing.

3.3.4 Conclusions

In order to completely fill 80-nm-wide trenches with high aspect-ratio (>6) Cu, we investigated the influence of pulse wave electroplating conditions on preferential Cu growth in the trenches. The following results were obtained.

- 1) Peak current density and current-off time in pulse wave plating were found to affect the bottom-up filling.
- 2) Bottom-up filling occurred when peak current density and current-off time were 100 mA/cm² and 300 ms, respectively.
- 3) The 80-nm-wide-trenches (aspect ratio > 6) could be completely filled using the above pulse wave conditions.
- 4) Grain sizes formed by pulse wave plating before and after annealing were 37.5 and 96 nm, respectively. These values were similar to those of DC plating.

3.4 Aspect ratio dependence of the resistivity of fine line Cu Interconnects

Copper is the usual interconnect material for high performance ultra large-scale integration circuits (ULSIs) due to its low electrical resistivity and high reliability. However, the significant increase in the resistivity of Cu with line widths of less than 100 nm is a critical issue [25-30].

This increase is mainly attributed to line widths being comparable to the mean free path of an electron (39 nm) which causes the electron scattering to occur at the grain boundaries of Cu interconnects [30]. In order to create nanoscale Si devices, the development of narrow copper interconnects with low resistivity is essential. Thus, coarsening the grain size in narrow Cu interconnects is essential for controlling the resistivity.

We previously reported the microstructures of 80 nm wide Cu interconnects in the longitudinal direction which were prepared by focused ion beam (FIB) milling and field emission transmission electron microscope (FETEM) techniques. In these papers, we discussed that larger grains were dominant in the upper part of Cu trenches, while smaller grains were predominant in the bottoms of the trenches [31-32]. These results suggest that the resistivity may change with the aspect-ratios of Cu interconnects.

In this paper, we will demonstrate the effect of varying the aspect-ratio of Cu trenches on grain growth behavior and resistivity changes of the Cu interconnects. These studies will provide a guideline for developing low resistance Cu interconnects with a suitable aspect-ratios.

3.4.1 Copper electroplating for features of 50 and 80 nm width

Figure 3.21 shows the cross-sectional scanning electron microscope (SEM) images of 50 and 80 nm wide with 300 nm high Cu interconnects before Cu electroplating. At the two edges of the trenches, the TaN/Ta/Cu layer is highlighted to distinguish it from the SiO₂. The

non-uniform thickness of the TaN/Ta/Cu layers results from sidewall shadowing during deposition on the trenches. A TaN/Ta barrier thickness was found to be 5 – 8 nm (nominal 20 nm) from TEM images.

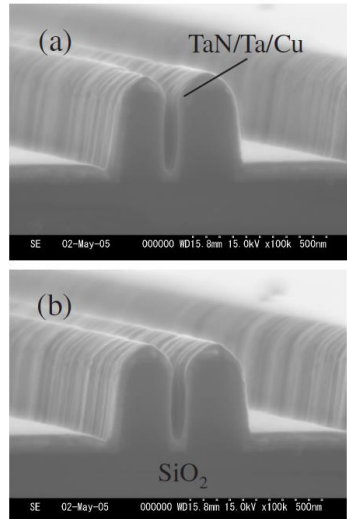


Fig. 3.21 Cross-sectional SEM images of 50 and 80 nm wide Cu interconnects with ultrathin TaN/Ta/Cu layers before Cu electroplating.

Figure 3.22 shows the cross-sectional SEM images of the Cu electroplated trenches of (a) 50 and (b) 80 nm widths after annealing. The SEM images revealed by FIB milling are also shown in (c) (50 nm width) and (d) (80 nm width). The DC electroplating of copper deposition was carried out at process conditions using 1 mA/cm^2 at room temperature. Representative SEM images show that both the narrow trenches with line height of 300 nm were completely filled with electroplated copper, but seams are observed at the center of the trenches. Based on the above observation, DC electroplating was then performed at a higher current density using the same process parameters. It was observed that electroplating at a current density of 5 mA/cm^2 resulted in super-bottom-up filling of 50 nm Cu interconnect with neither seams nor voids as shown in Fig. 3.23. It is evident that the current density for the formation of Cu interconnects can effects the filling characteristics.

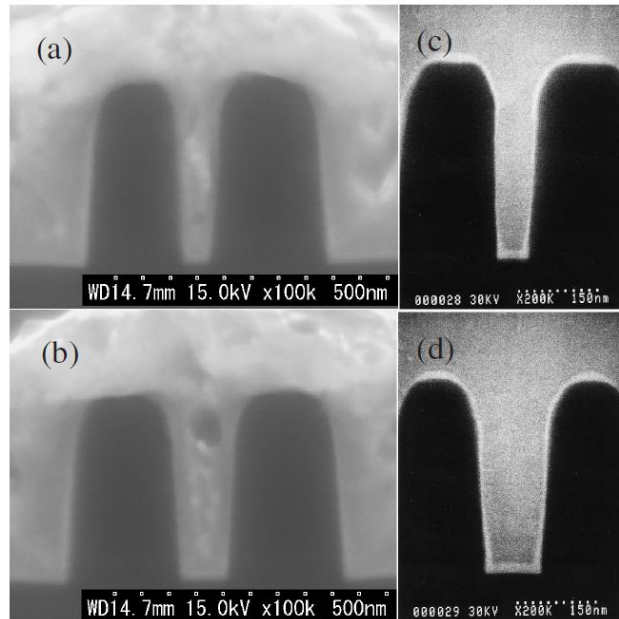


Fig. 3.22 Cross-sectional SEM images of Cu electroplated trenches of (a) 50 and (b) 80nm widths after annealing. SEM images revealed by FIB milling are shown in (c) 50 and (d) 80 nm widths. The DC electroplating was carried out using 1 mA/cm² and, seams were observed at the center of trenches.

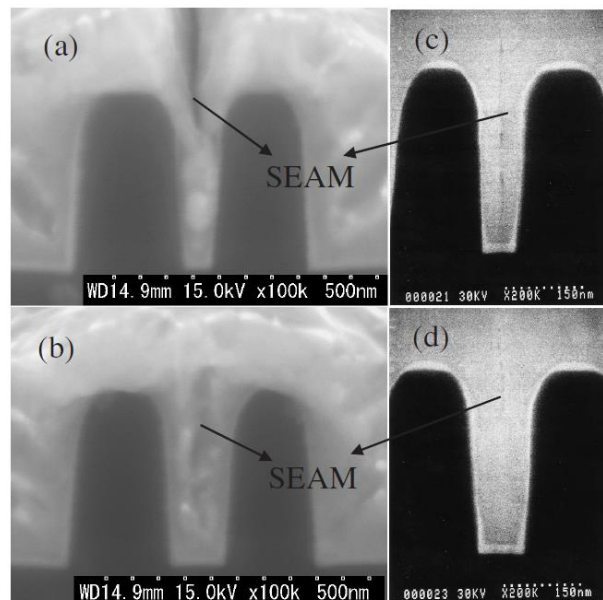


Fig. 3.23 Cross-sectional SEM images of Cu electroplated trenches of (a) 50 and (b) 80nm widths. SEM images revealed by FIB milling are shown in (c) 50 and (d) 80nm widths. DC electroplating was performed at a higher current density of 5 mA/cm² and resulted in complete filling with no seams or voids.

3.4.2 The resistivity and grain size of copper interconnects

The resistivities were obtained through multiplying the measured resistances by the cross-sectional areas of the Cu interconnect and dividing by the line length. Resistivity values were obtained from the measured resistances using dimensions obtained directly from the substrates. The CMP process is very important for the removal of excess Cu film from the trenches, and the non-uniformity of the CMP process results in different trench heights over the experimental substrates. Therefore, only approximate values for cross-section geometries can be given.

The resistivities of Cu interconnect after annealing at 400 °C for 0.5 h obtained for 180, 300, and 500 nm height are plotted against line width in Fig. 3.24. We clearly see that the resistivity of Cu interconnects increases significantly with decreasing line widths less than 100 nm, and the resistivity also increases with decreasing line height, i.e., the average value of 80 nm Cu interconnects is 2.85 $\mu\Omega$ cm for 500 nm height, 3.22 $\mu\Omega$ cm for 300 nm height, and it reaches an average value of about 3.75 $\mu\Omega$ cm for 180 nm height.

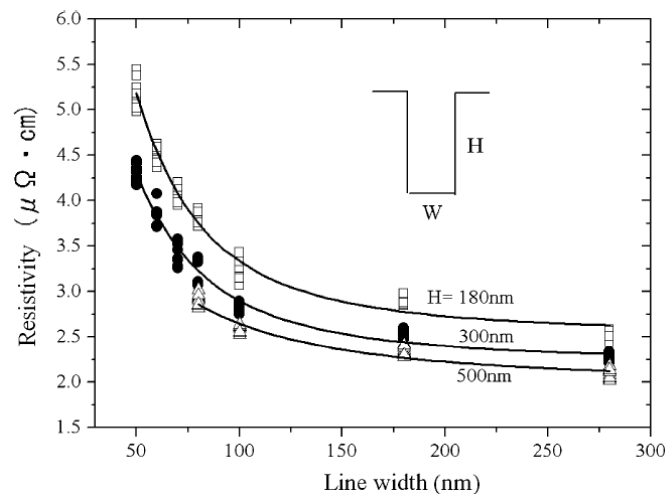


Fig. 3.24 Experimental resistivity data of Cu interconnects of 180, 300, and 500nm heights plotted versus the line width. The resistivity of Cu interconnects increases significantly with line widths less than 100 nm, and the resistivity also increases with decreasing line height.

Figure 3.25 shows the microstructural TEM images in the longitudinal direction of 300 and 500 nm high Cu interconnects with 80 nm width after annealing at 400 °C for 0.5 h. From these TEM images, many very small grains were observed at the bottom of the trench. This indicates the fact that grain growth is restricted by the sidewall at the bottom of the narrow trenches during annealing and, therefore, the grains at the bottom are much smaller than those in the upper part of the trench.



Fig. 3.25 Average grain size distribution of 80-nm-wide and 500-nm-high Cu interconnects after annealing at 400 °C for 0.5 h. The grain size increased with the distance from bottom of trench.

To quantify the grain length distribution in the depth direction of trenches, the average grain length was obtained by the following procedures as shown in Fig. 3.26: horizontal straight lines were drawn from the bottom of the trenches in 10-nm steps, and the length of the intercepts at the same depth was averaged and defined as the average grain length.

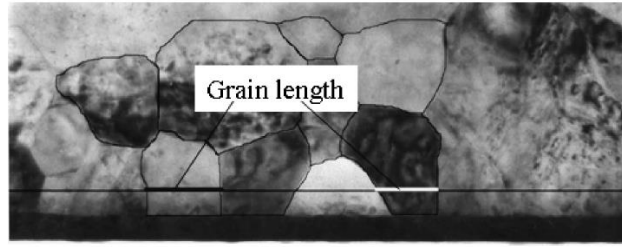


Fig. 3.26 Longitudinal cross-sectional TEM image of 80-nm-wide and 500-nm-high Cu interconnects after annealing at 400 °C for 0.5 h. Many very small grains are observed at the bottom of the trench.

Figure 3.27 shows the average grain length distribution plotted against the depth of the Cu trench from the above TEM images. We can observe that the grain length increases with distance from the bottom of trench, and larger grains are predominant in the upper part of the trench. The plot further shows that an average grain length of 500 nm height was found to be similar to 300 nm high Cu interconnects at the same depth, and the average grain length is becoming larger toward the surface part of 500 nm wide Cu interconnect.

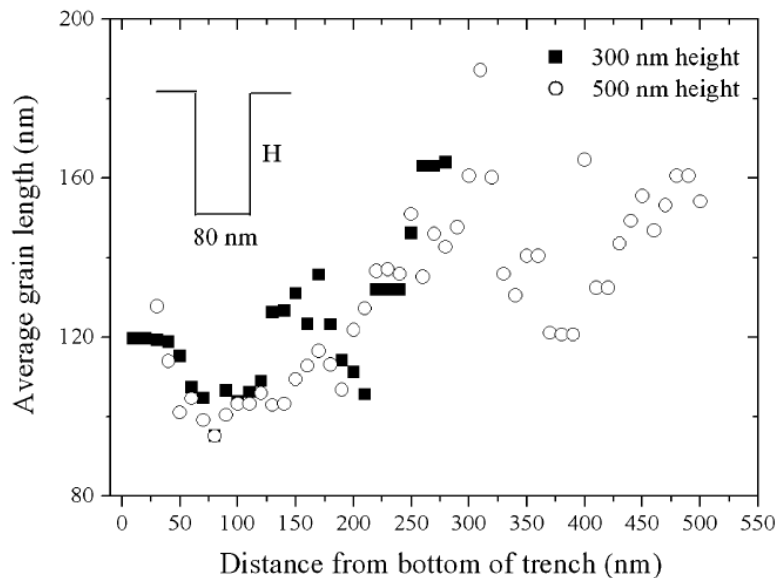


Fig. 3.27 A schematic representation of how to quantify the grain lengths of the narrow Cu interconnects cross-sectional microstructures in the longitudinal direction.

3.4.3 Copper resistivity dependence on the aspect ratio of lines

Figure 3.28 depicts the resistivity dependence on the reciprocal of line height H for the line widths of 50, 80, 100, 180, and 280 nm. The line heights are 180, 300, and 500 nm.

From this figure, the resistivity ρ is expressed by

$$\rho = \rho_0 + k/H \quad (3-3)$$

where ρ_0 is the resistivity of line height of infinity, and k is a coefficient calculated from the gradient of straight lines varying with the line widths. As the interconnect line heights are reduced when the line widths remain constant, the aspect-ratios of trenches are reduced, and therefore, the grain sizes in the upper part of Cu interconnect might then be reduced, resulting in the increase of resistivities.

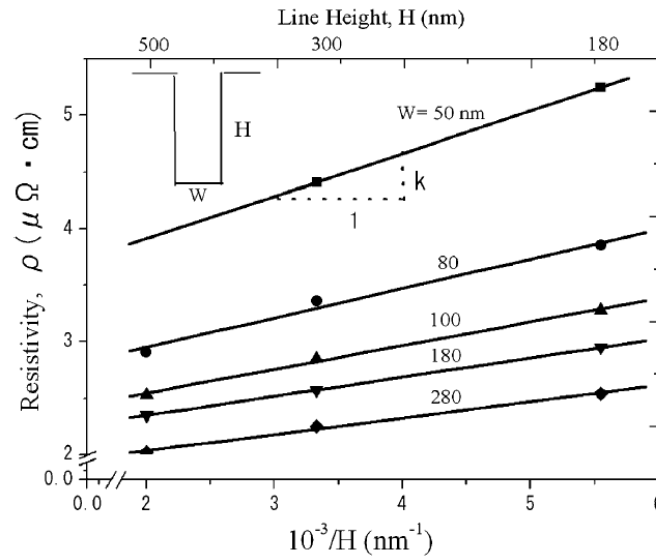


Fig. 3.28 Resistivity dependence on the reciprocal of line height, H . The resistivity ρ is expressed by $\rho = \rho_0 + k/H$, where ρ_0 is the resistivity of line height of infinity, and k is a coefficient.

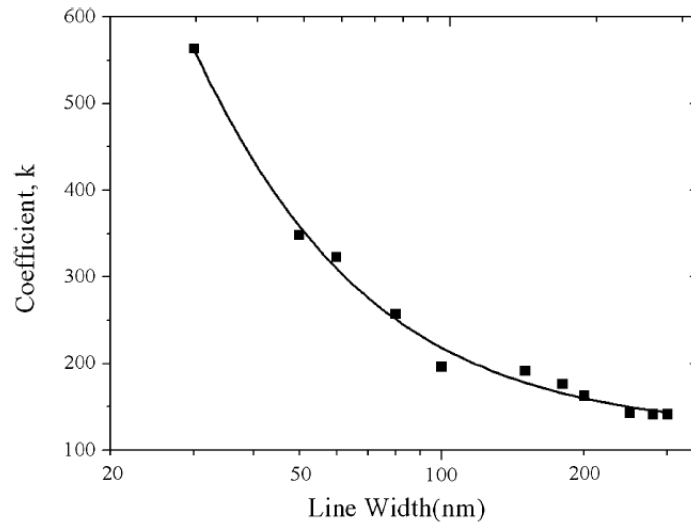


Fig. 3.29 Coefficient, k as plotted vs line widths. Observe that k increases dramatically as the line widths decrease.

The coefficient, k as plotted against the line widths as shown in Fig. 3.29. The value of k increases dramatically with the decrease in the line widths. The predictions in eq. (3-3) are illustrated in Fig. 3.30 as a function of the line widths for aspect-ratios of 2, 3, and 5. In this figure, the resistivity is normalized by that of an aspect ratio of 1. It can clearly be seen that resistivity decreases significantly with the increasing aspect-ratio in very fine line Cu wires of less than 100 nm. We can observe that the resistivity of Cu wires with an aspect-ratio greater than 3 reduces significantly with decreasing line widths. For example, in the 50 nm wide Cu interconnects, a larger aspect-ratio of greater than 3 generates lower resistivity, which in turn causes 45% lower resistivity compare to an aspect-ratio of 1. Thus, the effect of aspect-ratio on resistivity control becomes very effective to compensate the resistivity increase of very narrow wires.

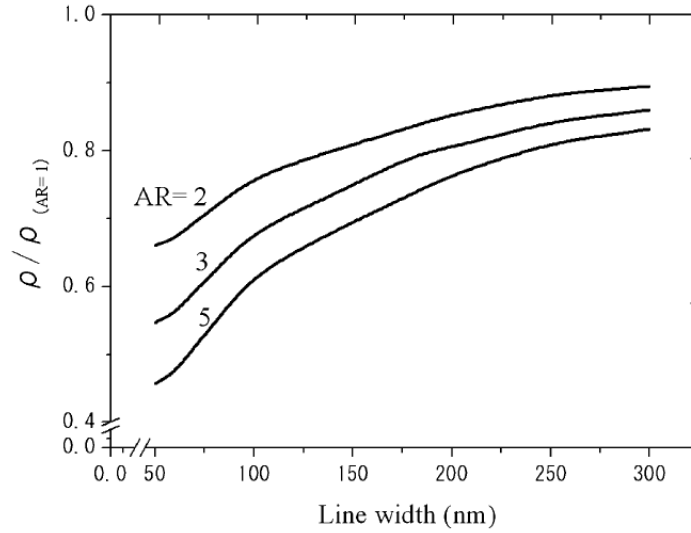


Fig. 3.30 Resistivity versus line widths for the aspect-ratios, AR of 2, 3, and 5. The resistivity was normalized by an aspect-ratio of 1. Observe that the resistivity of an aspect-ratio of 3 is significantly reduce with decreasing line widths.

As mentioned above, the effect of the aspect-ratio on resistivity control is extreme at narrower line widths. This can be attributed to grain size distributions where larger grains exist in the upper part of the Cu interconnects with higher aspect-ratios. Further, the H₂ annealing conditions of the Cu interconnects may induce additional grain growth, but the grain size will still be restricted by the side walls of the trench. Our experimental results show that Cu wires with high aspect-ratios greater than 3 are one of the most powerful candidates for lowering resistivity in very narrow Cu interconnects of less than 50 nm.

3.4.4 Conclusions

The effect of aspect-ratios of very narrow Cu interconnects less than 100 nm on the resistivity has been discussed. The resistivity of Cu interconnects increases significantly with decreasing line widths less than 100 nm, and the resistivity also increases with decreasing line height. These results coincide with the longitudinal cross-sectional TEM observation data that many very small grains were observed at the bottom of the trench, while larger grain

sizes are predominant in the upper part of the Cu interconnects. The predictions indicated that resistivity decreases dramatically with aspect-ratios of greater than 3 in fine line Cu wires due to the larger grain size distributions in the upper part of the Cu interconnects. This result demonstrate that the aspect ratio of Cu wires are effective for controlling the resistivity in future Cu interconnects with very narrow and shallow dimensions.

3.5 Microstructures of electrodeposited Cu Interconnects

In recent years, the continuous progress in fabrication of high performance ultralarge-scale integration circuits (ULSIs) has been driven by the desire to increase circuit speed, broaden chip functionality, and improve reliability of electronic interconnects. In response to these technical demands, a high integration LSI using the 65-nm technology node (90-nm line width) has already been commercialized, and Cu interconnects for a 45-nm technology node (70-nm line width) LSI are under development, and will be in use by the 2010, according to the International Technology Roadmap for Semiconductors (ITRS) [33].

However, there is a significant increase in resistivity in copper interconnects when line widths are less than 100 nm [33-39]. This is becoming a critical issue and is mainly due to the fact that the line widths are comparable to the mean free path of an electron (39 nm), which causes an increase in resistivity by electron scattering occurring at the grain boundaries of the Cu interconnects. Therefore, it is necessary to develop a grain coarsening process to achieve low resistivity in very narrow Cu interconnects.

Researchers have recently investigated cross-sectional microstructures and the resistivity of Cu films and interconnects [40-44] and reported experimental results for the microstructure have, e.g., an investigation of the grain sizes from the surface plane of Cu interconnects using an orientation imaging microscope (OIM) [40] or TEM (planeview

measurement) [42]. However, this investigation did not clarify the longitudinal grain size distribution that control resistivity.

Microstructures in the longitudinal direction of Cu interconnects with line widths greater than 170 nm that use electron backscattered diffraction (EBSD) have also been investigated [45]. But there have been no reports on grain size distribution in the longitudinal direction of Cu interconnects of less than 100 nm. This is because the fabrication of Cu interconnects of less than 100 nm in the longitudinal direction is very difficult. We have succeeded in fabricating 80-nmwide Cu interconnects along the longitudinal direction using focused ion beam (FIB) milling. Observations using field emission transmission electron microscopy (FETEM) techniques revealed that larger grains are predominant in the top part, and smaller grains are predominant in the bottom part of Cu trenches [46-47].

We assume sidewall-restricted grain growth at the bottom of narrow trenches, resulting in grain size distributions in the depth direction of the trench. The grain growth processes of a Cu interconnect strongly depend on trench widths, so the resistivity of next generation Cu interconnects using the 32- nm technology node (50-nm line width) is expected to increase further.

In this section, we statistically investigated the longitudinal grain size distributions of 50-nm-wide Cu interconnects and compared them with those of 70- and 80-nm-wide Cu interconnects. The resistivity of 50-nm wires was then compared with those of the 70- and 80-nm-wide Cu wires. After presenting our findings, we will discuss the possibility creating low resistivity Cu interconnects narrower than 50 nm.

3.5.1 SEM and TEM observations of fine copper interconnects

Figure 3.31 (a) and (b) show cross-sectional SEM images of Cu electroplated trenches of 50- and 80-nm widths after annealing, as revealed by FIB milling. Representative SEM

images show that the 50- and 80-nm-wide trenches with line heights of 300 nm were completely filled with electroplated copper. Figure 3.31 (c) and (d) show a surface view SEM image of 50- and 80-nm-wide Cu interconnects after CMP. It can be seen that the wires were not dished or eroded during the CMP.

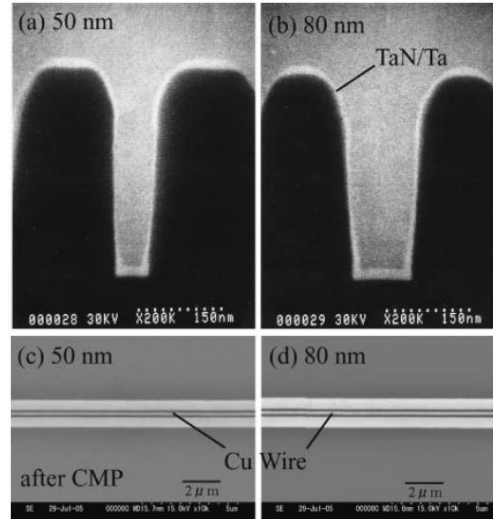


Fig. 3.31 Cross-sectional SEM images of (a) 50-nm, (b) 80-nm, and top surface of (c) 50-nm, (d) 80-nm-wide Cu interconnects with heights of 300nm were completely filled with electroplated copper leaving neither seams nor voids.

Figure 3.32 shows the resistivity of Cu interconnects with heights of 300 nm after annealing at 400 °C for 0.5 h. The resistivity of the Cu interconnects increases significantly as line widths decrease to less than 100 nm, i.e., the average value is 3.23 $\mu\Omega$ cm for an 80-nm width, 3.48 $\mu\Omega$ cm for a 70-nm width, and reaches an average value of about 4.18 $\mu\Omega$ cm for a 50-nm-width.

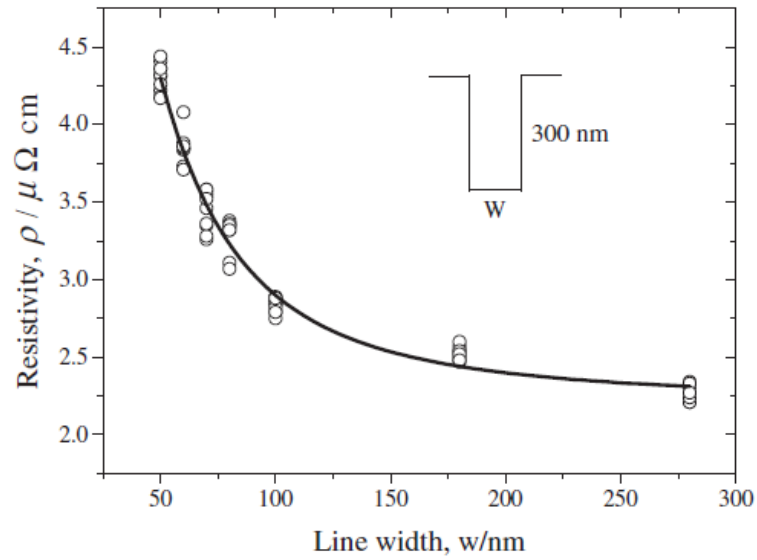


Fig. 3.32 Resistivity data of 300-nm-high Cu interconnects plotted versus line width. Resistivities increase significantly as line widths decrease to less than 100 nm.

Two methods were used to quantify grain sizes and grain size distributions of the 50-nm-wide Cu interconnects in the longitudinal direction in comparison with those of 70- and 80-nm-wide interconnects, as shown in Fig. 3.33. For grain length distribution in the trench depth direction, straight horizontal lines were drawn from the bottom to the surface of the trenches in 10-nm steps, and the length of intercepts between the horizontal lines and each grain at the depth of the trenches was obtained and averaged. This grain length exhibits grain size distribution in the depth direction. To obtain grain sizes, a line was drawn around the grain boundary of each grain in the trench, the sizes of the grains were computed assuming the grains to be circular, and the diameter of each grain was calculated from the circular grain area.

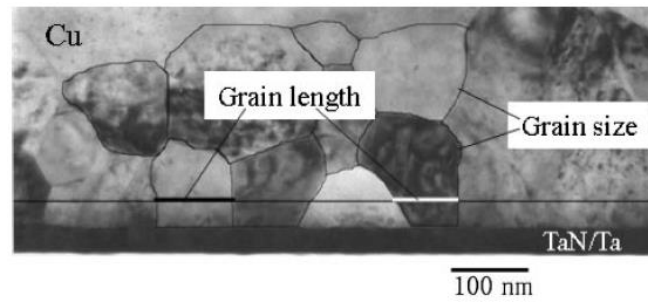


Fig. 3.33 Schematic representation of how to quantify grain sizes and average grain lengths of cross-sectional microstructures in longitudinal direction of 100-nm-wide Cu interconnects after annealed.

Figure 3.34 shows TEM images of the longitudinal microstructures for 50- and 80-nm Cu interconnects. The wires were 1 mm long. Figure 3.34 (a) shows an as-deposited 50-nmwide Cu interconnect. Many very small grains can be seen throughout the longitudinal dimension of the Cu wire. It was found that most grains were extremely small (approximately 20 nm), and were about one-third of the line width of the Cu interconnects. The resistivity of the interconnect is $4.96 \mu\Omega \text{ cm}$, which is about 18% higher than that of the 50-nm-wide Cu interconnects ($4.18 \mu\Omega \text{ cm}$) after annealing.

After annealing, the grain sizes of the annealed Cu interconnect with line widths of 50 nm are significantly different from that of the as-deposited Cu interconnect, as shown in Fig. 3.34 (b). Differences in grains sizes between the top and bottom parts of the trenches can also be seen. In particular, the Cu grain size in the bottom of the trench is significantly smaller than that at the top part of the Cu interconnects. The same tendency can be seen for the 80-nmwide Cu interconnects, as shown in Fig. 3.34 (c).

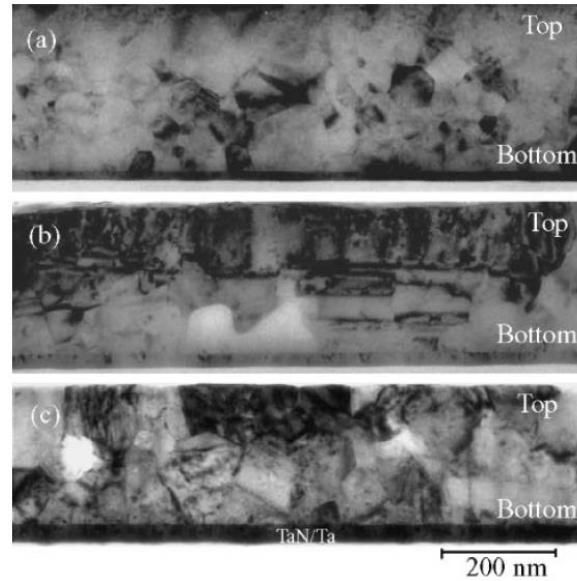


Fig. 3.34 TEM images in longitudinal direction of (a) as-deposited 50-nmwide Cu interconnects, (b) 50- and (c) 80-nm-wide Cu interconnects with line heights of 300nm after annealing.

As pointed out in the introduction, these results indicate that the Cu grain size and grain size distribution within the Cu trenches cannot be elucidated by inspection from the direction of the normal to the surface plane of the narrow Cu interconnects using OIM [40] or TEM (plane-view measurement) [42]. In the case of EBSD, the detectable grain size was estimated to be greater than 100 nm. Hence, transmission electron microscopy is the only technique that can measure individual grain sizes in the longitudinal direction of Cu wires of less than 80 nm.

3.5.2 Grain size distribution of fine copper interconnects

Figure 3.35 shows the average grain length distribution of 50-and 80-nm Cu interconnects as a function of distance from the bottom of a trench, as estimated from the images shown in Fig. 3.34 (b) and (c). It can be seen that both average grain lengths increase with distance from the bottom of trench. However, the average grain length of a 50-nm Cu wire is much smaller than that of an 80-nm wire.

The above results are explained as follows. It has been reported that grain growth originates in overburdened Cu film during annealing and extends into the Cu interconnect Trenches [49]. However, Cu grains inside the trench do not grow well because of the strong restrictions imposed by trench width [35]. This restriction increases as line width decreases. As a result, grain length distributions in the depth direction of the trench were formed, as shown in Fig. 3.35. The same tendency was observed for all of the samples after Annealing diameter of each grain was calculated from the circular grain area.

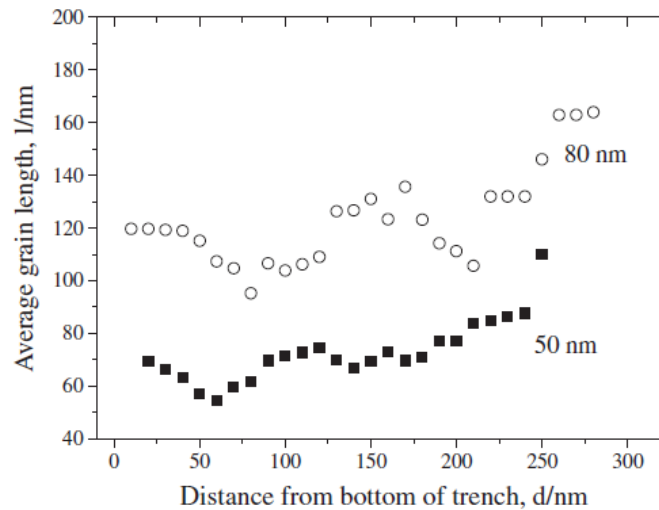


Fig. 3.35 Average grain length distribution of 50- and 80-nm-wide, 300-nm high Cu interconnects after annealing at 400 °C for 0.5 h. Grain length increased as distance from bottom of trench increased.

Figure 3.36 shows a normal distribution of grain sizes of 50-, 70- and 80-nm-wide Cu interconnects plotted as a histogram before and after annealing at 400 °C for 0.5 h. The grain sizes were obtained from the identified grain boundaries and computed assuming the grains to be circular, as shown in Fig. 3.33. The observed length is 4 mm for each interconnects. More than 240 grains were measured from the as-deposited 50-nm Cu interconnect, and 188, 58, and 45 grains were measured for annealed 50-, 70-, 80-nm-wide Cu interconnects, respectively. Twins were not considered to be grain boundaries.

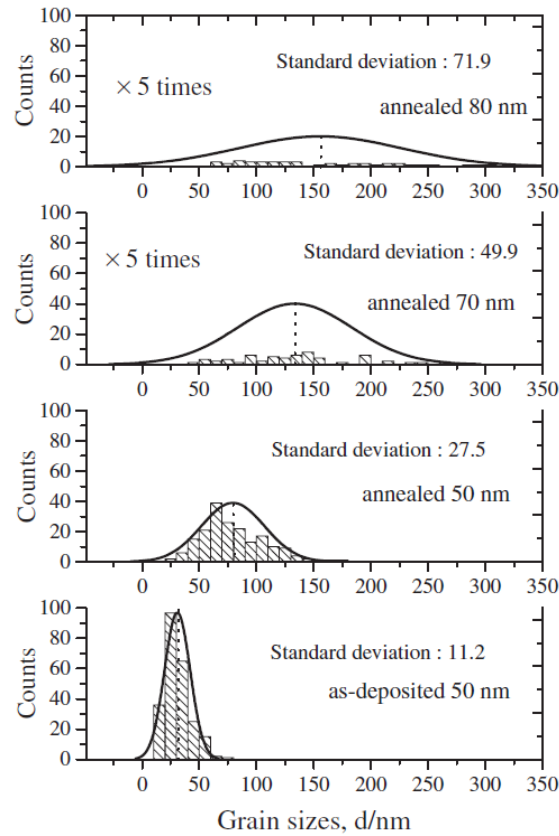


Fig. 3.36 Normal distribution of grain sizes for as-deposited 50-nm Cu interconnect and 50-, 80-nm-wide Cu interconnects are plotted as a histogram. Observed length is 4 mm for each interconnect.

The grain size distribution in the trench of each interconnect can be determined by comparing the standard deviation of normal distributions. The value of standard deviation for as-deposited 50-nm-wide Cu interconnects is 11.1 with a sharp normal distribution. After annealing, the standard deviation increases to 27.5 in the 50-nm Cu interconnects, and achieves a larger grain size microstructure than in the as-deposited Cu interconnect. As the line widths increase, the standard deviation of 70- and 80-nm Cu interconnects increases to 49.9 and 71.9, respectively. This indicates that the normal distributions become broader and that there are larger ranges of grain size as line width increases. That standard deviations

decrease as line width decreases can be attributed to the fact that grain size is constrained by the narrower line width.

Figure 3.37 shows the average grain size of 50-, 70- and 80- nm-wide Cu interconnects obtained from the measurements shown in Fig. 3.56. Average grain size increases as line width increases. The average grain size of the 50-nm-wide Cu interconnects grew to 80 nm and was 2.5 times the size of the grains in the 50-nm as-deposited Cu interconnect.

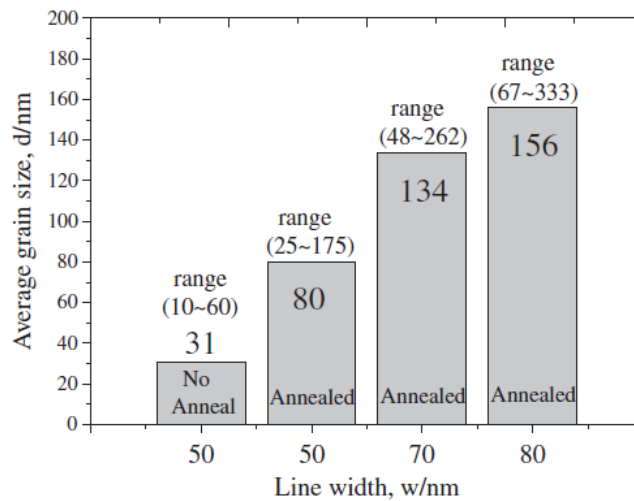


Fig. 3.37 Average grain sizes of 50, 70- and 80-nm-wide Cu interconnects

The resistivity of 50-, 70- and 80-nm-wide Cu interconnects was plotted against average grain size in Fig. 3.38. It can be seen that resistivity increases linearly with decreasing line width. This increase is mainly attributed to the density of grain boundary increasing with line widths that are comparable to the mean free path of electron (39 nm), which causes the electron scattering to occur at the grain boundaries of narrower Cu interconnects. To develop Cu interconnects with low resistivity, coarsening the grain size in narrow Cu interconnects is essential to lowering the resistivity.

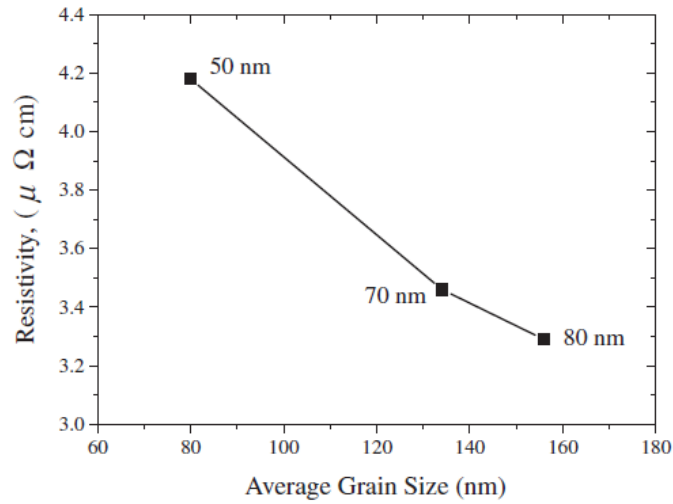


Fig. 3.38 Resistivity data versus average grain size are plotted for 50-, 70- and 80-nm-wide Cu interconnects.

3.5.3 Conclusion

The grain sizes, grain size distributions and resistivity of 50-nm-wide Cu interconnects in the longitudinal direction were evaluated and compared with those of 70- and 80-nm-wide Cu interconnects to develop a grain size coarsening process. Grain length increases with distance from the bottom of the trench, and Cu grains inside the trench may have difficulty growing because of the strong restrictions created by the trench geometry. The value of standard deviation in the normal distribution histogram for 50-nm wire was found to be much smaller than those for the 70- and 80-nm Cu wires after annealing. This implies that sufficient grain growth should not be expected in the very narrow Cu interconnect (less than 50 nm) of the future if conventional annealing process is used.

3.6 Conclusions

This chapter has investigated the mechanism of anisotropic copper growth in fine features and the characteristics of the deposited copper. The additives in the solution play an important role in anisotropic deposition at the bottom of a feature. A model for bottom-up

filling was proposed and confirmed by comparison of experimental and simulation results. Some kinds of dyes that adsorb on the copper surface and suppress copper deposition acted as additives for bottom-up filling. A trench with a width of 100 nm or less could be filled by using additives and controlling the current waveform for electroplating. The resistivity and microstructure of very narrow copper interconnects with a width of less than 100 nm were also investigated. The resistivity was found to decrease significantly with increased aspect ratio because of the larger grain size distribution in the upper part of copper interconnects with higher aspect ratios. After annealing, the average grain size was larger than that of the as-deposited 50-nm interconnects. The standard deviation of the grain sizes, however, was found to be much smaller after annealing for a 50-nm wire than for 70- and 80-nm interconnects. This implies that grain growth is necessary for very narrow copper interconnects (below 50 nm) to decrease the resistivity.

References

- [1] S. J. Lee, K. H. Chang, S. M. Choi, K. C. Park, H. D. Lee, H. K. Kang, J. T. Moon, Proceedings of Advanced Metallization Conference 2000, p. 121, 2000.
- [2] T. P. Moffat, D. Wheeler, S.-K. Kim, D. Josell, Journal of the Electrochemical Society, vol. 153 (2), p. C127-C132, 2006.
- [3] D. Josell, T. P. Moffat, D. Wheeler: Superfilling When Adsorbed Accelerators Are Mobile., Journal of The Electrochemical Society, vol. 154(4), D208-D214, 2007.
- [4] T. P. Moffat, D. Wheeler, M. D. Edelstein, D. Josell: Superconformal film growth: Mechanism and quantification. IBM J. RES. & DEV. Vol. 49 (1), p. 19, 2005.
- [5] S. Y. Chiu, J. M. Shieh, S. C. Chang, K. C. Lin, B. T. Dai, C. F. Chen, and M. S. Feng: Characterization of additive systems for damascene Cu electroplating by the superfilling profile monitor. J. Vac. Sci. Technol. B. vol. 18, p. 2835, 2000.
- [6] Kun-Cheng Lin, Shih-Chieh Chang, Bau-Tong Dai, Chia-Fu Chen and Ming-Shiann Feng: Electroplating copper in sub-100 nm gaps by additives with low consumption and diffusion ability. J. Vac. Sci. Technol. Vol. 20(3), p. 940, 2002.
- [7] K. Kobayashi, A. Sano, H. Akahoshi, T. Itabashi, T. Haba, S. Fukada, and H. Miyazaki: Trench and Via Filling Profile Simulations for Copper Electroplating Process. Proceedings of the 2000 International Interconnect Technology Conference p.34, 2000.
- [8] T. Haba, T. Itabashi, H. Akahoshi, A. Sano, K. Kobayashi, and H. Miyazaki: Electrochemical and Simulative Studies of Trench Filling Mechanisms in the Copper Damascene Electroplating Process. Materials Transactions vol. 43, p. 1593, 2002.
- [9] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, H. Deligianni: Damascene copper electroplating for chip interconnections. IBM Journal of Research and Development vol. 42 (5), p. 567, 1998.
- [10] Y. Cao, P. Taephaisitphongse, R. Chalupa, and A. C. West: Three-Additive Model of Superfilling of Copper. J. Electrochem Soc. Vol. 148, p. C466, 2001.
- [11] J. Reid, S. Mayer, E. Broadbent, E. Klawuhn, and K. Ashitani: Factors influencing damascene feature fill using copper PVD and electroplating. Solid State Technology vol. 86, p. 43, 2000.
- [12] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligia: Damascene copper electroplating for chip interconnections. IBM J. Res. Develop. Vol. 42, p. 567, 1998.
- [13] P. C. Andricacos, Interface, vol. 8 p. 32, 1999.

- [14] K. M. Takahashi and M. E. Gross, *J. Electrochem. Soc.*, vol. 146, p. 4499, 1999.
- [15] J. J. Kelly, C. Tian, A. C. West, *J. Electrochem. Soc.*, vol. 146, p. 2540, 1999.
- [16] J. J. Kelly, A. C. West, *Electrochemical and Solid-State Letters*, vol. 2, p. 561, 1999.
- [17] A. J. Bard, L. R. Faulkner, *Electrochemical methods* (John Wiley & Sons, New York, 1980), p.96
- [18] R. M. Wightman and D. O. Wipf, *Voltammetry at Ultramicroelectrodes in Electroanalytical Chemistry* (Marcel Dekker, New York, 1989), Vol.15, pp.267-353
- [19] N. Owada, *Materia Japan*, vol. 43, No. 1, p. 7, 2004 (in Japanese).
- [20] J. Reid et al., *Appl. Phys. Vol.* 40, p. 2650, 2001.
- [21] K. Hinode, Y. Hanaoka, K. Takeda and S. Kondo, *Jpn. J. Appl. Phys.*, vol. 40, p. L1097, 2001.
- [22] W. Steinhögl, G. Schindler, G. Steinlesberger and M. Engelhardt, *Phys. Rev. B*, vol. 66, p. 75414, 2002
- [23] G. Ritter, P. McHugh, G. Wilson and T. Ritzdorf, *Solid-State Electron.*, vol. 44, p. 797, 2000.
- [24] T. Fujikawa, T. Onishi and T. Sato, *Jpn. J. Appl. Phys.*, vol. 40, p. 2191, 2001.
- [25] A. F. Mayadas and M. Shatzkes: *Phys. Rev. B* vol. 1, p. 1382, 1970.
- [26] K. Hinode, Y. Hanaoka, K. Takeda, and S. Kondo, *Jpn. J. Appl. Phys.*, vol. 40, p. L1097, 2001.
- [27] W. Steinhögl, G. Schindler, G. Steinlesberger, and M. Engelhardt, *Phys. Rev. B*, vol. 66, p. 75414, 2002.
- [28] The International Technology Roadmap for Semiconductors, 2005.
- [29] G. Steinlesberger, M. Engelhardt, G. Schindler, and W. Steinhögl, *Solid-State Electron.*, vol. 47, p. 1237, 2003.
- [30] W. Wu, S. H. Brongersma, M. Van Hove, and K. Maex, *Appl. Phys Lett.*, vol. 84, p. 2838, 2004.
- [31] K. P. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, T. Tobita, M. Chiba, T. Saito, and K. Ishikawa, *Jpn. J. Appl. Phys.*, vol. 45, p. L852, 2006.
- [32] K. P. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, T. Tobita, M. Chiba, T. Saito, and K. Ishikawa: *Proc. Advanced Metallization Conf.*, Tokyo, 2006, p. 58.
- [33] The International Technology Roadmap for Semiconductors, 2005.
- [34] K. Hinode, Y. Hanaoka, K. Takeda and S. Kondo: *Jpn. J. Appl. Phys.*, vol. 40, p. L1097–L1099, 2001.

- [35] W. Steinhögl, G. Schindler, G. Steinlesberger and M. Engelhardt, *Phys. Rev. B*, vol. 66, p. 75414, 2002.
- [36] G. Steinlesberger, M. Engelhardt, G. Schindler and W. Steinhögl, *Solid-State Electron*, vol. 47, p. 1233–1237, 2003.
- [37] G. Steinlesberger, M. Engelhardt, G. Schindler, W. Steinhögl, A. V. Glasow, K. Mosig and E. Bertagnolli, *Microelectron. Eng.*, vol. 64, p. 409–416, 2005.
- [38] C.-U. Kim, J. Park, N. Michael, P. Gillespie and R. Augur, *J. Electron Mater.*, vol. 32, p. 982–987, 2003.
- [39] W. Wu, S. H. Brongersma, M. Van Hove and K. Maex, *Appl. Phys. Lett.*, vol. 84, p. 2838, 2004.
- [40] K. Mirpuri and J. Szpunar, *Micron*, vol. 35, p. 575, 2004.
- [41] H. J. Lee, D. I. Kim, J. H. Ahn and D. N. Lee, *Thin Solid Films*, vol. 474, p. 250, 2005.
- [42] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving and M. Engelhardt, *J. Appl. Phys.*, vol. 97, p. 023706, 2005.
- [43] M. Moriyama, K. Matsunaga, T. Morita, S. Tsukimoto and M. Murakami, *Mater. Trans.*, vol. 45, p. 3033, 2004.
- [44] S. M. Rossnagel and T. S. Kuan, *J. Vac. Sci. & Tech. B, Microelectronics and Nanometer Structures*, vol. 22, p. 240, 2004.
- [45] Y. Hirose, N. Hashikawa, K. Fukumoto and Y. Mashiko, *J. Electron Microscopy*, vol. 53, p. 567, 2004.
- [46] K. P. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, T. Tobita M. Chiba, T. Saito and K. Ishikawa, *Jpn. J. Appl. Phys.*, vol. 45, p. L852–L853, 2006.
- [47] K. P. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, T. Tobita, M. Chiba, T. Saito and K. Ishikawa, *Advanced Metallization Conference*, Tokyo, September, p. 58, 2006.
- [48] T. Ritzdorf, L. Graham, S. Jin, C. Mu and D. Fraser, *IEEE Proc. Int’l Interconnect Tech. Conf.*, p. 106–108, 1998.
- [49] W. Wu, D. Ermur, S. H. Brongersma, M. Van Hove and K. Maex, *Microelectron. Eng.*, vol. 76, p. 190–194, 2004.

Chapter 4

Anisotropic and Selective deposition of Copper to Make Bumps and Wirings¹

4.1 Introduction

Selective or anisotropic metallization is often desired to fabricate fine structures such as bumps and interconnects in electronic applications [1-6]. Metal can be selectively deposited using resist masks with a photolithographic process by galvanic or electroless deposition. However, the process that uses no resist masks normally results in lateral growth because the plating process is generally isotropic. A selective and anisotropic metallization process has an advantage that the process does not use a resist mask. A resistless process is expected to be a lower cost, more environmentally friendly process. The process can reduce the use of environmentally harmful chemicals, such as a developer solution, a resist stripper, and the metal-etching solution.

Several methods have been reported to deposit metal selectively or anisotropically without the resist mask. Anisotropic deposition of electroless Ni has been reported in the past [7, 8]. A Pb^{2+} additive is added to the electroless bath and suppresses the deposition of Ni on the edges of a pattern. The presence of the Pb^{2+} inorganic additive leads to anisotropic Ni metallization. Anisotropic deposition of copper is known as bottom-up filling (BUF) or superfilling [9, 10]. Organic additives are important to achieve anisotropic electroplating in the BUF process. Three types of additives are typically used to achieve the BUF process:

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suppressors, accelerators, levelers. Suppressors are usually polyether molecules that inhibit copper deposition. Accelerators are usually sulfide molecules that act to depolarize the Cu surface in the presence of inhibiting additives. Levelers are molecules such as dyes, cationic surfactants, and alkyltrimethylammonium salts, which inhibit Cu deposition and prevent bump formation on the filled features [11, 12]. Two mechanisms of the BUF process have been developed. The first mechanism is curvature enhanced accelerator coverage (CEAC) [13]. In CEAC, BUF is attributed to a local coverage increase in accelerating additives in the feature by decreasing the surface area of the feature. Accumulation of the accelerating additives results in an undesirable overburden [12, 14]. The second mechanism is diffusion-adsorption consumption of an inhibiting additive [15, 16]. In this mechanism, the inhibiting additives make their concentration field by their adsorption and/or consumption on the Cu surface. Akolkar and Dubin have shown the effects of pattern-density-dependent modulation of the suppressor concentration field in the BUF process [17]. Both mechanisms are important to explain the BUF process.

In this paper, we demonstrate that copper can be selectively and anisotropically electroplated using an inhibiting additive and the feature on the substrate. Then, we clarify the role of an inhibiting additive, Basic Red 12, for selective electrodeposition of Cu surface in sulfuric acid solutions by using linear sweep voltammetry (LSV), cyclic voltammetry (CV) and in situ SERS measurements.

Our basic concept is to use Cu overburden to fabricate micrometer copper structures. Cyanine dye was used as an inhibiting additive and was not classified as one of the typical three types of additives described above. We have shown that Basic Red 12, which is a cyanine dye, strongly suppressed Cu deposition and affected the BUF process [18]. When this additive was added, Cu overburden was observed on the surface to have features without accelerators. Moffat et al. proposed a curvature enhanced accelerator coverage (CEAC)

model to explain the origin of Cu overburden in solution containing accelerating additives. According to the CEAC model, Cu overburden is attributed to the increase of a local coverage of accelerating additives in the vicinity of the feature. The CEAC model, however, cannot be applied to the Cu overburden in solution containing inhibiting additives such as Basic Red 12 and we proposed that diffusion-adsorption consumption of Basic Red 12 is the origin of the selective deposition of Cu [19]. The detailed mechanism of the role of Basic Red 12 is, however, not clear yet.

It is essential to understand the role of additives in the electrochemical deposition process to control the selective deposition. For that purpose, potential dependent adsorption/desorption behavior of Basic Red 12 on electrode surfaces should be understood. Vibrational spectroscopy is indispensable for obtaining detailed information on structures and orientations of adsorbed molecules. Among several types of vibrational spectroscopic techniques having monolayer sensitivity, surface enhanced Raman spectroscopy (SERS) is a powerful tool for obtaining detailed information on adsorption structures and orientations of molecules [20, 21, 22, 23, 24].

4.2 Results

4.2.1 Anisotropic copper deposition with varying an additive concentration

Figure 4.1 shows the tilted SEM images of electroplated Cu surfaces on the features with varying Basic Red 12 concentrations. Figure 4.1 also shows a substrate surface before plating, which had the 0.25 μm wide trenches and was completely covered by Cu seed layer. The corresponding Cu thicknesses on the feature and on the flat surface are indicated in Fig. 4.2.

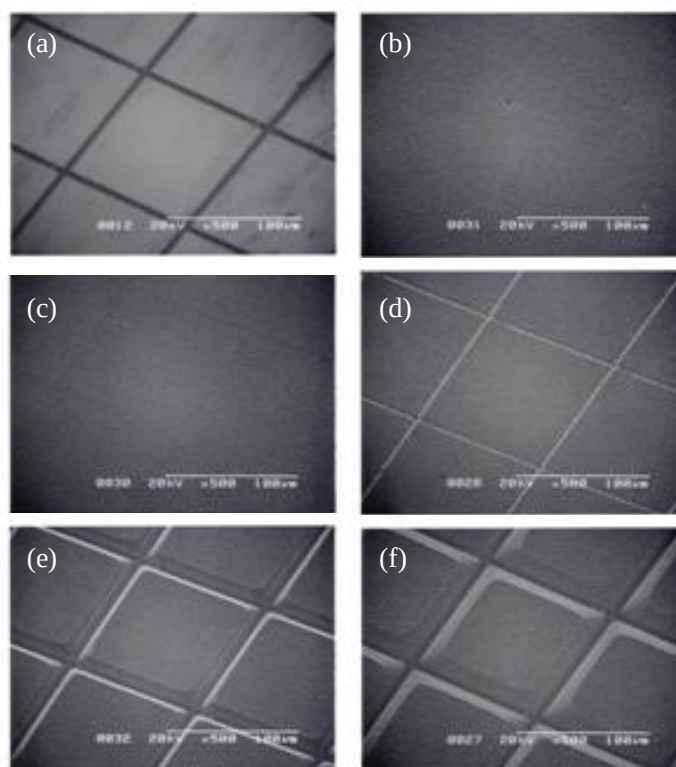


Fig. 4.1 SEM images of patterned wafer surface as function of Basic Red 12 concentration in electrolyte. (a) Before plating (b) 0 mol/dm³ (c) 0.6×10^{-5} mol/dm³ (d) 1.3×10^{-5} mol/dm³ (e) 1.9×10^{-5} mol/dm³ (f) 2.5×10^{-5} mol/dm³. Copper was electroplated at 1.0 A/dm² for 10 min.

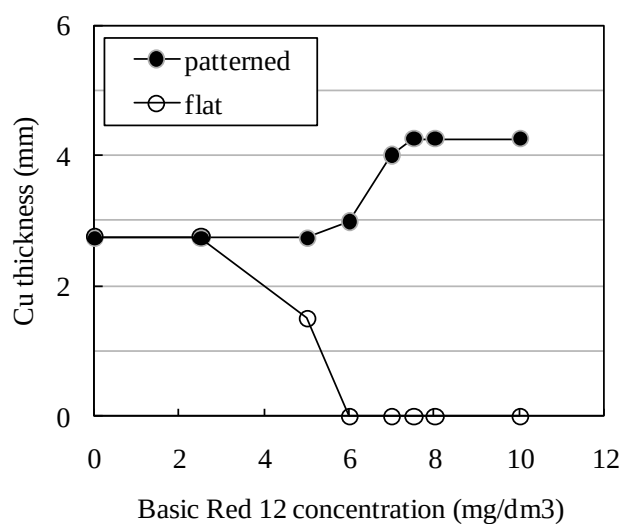


Fig. 4.2 Basic Red 12 concentration dependence of Cu thickness on patterned region and flat region at 1.0 A/dm² for 10 min.

In the concentration range of $1.8\text{--}2.5 \times 10^{-5} \text{ mol/dm}^3$, Cu growth was suppressed on the flat surface, and flattened pyramid-like Cu bumps were grown on the feature. Copper thickness on the feature was $4 \mu\text{m}$ in the concentration range of $1.8\text{--}2.5 \times 10^{-5} \text{ mol/dm}^3$. Copper thickness on the flat surface was less than $0.1 \mu\text{m}$. As described above, the ratio between the Cu thickness on the feature and on the flat surface was approximately 40:1. Despite the all of the surface being electrochemically active, the ratio of the copper thickness was very large. Lateral growth of Cu from the Cu bump on the feature was eliminated. When the Basic Red 12 concentration decreased to 5 mg/dm^3 , Cu thickness on the features was thicker than on the flat surface. In the case of a low concentration of Basic Red 12 ($0\text{--}0.6 \times 10^{-5} \text{ mol/dm}^3$), the plated surface was flat. Copper thickness on the feature was equal to the flat surface. Adding more than $1.3 \times 10^{-5} \text{ mol/dm}^3$ Basic Red 12 made selective deposition feasible. The angle of the bevel at the plated Cu on the feature decreased as Basic Red 12 concentration increased in the bath.

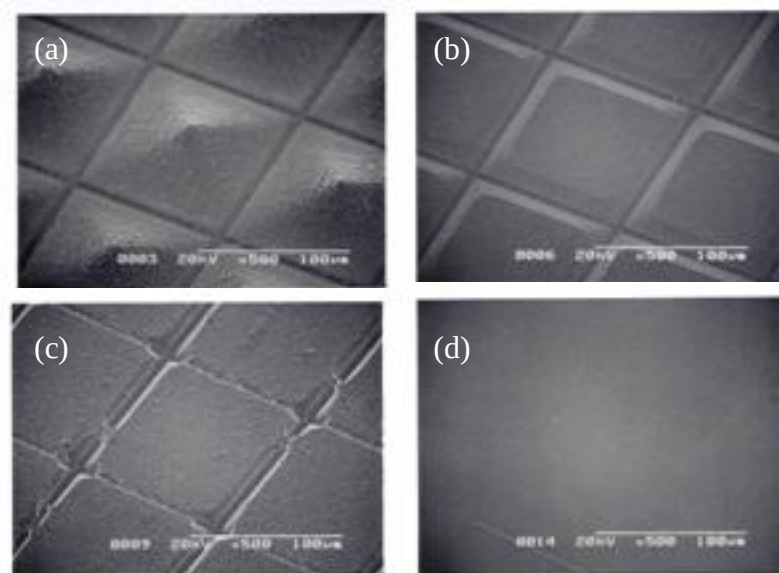


Fig. 4.3 SEM images of patterned wafer surface as function of plating current density (a) 0.5 A/dm^2 , 20 min (b) 1.0 A/dm^2 , 10 min (c) 1.25 A/dm^2 , 8 min (d) 1.5 A/dm^2 , 6.7 min, in electrolyte containing $1.8 \times 10^{-5} \text{ mol/dm}^3$ Basic Red 12.

4.2.2 Anisotropic copper deposition with varying an additive concentration

Figure 4.3 shows the tilted SEM images of electroplated Cu surfaces on the features with varying plating current density in the solution containing $1.8 \times 10^{-5} \text{ mol/dm}^3$ Basic Red 12. The charge at each plating process remained constant. The shapes and thickness of plated Cu changed with the current density. For 0.5 A/dm^2 , plated Cu was pyramid-like. When the current density increased to 1.25 A/dm^2 , Cu deposition was observed on a part of the flat surface. At the current density of 1.5 A/dm^2 , plated Cu was flat over the surface and no selective deposition was observed. The selectivity of plating between patterned surface and flat surface decreased as current density increased. Meanwhile, Cu thickness on the feature varied over the plated area, especially at lower current density.

4.3 Discussion

Copper overburden is caused by accelerators that adsorb on the Cu surface without being incorporated into deposited Cu and accumulate over the feature. Cu overburden was observed in the electrolyte with Basic Red 12 that has only an inhibiting effect on Cu deposition [18]. This phenomenon is not simply explained by the accelerator model. In CEAE, Cu overburden is formed by enrichment of accelerators on the deposited Cu surface. The extent and magnitude of overburden is a function of the feature size and pattern density. The differences in Cu thickness on the feature and on the flat surface, which correspond to selectivity of plating, depend on the surface coverage of accelerators as determined by pattern size and density of the feature. One plausible explanation for the selectivity of plating is the inhomogeneity of the inhibiting additive concentration enhanced by the patterned regions on the surface. The inhomogeneity of the additive concentration can be explained on the basis of the diffusion-adsorption consumption of an inhibiting additive mechanism. The consumption of additives on the patterned surface has been previously reported [16-17]. In this mechanism, Cu overburden may be formed by maintaining the inhibiting additive depletion

over the feature. The morphology of the deposited Cu was varied by the Basic Red 12 concentration and current density. The shape-change dependence of Basic Red 12 concentration in Fig. 4.1 indicates that the concentration of 6 mg/dm^3 in the electrolyte is necessary to suppress the Cu deposition on the flat surface. Current density-dependent selectivity of plating is interrupted by the change in the inhibiting effect of Cu deposition. At the lower current density in Fig. 4.4, the inhibiting effect was maintained on the flat surface but not the patterned region. At the higher current density, inhibiting additives cannot maintain a strong enough inhibiting effect to selectively deposit Cu. It is difficult to suppress the Cu deposition on all surfaces including the flat surface by using inhibiting additives since the Cu deposition overpotential increases at higher current densities. For this reason, selective deposition was not observed at the higher current density, although the additive concentration field enhanced by the patterned regions was expected to be formed. The difference in Cu thickness on the feature and the flat surface is determined by an inhibiting additive concentration field and suppressing effects of additives. The suppressing effect of additives varies with additive molecules. The strong suppressing effect on the surface and the relatively high concentration depletion on the feature compared to the flat surface are desirable to selectively deposit Cu. The diffusion-adsorption consumption of an inhibiting additive mechanism has an advantage to achieve high selectivity of plating. In this mechanism, we can keep a low plating rate on the flat surface to use additives that strongly suppress Cu deposition, such as Basic Red 12. In the CEAE, it is difficult to suppress the Cu deposition on the flat surface to achieve high selectivity between the patterned and flat regions. The morphology of the deposited Cu was controlled by the Basic Red 12 concentration and current density. A pyramid array could be fabricated with this process. The diffusion-adsorption consumption of an inhibiting additive mechanism cannot explain the shape of deposited Cu as shown in Fig. 4.3. The shape variation of plated Cu with current

density is similar to that of electroless deposited Ni bump with a Pb^{2+} additive.⁷ These results indicate that additive adsorption affects the shape variation of Cu. The mechanism of the selectivity of plating is unclear in this section. Further experimental studies are required to explain the shape change of deposited Cu and a role of the additives in the deposition process. Further experimental studies are required to explain the change in shape of deposited Cu and the role of the additives in the deposition process. Electrochemical and spectroscopic studies are currently under way.

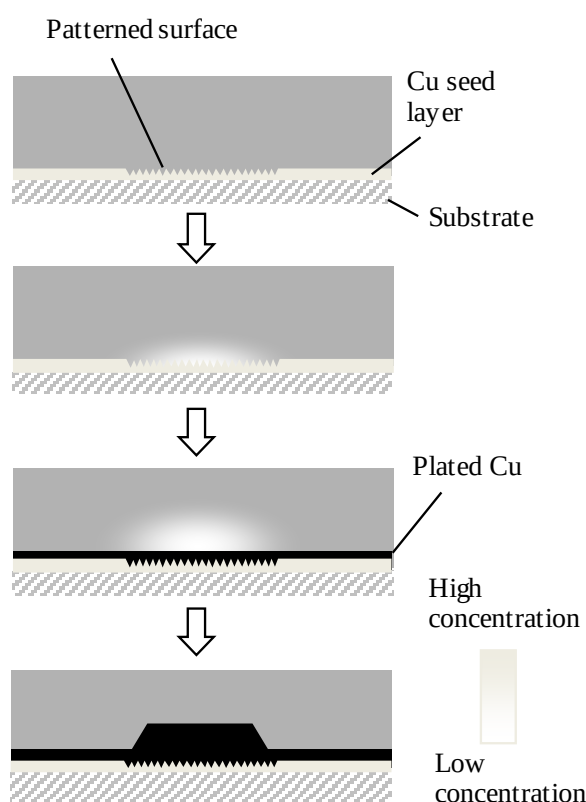


Figure 4.4. Schematic diagrams of additive distribution on the surface and in the electrolyte during deposition by the diffusion-adsorption consumption of an inhibiting additive model.

4.4 Conclusions

Copper was selectively and anisotropically electroplated using an inhibiting additive Basic Red 12 and features on the substrate. We used Cu overburden to selectively and anisotropically deposit the copper. When Basic Red 12 was added to the electrolyte, Cu overburden was observed on the surface to have features without accelerators. The shapes of the deposited copper varied as a function of the additive concentration and plating current density. This process is applied in fabricating micrometer copper structures without a patterned resist layer.

References

- [1] V.M. Dubin, Y. Shacham-Diamand, B. Zhoo, P. K. Vasudev, and C. H. Ting, J. Electrochem. Soc., vol. 144, p. 898, 1997.
- [2] P.C. Hidber, P. F. Nealey, W. Helbig, and G. M. Whitesides, Langmuir, vol. 12, p. 5209, 1996.
- [3] N. D. Sankir and R. O. Claus, Journal of Materials Processing Technology, vol. 196, p. 155, 2008.
- [4] M. Geissler, H. Kind, P. Schmidt-Winkel, B. Michel, and E. Delamarche, Langmuir, vol. 19, p. 6238, 2003.
- [5] T. R. Hendricks and I. Lee, Thin Solid Films, vol. 515, p. 2347, 2006.
- [6] C. S. Lin, C. Y. Lee, J. H. Yang, and Y. S. Huang, Electrochem. Solid-State Lett., vol. 8, p. C125, 2005.
- [7] A. M. T. van der Putten and J. W. G. de Bakker, J. Electrochem. Soc., vol. 140, p. 2221, 1993.
- [8] S. Zhang, J. De Baets, M. Vereeken, A. Vervaet, and A. Van Calster, J. Electrochem. Soc., vol. 146, p. 2870, 1999.
- [9] J. Reid, Jpn. J. Appl. Phys., vol. 40, p. 2650, 2001.
- [10] S. Soukane, S. Sen, and T. S. Cale, J. Electrochem. Soc., vol. 149, p. C74, 2002.
- [11] M. Hasegawa, Y. Negishi, T. Nakanishi, and T. Osaka, J. Electrochem. Soc., vol. 152, p. C221, 2005.
- [12] S.-K. Kim, D. Josell, and T. P. Moffat, J. Electrochem. Soc., vol. 153, p. C826, 2006.
- [13] T. P. Moffat, D. Wheeler, S. -K. Kim, and D. Josell, Electrochim. Acta, vol. 53, p. 145, 2007.
- [14] Y. H. Im, M. O. Bloomfield, S. Sen, and T. S. Cale, Electrochem. Solid-State Lett., vol. 6, p. C42, 2003.
- [15] P.C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, IBM J. Res. Dev., vol. 42, p. 567, 1998.
- [16] M. Hayase, M. Taketani, T. Hatsukawa, and K. Hayabusa, Electrochem. Solid-State Lett., vol. 6, p. C92, 2003.
- [17] R. Akolkar and V. Dubin, Electrochem. Solid-State Lett., vol. 10, p. D55, 2007.
- [18] T. Haba, T. Itabashi, H. Akahoshi, and H. Miyazaki, Advanced Metallization Conference 2002, B. M. Melnick, T. S. Cale, S. Zaima, and T. Ohta, Editors, p. 361, Materials Research Society, 2003.

- [19] M. Lefebvre, G. Allardyce, M. Seita, H. Tsuchida, M. Kusaka, and S. Hayashi, *Circuit World*, vol. 29(2), p. 9, 2003.

Chapter 5

Electrochemical and In Situ SERS Studies on the Role of Inhibiting Additives in Selective Electrodeposition of Copper in Sulfuric Acid

5.1 Introduction

Cu electrodeposition from acidic sulfate solution has been widely investigated because of its technological importance [1-3] and selective and anisotropic Cu deposition is one of the most important technologies in device processing as copper interconnects can be fabricated without resist mask. Various additives in a solution have been used to control the shape of Cu deposits as accelerator, suppressor or leveler [4]. Selective and anisotropic Cu deposition is, however, difficult to achieve since electrodeposition process is generally non-selective and isotropic.

Recently, we demonstrated that the selective and anisotropic Cu electrodeposition can be realized using an inhibiting additive, 2-[3-(1, 3-Dihydro-1, 3, 3-trimethyl-2H-indol-2-ylidene)-1-propenyl]-1, 3, 3-trimethyl-3H-indolium chloride (Basic Red 12) [5-6]. Figure 5.1 shows the SEM images of the Cu deposit, which was electrodeposited in an acidic CuSO₄ solution containing Basic Red 12 as an additive on the patterned wafer surface.² Preferential deposition of Cu, i.e., Cu overburden, took place on trench arrays of sub-micron line width and space. According to a curvature enhanced accelerator coverage (CEAC) model, the origin of Cu overburden in solution containing accelerating additives is attributed to the increase of

² The patterned Si wafers covered with sputtered Cu had a trench pattern of 0.25 μm wide and 0.5 μm deep at a 0.5 μm pitch. The patterned regions are 15 μm wide and are separated by 15 μm wide flat regions.

a local coverage of accelerating additives at the feature. The CEAC model, however, cannot be applied to the Cu overburden in solution containing inhibiting additives such as Basic Red 12 and we proposed that diffusion-adsorption consumption of Basic Red 12 is the origin of the selective deposition of Cu [5]. The detailed mechanism of the role of Basic Red 12 is, however, not clear yet.

In this section, potential dependent adsorption/desorption behavior of Basic Red 12 on electrode surfaces is studied to clarify the role of an inhibiting additive, Basic Red 12, for selective electrodeposition of Cu surface in sulfuric acid solutions by using linear sweep voltammetry (LSV), cyclic voltammetry (CV) and in situ surface enhanced Raman scattering (SERS), which is a powerful tool for obtaining detailed information on adsorption structures and orientations of molecules [7-11], measurements.

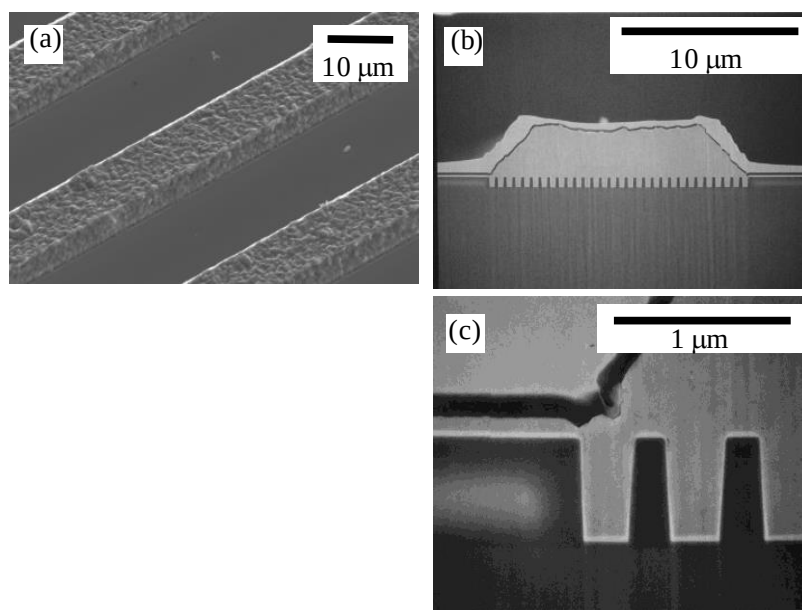


Figure 5.1 SEM images of the electrodeposited Cu on the patterned wafer surface covered with Cu seed layer (a) top view (b, c) cross-sectional views of two different magnifications. Cu was deposited in a solution containing $2.5 \times 10^{-5} \text{ mol/dm}^3$ Basic Red 12 at 2.5 mA/cm^2 . Carbon coating was deposited on Cu prior to focused ion beam milling.

5.2 Results and Discussion

5.2.1 Electrochemical measurements

Figure 5.2 shows CVs of an Au electrode in a solution containing 0.3 M CuSO₄, 1.8 M H₂SO₄, 1.6 × 10⁻³ M HCl and various concentrations of Basic Red 12 in the potential range between +0.2 V and -0.5 V. While the deposition of Cu started at + 0.1 V in the solution without Basic Red 12, it started from more negative potential with Basic Red 12, showing the inhibition effect of Basic Red 12 on Cu deposition. The higher the concentration, the more negative the onset for Cu deposition. The current reached limited current, which flowed up to very positive potential in the backward scan, showing that although Basic Red 12 inhibits the Cu deposition at the initial stage of deposition, inhibition effect is lost once copper deposition has started.

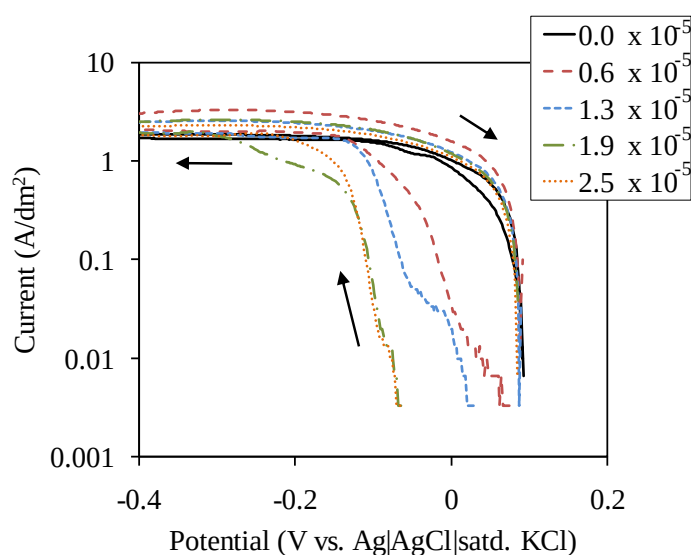


Figure 5.2 CVs of a Au electrode in a solution containing 0.3 M CuSO₄, 1.8 M H₂SO₄, 1.6 × 10⁻³ M HCl and Basic Red 12 (0 to 2.5 × 10⁻⁵ M) of an. Scan rate: 1 mV/s.

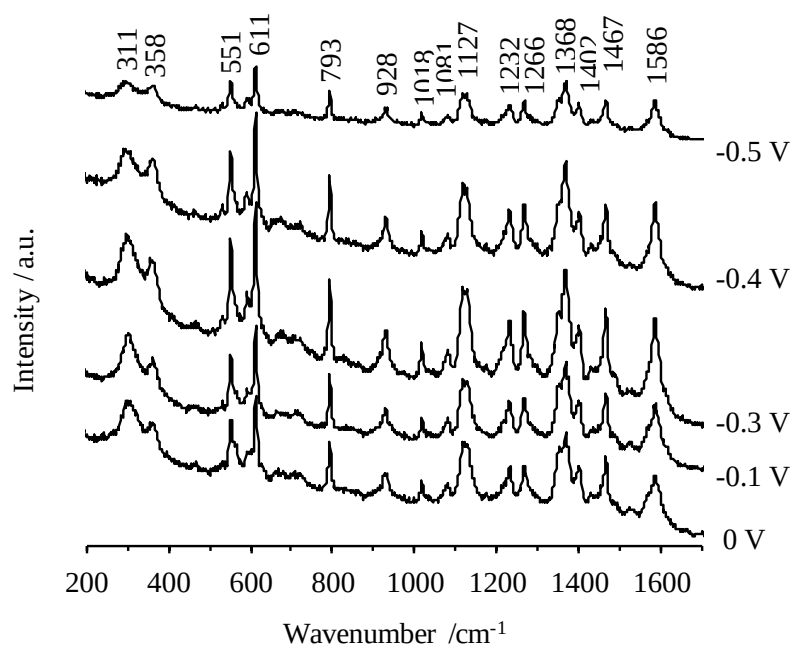


Figure 5.3 In situ SERS spectra of Basic Red 12 on a Cu electrode in a solution containing 1.8 M H_2SO_4 , 1.6×10^{-3} M HCl and 2.5×10^{-5} M Basic Red 12 at potentials from 0 V to -0.5 V.

Table 5.1 List of major SERS bands of Basic Red 12 and corresponding assignments

In situ	Calculation	Band assignment
551	533	Heteroaromatic condensed ring C—N bending
611	604	Heteroaromatic condensed ring vibrations
793	—	—
928	931	Olefinic C=C bending, Heteroaromatic condensed ring vibrations
—	984	Heteroaromatic condensed ring C=C stretching, Olefinic C=C stretching
1018	1013	Heteroaromatic condensed ring C=C stretching
1081	1051	Heteroaromatic condensed ring vibrations
1127	1111	CH_3 rocking, Heteroaromatic condensed ring C—H rocking
1232	1179	Heteroaromatic condensed ring vibrations
1266	1276	Heteroaromatic condensed ring C—H rocking
1368	1339	Heteroaromatic condensed ring C=C stretching
1402	1397	CH_3 wagging
1467	1436/1456	CH_3 scissoring
1586	1577	Olefinic C=C stretching

*Peaks at 311 and 358 cm^{-1} are assigned to the Cu—Cl of adsorbed chloride ion.

5.2.2 In situ SERS measurements

Figure 5.3 shows in situ SERS spectra at various potentials for a Cu electrode in a solution containing 1.8 M H₂SO₄, 1.6 x 10⁻³ M HCl, and 2.5 x 10⁻⁵ M Basic Red 12. Well-characterized spectra of Basic Red 12 were obtained for the entire potential region. Table 5.1 summarizes the band assignments. The peak intensity was dependent on the potential, but the relative peak intensities and peak positions were not, showing that the potential did not affect the orientation or structure but rather the surface coverage of Basic Red 12 on Cu.

Because the SERS peak intensity change is affected not only by the coverage of Basic Red 12 but also by the morphology of the electrode surface, the latter contribution was removed by normalizing the SERS spectra with the intensity of the background plasmonic emission [9]. Figure 5.4 shows the potential dependence of the normalized intensity of the 611-cm⁻¹ peak during a potential scan from +1.0 to -0.5 V at a scan rate of 1 mV/s. The SERS peak intensity continuously increased at first as the potential became negative but then started to decrease around 0 V at the Cu electrode. Similar potential dependence was observed at a Au electrode in a solution with 0.3 M CuSO₄, but the signal started to decrease at +0.4 V without the CuSO₄. The presence of Cu on the Au surface seemed to increase the peak intensity. The peak intensity was also smaller during the positive scan than in the negative scan. The coverage of Basic Red 12 decreased after Cu deposition in the potential range from 0 to -0.5 V. Both the Cu deposition current in the CV results and the peak intensity of the in situ SERS spectra showed hysteresis. After Cu deposition, the deposition current increased, while the SERS peak intensity decreased. In the negative potential range from -0.3 to -0.5 V, the roughness of the deposited Cu surface had to increase, because the rate of the Cu deposition reaction is limited by the diffusion of Cu²⁺ ions. Consequently, decreases in the peak intensity mean decreases in the surface coverage of Basic Red 12.

Basic Red 12 strongly adsorbs over the surface before Cu deposition and then inhibits the deposition. This inhibiting effect increased with the Basic Red 12 concentration. Once Cu electrodeposition starts on some areas, the Basic Red 12 desorbs or decomposes on those areas. The decreased Basic Red 12 concentration on those specific areas leads to preferential growth of Cu over other areas. This demonstrates that a difference in surface roughness and a proper current density and Basic Red 12 concentration are necessary for selective deposition of Cu [5]. These results further indicate that Basic Red 12 generates a concentration gradient due to its consumption on a Cu surface having features. In the diffusion-adsorption consumption of the inhibiting-additive mechanism, a Cu overburden may be formed by depletion of the inhibiting additive near features in the plating solution.

The peaks at 311 and 358 cm^{-1} were assigned to the Cu-Cl bonds of adsorbed Cl^- ions. Figure 5.5 shows the potential-dependent peak position shift of the Raman spectra. The peaks attributed to Basic Red 12 did not change, whereas the Cu-Cl peaks shifted to lower values. This suggests that Basic Red 12 does not change its structure during the Cu deposition reaction, and that the adsorption state of Cl^- ions changes with the electrode potential. These results suggest a reaction model for Basic Red 12 on the surface, as shown in Fig. 5.6. Basic Red 12 adsorbs to the Cu surface via Cl^- ions and suppresses the Cu deposition reaction. As the overvoltage increases, the Cu deposition rate increases, while at the same time the interaction between the Cl^- ions and Basic Red 12 weakens. As a result, the Basic Red 12 desorbs from the surface, and a decrease in its peak intensity is observed. Further investigation is necessary to clarify the role of the Cl^- ions.

5.3 Conclusions

The role of Basic Red 12, an inhibiting additive, in selective Cu deposition was clarified by LSV, CV, and in situ SERS measurements. The normalized SERS peak intensity of Basic

Red 12 varied with the potential, but no change in the peak position was observed. Both the SERS peak intensity and the current for Cu deposition showed hysteresis in the potential range between +0.1 and -0.5 V. These results indicate that the coverage of Basic Red 12 varied with the potential, leading to inhomogeneity of the inhibition effect of Basic Red 12 on the Cu surface, thus enhancing the difference in thickness of the deposited Cu.

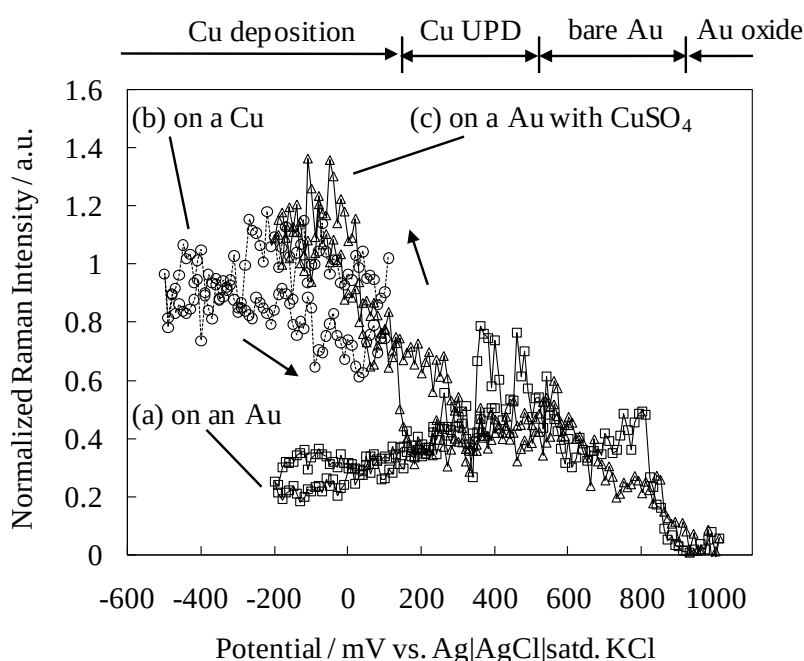


Figure 5.4 Potential dependence of the normalized SERS intensity of the 611-cm⁻¹ band during a potential scan (scan rate: 1 mV/s) in a solution containing 1.8 M H₂SO₄, 1.6 × 10⁻³ M HCl, and 2.5 × 10⁻⁵ M Basic Red 12 at (a) a Au electrode, (b) a Cu electrode, and (c) a Au electrode with 0.3 M CuSO₄.

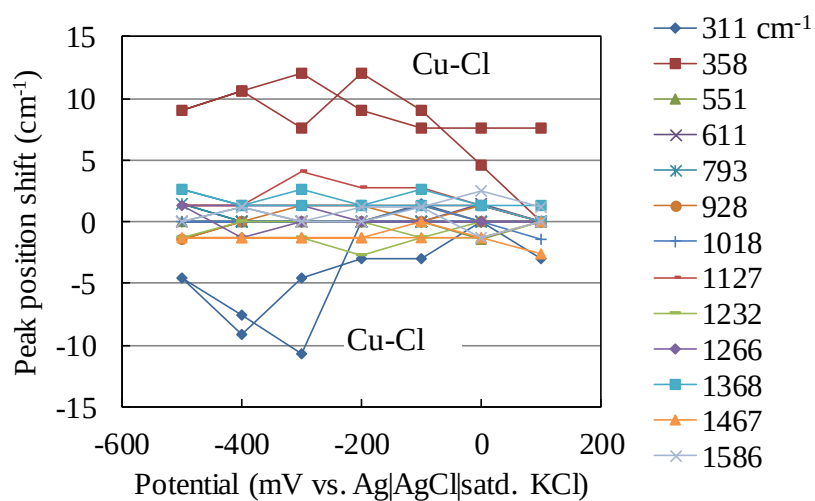


Figure 5.5 Potential dependence of the peak position shift for in situ SERS of Basic Red 12.

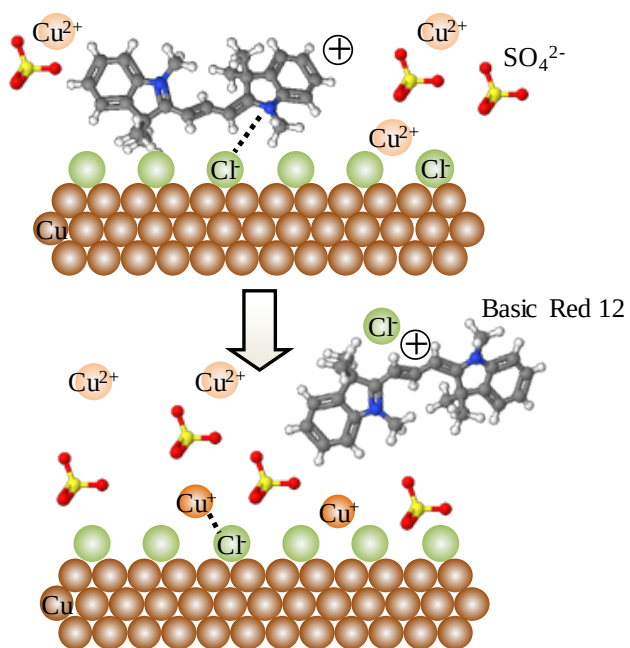


Figure 5.6 Schematic diagrams of Basic Red 12 on the Cu surface in the electrolyte during Cu deposition.

References

- [1] P.C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, H. Deligianni, IBM J. Res. Dev., vol. 4, p. 567, 1998.
- [2] A. Bhatnagar et al., Solid State Technology, vol. 52, p. 16, 2009.
- [3] M. Lefebvre, G. Allardyce, M. Seita, H. Tsuchida, M. Kusaka, S. Hayashi, Circuit World, vol. 29, p. 9, 2003.
- [4] T. P. Moffat, D. Wheeler, S. -K. Kim, D. Josell, Electrochim. Acta, vol. 53, p. 145, 2007.
- [5] T. Haba, H. Suzuki, H. Yoshida, H. Akahoshi, A. Chinda, Electrochem. Solid-State Lett., vol. 13, p. D23, 2010.
- [6] H. Nakano, H. Suzuki, T. Haba, H. Yoshida, A. Chinda, H. Akahoshi, Proceedings of 60th Electronics Components and Technology Conference 2010, Las Vegas, Nevada, IEEE, p. 612, 2010.
- [7] J. P. Healy, D. Pletcher, M. Goodenough, J. Electroanal. Chem., vol. 338, p. 155, 1992.
- [8] G. A. Hope, R. Woods, J. Electrochem. Soc., vol. 151, p. C550, 2004.
- [9] Z. D. Schultz, Z. V. Feng, M. E. Biggin, A. A. Gewirth, J. Electrochem. Soc., vol. 153, p. C97, 2006.
- [10] B. Bozzini, L. D'urzo, M. Re, F. De Riccardis, J. Appl. Electrochem., vol. 38, p. 1561, 2008.
- [11] K. Ikeda, N. Fujimoto, H. Uehara, K. Uosaki, Chem. Phys. Lett., vol. 460, p. 205, 2008.
- [12] T. Haba, T. Itabashi, H. Akahoshi, H. Miyazaki, Proceedings of Advanced Metallization Conference 2002, ed. by B. M. Melnick, T. S. Cale, S. Zaima, T. Ohta, MRS, pp. 361, 2003.

Chapter 6

General Conclusion and Future Prospects

6.1 General conclusion

This dissertation has investigated the mechanisms of an anisotropic electrochemical copper deposition reaction with an additive in solution, by using electrochemical measurements, numerical simulation, shape observation of deposited metal by scanning and transmission electron microscopy (SEM and TEM), and in situ surface-enhanced Raman spectroscopy (SERS).

In section 3.2, the role of additives in the copper electroplating bath of the damascene process was investigated. A bottom-up filling model was proposed and confirmed by comparing experimental and simulation results. Janus Green B and Basic Blue 3, two dyes that adsorb on the copper surface and suppress copper deposition, were examined for use as additives to improve the filling capability. Damascene copper grew uniformly in a bath that contained Basic Blue 3, but it grew preferentially from the bottom of a trench with Janus Green B. Addition of Janus Green B thus produced a continuous concentration gradient in a sub-micrometer trench when its diffusion and consumption rates on the copper surface were well balanced. Filling profiles were estimated by numerical simulation using parameters determined by an electrochemical method. These profiles agreed well with the experimental results.

In section 3.3, to completely fill 80-nm-wide trenches with a high aspect ratio (>6) by copper electroplating, the influence of pulse-wave electroplating conditions was investigated. The peak current density and current-off time during pulse-wave plating were found to affect bottom-up filling. Specifically, bottom-up filling was confirmed to occur when the peak

current density, current-on time, and current-off time were 100 mA/cm², 3 ms, and 300 ms, respectively. The microstructure of the trench was observed by TEM before and after annealing at 673 K. After annealing, the grain size increased and grains could span the trench width. The sizes of grains formed by pulse-wave plating were 37.5 and 96 nm before and after annealing, respectively. These values were similar to those for DC plating. Pulse wave-electroplating is, therefore, promising as a step in the dual damascene process for fabricating very narrow, high-aspect-ratio copper wiring.

In section 3.4, the effect of the aspect ratio of very narrow copper interconnects less than 100-nm wide on the resistivity was discussed. From longitudinal and cross-sectional TEM observation, many very small grains were observed at trench bottoms, while larger grain sizes were predominant in the upper portions of the interconnects. The resistivity was found to decrease significantly with increased aspect ratio for fine-pitch copper wiring because of the larger grain size distributions in the upper portions of the interconnects with higher aspect ratios. This result demonstrates that control of the aspect ratio will be effective for controlling the resistivity in future copper interconnects with very narrow and shallow dimensions.

Section 3.5 evaluated the grain size distributions and average grain sizes along the longitudinal direction of 50-, 70- and 80-nm-wide copper interconnects and compared the resistivities. After annealing, the standard deviation of the grain sizes in the 50-nm copper interconnects increased to 27.5 nm, and the average grain size grew larger than that of the as-deposited interconnects. Furthermore, the standard deviation of the grain sizes in the normal distribution histogram for the 50-nm wires was found to be much smaller than those for the 70- and 80-nm wires after annealing. This implies that adequate grain growth should not be expected in the very narrow (less than 50 nm) copper interconnects of the future if they are made by the conventional annealing process.

Next, chapter 4 described selective, anisotropic electroplating for a resistless metallization process using a copper overburden with an inhibiting additive. A dye, Basic Red 12 (2-[3-(1, 3-Dihydro-1, 3, 3-trimethyl-2H-indol-2-ylidene)-1-propenyl]-1, 3, 3-trimethyl-3H-indolium chloride), was used as the inhibiting additive in the electroplating bath. When this additive was added, the copper overburden was observed on the surface to form features without an accelerating additive. The shapes of the deposited copper varied as a function of the additive concentration and the plating current density. This process shows significant advantages for fabricating micrometer-scale copper structures without a patterned resist layer.

In chapter 5, the role of the inhibiting additive in selective copper deposition was investigated with linear sweep and cyclic voltammetry and in situ SERS measurements. The SERS peak intensity for Basic Red 12 was normalized. The copper deposition current showed hysteresis, indicating that the coverage of Basic Red 12 varied with the potential. This leads to inhomogeneity of the inhibition effect of Basic Red 12 on the copper surface.

6.2 Future Prospects

This dissertation has examined the influence of additives on the shapes and properties of copper deposited by an anisotropic electrodeposition reaction. Application of these results should enable progress in developing manufacturing processes using anisotropic deposition for fine copper wiring.

The downsizing trend of current LSI technology is steadily approaching its physical limit, so the development of novel devices is necessary. Although copper interconnects have been used for LSI devices for 20 years, the increase in the resistance of copper interconnects is becoming too large to ignore. Therefore, we should be trying to develop new materials and processes for interconnection by applying electrochemical methods.

List of Publications

- (1) A. Sano, K. Kobayashi, H. Akahoshi, T. Itabashi, **T. Haba**, S. Fukada, H. Miyazaki: "Filling Profile Simulations for Copper Electroplating Process", J. Surf. Finish. Soc. Jpn., Vol. 52, No.1, p. 54-55, 2001.
- (2) **T. Haba**, T. Itabashi, H. Akahoshi, A. Sano, K. Kobayashi, H. Miyazaki: "Electrochemical and simulative studies of trench filling mechanisms in the copper damascene electroplating process", Materials transactions, Vol. 43, No. 7, p. 1593-1598, 2002.
- (3) Y. Chonan, J. Onuki, T. Nagano, K. Khoo, T. Aoyama, H. Akahoshi, **T. Haba**, T. Saito: "Filling 80-nm-Wide and High-Aspect-Ratio Trench with Pulse Wave Copper Electroplating and Observation of the Microstructure", Japanese Journal of Applied Physics, Vol. 45, No. 11, p. 8604-8607, 2006.
- (4) K. Khoo, J. Onuki, T. Nagano, S. Tashiro, Y. Chonan, H. Akahoshi, **T. Haba**, T. Tobita, M. Chiba, K. Ishikawa: "Microstructures of 50-nm Cu Interconnects along the Longitudinal Direction", Materials transactions, Vol. 48, No. 10, p. 2703-2707, 2007.
- (5) K. Khoo, J. Onuki, T. Nagano, Y. Chonan, H. Akahoshi, **T. Haba**, T. Tobita, M. Chiba, K. Ishikawa: "Aspect Ratio Dependence of the Resistivity of Fine Line Cu Interconnects", Japanese Journal of Applied Physics, Vol. 46, No. 7A, p. 4070–4073, 2007.
- (6) **T. Haba**, H. Suzuki, H. Yoshida, H. Akahoshi, A. Chinda: "Selective and Anisotropic Copper Electroplating Using Copper Overburden with an Inhibiting Additive", Electrochem. Solid-State Lett., Vol. 13, No. 5, p. D23-D25, 2010.
- (7) H. Nakano, H. Suzuki, **T. Haba**, H. Yoshida, A. Chinda, and H. Aakahoshi: "Advanced Trench Filling Process by Selective Copper Electrodeposition for Ultra Fine Printed Wiring Board Fabrication", IEICE TRANSACTIONS on Electronics C, Vol. J94-C, No. 11, p.380-385, 2011.
- (8) **T. Haba**, K. Ikeda, K. Uosaki: "Electrochemical and in situ SERS study of the role of an inhibiting additive in selective electrodeposition of copper in sulfuric acid", Electrochemistry Communications, Vol. 98, p. 19-22, 2019.

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