FABRICATION OF GaAs-BASED INTEGRATED HALF AND FULL ADDERS BY NOVEL HEXAGONAL BDD QUANTUM CIRCUIT APPROACH

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Abstract

Feasibility of a novel hexagonal binary decision diagram (BDD) quantum circuit approach based on Schottky wrap gate (WPG) control of GaAs/AlGaAs hexagonal nanowire network has been demonstrated through fabrication of half adders and full adders. Quantum BDD node devices were designed and realized utilizing WPG-controlled quantum wire (QWR) and single electron (SE) switches. BDD half sum and carry elements of a half adder were fabricated by integrating the WPG BDD node devices and they operated correctly through either quantum transport at low temperature or many electron classical transport at room temperature. Successful design of hexagonal BDD full adders for arbitrary bits on a hexagonal network without nanowire crossover and fabrication of QWR-based BDD 2-bit full adder on the AlGaAs/GaAs etched hexagonal nanowire network with node density of 10^7 cm^{-2} clearly indicated the capability of the present approach for large scale quantum device integration.

1. INTRODUCTION

Semiconductor quantum nanodevices and their integrated circuits are expected to play important roles in future information technology and multi-disciplinary nanotechnology covering chemistry and biology, for nano-sensing, nano-scale signal processing and nano-control. This is because the size of the nanodevices is essentially small, and dissipative quantum switches such as quantum wire transistors (QWRTrs) and single electron transistors (SETs) can operate near the quantum limit of power-delay product (PDP)[1]. They provide opportunities to realize traditional Boolean logic circuits at the smallest possible PDP and high circuit densities beyond the limits of silicon roadmap devices[2]. In the far future, non-dissipative semiconductor quantum circuits that realize massively parallel and highly sophisticated quantum computation/processing may be available, however, at present, there exists no realistic approach even for dissipative quantum circuits. This is because quantum devices are weak and sensitive, which makes it difficult to replace Si CMOS devices by quantum devices for conventional Boolean logic gate architecture that requires uniform and robust devices.

To overcome this situation, we have recently proposed a hexagonal binary decision diagram (BDD) quantum circuit approach for high density integration of III-V quantum devices[3,4]. The purpose of this paper is to investigate the feasibility of the novel hexagonal BDD quantum circuit approach for quantum LSIs (Q-LSIs) through design and fabrication of GaAs-based BDD half adder and full adder circuits.

2. CONCEPT OF HEXAGONAL BDD QUANTUM LOGIC CIRCUITS

2.1 Basic concept

The basic concept of the novel hexagonal BDD circuit is shown in **Fig. 1(a)**. The BDD is a digital logic architecture representing a logic function by a directed graph, which was originally proposed by Akers[5]. In the present approach, the BDD is implemented by a wired array of gated quantum BDD node devices on a hexagonal nanowire network. Each node device has one entry- and two exit-branches as shown in **Fig. 1(b)**. It selects one of exit-branches for the incoming information messenger depending on gate input x_i. Here, the messenger is either a single electron or a few electrons and is controlled through gate-controlled quantum transport as in quantum wire (QWR) or single electron (SE) devices. The value of the logic function, r_i, is determined by checking whether the root terminal is connected to terminal-1 or to terminal-0, moving the messenger from the root to the terminals. Paying attention to the basic three-fold symmetry of the node device configuration, we found that a hexagonal closed packed nanowire network shown in **Fig. 1(a)** is suitable for planar integration. Ungated portions of the network serve as interconnects. To form a graph representing a logic function, unnecessary branches are cut out.

Any combinational logic function can be implemented as BDD circuits[6]. As examples, hexagonal BDD implementations of AND, exclusive OR and NOR functions are shown in **Figs. 1(c)-(e)**, respectively. The AND and exclusive OR circuits work as a carry and a half sum of a half adder, respectively. Other basic logic functions, such as OR and NAND, can be also designed on a hexagon integrating within three node devices. Full adders, multipliers and other standard circuit blocks can be formed using multi-hexagon layouts. For a large logic system including feedback, the circuit is divided into fairly large BDD combinational logic blocks. Then, terminal outputs of each block are sent to a buffer register circuit consisting of QWRTrs, HEMTs and so on for 0/1 detection, possible amplification, voltage level shifting and timing control. Outputs of the register are returned to input gates of other circuit blocks. This allows a logic

system design at register transfer level using a suitable BDD logic partition theory.

Features of our novel approach are the following. Quantum devices are used for implementation and the circuit can operate with an ultra-small power-delay product near the quantum limit. This is because the BDD requires no large voltage gain, no precise input-output voltage matching, and no large current drivability of node devices, because there is no direct output-to-input cascade connection; therefore the present approach can use non-robust dissipative quantum switches. A hexagonal nanowire network structure promises high-density integration. Smaller device counts in BDD circuits than in logic gate circuits[6] also help dense integration. Furthermore, node devices are interconnected by nanowires without source/drain contacts and this avoids the serious contact problem in ULSIs. The absence of output-to-input cascade interconnections and the use of ungated nanowires as interconnects reduce the number of interconnection metalization levels and the average interconnection lengths.

2.2 Implementation

In this study, the hexagonal BDD quantum circuits were implemented on AlGaAs/GaAs etched hexagonal nanowire networks. Quantum node devices were realized by controlling the nanowire networks with nanometer-scale Schottky wrap gates (WPGs)[7,8], schematically shown in **Fig. 2(a)**. The WPG has a simple lateral structure suitable for planar integration and gives tight potential control. The confinement potential is stronger than that in the split gate structure. WPG BDD node devices utilizing QWR transport or SE transport are shown in **Figs. 2(b)-(d)**. The devices have basic Y-arrangement of three nanowire branches. The Branch having a single WPG shown in **Fig. 2(b)** operates as a QWRTr, where the nanowire is squeezed by depletion under suitable negative gate voltage. The branch having two nm-size WPGs with a narrow spacing shown in **Fig. 2(c)** forms double tunneling barriers and a quantum dot in between and operates as

a SET. The device in **Fig. 2(d)** also forms a dot in the node. SE node devices can realize ultra-low power consumption due to small current operation and PDP values can be close to the quantum limit[1]. On the other hand, the QWR node devices showing larger conductance values than those in the SE devices have the possibility to realize smaller delay times. Conductance quantization can give a gate voltage margin for on/off switching. By reducing gate length, capacitance values become small and the number of messenger electrons decreases, so that its PDP value will also be close to the quantum limit. In addition, the present approach is also applicable to Si on Insulator (SOI) structures and molecular nanowire networks, including multi-branch carbon nanotubes[9].

3. FABRICATION AND CHARACTERIZATION OF BDD DEVICES AND ADDER CIRCUITS

3.1 Fabrication

The WPG device fabrication process is simple, as follows. First, AlGaAs/GaAs hexagonal nanowire networks were formed on a conventional AlGaAs/GaAs heterostructure wafer using electron beam (EB) lithography and wet chemical etching. Typical geometrical wire width was 500 nm. After metalization of ohmic contacts for terminals, WPGs were formed on the nanowires by EB lithography, metal deposition, and lift-off process. WPG gate length for QWR and SE devices were 300 nm and 50 ~ 80 nm, respectively. For gate input interconnection in the integrated circuits, second-layer metalization was made by coating with SiO_2, forming contact holes with wet etching, metal deposition, and lift-off process. This WPG device/circuit fabrication process is compatible with that of mature III-V FETs and their circuits, which helps high-density integration and gives reproducibility and uniformity in the present circuit fabrication process.

3.2 WPG BDD quantum node device

SEM images of fabricated WPG QWR and SE branch-switch BDD node devices are shown **Figs. 3(a)** and **3(b)**, respectively. Quantum transport in the WPG BDD node devices was confirmed by conductance measurements on each exit branch switch. The results are shown in **Figs. 4**. At low temperature, the fabricated QWR branches showed clear conductance quantization and the SE branches showed clear conductance oscillations. The SE node-switch type device in **Fig. 2(d)** also showed clear conductance oscillations[3]. It is also seen that the WPG has an ideal characteristic for realizing sharp gate control near the pinch-off due to tight potential control. As shown in **Fig. 4(b)**, they could control current even when the temperature increased and the quantum transport vanished. This indicates that they can gradually change operational modes with increasing temperature from the single electron quantum regime to a few electron quantum regime, and finally to the many electron classical regime.

Fabricated WPG node devices also showed clear path switching characteristics by applying WPG voltage on each exit branch in complementary way at low temperature, where the WPG bias was adjusted to use conductance quantization or conductance oscillation peaks so that the operation was in the quantum regime. The switching operations were continued up to room temperature by adjusting gate bias and further increasing voltage swing [10], where the operational mode changed into the many electron classical regime.

3.2 Half adder

As fundamental logic elements in adders, carry out and half sum of a half adder were fabricated on a single AlGaAs/GaAs nanowire hexagon and characterized. An SEM image of the WPG BDD quantum circuit for half sum and its diagram are shown in **Figs. 5(a)** and **5(b)**,

respectively. In this circuit, three QWR-based node devices were integrated on the hexagon. Only a terminal-1 was used for output detection as shown in **Fig. 5(b)** and the logic was determined by checking whether the messenger reaches the terminal-1 or not. 2nd level interconnects for gate input connection were formed, which connected with suitable WPGs through contact holes. The fabricated circuit can also work as carry by exchanging gate inputs and terminals as shown in **Fig. 5(c)**.

Input/output waveforms of BDD carry under pulsed condition at 1.6 K is shown in **Fig. 6(a)**. The logic operation was tested by adjusting the d.c. bias for two node devices to cause path switching in the first conductance step and then correct output was obtained in the quantum regime. When the temperature increased to 300 K, the circuit could also gave correct output as shown in **Fig. 6(b)**. In this case, to keep the logic operation error-free, the gate bias was re-adjusted and the voltage swing was increased, which also increased the switching PDP value. This indicates that proposed BDD circuits can operate over a wide temperature range by trading off between PDP and temperature. **Figure 6(c)** shows input/output waveforms of BDD half sum at room temperature. This circuit also gave correct output, where three node devices took part in the operation. From these results, it is found that half adders can be realized with the present circuit approach. The results also indicate that the basic Boolean logic functions can be implemented by the WPG BDD quantum node devices.

3.4 Full adder

Hexagonal BDD adder circuits for arbitrary bits were designed by integrating BDD node devices. A possible design of an n-bit full adder is shown in **Fig. 7**. The circuit has complete hexagonal layout without nanowire crossover. The n-bit adder can be realized by stacking adder units shown in **Fig. 7** n times. Such a layout is similar to a ripple carry adder of CMOS logic

gates which is designed by stacking full adders. It is noted that the BDD adder unit sends its carry out signals to the next unit terminals, not to gate inputs. The number of BDD node devices in an adder unit is 11, whereas 24 transistors are required in a full adder of Si CMOS logic. Therefore, with the present approach, it seems possible to design complex combinatorial logic circuits with small device counts and small circuit areas.

To experimentally clarify the capability of the present approach for large-scale integration, a BDD 2-bit full adder circuit integrating WPG QWR node devices was fabricated on an etched GaAs hexagonal nanowire network. An SEM image of the fabricated circuit is shown in **Fig. 8**. In this circuit, 14 node devices were integrated. The 0-terminal was omitted for circuit simplicity. The fabrication process was identical to that used for BDD basic logic circuits and only two levels of metalization were used for WPG formation and gate input interconnections. The main circuit area was 30 μm x 15 μm and each hexagon had 4.5 μm x 2.5 μm area. This corresponded to a possible node device density of 10^7 devices/cm^2. Operation of this circuit has been under test at room temperature and correct outputs were partly obtained in the classical regime.

Reducing the nanowire width and hexagon size is necessary for high-density integration and operation in quantum regimes with small PDP at room temperature. For further reduction of the size, hexagonal networks utilizing embedded nanowires with a few 10 nm wire-widths have been studied utilizing selective MBE growth of the AlGaAs/GaAs and InAlAs/InGaAs systems. A minimum nanowire width of sub 10 nm has been realized in a linear array of QWR[11], and a hexagonal nanowire network with node density up to 10^8 cm^{-2} has been obtained in the InAlAs/InGaAs system[12].

4. CONCLUSIONS

A novel hexagonal BDD quantum circuit approach based on Schottky WPG control of a GaAs/AlGaAs hexagonal nanowire network has been demonstrated through the successful design and fabrication of half adders and full adders. Quantum BDD node devices were realized utilizing WPG-controlled quantum wire (QWR) and single electron (SE) switches. BDD half sum and carry circuits were fabricated by integrating WPG QWR BDD node devices and they operated correctly through either quantum transport at low temperature or classical many electron transport at room temperature. Successful design of arbitrary-bit full adders on hexagonal network without crossover and successful fabrication of a QWR-based BDD 2-bit full adder on the GaAs/AlGaAs etched hexagonal nanowire network with node density up to 10^7 cm^{-2} confirmed the capability of the present approach for large scale integration.

Acknowledgements --- The present study is supported financially in part by a Grant-in-Aid for Scientific Research A (#13305020), a Grant-in-Aid for Scientific Research B (#12555083) and a Grant-in-Aid for Encouragement of Young Scientists (#12750286) from the Ministry of Science, Technology, Education, Culture and Sports, Japan.

REFERENCES

[1] J. E. Mooji, Extended Abst. of 1993 Int. Conf. Solid State Devices and Materials, 339.

[2] International Technology Roadmap for Semiconductors 2000 Edition [online]. Available: http://public.itrs.net/

[3] S. Kasai, Y. Amemiya and H. Hasegawa, Tech. Dig. of 2000 Int. Electron Devices Meeting, 2000; 585.

[4] H. Hasegawa and S. Kasai, Physica E, 2001;10: 149.

[5] S. B. Akers, IEEE Trans. Compt., 1978; C27:509.

[6] K. Yano, Y. Sasaki, K. Rikino and K. Seki, IEEE J. Solid-State Circuits, 1996; 31:792.

[7] S. Kasai, K. Jinushi, H. Tomozawa and H. Hasegawa, Jpn. J. Appl. Phys., 1997; 36:1678.

[8] S. Kasai and H. Hasegawa, Conf. Dig. of 58th Device Research Conference, 155.

[9] B. C. Satishkumar, P. John Thomas, A. Govindaraj, and C. N. R. Rao, Appl. Phys. Lett., 2000; 77: 2530.

[10] M. Yumoto, S. Kasai and H. Hasegawa, presented at 2001 Int. Conf. on Solid State Material and Devices, Sep. 26-28, 2001, Tokyo, Japan.

[11] T. Muranaka, C. Jiang, A. Ito and H. Hasegawa, Thin Solid Films, 2000; 380: 189.

[12] A. Ito, T. Muranaka, C. Jiang and H. Hasegawa, presented at 8th Int. Conf. on Formation of Semiconductor Interfaces, June 10-15, 2001, Sapporo, Japan, to be published in Appl. Surf. Sci.

Figure captions

Fig.1 (a) Basic concept of a hexagonal BDD quantum circuit and (b) a BDD node device. Hexagonal BDD layouts of (a) AND, (b) exclusive OR and (c) NOR.

Fig.2 (a) A basic structure of WPG and designs of WPG quantum BDD node devices: (b) QWR branch switch type, (c) SE branch switch type and (d) SE node switch type.

Fig. 3 SEM images of fabricated WPG BDD quantum node devices: (a) QWR branch switch type and (b) SE branch switch type.

Fig.4 (a) Conductance quantization of a WPG QWR branch and (b) conductance oscillation of a WPG SE branch.

Fig.5 (a) An SEM image of a fabricated WPG QWR BDD half sum on an AlGaAs/GaAs nanowire hexagon and circuit diagrams of (b) half sum and (c) carry out.

Fig.6 Half adder operation. (a) Carry out at 1.6 K, (b) carry out at 300 K and (c) half sum at 300 K.

Fig.7 Hexagonal BDD circuit diagram of an n-bit full adder.

Fig.8 SEM image of fabricated hexagonal BDD 2-bit adder.

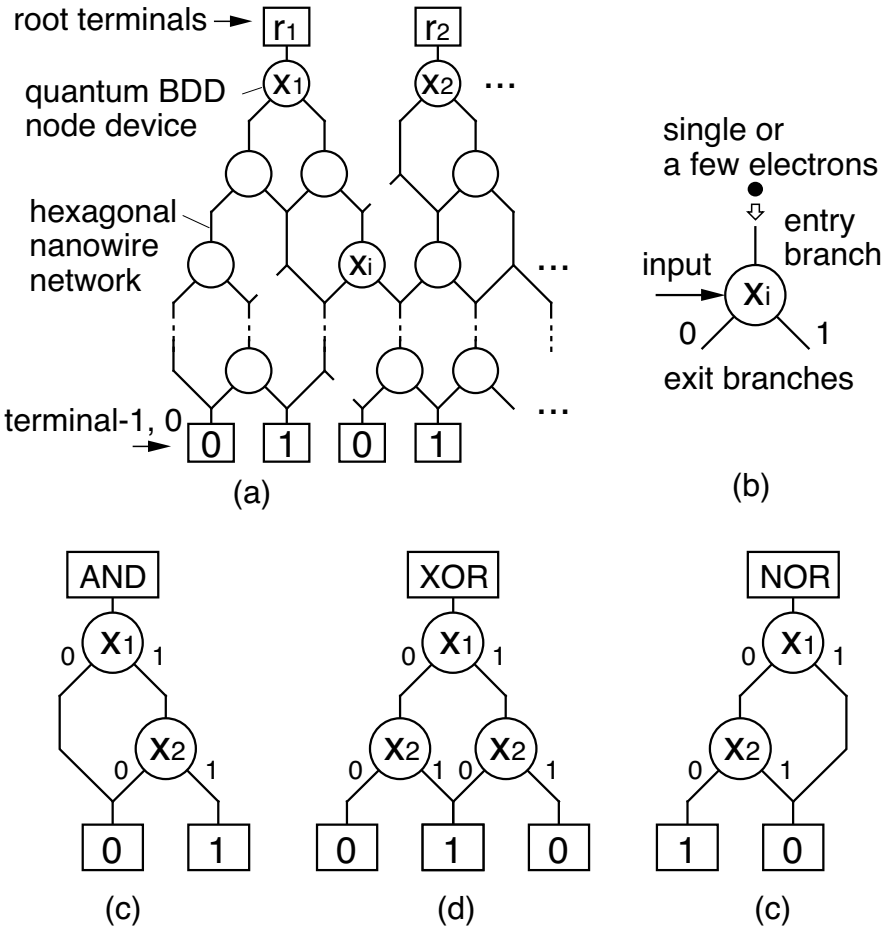


Figure 1 Kasai et al.

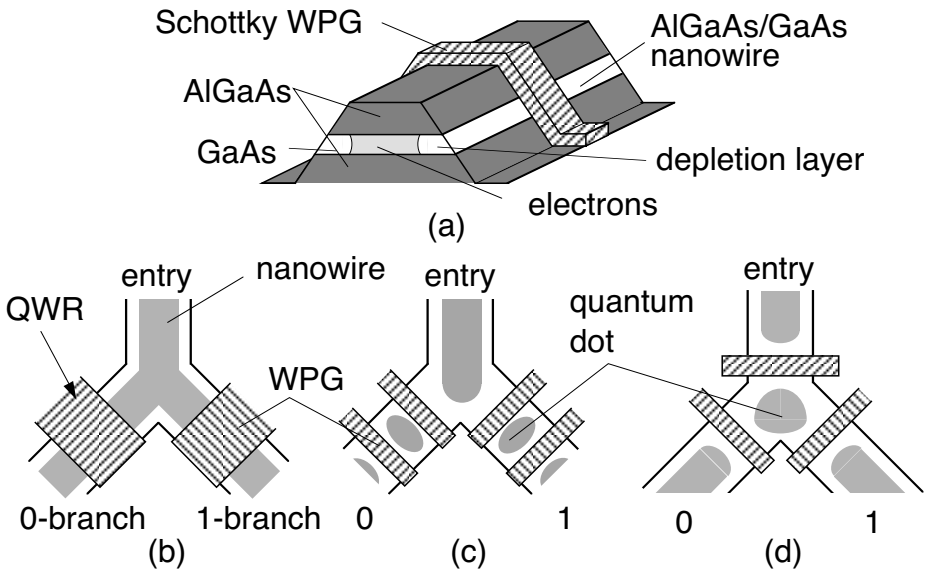


Figure 2 Kasai et al.

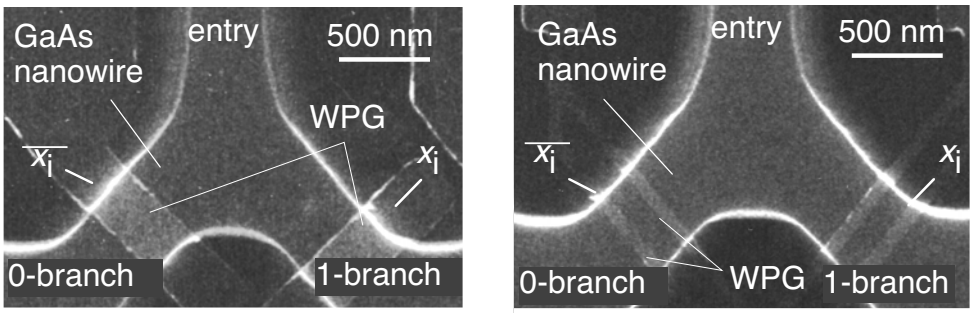


Figure 3 Kasai et al.

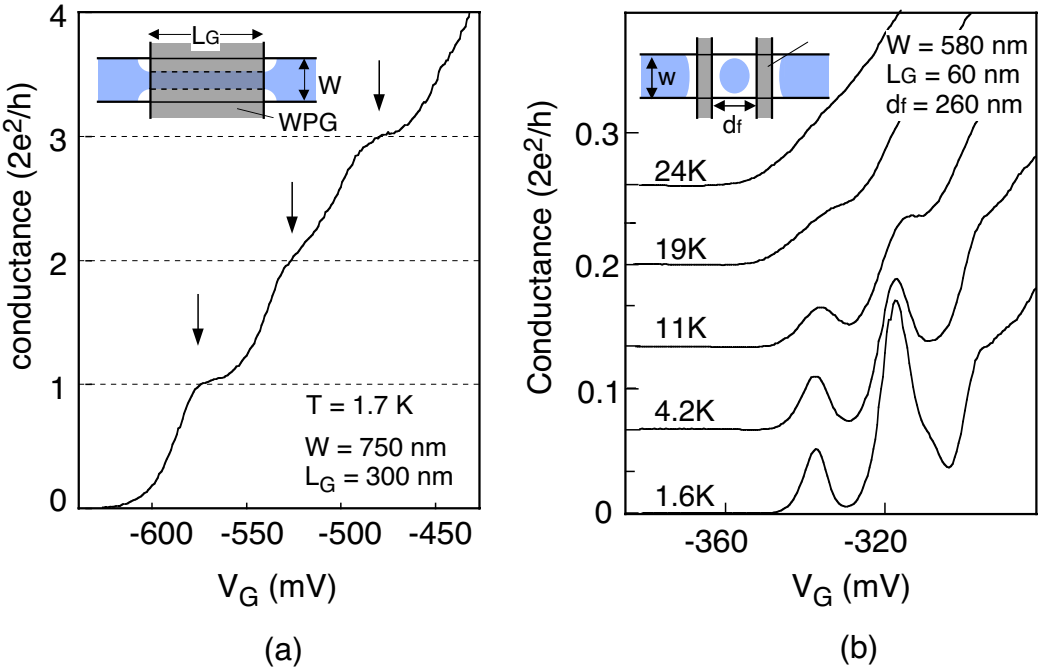


Figure 4 Kasai et al.

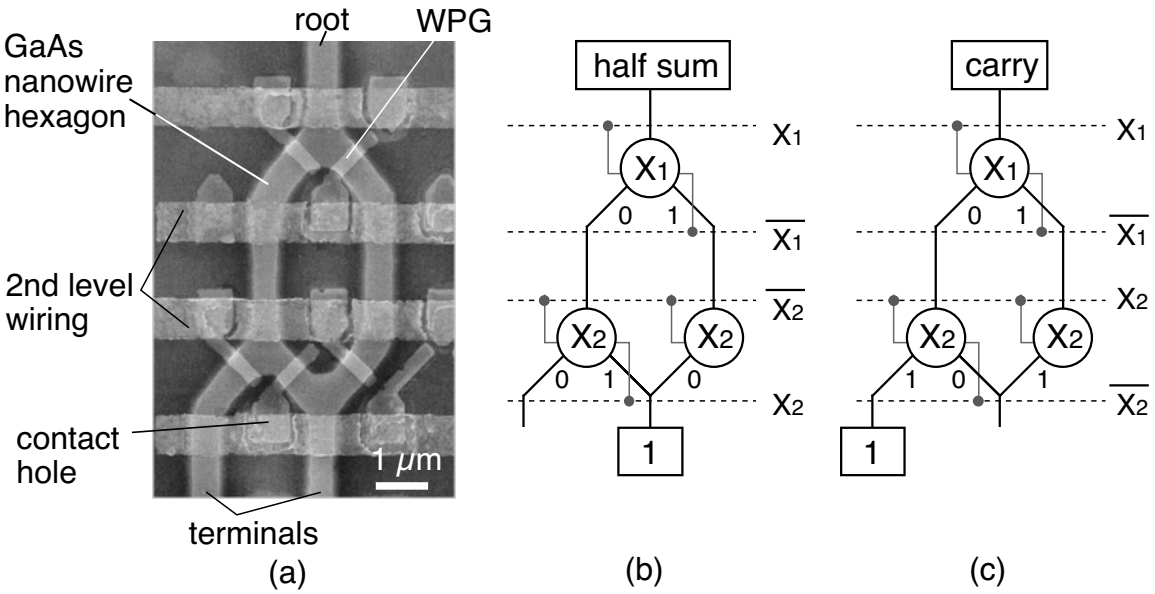


Figure 5 Kasai et al.

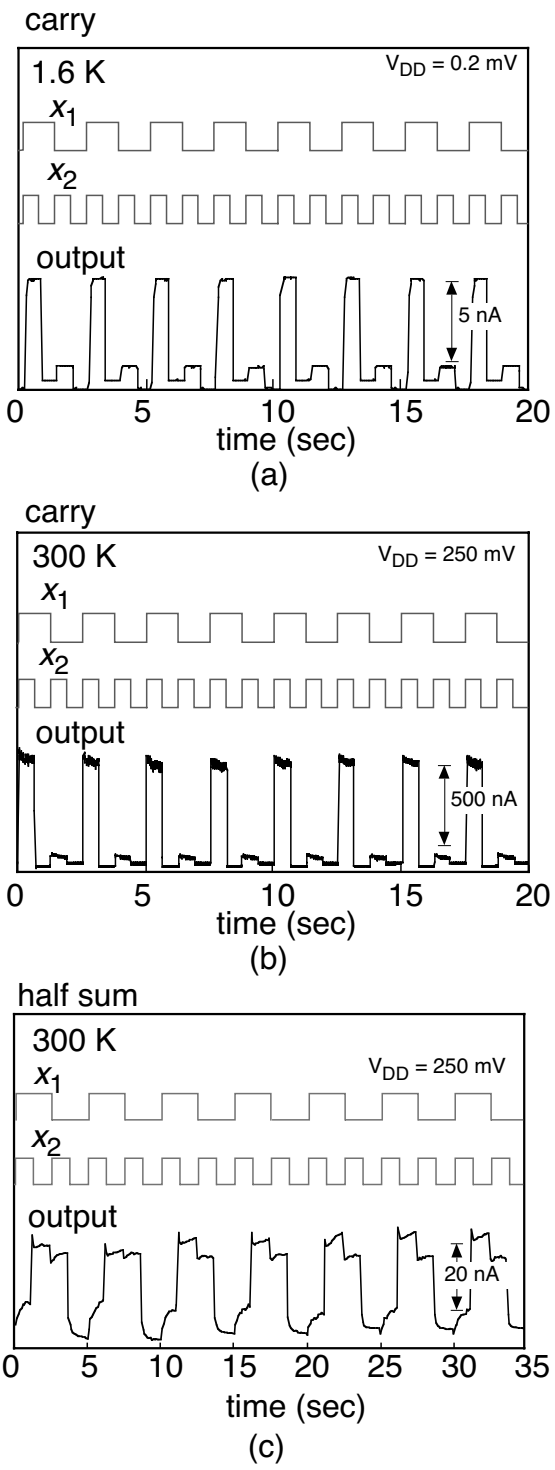
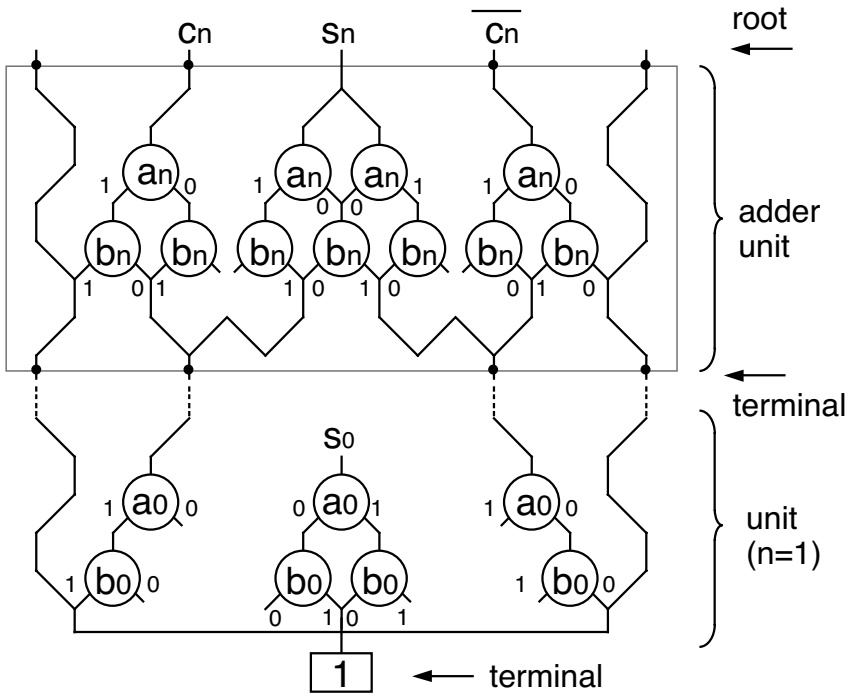


Figure 6 Kasai et al.



$$\begin{array}{rl} & a_n\ a_{n-1}\ \ldots\ a_0 \\ +) & b_n\ b_{n-1}\ \ldots\ b_0 \\ \hline & C_n\ S_n\ S_{n-1}\ \ldots\ S_0 \end{array}$$

Figure 7 Kasai et al.

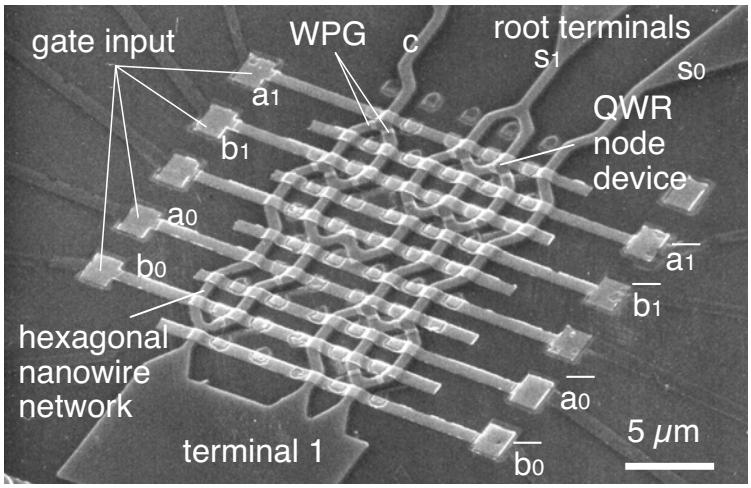


Figure 8 Kasai et al.