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GaAs and InGaAs Single Electron Hexagonal Nanowire Circuits Based on Binary Decision Diagram Logic Architecture

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Abstract

The feasibility of a novel approach for single electron quantum LSIs (Q-LSIs) is investigated. It is based on the binary-decision-diagram (BDD) logic architecture, using arrays of GaAs and InGaAs single electron BDD node devices formed on hexagonal nanowire networks. Single electron branch switches using nanometer-scale Schottky wrap gates (WPGs) on AlGaAs/GaAs etched nanowires and on InGaAs nanowires by selective MBE growth were fabricated. They showed clear conductance oscillation characteristics controlled by a single electron lateral resonant tunneling. Successful design and fabrication of GaAs-based single electron BDD node devices and circuits including OR logic elements and a 2 bit adder indicates basic feasibility of realizing single electron Q-LSIs by the novel approach.

Keywords: GaAs, InGaAs, Hexagonal nanowire network, BDD, Single electron circuit

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1. Introduction

Recent progress of the information technology (IT) has opened up a world-wide internet era. The demand of society is increasing for further development of the IT and this will soon exceed the scale down limit of the conventional Si CMOS LSI technology. Nanoelectronics based on semiconductor quantum devices and quantum large scale integrated circuits (Q-LSIs) are promising candidates to overcome such limitation, since they can realize further miniaturization of device dimensions, and they operate on a new principle with ultra-small delay-power products near the quantum limit. The nanoelectronics providing nano-sensing and nano-control is also expected to play important roles in rapidly grown nanotechnology that covers wide research areas. However, no realistic prospect for Q-LSIs exists at present. One of the reasons is that one tends to stick to the Boolean logic gate architecture that requires very uniform and robust devices.

This paper investigates the feasibility of our novel approach[1,2] for single electron (SE) Q-LSIs based on the binary-decision-diagram (BDD) logic architecture[3], using arrays of GaAs and InGaAs SE BDD node devices formed on hexagonal nanowire networks.

2. Concept of hexagonal single electron BDD

The concept of the hexagonal single electron BDD approach is shown in **Fig.1**. In this approach, the graph representing a logic function is implemented on a hexagonal network as shown in **Fig. 1a** and a single electron is used as a signal messenger. Each node devices placed at proper node positions on the network has one entry- and two exit-branches as shown in **Fig. 1b**. Because the node device has the basic three-fold branch symmetry, closely packed hexagonal networks provides most suitable layouts and high-density integration of devices. The BDD requires no direct output-to-input connection, thereby none of large voltage gain, precise

input-output voltage matching, large fan-in and fan-out numbers and large current drivability are necessary. These are suited to non-robust SE devices which can be operated near ultra small delay-power product near the quantum limit[4].

For hardware implementation, GaAs and InGaAs hexagonal nanowire networks controlled by nanometer scale Schottky wrap gates (WPGs)[5] shown in **Figs. 1c** and **1d** are used. The WPG structure provides tight gate control, strong electron confinement. Its simple lateral structure is suitable for planar integration. Examples of SE BDD node devices designed utilizing the WPG are shown in **Figs. 1e** and **1f**. The former is a node-switch device having three WPGs and a quantum dot[1]. The latter is a branch-switch device consisting of two 2-gate WPG single electron transistors (SETs).

3. GaAs and InGaAs hexagonal nanowire networks

The GaAs hexagonal nanowire networks were formed on the AlGaAs/GaAs modulation doped heterostructure by EB lithography and wet chemical etching. This is a conventional mature process and it is suitable for studying feasibility of our approach. An example of a fabricated structure is shown in **Fig. 2a**. The geometrical nanowire width, W , was 450 nm. Each hexagon had $4.5 \mu\text{m} \times 2.5 \mu\text{m}$ area and this corresponds to a node density of 10^7 cm^{-2} .

The InGaAs hexagonal nanowire networks were fabricated by a selective MBE growth of InAlAs/InGaAs heterostructure on InP substrates with hexagonal pattern. This selective MBE technique can potentially provide narrow nanowires necessary for room temperature operation in the single electron regime. For the growth, low-temperature atomic hydrogen (H^*) cleaning of InP substrate and H^* assisted growth were applied to the formation of initial ridge structure in order to obtain uniform nanowire without discontinuity [6]. **Figure 2b** shows an example of the fabricated InGaAs hexagonal nanowire network. Smooth and uniform structure was obtained.

The wire width can be controlled by growth condition and a minimum effective nanowire width of 6 nm has been achieved[6]. Overall optimization of the growth process has led to a successful formation of a network structure with a sub-micrometer pitch[7]. This structure allows a node density of 10^8 cm^{-2} .

To construct SE branch switches, two 50-100 nm-length WPGs with a few hundred nm spacing were formed on the nanowire by the EB lithography, metal deposition and lift-off process. Examples of the fabricated GaAs SE BDD node devices are shown in **Figs. 2c** and **2d**.

4. WPG control of nanowires

The single electron transport was confirmed by conductance measurement on SE branch-switch devices utilizing GaAs and InGaAs nanowires. **Figures 3a** and **3b** show conductance oscillation characteristics in fabricated GaAs and InGaAs SE branch switches with 2-gate WPG SETs in **Figs. 1d** and **1e**, respectively. They showed a small number of high conductance peaks which were visible up to 20-30 K. This behavior is quite different from that of conventional metal SETs and III-V SETs using Schottky split gates[8,9]. The present InGaAs device had a wire width of 100 nm and operation in the quantum regime at higher temperatures can be expected in InGaAs devices by reducing the nanowire width.

The conductance peak height is an important parameter to determine the delay-power product for single electron devices[4]. **Figure 3c** shows the conductance peak height as a function of temperature in the GaAs WPG SE branch switch. Theoretical behavior by a single electron resonant tunneling is also shown. Here, the Breit-Wigner formula[10] was used for tunneling probability, $T(E)$. Γ is the line width of $T(E)$. The theory well reproduced the experimental results. In the low temperature limit, the peak height becomes less dependent on temperature and approaches to e^2/h as predicted by the Breit-Wigner formula. This shows that the

transport in the WPG SE devices is controlled by a single electron resonant tunneling. Based on this model, device design including conductance characteristics became possible.

5. Single electron BDD circuits

Arrays of SE BDD node devices can be fabricated using the hexagonal nanowire networks. Both of fabricated SE node devices based on GaAs WPG structures as shown in **Fig. 2c** and **2d** exhibited proper switching operation with the single electron transport at 1.5 K. However, the branch-switch device seems to be better from viewpoints of reducing dot size and wiring. The GaAs WPG node devices can show proper switching operation at room temperature[11], since the WPG can act as a classical FET switch at high temperatures.

Fundamental operation of the SE BDD logic circuit was confirmed by fabrication and characterization of OR logic elements which have one node-switch device and one branch-switch device as shown in **Fig 4a**. The operation of the circuit at 1.5 K is shown in **Fig. 4b**. The messenger electrons were sent from the root to the terminal-1 by applying a voltage of $V_{DD} = 1$ mV between them, and the current in the terminal-1 was measured as an output signal in response to two gate input voltage pulses, x_1 and x_2 , with amplitudes, $\Delta V_{Gx1} = 100$ meV and $\Delta V_{Gx2} = 400$ meV, respectively. Clear waveforms were obtained. Correct output was also obtained even at 120 K in the classical regime. Reduction of the wire size by applying the InGaAs nanowire should lead to room temperature operation in the single electron quantum regime. Possible switching speed and power consumption at low temperature were estimated from the charging energy and the conductance[4] and resulted in 1 ns and 0.1 pW, respectively. Estimated delay-power product is 10^{-22} J which is much smaller than 10^{-15} J of the conventional Si CMOS transistor switch.

To see the feasibility of our hexagonal BDD approach for large-scale integration, a hexagonal SE BDD 2-bit adder was designed as shown in **Fig. 5(a)**. Suitable layout design of the

circuit can be successfully made on the hexagonal network without any nanowire crossover. In this circuit, 14 devices are integrated. Based on this design, the adder with branch switch devices could be successfully fabricated as shown in **Fig. 5b**. This utilizes the GaAs hexagonal nanowire network shown in **Fig. 2a** and the circuit size is $27\ \mu\text{m} \times 15\ \mu\text{m}$. Using the submicron pitch InGaAs hexagonal nanowire network[7], the size is reduced down to $9\ \mu\text{m} \times 6\ \mu\text{m}$. Gate inputs were wired by a conventional multi-layer wiring process. The operation of this circuit is under test at present, and will be reported elsewhere.

6. Conclusion

This work investigated basic feasibility of a novel approach for single electron (SE) Q-LSIs based on the BDD logic architecture, using arrays of GaAs and InGaAs SE node devices on hexagonal nanowire networks. The SE branch switches using GaAs etched nanowires and selective MBE grown InGaAs nanowires controlled by Schottky WPGs were fabricated and they showed clear conductance oscillations controlled by a single electron lateral resonant tunneling. Successful design and fabrication of SE BDD node devices and circuits based on GaAs WPG structures, including OR logic elements and a 2-bit adder, seems to indicate feasibility of realization of SE Q-LSIs by the novel approach.

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Figure captions

Fig.1 Basic concept of the hexagonal single electron BDD. (a) architecture. (b) single electron BDD node device. (c) and (d) : WPG controlled GaAs and InGaAs nanowires. (e) and (f) : examples of WPG SE BDD node devices.

Fig.2 SEM images of fabricated (a) GaAs and (b) InGaAs hexagonal nanowire networks, and (c) and (d) fabricated GaAs SE BDD node devices.

Fig.3 Conductance oscillations in WPG SE BDD node devices using (a) GaAs and (b) InGaAs nanowires. (c) Temperature dependence of the conductance peak height in the GaAs device.

Fig. 4 (a) SEM image and schematic diagram of GaAs SE BDD OR logic element and (b) its input/output waveform.

Fig. 5 (a) Circuit design of the hexagonal SE BDD 2-bit adder and (b) an SEM image of the fabricated circuit.

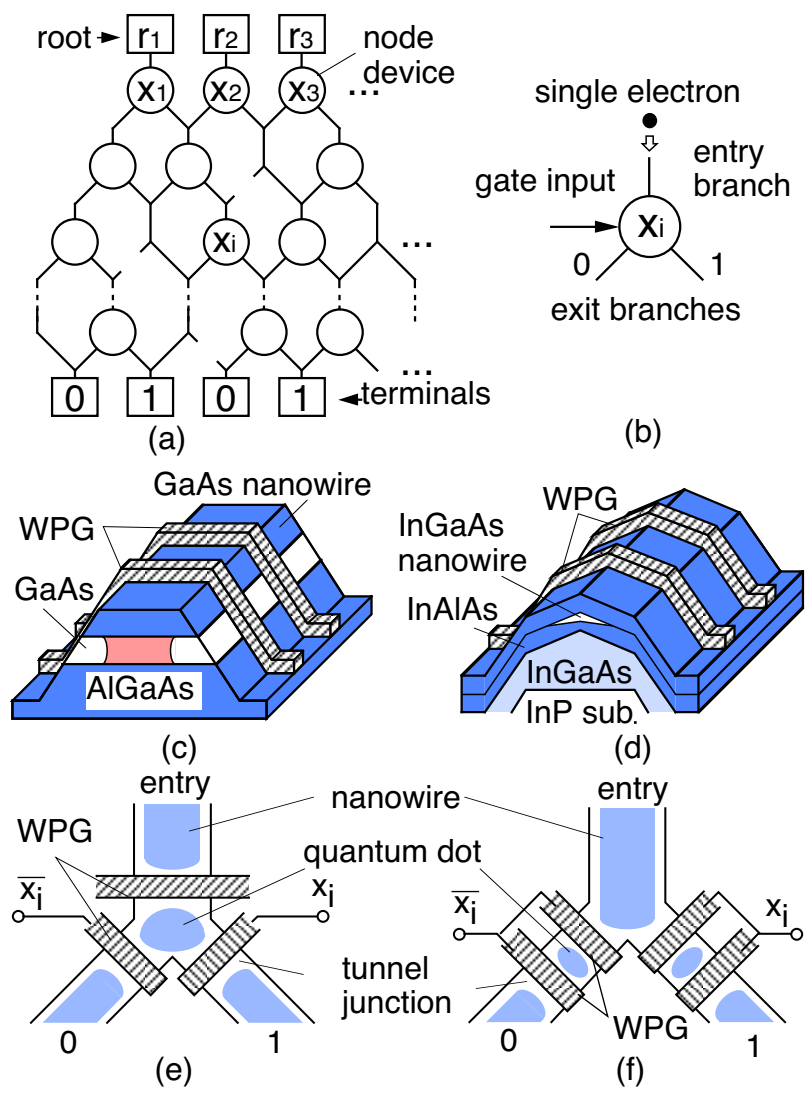


Figure 1 Kasai et al.

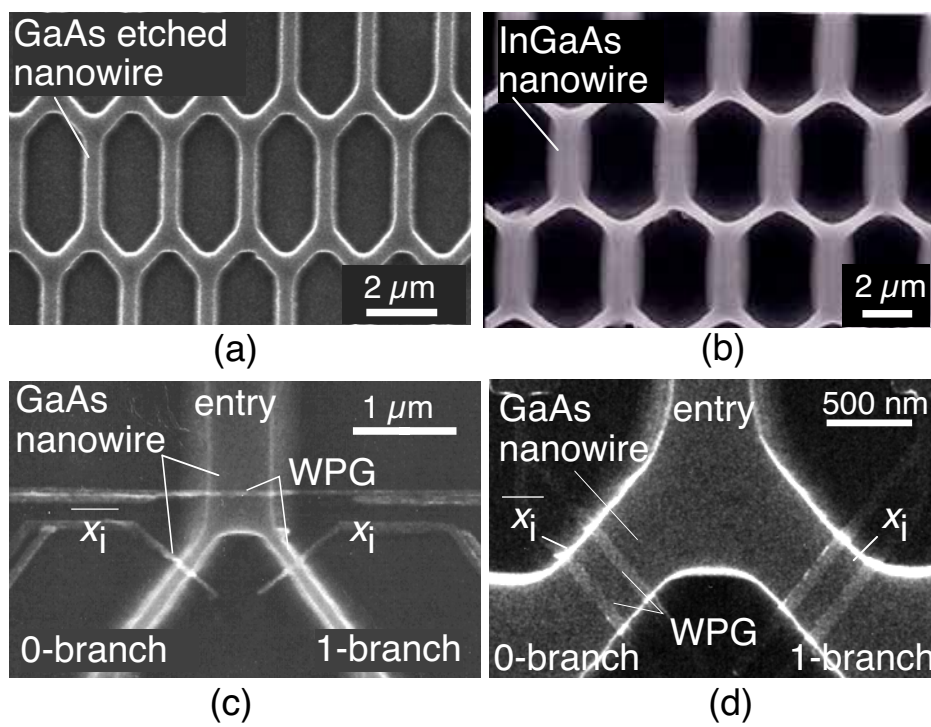


Figure 2 Kasai et al.

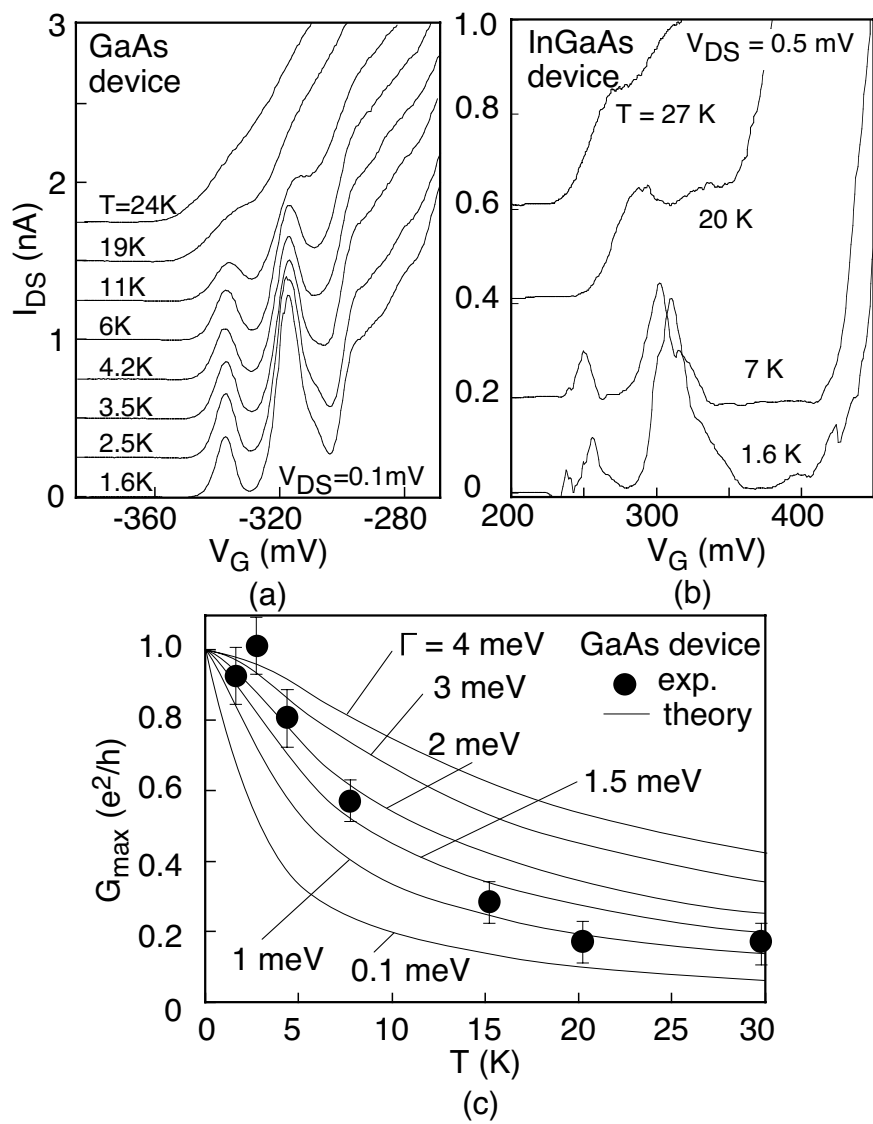
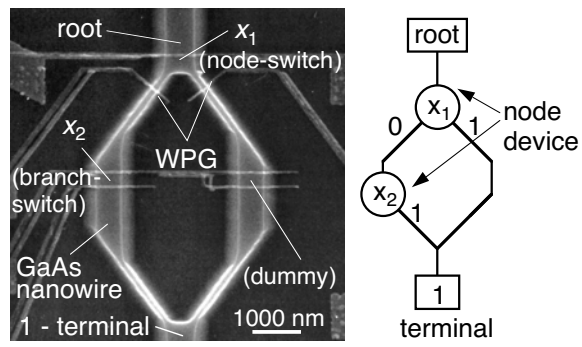
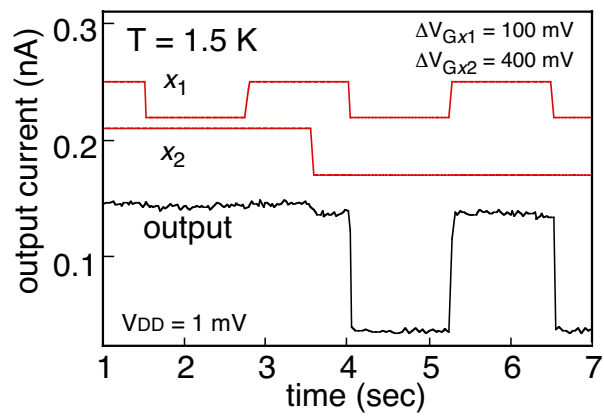


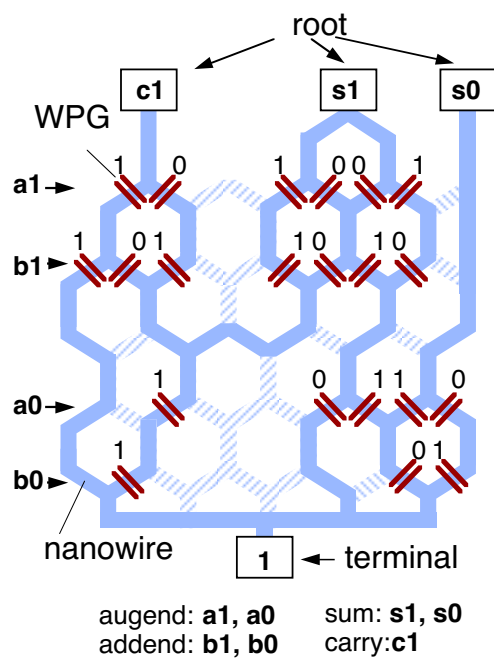
Figure 3 Kasai et al.



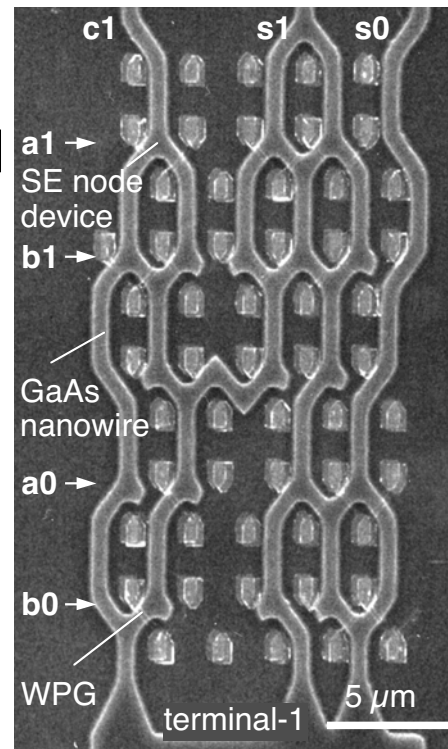
(a)



(b)



(a)



(b)