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GaAs quantum wire transistors and single electron transistors using Schottky wrap gates for quantum integrated circuits

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Abstract. Basic electrical properties of Schottky wrap-gate (WPG) controlled GaAs quantum wire transistors (QWTrs) and single electron transistors (SETs) are investigated to clarify their applicability to future quantum integrated circuits. The fabricated WPG QWTrs showed excellent gate-control characteristics and conductance quantization, indicating that the WPG can produce a strong lateral confinement potential. The WPG SETs showed clear and high conductance peaks that were suitable for switching device application. A WPG SET-based inverter logic circuits combining a WPG QWTr active load with a WPG SET was fabricated and it showed a clear inverter action, whose inverter gain was in reasonable agreement with the voltage gain of the driver two-gate WPG SET estimated from the Coulomb diamond plot.

1. Introduction

Integrated Circuits (ICs) based on III-V compound semiconductor quantum devices are promising candidates for next-generation III-V heterostructure microelectronics featuring high-speed, low-power and rich functionality. One of the key issues in this area is to establish a new gate technology for quantum devices which can realize a sufficiently strong gated quantum confinement and precise control of potential and carrier number, and whose structure is suited for high-density planar integration.

The purpose of this paper is to fabricate and characterize a new class of quantum devices based on the Schottky wrap gate (WPG) technology in order to investigate their potential for future quantum ICs. Using Schottky WPG structures proposed by the authors[1], GaAs quantum wire transistors (QWTrs), single electron transistors (SETs) and a inverter circuit combining a SET and a QWTr were fabricated and their properties were characterized.

2. Device structure and fabrication

The device structure of a WPG QWTr using the AlGaAs/GaAs heterostructure wafer is schematically shown in Fig.1(a). A WPG gate is wrapped around an etched AlGaAs/GaAs nanowire. The nanowire has a trapezoidal cross-section with vertical and horizontal electron confinement as schematically shown in Fig.1(b). This gate structure can provide charge

control, confinement potential control and tunnel barrier formation. In this paper, we investigated WPG QWTrs and two-gate WPG SETs as shown in Figs.1(c) and (d), respectively. By changing the arrangement of the WPGs and nanowires, various other quantum devices and SET devices having different functions can also be realized. The advantages of the WPG devices are flexibility of device design, stronger electron confinement than the split gate structure, their lateral structure suited for planar integration, and simplicity of the device fabrication process.

The WPG quantum devices were fabricated as follow. First, <$\bar{1}$10> oriented GaAs etched nanowires were formed on δ-doped MBE-grown AlGaAs/GaAs 2DEG wafers by the electron beam (EB) lithography and wet chemical etching. After formation of ohmic electrodes, Cr/Au Schottky wrap gates were formed by EB lithography and by a conventional lift-off process. Inverter circuits could be also fabricated by using the same process.

3. Results and discussions

3.1. *Quantum wire transistor (QWTr)*

The gate control characteristics of the WPG structure were confirmed by a long-channel QWTr (wire length, L_G = 7 μm, wire width, W = 620 nm). A Landau plot from magnetoresistance measurements showed nonlinear behavior, indicating one-dimensional carrier transport. Figure 2 shows the effective channel width, W_{eff}, as a function of gate voltage, V_G, obtained from the cyclotron diameter[2]. In the small negative gate bias region, W_{eff} remained almost constant, changing only the electron number, but W_{eff} rapidly decreased by large negative gate bias near pinch-off. The observed W_{eff} -V_G characteristics were well explained by the numerical simulation for WPG structures already reported in ref.[2].

The WPG QWTrs showed excellent gate-control characteristics with good pinch-off from a few K up to room temperature as shown in Fig.3(a). Near pinch-off, conductance quantization was clearly seen at low temperatures as shown in Fig.3(b), even for a device whose wire length was as long as 7 μm. The observed small conductance step height in Fig.3(b) seems to be due to various reason including series resistance of the ungated channel region, backscattering and non-adiabatic effects in the long wire[3].

3.2. *Single electron transistors (SETs)*

Fabricated two-gate WPG SETs showed clear conductance oscillation characteristics as shown in Fig.4(a). WPG SETs showed high and temperature-dependent conductance peaks, and their spacing were aperiodic. Number of peaks was usually limited to one to three or four. By a simulation with a simple quantum mechanical approach, resonant tunneling through quantized states in the dot was found to produce conductance oscillations in the WPG SET[4], whose number of peaks is limited due to the fact that the tunneling barrier height changes also with the gate bias from too high to tunnel through to too low to form a well-defined dot. From a viewpoint of device engineering, it should be noted that presence of a single high conductance peak is sufficient for switching device applications in logic gates as well as in binary decision diagram (BDD) devices[5]. In small negative-gate-bias conditions, the conductance shows conventional FET like behavior due to broadening and merging of peaks by thermal effect.

The voltage gain was evaluated experimentally from the Coulomb diamond plot as shown in Fig.4(b). A maximum voltage gain of 0.26 was obtained near pinch off.

3.3. *Application to inverter circuit*

As a combination of the QWTr and SET devices, a SET-based resistive loaded inverter circuit was fabricated and characterized. It included a driver two-gate WPG SET and a WPG QWTr as an active load. The WPG width of 50 nm was used, and an SEM micrograph of the completed inverter is shown in Fig.5(a). The measured input-output characteristics are shown in Fig.5(b). One can see a clear inverter operation and find that the input-output voltage gain of 0.21 was obtained when the resistance of the active load was tuned high by biasing the QWTr near pinch-off. This value was found close to the voltage gain of the

discrete two-gate SET, estimated from the Coulomb diamond plot. Oscillations were observed in the low voltage portion of the output voltage, reflecting Coulomb additional oscillation peaks of the driver SET. Although the inverter gain in the present two-gate WPG SET-based inverter is below unity, being consistent with the Coulomb diamond plot, it has also been found that the voltage gain of the three-gate WPG SET can be made larger than unity[6]. Thus the inverter circuit including such three-gate WPG SET should posses a gain larger than unity. A simple estimate shows that such an inverter should show a switching speed of several pico-seconds or so with the power consumption of 10^{-10} W, realizing a delay-power product in the range of 10^{-22} J close to the quantum limit. Thus, realization of a logic gate density of 10^{10} cm^{-2} seems possible.

4. Conclusion

For realization of quantum device integrated circuits, GaAs-based Schottky wrap-gate (WPG) quantum wire transistors (QWTrs) and single electron transistors (SETs) were developed and applied to a single electron inverter logic circuit. The fabricated WPG QWTrs showed excellent gate-control characteristics and one-dimensional transport. WPGs could produce a strong lateral confinement potential. The WPG SETs showed clear and high conductance peaks. WPG SET-based inverter logic circuits combining a WPG QWTr active load was fabricated and it showed a clear inverter action and its input-output gain was in reasonable agreement with the voltage gain of the driver two-gate WPG SET estimated by the Coulomb diamond plot.

Acknowledgement

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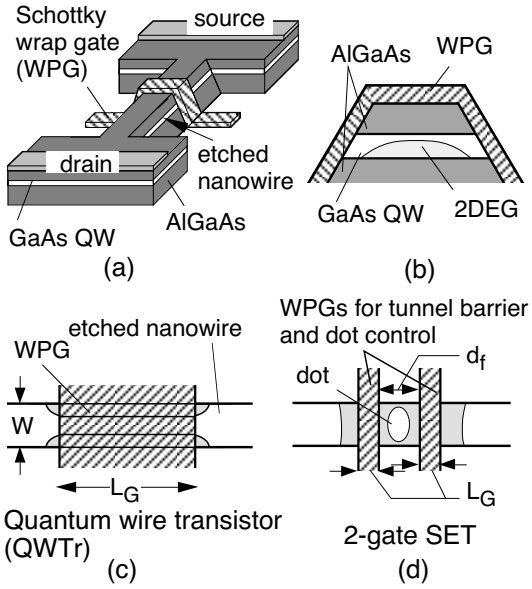

Fig.1 Basic structure and quantum devices using Schottky wrap gates (WPGs).

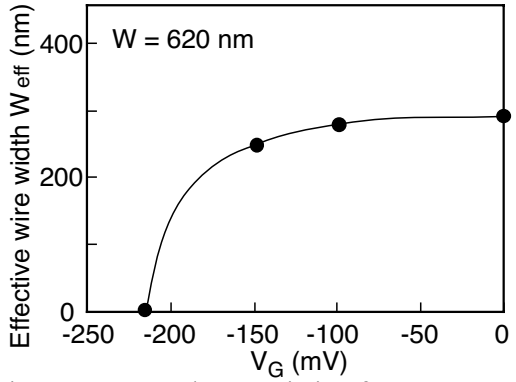

Fig.2 W_{eff}-V_G characteristic of WPG QWTr.

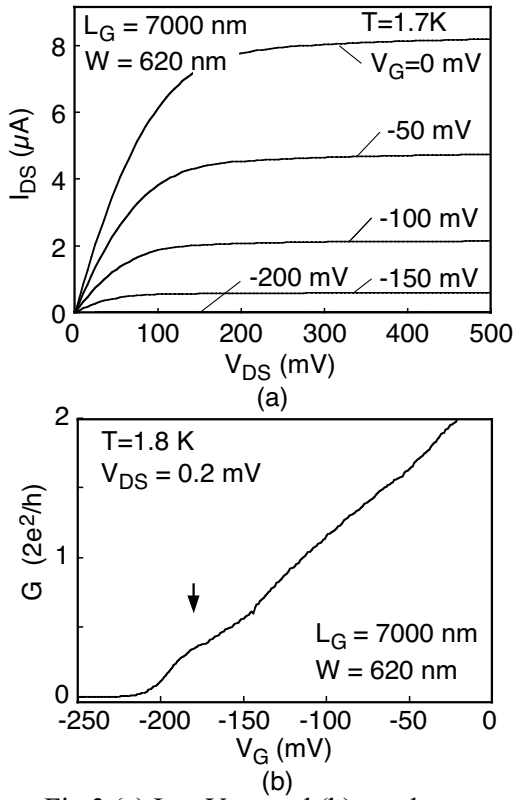

Fig.3 (a) I_{DS}-V_{DS} and (b) conductance characteristic of WPG QWTr.

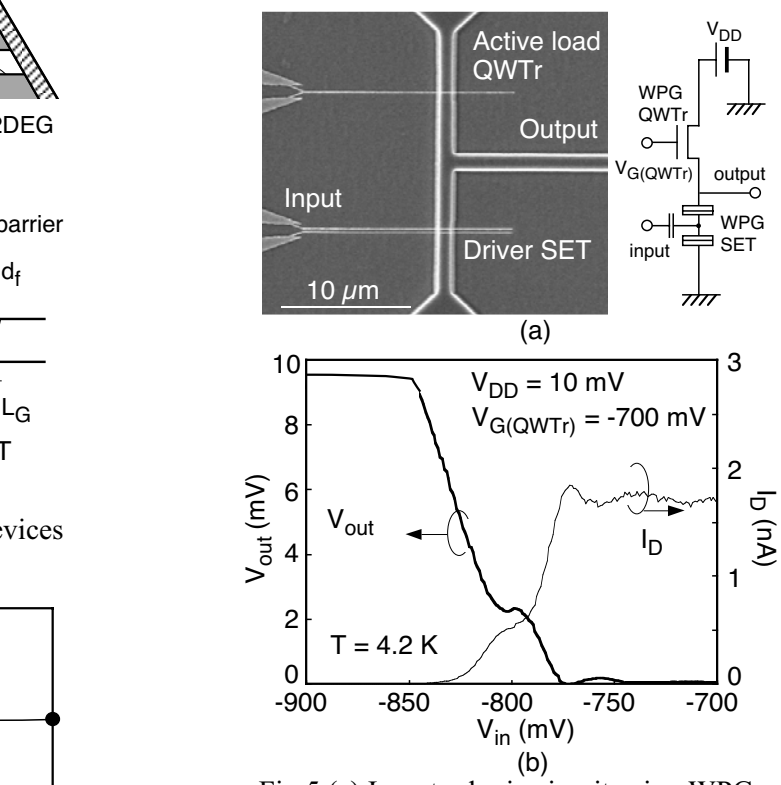

Fig.5 (a) Inverter logic circuit using WPG quantum devices and (b) its input-output characteristics.

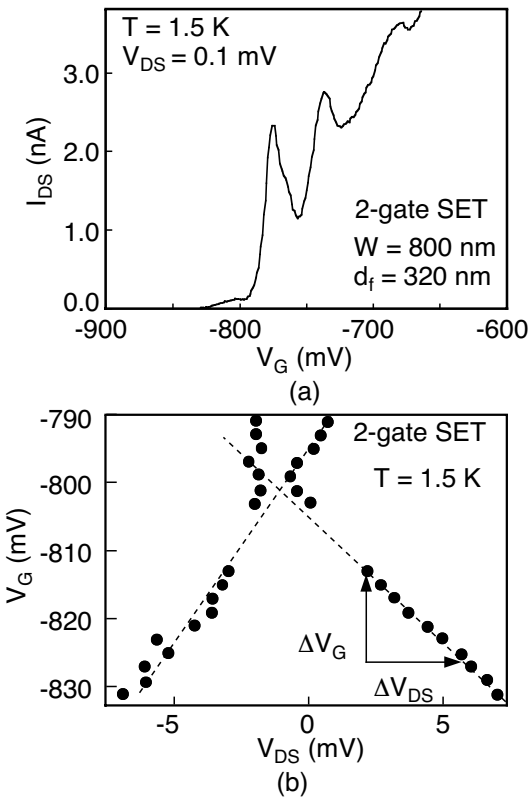

Fig.4 (a) Conductance characteristic and (b) Coulomb diamond plot of WPG SET.