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Conductance Oscillation Characteristics of GaAs Schottky Wrap-Gate Single Electron Transistors

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Conductance oscillation characteristics in GaAs-based Schottky wrap gate (WPG) single electron transistors (SETs) were investigated both experimentally and theoretically in view of application as a key switching device in future quantum integrated circuits. Fabricated WPG SETs showed that clear conductance oscillation characteristics with a small number of high conductance peaks. A simple theory based on a quantum mechanical treatment reproduced qualitatively the features of the experimentally observed conductance peaks, indicating that the resonant tunneling contributes to currents in the WPG SETs. However, quantitatively, a discrepancy existed between theory and experiment on the temperature dependence of peak heights.

Key words: single electron transistor (SET), Schottky wrap gate (WPG), GaAs, conductance oscillation

1. Introduction

Single electron transistors (SETs) based on III-V compound semiconductors have so far been utilized primarily as a novel means of spectroscopy in fundamental semiconductor physics, recently revealing "artificial atom" and "artificial molecule" properties of quantum dots[1,2]. However, as expected from high-speed and low-power performances of existing III-V electron devices, the III-V SET possesses a high potential as a key device for future quantum integrated circuits (QICs), realizing an ultimate speed-power performance near the quantum limit. For this purpose, we have proposed recently a Schottky wrap-gate (WPG) SET[3] which has a simple lateral structure suitable for high density planar integration, and provides much stronger confinement potentials than the previous split gate SETs. Its three-gate version has recently realized experimentally a voltage gain larger than unity for the first time as a III-V SET[4].

The purpose of this paper is to clarify the output conductance characteristics of GaAs Schottky WPG SETs both theoretically and experimentally. Two-gate WPG SETs with different sizes were fabricated and characterized. The behavior of the observed conductance peak was explained by a simple quantum mechanical theory that has been developed for design and analysis of WPG SETs.

2. Device Structure and Fabrication

The structure of the WPG SET device is schematically shown in Fig.1(a). Two narrow Schottky WPG electrodes with a spacing, d_f , are wrapped around a III-V nanowire with a width, W . The nanowire has a trapezoidal cross-section with vertical and horizontal electron confinement as schematically shown in Fig.1(b). Two Schottky electrodes, kept at the same gate bias, V_G , completely deplete electrons underneath and form two tunneling barriers. At the same time, they control the size of the dot in between through the lateral extension of electric field lines.

Two-gate WPG SETs with different gate spacings of $d_f = 160, 260$ and 310 nm were fabricated. For this, $\langle 110 \rangle$ oriented AlGaAs/GaAs etched wires were formed on δ -doped MBE-grown 2DEG wafers by electron beam (EB) lithography and wet chemical etching. Then, Cr/Au Schottky wrap gates were formed by the EB lithography and a conventional lift-off process.

An example of the fabricated WPG SET is shown in Fig.1(c).

3. Conductance Characteristics and Discussion

Figure 2 shows an example of the observed conductance oscillation for a WPG SET having $d_f = 160$ nm. Within the gate bias range shown, the device showed a first single high peak and a second broad peak only. Those conductance peaks were visible up to 20 K. The height of the first peak was $0.3G_0$ ($G_0 = 2e^2/h$), and is higher than those of previous SETs reported in literature. As shown in Fig.2(b), the shape of the first peak could be fitted very well into a $\cosh^{-2}(x)$ form as predicted theoretically by Beenakker[5]. Other fabricated devices with large values of d_f also showed two to three conductance peaks, however, the peak heights were lower than the WPG SET shown in Fig.2.

From a view-point of device engineering, it should be noted that presence of a single high peak is sufficient for switching device applications in logic gates as well as in binary decision diagram (BDD) devices[6], although presence of many peaks may be preferred for spectroscopy in physics. For device applications, on the other hand, the height, width and position of the peak as well as their temperature dependences should be predictable for device and circuit design.

For this purpose, analysis of the conductance oscillation characteristics of the present WPG SET was made using a simple quantum mechanical approach. The conductance characteristics was calculated on computer in the following way. First, the tunnel-barrier potential profile near pinch-off was obtained from a three-dimensional potential calculation using a SOR method. Next, a tunneling probability through the double tunnel barrier potential was calculated using a quasi-one dimensional transfer matrix scheme. For simplicity, Coulomb charging energy in the dot was ignored in the calculation, since its rigorous treatment requires a full self-consistent treatment of the problem. Then, current, I , was evaluated by using following formula[7],

$$I = \frac{2e^2}{h} \int |T(E)|^2 [f(E) - f(E + qV_{DS})] dE \quad (1)$$

where $|T(E)|^2$ is a tunneling probability through the double barrier and $f(E)$ is Fermi-Dirac distribution function, and V_{DS} is the drain-to-source voltage.

An example of a simulated conductance near pinch-off is shown in Fig.3. The inset shows the corresponding tunnel barrier potential from the potential simulation. The horizontal axis in Fig.3 is the Fermi energy measured from the bottom of the potential at the dot center. A clear single peak appeared by setting $d_f = 160$ nm and tunneling barrier height, $V_B = 80$ meV. The result reproduces the observed temperature-dependent behavior of the peak in Fig.2 qualitatively very well. Theoretically, oscillation characteristics arose from the resonant tunneling through an quantized state in the dot. The reason for the experimental observation that only one or small number of peaks appeared over a wide gate bias sweep was found to be due to the fact that the tunneling barrier profile, Fermi level position as well as dot size change rapidly with gate bias in this structure, making the barriers, too high and thick for tunneling on one extreme and making them disappear on the other extreme.

The temperature dependence of the conductance height of the first peak in the fabricated WPG SETs was investigated in detail for three devices and compared with the calculation as shown in Fig.4. The peak heights showed roughly T^{-1} dependence on the temperature, T , and the dependence was stronger for the SET with the narrowest d_f of 160 nm. In the case of $d_f = 260$ nm and 310 nm, the peak heights were small ($< 0.05G_0$) and the temperature dependences were relatively weak. The solid lines in Fig.4 are simulated curves for various d_f . Qualitatively, they reproduce the observed behavior reasonably well. However, quantitatively, a fairly large discrepancy appears at higher temperatures for the device with $d_f = 160$ nm. The possible reasons for this discrepancy are the following. Firstly, the calculation here ignores the charging effect in the dot. Proper inclusion of the charging effect should widen the peak separation and reduces the overlaps of thermally broadened peaks. Secondly, the present analysis includes contribution from tunneling process through excited states by electrons with a thermally broadened energy distribution in the framework of the quasi-one-dimensional transfer matrix treatment. However, these contributions require a full three-dimensional self-consistent treatment for quantitative discussion.

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Figure captions

Fig.1 WPG SET structure and an SEM image of a WPG SET.

Fig.2 The observed conductance oscillation characteristics.

Fig.3 Calculated conductance characteristics.

Fig.4 Temperature dependences of the conductance peak height.

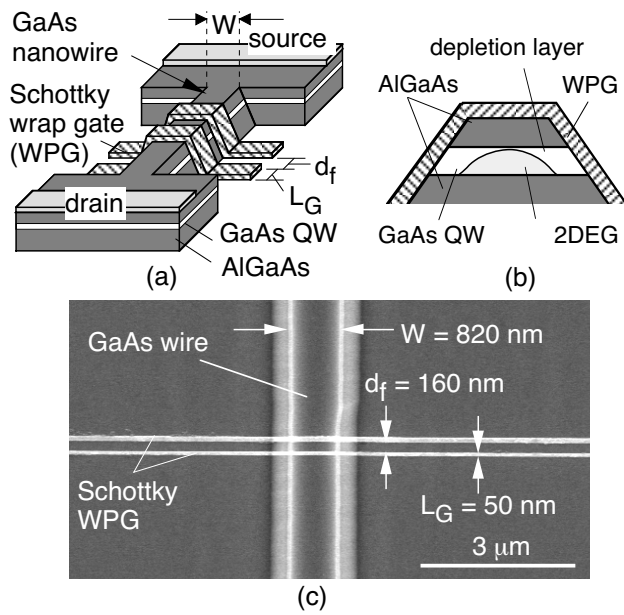


Figure 1 Kasai et al.

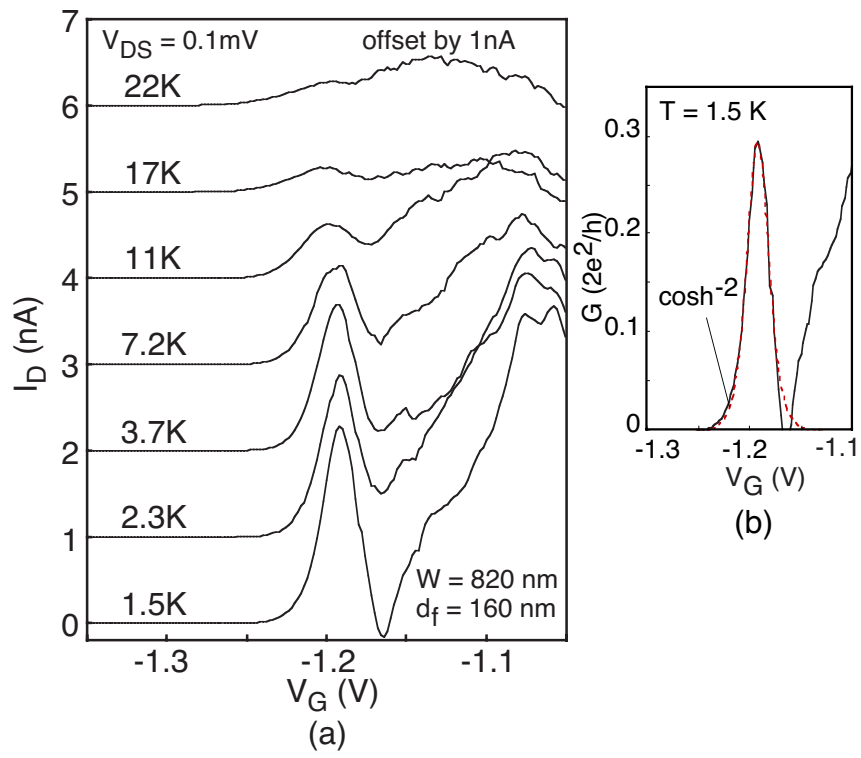


Figure 2 Kasai et al.

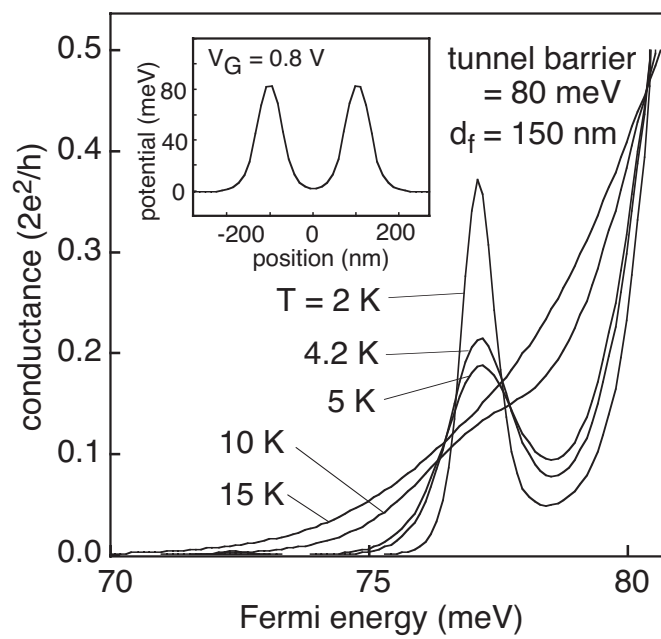


Figure 3 Kasai et al.

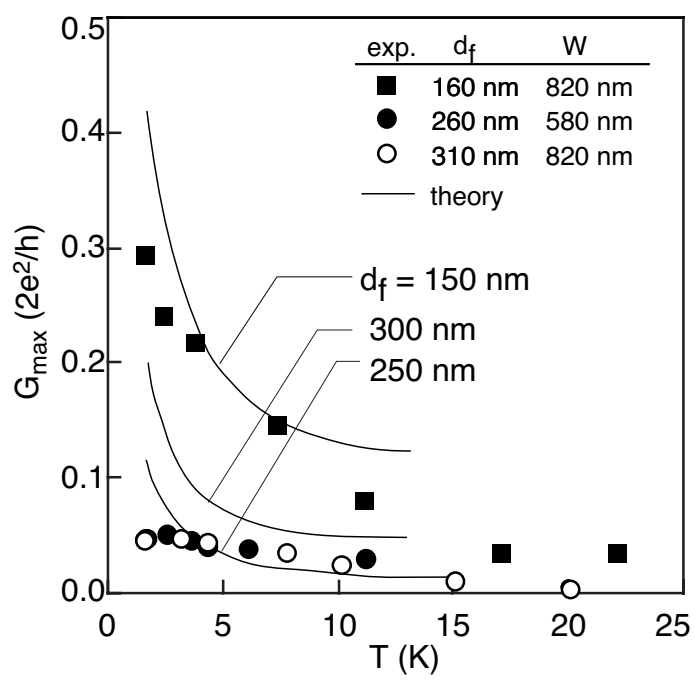


Figure 4 Kasai et al.