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Design and Implementation of Ultra-Small-Size and Ultra-Low-Power Digital Systems on GaAs-based Hexagonal Nanowire Networks Utilizing a Hexagonal BDD Quantum Circuit Approach

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ABSTRACT

This paper discusses feasibility of design and future implementation of ultra-small-size and ultra-low-power digital logic systems by a hexagonal BDD (binary-decision diagram) quantum circuit approach. The discussion is based on various circuits formed on GaAs-based hexagonal nanowire networks controlled by nanometer scale Schottky wrap gates (WPGs). Starting from basic node devices and elementary logic function blocks, fabrication technology of hexagonal BDD quantum circuits up to 8-bit adders with node densities over 45 million nodes/cm² has been successfully developed. Their correct operations at low temperatures and room temperature have been confirmed by experiments and simulation. Various circuit components in logic processors, including arithmetic logic unit (ALU), controller and decoders have been successfully designed as hexagonal BDD layouts without nanowire crossover. For sequential circuits, WPG-controlled nanowire FETs on hexagonal networks have been investigated, and registers and counters have been implemented using these nanowire FETs showing correct operation. Hexagonal BDD-based static 2-bit nano-processor unit (NPU) has been successfully designed completely on hexagonal nanowire network. Ultra high-density GaAs hexagonal nanowire networks with much smaller wire sizes than those of etched nanowire networks have been successfully formed by selective MBE growth, showing great promise for room temperature operation in quantum regime as well as reduction of system area and power consumption.

I. INTRODUCTION

Key hardwares in future ubiquitous network society are intelligent digital systems formed on ultra-small-size chips and operating at ultra-low power consumptions. For their realization, further advance of the LSI technology is required. However, the mainstream Si CMOS LSI technology is quickly saturating, facing various problems not only related to devices but also to logic and system architectures [1]. Therefore, exploration of a completely new LSI technology beyond the scaling limit of the Si CMOS LSI is desirable.

As a possible approach, quantum circuits utilizing quantum nanodevices, such as

quantum wire transistors (QWRTrs) and single electron transistors (SETs), have been studied for many years, paying attention to their rich functionality and capability of high-speed switching at ultra-small-size and ultra-low power dissipation levels. However, no realistic approach for their large-scale integration has been established up to now. The difficulty seems to have come from the fact that most of the previous attempts have aimed at implementing the logic gate architecture used in Si CMOS LSIs. This architecture requires cascade connection of logic gates formed by robust switches which possess large voltage gain, large current drivability and high uniformity of the threshold voltage. On the other hand, quantum nanodevices can handle only very small currents with small voltage gain and poor controllability of threshold voltages. Additionally, room temperature operation is difficult because quantum effects appear only at low temperatures.

To solve these problems and realize large-scale integration of quantum devices, the authors' group has recently proposed a novel hexagonal BDD quantum circuit approach [2,3] for integration of QWRTrs and SETs. Here, quantum circuits have been reconsidered, not from the device level, but from the logic architecture level in order to realize optimal use of quantum devices for digital information processing systems in a realistic way. The feasibility of the new approach has been investigated through fabrication of small-scale circuits [4-7].

The purpose of this paper is to discuss, on the basis of the promising results obtained so far, feasibility of designing and implementing digital systems with ultra-small sizes and ultra-low-power consumptions by the hexagonal BDD quantum circuit approach. A special focus is put on a design of a new "nano-processor unit (NPU)" on a GaAs-based hexagonal nanowire network controlled by nano-Schottky wrap gates (WPGs).

II. BASIC CONCEPT OF HEXAGONAL BDD QUANTUM CIRCUIT APPROACH AND ITS IMPLEMENTATIONS

Instead of the conventional logic gate architecture, the hexagonal BDD quantum circuit approach [2,3] utilizes the binary-decision-diagram (BDD) logic architecture [8,9] where a logic function is represented by a directed graph connecting nodes through which an information messenger travels down in one way. More specifically, a BDD circuit consists of binary path-switching node devices suitably interconnected on a hexagonal network to represent a logic function, f , as shown in **Fig. 1(a)**. Each node device has one entry branch and two exit branches and it selects one of the exit branches according to the binary logic input, $x_i = 0$ or 1 , as shown in **Fig. 1(b)**. Then, the value of a logic function, f , is evaluated by propagating a messenger from the top root toward bottom terminals in **Fig. 1(a)** through the path selected by each node device at each node. If the messenger reaches the terminal-1, then the logic value is unity, and if it reaches the terminal-0, then it is zero. Because of the three-fold symmetry of the node device, arranging the node devices on a hexagonal layout naturally provides the highest possible packing density.

The unique feature of the BDD architecture is that it does not have a direct input-output connection, and this results in advantages that no large transfer gain, no high current drivability and no precise threshold voltage control are required for the node device. Although various kinds of combinations of node devices and information messengers can be operated as BDD circuits, the above features are particularly suitable to non-robust and structure- and charge- sensitive quantum nanodevices controlling quantum transport of a single electron (SE) or a few electrons used as the messenger. In

such a combination, the power-delay product (PDP) for switching decreases greatly and approaches to the quantum limit given by the Heisenberg uncertainty principle.

For actual hardware implementation of the hexagonal BDD quantum circuit approach, we have been investigating a GaAs-based hexagonal nanowire network structures controlled by Schottky wrap gates (WPGs), as shown in **Fig. 2(b)**. The Schottky wrap gate [10] has a structure where a nanometer sized Schottky gate is wrapped around the nanowire. It has a simple lateral planar structure suitable for planar integration, and can produce tight gate control and strong electron confinement. The nanowire is formed by wet etching of AlGaAs/GaAs modulation doped heterostructure wafers using conventional electron beam (EB) lithography. Here, combination of superb quantum transport along high quality heterointerface and well-behaved Schottky interfaces with sufficiently high barrier height can be utilized.

Various types of node devices can be designed by the WPG arrangements on the nanowire network, as shown in **Fig. 2(b)**. A nanowire piece with a single WPG operates as a QWRTr. A nanowire piece controlled by a couple of narrow WPGs with a small spacing produces double tunneling barriers with a quantum dot in between under suitable WPG voltage and this structure operates as a SET. We call a type of node device having QWR or single electron (SE) switches on each exit branches as the branch-switch type node devices. On the other hand, a SE node device having narrow WPGs on each of three branches, where a quantum dot surrounded by three tunneling barriers is formed at the node position, is called the node-switch type SE node device. The branch-switch and node-switch type SE node devices can precisely control single electrons, and can realize small values of PDPs. On the other hand, branch-switch type QWR node devices have structure simpler to realize, and useful for feasibility study of integration.

III. DESIGN, FABRICATION AND CHARACTERIZATION OF SMALL-SCALE HEXAGONAL BDD QUANTUM CIRCUITS

Figure 3(a) shows an SEM image of a fabricated BDD branch-switch QWR node device with its I-V characteristics at room temperature shown in **Fig. 3(b)**. At low temperatures, nanowire branches controlled by WPGs in QWR and SE node devices showed clear conductance quantization and conductance oscillation characteristics, respectively, as shown in **Fig. 3(c)**. These characteristics in the quantum regime are maintained up to a few ten K. Fabricated devices exhibited clear path switching characteristics based quantum transports as shown in **Fig. 3(d)** for a QWR node device as an example. Successful path switching was also obtained even at room temperature as also shown in **Fig. 3(d)** where quantum transport should disappear. This is because WPG-controlled nanowires can also operate as conventional semi-classical FETs at high temperatures as can be seen in **Fig. 3(b)** with excellent gate control. The difference is that the number of electrons should be increased for proper operation, and this results in increase of the PDP value. Thus, hexagonal BDD circuits can operate at room temperature, and since substantial partial involvements of quantum transport mode are expected even at room temperature, reduced PDP values can be expected as compared with those of classical counterparts.

Elemental small-scale logic circuits integrating a few node devices have been successfully fabricated and their correct operations have been realized. **Figure 4(a)** shows an SEM image of a fabricated QWR-type AND logic and its input-output waveforms. It realized correct switching between 0-th and 1st quantized steps of conductance steps. It could also operate at room temperature in the classical regime

adjusting gate and terminal voltage. SE-type OR logic has been also fabricated and their correct operations have been confirmed both in quantum regime with single electron transport and in the classical regime as shown in **Fig. 4(b)**.

As a basis to judge the suitability of the present approach for construction of large scale digital systems, we have estimated power-delay product (PDP) values of the fabricated WPG-based QWR and SE switches, using a simple approximate relation of $PDP = C_G \Delta V_G^2$, where C_G is a gate capacitance and ΔV_G a gate voltage swing [3]. Gate capacitances were evaluated experimentally from gate-voltage-dependent Landou plots by magneto-resistance measurement for QWR devices [4] and from Coulomb blockade characteristics for SE devices. Small PDP value of 10^{-22} J was obtained in SE devices at 1.6 K. This is four orders of magnitude smaller than 10^{-17} J of 20 nm-gate Si MOSFET at 300 K [11]. The values for QWR devices were 10^{-20} J for the WPG length, $L_G = 630$ nm and 10^{-21} J for $L_G = 65$ nm, which are also much smaller than that of the Si MOSFETs. These results indicate the capability of ultra-small power consumption of the hexagonal BDD quantum circuits. The obtained PDPs of QWR devices depend on the WPG size. This shows that further small PDP values can be realized by scale down of WPG size.

Switching speeds of branch switches have been evaluated for QWR devices by direct high-frequency S parameter measurements at room temperature, using a vector network analyzer. Here, special devices having 90 nanowire switches are integrated in parallel have been used to cope with the high impedance nature of quantum device. The results have indicated GHz clock operation capability of branch switches from measured cutoff frequencies over 2 GHz for 110 nm-gate QWR-type devices [6,7].

On the basis of these encouraging results, feasibility of design and fabrication of standard circuit blocks for digital signal processing has been investigated. Here, it is important to be able to design any of such standard circuits on hexagonal nanowire networks without crossover of nanowires. A useful design guidance has been found to be the following; 1) omitting of terminal-0 (because the logic value can be determined by checking whether the messenger has arrived at the terminal-1 or not), 2) representation of a logic function by a principal disjunctive canonical form and 3) removal of redundant/equivalent nodes and branches without causing nanowire crossing. Various circuits for arbitrary bit number can be designed using this design approach. The BDD circuit diagrams of n-bit adder, subtractor and comparator are shown in **Fig. 5**, as examples. In these examples, any standard circuits for any number of bits can be designed by stacking basic units. It should be mentioned that BDD circuits require smaller number of devices than those in the CMOS logic gate architecture [12]. For example, an adder unit in the hexagonal BDD for requires 11 devices, whereas that of the CMOS logic gate requires 24 transistors. Other combinational circuits including decoder, encoder and parity checker have been also designed using the hexagonal BDD quantum circuit approach.

Some of the hexagonal BDD-based circuits have been successfully fabricated on hexagonal nanowire networks having node densities of a few ten mega nodes per cm^2 formed by EB-lithography and wet chemical etching. **Figure 6(a)** shows a fabricated QWR-type 2-bit adder as an example. This circuit integrates 14 node devices with a node density of $25\text{M}/\text{cm}^2$. The correct operation of this adder circuit was confirmed at room temperature as shown in **Fig. 6(b)**. Here, input logic swing and offset voltages are kept the same for all devices. This indicates that device characteristics are fairly uniform. It may be also the case that the hexagonal BDD circuits can operate allow rather wide variations of device parameters for correct performance. **Fig. 7** shows a fabricated QWR-type 8-bit adder, where 84 devices are integrated on $74\mu\text{m} \times 19\mu\text{m}$ area using a network

of 25 M nodes/cm² fabrication process. This is the highest scale of device integration so far reported for the quantum nanodevice circuits. Large number of BDD devices can be integrated without nanowire crossover. At present, 45 M nodes/cm² circuit fabrication process is being developed.

IV. TOWARD HEXAOGNAL BDD-BASED DIGITAL SYSTEMS

In order to see the feasibility of digital signal processing systems based on the hexagonal BDD quantum circuit approach, a 2-bit arithmetic logic unit (ALU) has been designed as a first step. The circuit diagram of a 8-instruction 2-bit ALU is shown in **Fig. 8(a)**. This ALU consists of circuits for each instruction combined with selector circuits for each bit. This is a very simple design approach, and makes it easy to check the logic operation even in the case when the numbers of bits and instructions are increased. The device count of the hexagonal BDD is 56 whereas the transistor count of a 7-instruction 2-bit CMOS ALU is 144. This is useful for reducing both the circuit area and the power consumption. This ALU will occupy areas of 360 μm^2 and 16 μm^2 nanowire network structures with node densities of 45 M and 1G nodes/cm², respectively. The SEM image of the fabricated QWR-type test ALU structure using 45 M nodes/cm² fabrication process is shown in **Fig. 8(b)**. The correct operation of the circuit has been confirmed by a SPICE circuit simulation as shown in **Fig. 8(c)**, although experimental confirmations need more time.

Most digital systems require sequential circuits such as registers. These circuits are difficult to implement by the BDD logic architecture with path switching at nodes. Sense amplifier and level adjusters are also necessary for signal level matching between different BDD logic blocks and between BDD and other blocks such as memory. For this purpose, use of WPG-controlled nanowire FETs formed on hexagonal networks has been investigated. As already shown in **Fig. 3(b)**, WPG-controlled nanowire pieces can operate as FETs. Fabricated inverters using the FETs on a hexagonal nanowire network have shown a transfer gain of 3, even at room temperature, and this is sufficient for implementation of sequential circuits and amplifiers. They obviously can operate also at low temperatures. Thus, whole of the system working from low temperatures to room temperature can be implemented on a hexagonal network structure. As shown in **Fig. 9(a)**, RS flip-flop (FF) circuits have been fabricated and their correct operations have been confirmed experimentally. This also confirms the capability of realization of static RAM (SRAM) on the hexagonal nanowire networks. As an example, a 128 bit SRAM designed on a hexagonal network with 66 x 44 hexagons is shown in **Fig. 9(b)**. Registers by D-FF and counters by T-FF were also successfully designed and correct operations were confirmed by SPICE simulation as shown in **Fig. 10**, allowing use of small input voltage swings.

Design Feasibility of the present circuit approach for the implementation of digital systems has been confirmed by a successful design of a static 2-bit nano-processor (NPU) as shown in **Fig. 11(a)**. Its system architecture is shown in **Fig. 11(b)**. Execution cores of this system, ALU and controller, are implemented by quantum BDD circuits. Here, the four ALU instructions are implemented. The device count of the hexagonal BDD-based 2-bit NPU is 381 devices, and this number is much smaller than that of about 700 transistors for a processor designed with CMOS logic gates using the same system architecture shown in **Fig. 11(b)**. The 2-bit nano-processor in **Fig. 11(a)** is now in the process of actual fabrication. Power consumption of the NPU has also been estimated. The system power consumption is estimated from activity factor, a , device count based

on this system architecture, n_d , and clock frequency, f_{clock} , by a formula, $P = a \cdot n_d \cdot \text{PDP} \cdot f_{\text{clock}}$. By counting the number of switching events in each component for typical system instructions and data processing, the activity factor has been estimated for each component. The average value is 0.2. Total power consumption can be obtained by summation of power consumptions of each component. Then the power consumption of the hexagonal BDD-based 2-bit NPU using SE-type devices in the quantum regime is estimated only 0.01 nW at 10 MHz clock. Here, 10 times large supply and logic swing voltages have been assumed for the sequential circuits. Even in the classical regime, the system consumes 1 μW at the same clock frequency, where $\Delta V_G = 400\text{mV}$ from the data in **Fig. 6(b)** has been assumed. It is seen that most of the power is consumed in sequential circuits in the present system architecture. Further sophisticated design of the system architecture and exploring other approaches to implement sequential circuits are thus desirable. On the other hand, when the number of bit increased, system power consumption is dominated by combinational circuits, because their device count increases rapidly with the order of $(n^2 + n) \cdot N$, where n is the number of bit and N is the number of ALU instructions, although the other parts increases with the order of n or $n \cdot N$. In addition, the device counts in BDD-based combinational circuits is smaller than that of CMOS logic gate combinational circuits [12]. Therefore, the power consumption of the hexagonal BDD-based digital systems for large number of bits will become much smaller than that of the CMOS systems.

For further high-density integration of the system and its quantum regime operation at room temperature, denser hexagonal networks with narrower nanowires realizing strong electron confinement are required. For this purpose, formation of embedded GaAs nanowires by selective MBE growth on patterned substrates [13,14] has been investigated. The selective MBE growth can realize size- and position-controlled nanowires with smaller size than the lithography size where the GaAs nanowires are completely embedded in AlGaAs layer as shown in **Fig. 12(a)** so as to form high quality heterointerface. Thus, strong one-dimensional confinement is realized, and the operation temperature range of BDD node devices in the quantum regime is increased. As shown in **Fig. 12(b)**, a hexagonal nanowire network structure over 200M nodes/cm² has been successfully formed, and this will realize the 2-bit NPU discussed here on an area of only 20 x 29 μm^2 . The nanowire network structure having Giga-node density has also been realized by the selective MBE growth of InP-based materials [15]. QWR-type node devices using the embedded nanowires controlled by WPGs has been fabricated [16,17] and their excellent path switching characteristics have indicated good prospects for realization of the highly dense hexagonal BDD-based digital systems using the hexagonal nanowire networks by the selective MBE growth.

V. CONCLUSIONS

Feasibility of design and implementation of ultra-small-size and ultra-low-power digital systems utilizing the hexagonal BDD quantum circuit approach has been discussed on the basis of circuits formed on GaAs-based hexagonal nanowire networks controlled by nanometer scale Schottky wrap gates (WPGs). Starting from basic node devices and elementary logic function blocks, fabrication technology of hexagonal BDD quantum circuits up to 8-bit adders with node densities over 45 million nodes/cm² has been successful developed. Correct circuit operations at low temperatures and room temperature have been confirmed by experiments and simulation. Various circuit components in logic processors, including arithmetic logic unit (ALU), controller and

decoders have been successfully designed as hexagonal BDD layouts without nanowire crossover. For sequential circuits, WPG-controlled nanowire FETs on hexagonal networks have been investigated, and registers and counters have been implemented using these nanowire FETs showing correct operation. Hexagonal BDD-based static 2-bit nano-processor unit (NPU) has been successfully designed completely on hexagonal nanowire network. Ultra high-density GaAs hexagonal nanowire networks with much smaller wire sizes than those of etched nanowire networks have been successfully formed by selective MBE growth, showing great promise for room temperature operation in quantum regime as well as reduction of system area and power consumption.

ACKNOWLEDGMENT

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References

- [1] International Technology Roadmap for Semiconductors, <http://public.itrs.net/>
- [2] H. Hasegawa and S. Kasai, *Physica E* 11, 149 (2001).
- [3] S. Kasai and H. Hasegawa, *IEEE Electron Device Letter* 23, 446 (2002).
- [4] M. Yumoto, S. Kasai and H. Hasegawa, *Micro-electronic. Eng.* 63, 287 (2002).
- [5] S. Kasai, M. Yumoto and H. Hasegawa, *Solid-State Electronics* 47, 199 (2003).
- [6] M. Yumoto, S. Kasai and H. Hasegawa, presented at 45th Electronic Materials Conference (EMC), June 25 - 27, 2003, Salt Lake City, Utah, USA.
- [7] M. Yumoto, S. Kasai and H. Hasegawa, to be presented at 31st International Symposium on Compound Semiconductors, Sep. 12-16, 2004, Seoul, Korea.
- [8] S. B. Akers, *IEEE Trans. Compt. C-27*, 509 (1978).
- [9] N. Asahi, M. Akazawa, and Y. Amemiya, *IEEE Trans. Electron Devices* 44, 1109 (1997).
- [10] S. Kasai, K. Jinushi, H. Tomozawa and H. Hasegawa, *Jpn. J. Appl. Phys.* 36, 1678 (1997).
- [11] R. Chau, presented at 2001 Silicon Nanoelectronics Workshop, June 10-11, 2001, Kyoto, Japan.
- [12] K. Yano, Y. Sasaki, K. Rikino and K. Seki, *IEEE J. Solid-State Circuits* 31, 792 (1996).
- [13] T. Sato, I. Tamai, C. Jiang and H. Hasegawa, *Institute of Physics Conference Series* 170, 325 (2002).
- [14] I. Tamai, T. Sato and H. Hasegawa, *Physica E* 21, 521 (2004).
- [15] T. Fukushi, T. Muranaka, and H. Hasegawa, presented at 5th International Conference on Indium Phosphide and Related Materials, May 12-16, 2003, Santa Barbara, USA.
- [16] M. Yumoto, T. Tamura, T. Sato and H. Hasegawa, *Superlattice and Microstructures* 34, 485 (2004).
- [17] T. Tamura, M. Yumoto, T. Sato and H. Hasegawa, presented at 46th Electronic Materials Conference, Jun. 23-25, 2004, Nortre Dame.

Figure 1: Basic concept of hexagonal BDD quantum circuits.

Figure 2: (a) Implementation of the hexagonal BDD quantum circuit and Schottky wrap gate (WPG) structure and (b) designs of WPG-based BDD quantum node devices.

Figure 3: (a) SEM image of fabricated WPG-based QWE-type BDD quantum node device, (b) its $I_{DS}-V_{DS}$ characteristics, (c) conductance characteristics of branch switches in QWR and SE-type devices, and (d) path switching characteristics of the QWR-type node devices.

Figure 4: Basic BDD logic elements and their operations. (a) QWR-type AND logic and (b) SE-type OR logic.

Figure 5: Circuit diagrams of hexagonal BDD subsystems. (a) Adder, (b) subtractor and (c) comparator.

Figure 6: (a) SEM image of fabricated hexagonal BDD QWR-type 2-bit adder and (b) its input-output waveforms.

Figure 7: SEM image of fabricated hexagonal BDD QWR-type 8-bit adder.

Figure 8: (a) Circuit diagram of hexagonal BDD 8-instruction 2-bit ALU, (b) SEM image for fabricated circuit and (c) input-output waveforms by simulation.

Figure 9: (a) RS flip flop design and measured input-output waveforms and (b) 128-bit SRAM design.

Figure 10: Design of D-FF and T-FF, and input-output waveforms for register and 3-bit counter.

Figure 11: (a) Hexagonal BDD-based static 2-bit nano-processor design and (b) its system architecture.

Figure 12: (a) Cross section of the selectively MBE grown GaAs nanowire and (b) high-density hexagonal GaAs-embedded nanowire network with node density of 2.3×10^8 nodes/cm².

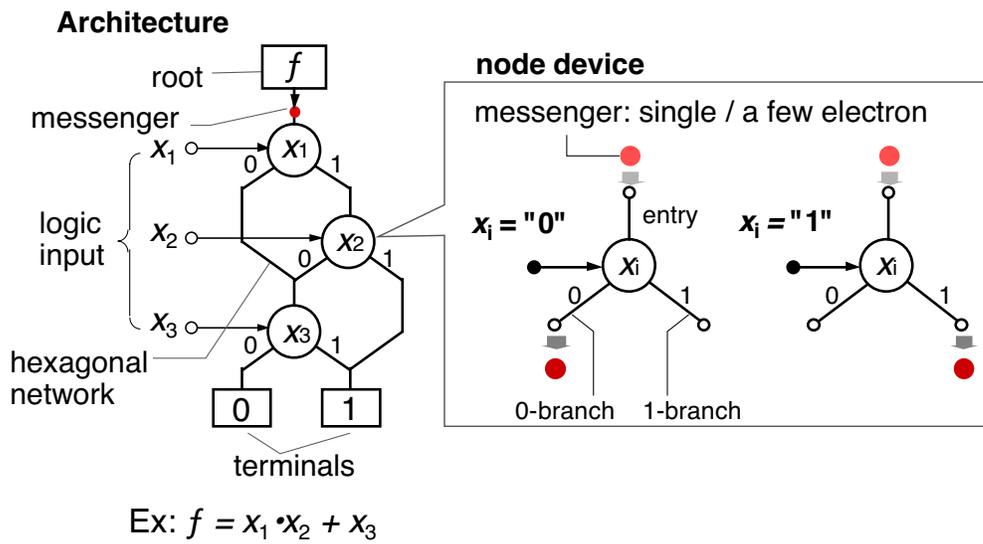


Figure 1: Basic concept of hexagonal BDD quantum circuit approach.

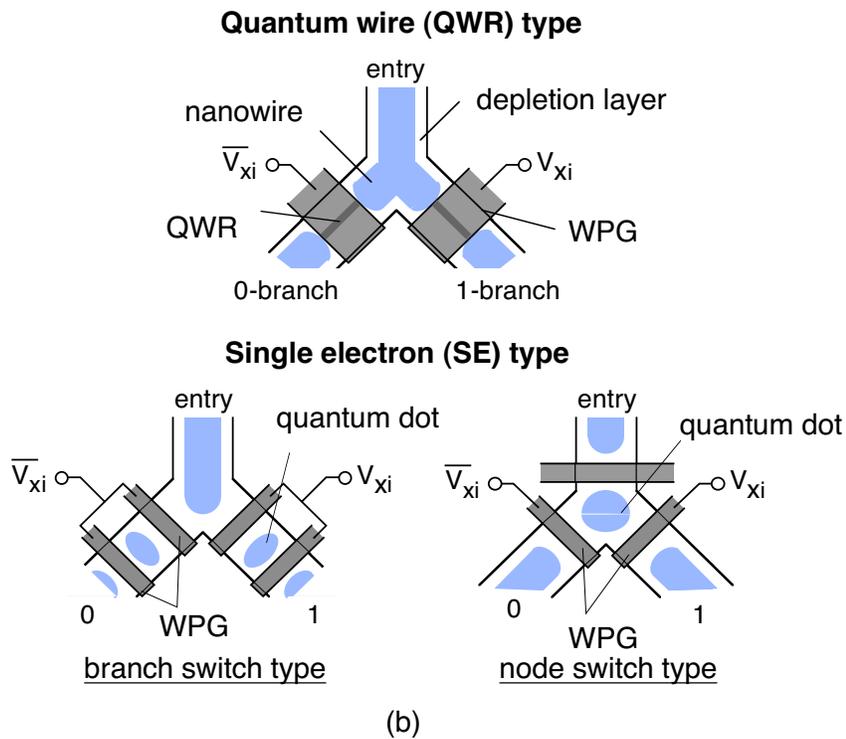
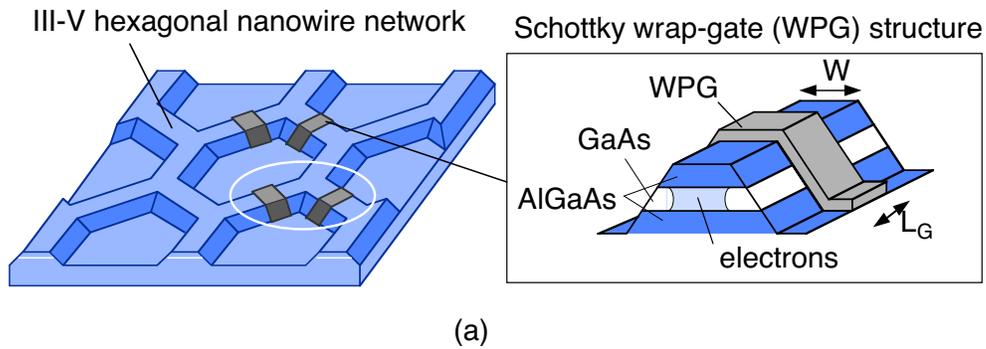


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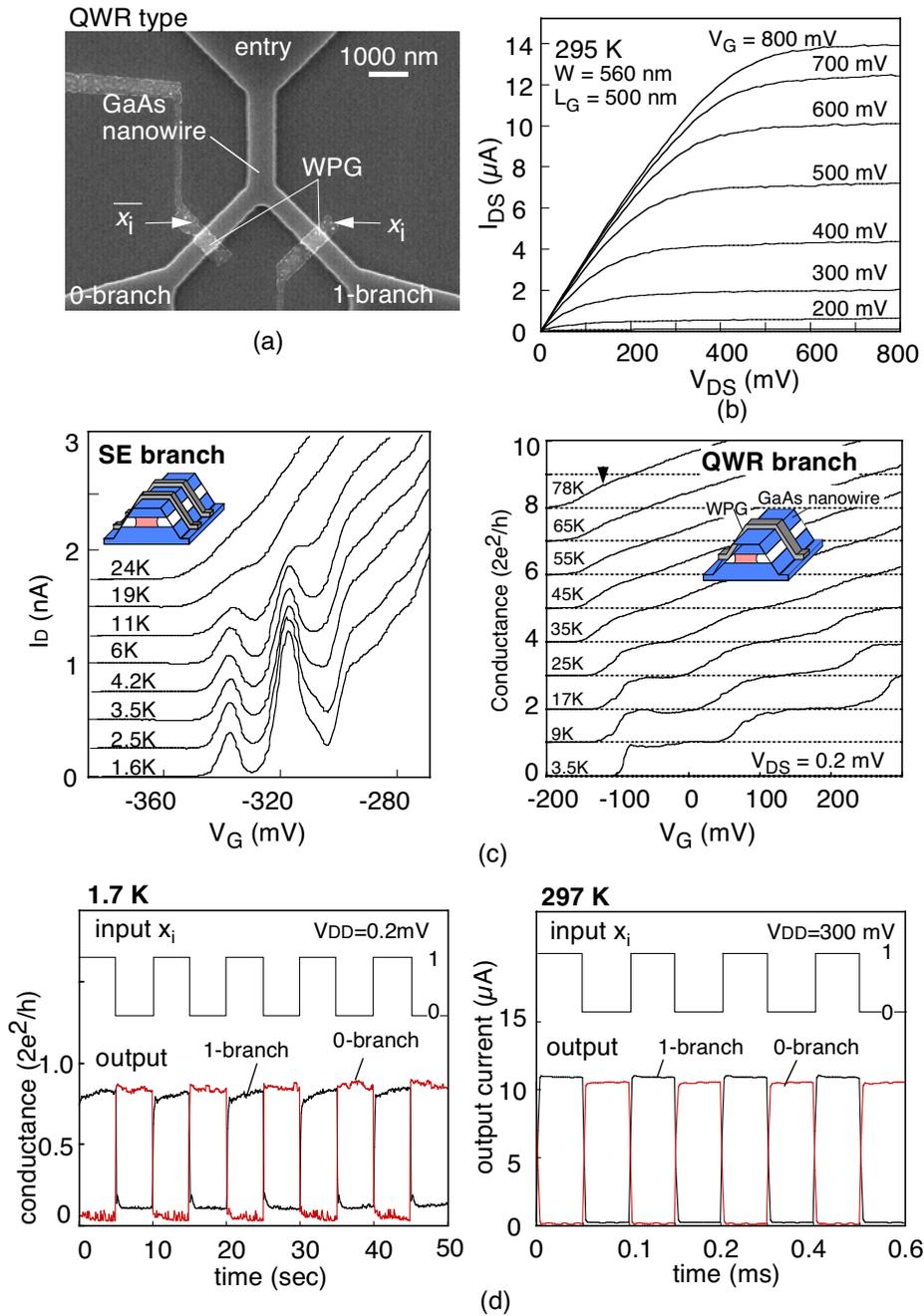


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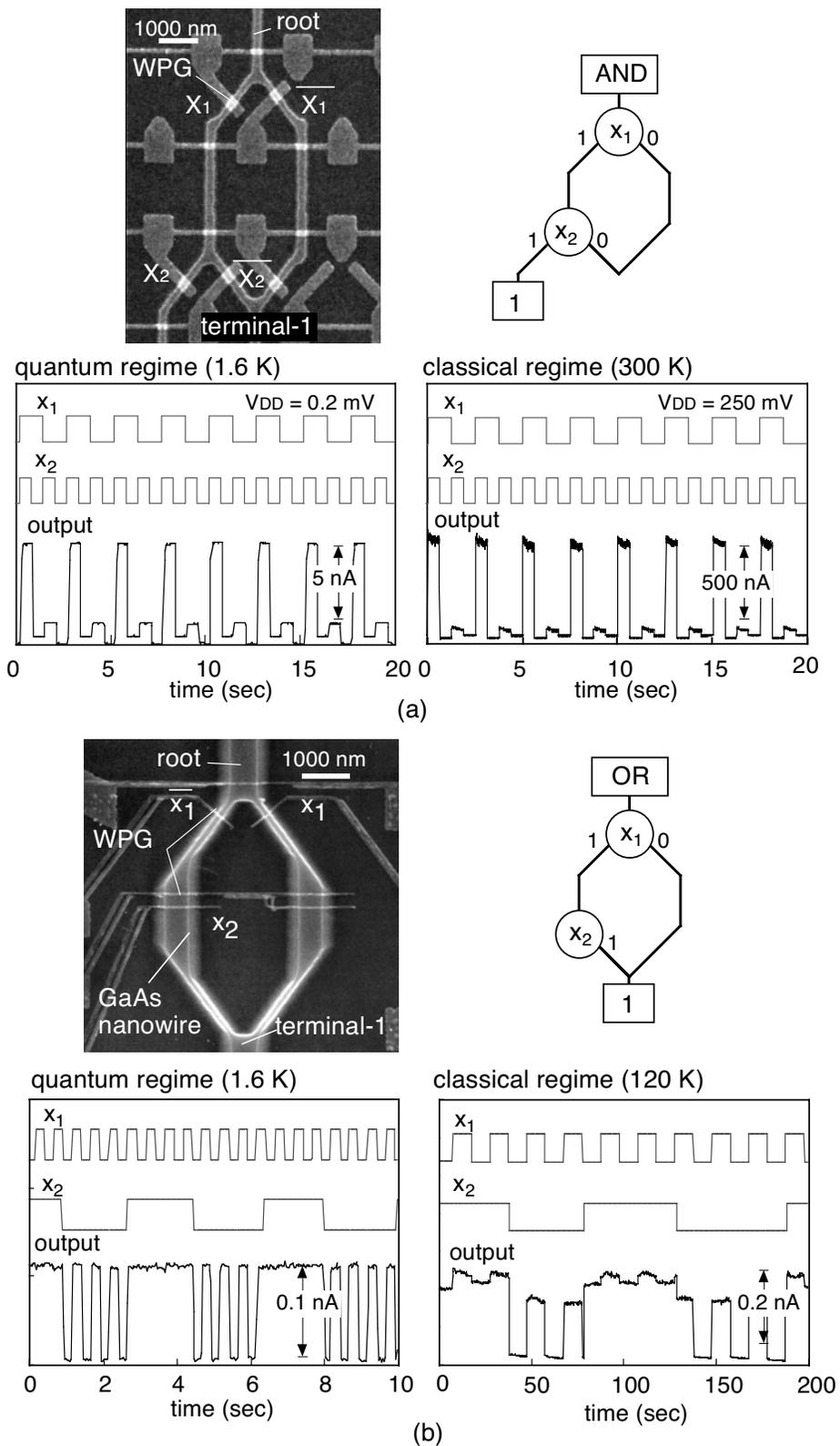


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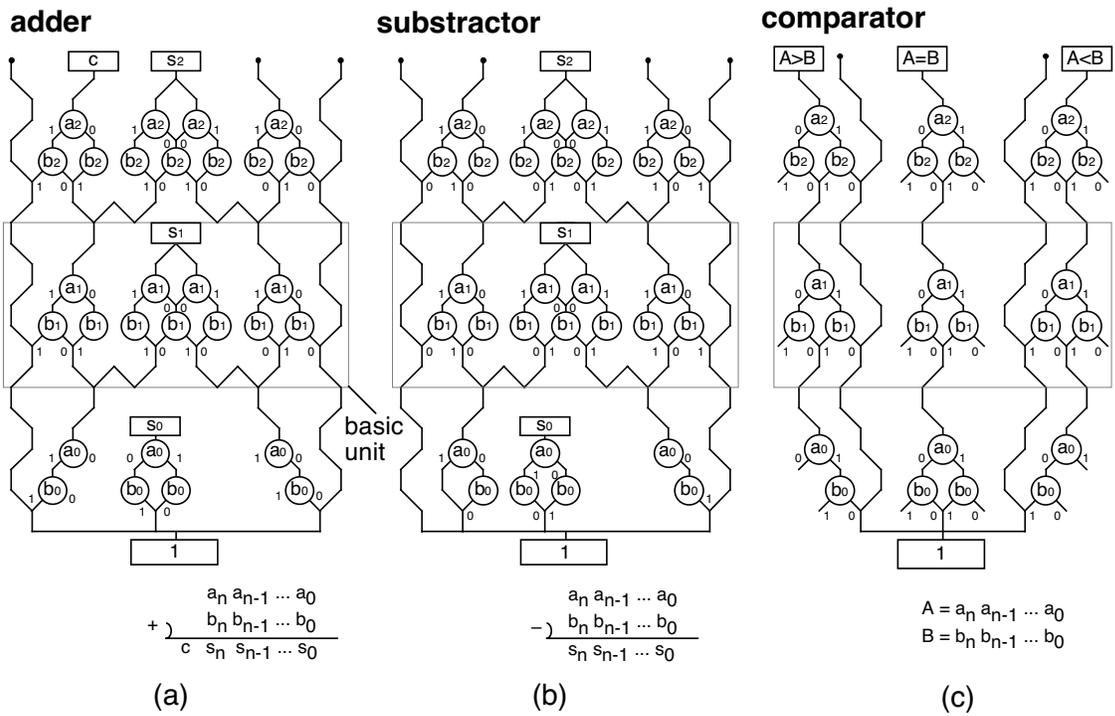
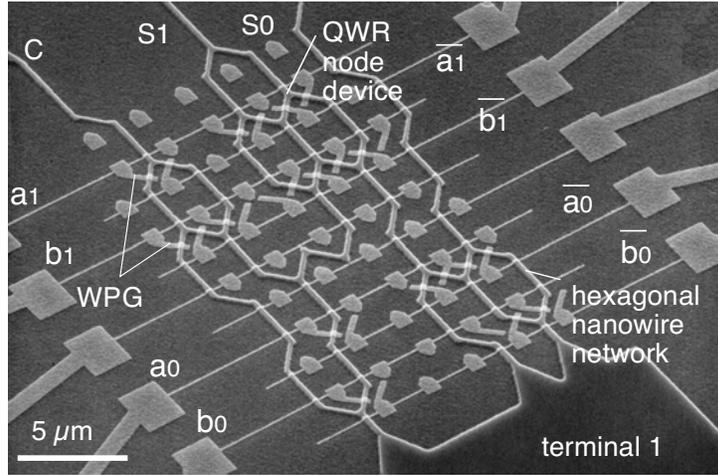


Figure 5: Circuit diagram of hexagonal BDD subsystems. (a) Adder, (b) subtractor and (c) comparator.



$$\begin{aligned}
 c1 &= a1 \cdot b1 + a0 \cdot b0 \cdot (a1 + b1) \\
 s0 &= a0 \oplus b0 \\
 s1 &= \overline{a0} \cdot \overline{b0} \cdot (a1 \oplus b1) + a0 \cdot b0 \cdot (\overline{a1 \oplus b1})
 \end{aligned}$$

(a)

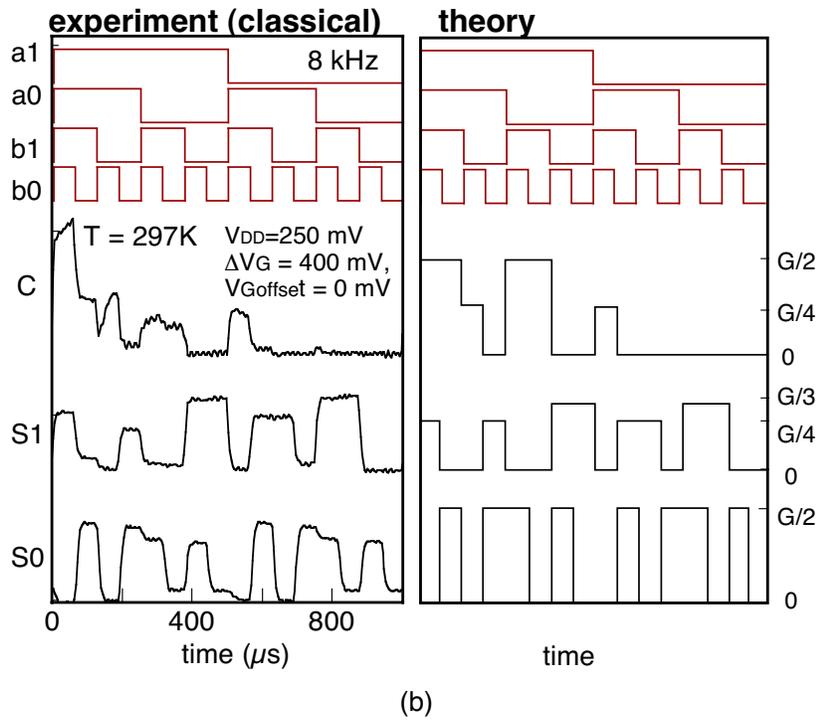


Figure 6: (a) SEM image of fabricated hexagonal BDD QWR-type 2-bit adder and (b) its input-output waveforms.

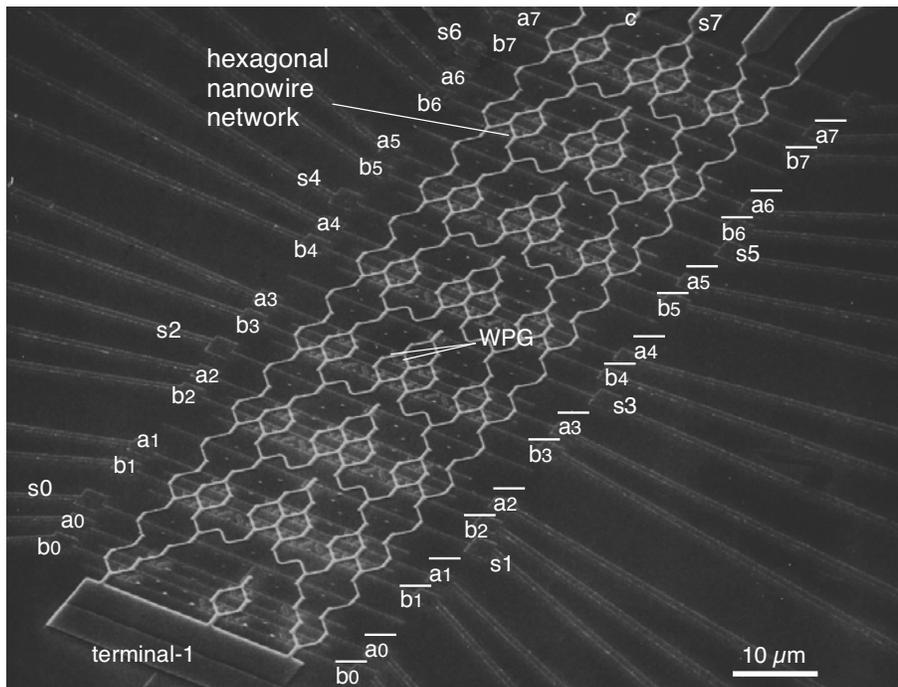
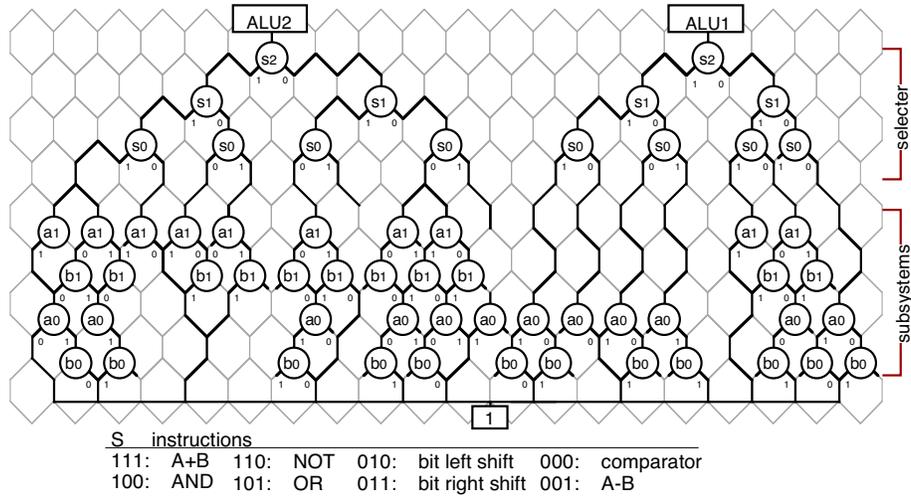
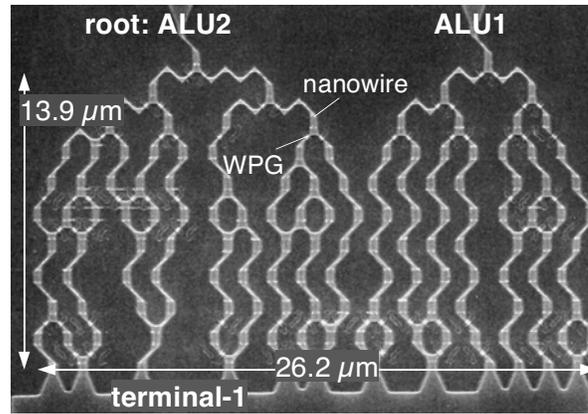


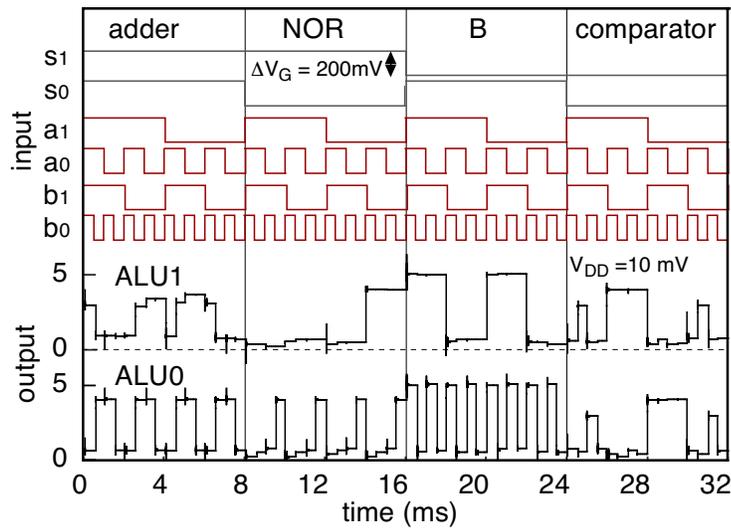
Figure 7: SEM image of fabricated hexagonal BDD QWR-type 8-bit adder.



(a)



(b)



(c)

Figure 8: (a) Circuit diagram of hexagonal BDD 8-instruction 2-bit ALU, (b) SEM image for fabricated circuit and (c) input-output waveforms by simulation.

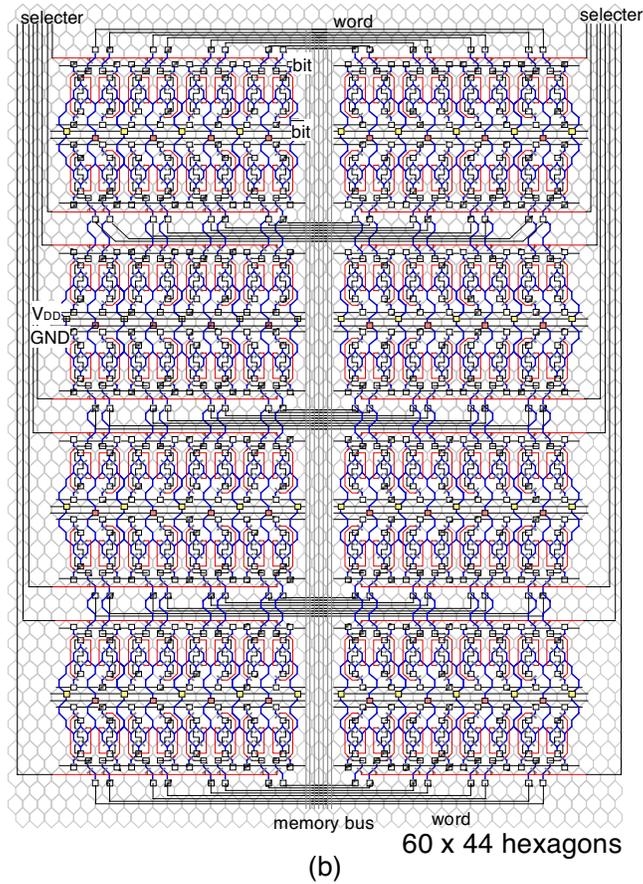
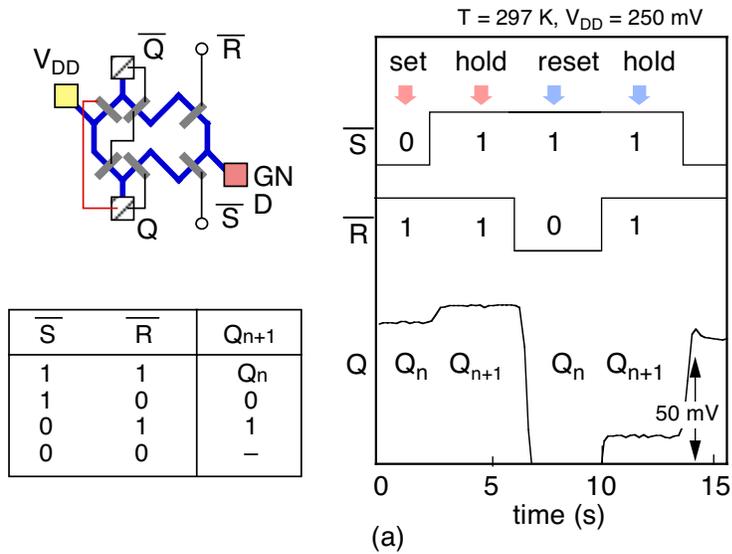
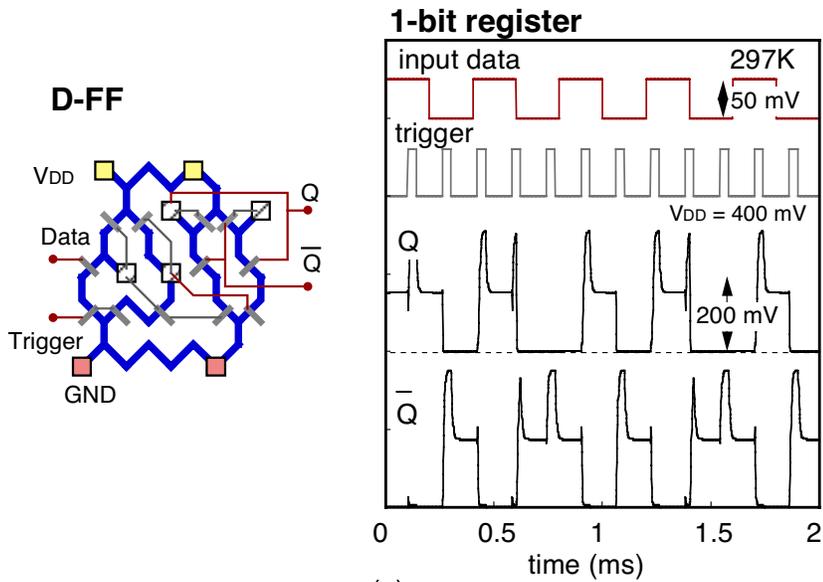
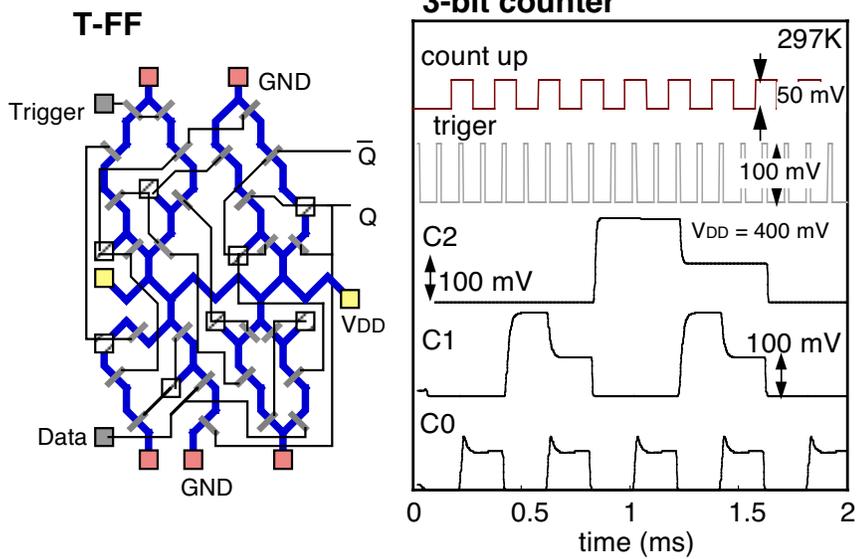


Figure 9: (a) RS flip flop design and measured input-output waveforms and (b) 128-bit SRAM design.



(a)



(b)

Figure 10: (a) Design of a D-FF and input-output waveforms of a register, and (b) design of T-FF and input-output waveforms of 3-bit counter by T-FF.

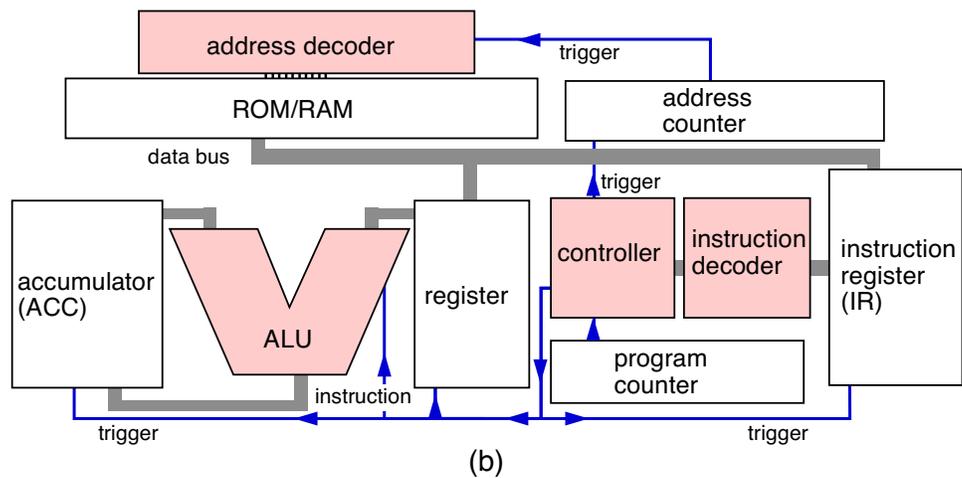
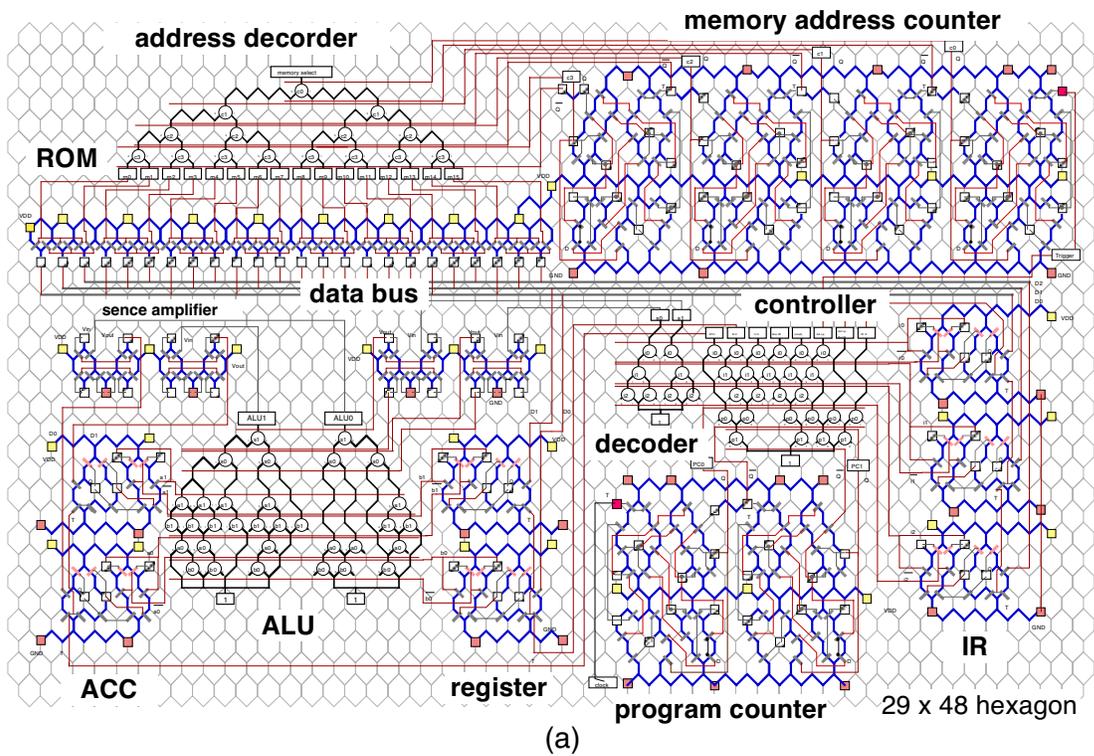
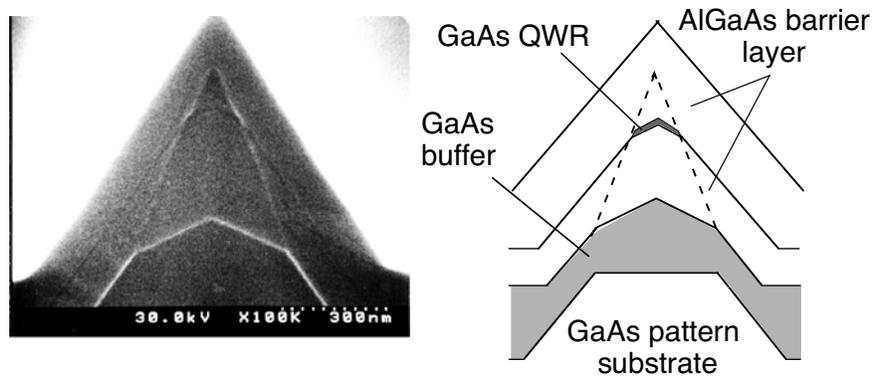
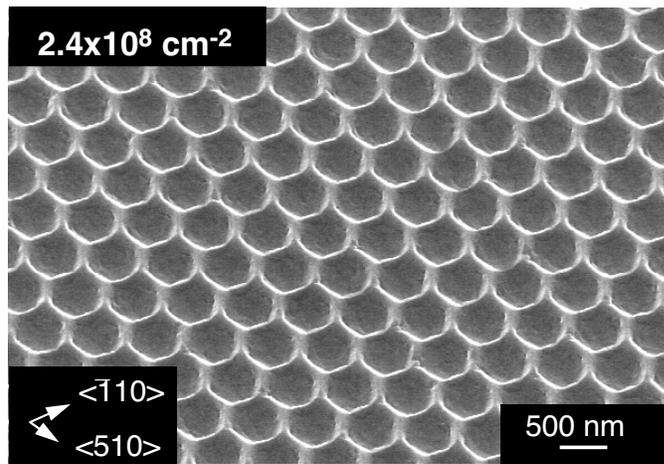


Figure 11: (a) Hexagonal BDD-based static 2-bit nano-processor design and (b) its architecture.



(a)



(b)

Figure 12: (a) Cross section of the selectively MBE grown GaAs nanowire and (b) high-density hexagonal GaAs-embedded nanowire network with node density of 2.3×10^8 nodes/cm².