Doctoral Dissertation

博士論文

Growth of III-V Compound Semiconductor Nanowire Heterostructures and Their Electron Device Applications

（III-V 族化合物半導体ナノワイヤヘテロ構造の成長と電子デバイス応用）

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Chapter 1

Introduction

1.1 Background

The first integrated circuits based on bipolar transistors were fabricated in 1959 [1], and the semiconductor industry has achieved rapid progress over the past 60 years. Integrated circuits have progressed by increasing integration in accordance with Moore's Law of scaling. This "law" notes that the number of devices on integrated circuits increases exponentially, doubling every 2-3 years. High integration, or miniaturization of transistors, reduces the cost per function of integrated circuits while improving circuit characteristics (speed in the on-state, power consumption, etc.). This geometric scaling, the "Dennard scaling," has been the guiding principle over the past 50 years [2]. The scaling means reducing the transistor size (gate length, L, gate width, W, gate oxide thickness, t_{ox}) of integrated circuits and improving performance by lowering the supply voltage and increasing impurity doping concentration to keep the electric field in the device constant. However, at the 22 nm technology node and beyond, the tradeoff between improved performance gain and reasonable power consumption has become

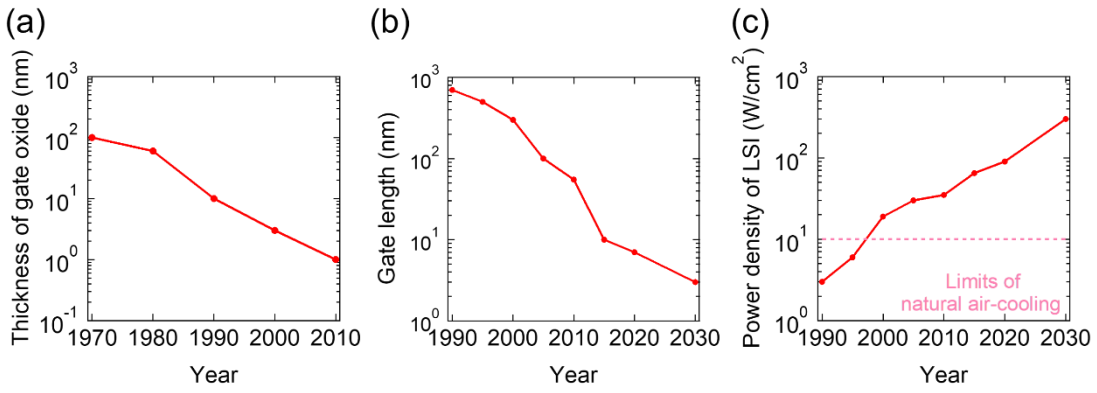

Figure 1-1: (a) Progress in gate oxide scaling. (b) Evolution of gate length. (c) Power density scaling trend.

more challenging with conventional scaling. As shown in Fig. 1.1(a), the scaling of gate dielectrics has progressed, and the thickness of gate dielectrics using SiO_2 has reached about 1 nm. The geometric scaling of the gate dielectric has reached fundamental limitations due to the direct tunneling of electrons. As shown in Fig. 1.1(b), the gate length also shrinks, and the short-channel effects (SCEs) became apparent from the 22 nm technology node. SCEs lead to severe issues, including threshold voltage roll-off, drain-induced barrier lowering (DIBL), velocity saturation, leakage current rise, mobility reduction, hot carrier effects, and other annoyances. One solution to this problem is reducing the gate oxide thickness to improve electrostatic gate control, but it is difficult due to the tunneling current. Another solution is to increase the doping of the channel. However, ionized impurity scattering increases with increasing impurity density, resulting in lower on-current due to lower mobility. Thus, in order to extend scaling, specific strategies must be implemented to circumvent these SCEs.

On the other hand, power consumption is expected to increase further with the expansion of the Internet, as shown in Fig. 1.1(c). The Internet of Things, computational algorithms, and other application technologies that require more computational functions than ever before are attracting attention, and integrated circuits require even faster-switching speeds and lower-power consumption. A Complimentary Metal-Oxide-Semiconductor (CMOS) based logic integrated circuit is proportional to the square of the drive voltage. Reduction in drive voltage is necessary to reduce low power consumption while improving the performance of individual field-effect transistors (FETs). In order to maintain the scaling at low voltages, next-generation technologies have focused on technology boosters to improve performance, such as introducing strain to channels, new channel materials, high-κ dielectrics/metal gate stacks, lowering contact resistance, and multi-gate structures [3–7].

1.2 Technology Boosters

The technology boosters have continued FET performance improvement and reduction in power density. Figure 1.2 shows the transition to new device architectures. The novel FET structure is expected to switch from planar structures to nanosheet and nanowire gate-all-around (GAA) or surrounding-gate (SG) structures. The tri-gate architecture (Fin

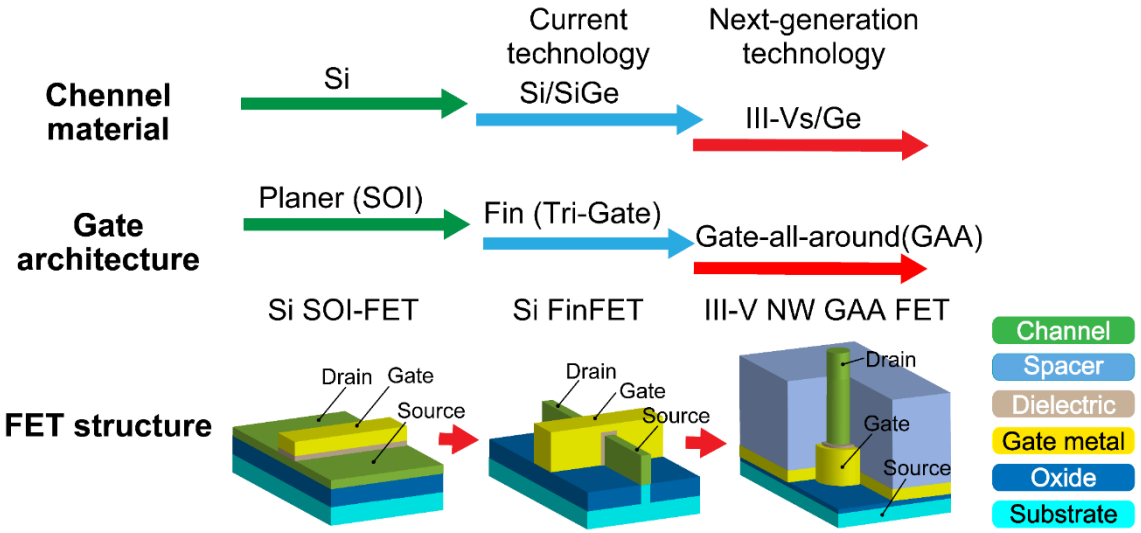

Figure 1-2: Integrated circuit technology transition. FET structure transition from planer Si SOI-FETs to III-V nanowire vertical GAA-FETs.

FET) was already introduced by *intel* in 2012 for their 22 nm node technology. The multi-gate structure can improve gate controllability and suppress short-channel effects. The GAA structure will likely be the final miniaturized transistor solution.

The gate leakage problem has been apparent since the late 1990s due to the tunneling current [8]. The tunneling currents decrease exponentially with increasing distance. To solve this tunneling problem, SiO_2 must be replaced by a thicker layer of new material with a higher relative dielectric constant. It is possible to realize MOSFETs that operate electrically equivalent to SiO_2 gate dielectrics thinner than 1.2 nm by using high-κ dielectrics such as HfO_2 with a high relative dielectric constant. A channel material with high mobility can increase ON-state current and reduce delay. III-V compound semiconductors, Ge, and two-dimensional materials have higher carrier mobilities than silicon, making them potentially useful for low-power and high-speed computations [9–12]. However, most high-mobility materials have significantly smaller bandgap than Si, resulting in substantial band-to-band tunneling leakage currents, ultimately limiting scalability. As shown in Figure 1-2, it is essential to simultaneously advance these technologies and utilize Si platform technology by forming new channel materials such as III-V compound semiconductors and Ge on Si substrates from the viewpoint of cost and mass production.

1.3 III-V MOSFET on Si

There are two challenges to realizing CMOS consisting of III-V compound semiconductor channels on Si substrates, as follows

(1) Cointegration on Si substrate

(2) Realization of high-performance n-type and p-type MOSFETs

1.3.1 Cointegration on Si

The heteroepitaxial growth technology for III-V compound semiconductors on Si substrates has problems such as lattice mismatch, the difference in thermal expansion coefficient, and antiphase domain. It has become clear that the selective growth method, in which the growth region is reduced to the nanometer scale and defect formation due to lattice relaxation is suppressed, and the method in which only high-quality crystal layers were epitaxially grown on a different substrate is separated from the substrate and bonded onto Si can overcome the hetero-accumulation issues [13]. The former selective growth method can suppress the formation of antiphase domains by growing hetero on the (111) plane. Also, with regard to the difference in thermal expansion coefficients, destructive stresses are less likely to act on microcrystals such as nanowires. On the other hand, a drawback of the selective growth method is that the composition, crystal shape, impurity doping control, and other factors are affected by the design of the growth region during initial nucleation and subsequent epitaxy, and the control is not easy.

1.3.2 High-Performance N- and P-type MOSFETs

With the limitations of Si CMOS scaling, expectations for technology booster technologies have increased, and post-scaling generation CMOS technologies using III-V compound semiconductors and Ge channels that outperform the current channel material, strained Si, are being considered. Table 1-1 summarizes the important properties of the major III-V compound semiconductors. Considering process complexity, it is

Table 1-1: Representative semiconductor properties

	Si	Ge	GaAs	InP	InGaAs (In53%)	InAs	GaSb	InSb
Electron mobility (cm^2/Vs)	1600	3900	9200	5400	12000	33000	3000	77000
Effective Mass of electron, m_e/m_0	0.19	0.082	0.067	0.082	0.041	0.023	0.041	0.014
Hole mobility (cm^2/Vs)	450	1900	400	200	300	500	800	850
Bandgap (eV)	1.12	0.66	1.42	1.34	0.74	0.36	0.73	0.17
Effective DOS in conduction band (10^{19} cm^{-3})	3.2	1.0	0.047	0.057	0.021	0.0087	0.021	0.0042

desirable to use the same channel for both n-type and p-type, but most III-V materials have low hole mobility. Therefore, selecting various semiconductors for n-type and p-type channels is necessary. As seen from Table 1-1, semiconductors with small electron effective mass also have a small effective density of states in the conduction band and large electron mobility, contributing to increased on-current.

On the other hand, the free electron density is the value obtained by multiplying the electron density of states by the Fermi-Dirac distribution function and integrating from the lower end of the conduction band to the infinity point. This tradeoff between mobility and the density of states may offset the increase in on-current due to high mobility. This tradeoff between mobility and density of states is one of the considerations in semiconductor selection. In addition, under a high electric field, a transition occurs from the energetically stable Γ valley to the L valley, which has a large electron-effective mass. Another consideration is that a large energy difference between these valleys is desirable to avoid mobility reduction due to valley scattering. Based on these factors, InAs and InGaAs as n-type channel materials and Sb-based semiconductors as p-type channels are expected. Worldwide, reports of n-type FET devices using III-V compound semiconductors have been increasing in recent years. On the other hand, there have been few reports on p-type FET devices, and good switching characteristics have not been obtained. This is because the crystal growth technology for Sb-based semiconductors with high hole mobility is still immature, and high-quality crystals have not been obtained.

Furthermore, the intrinsic physical difference between electrons and holes results in a mobility difference of 2~10 times, making it impossible to match the current density in a circuit. Therefore, to match the current density, it is necessary to reduce the device size, adjust the integration area compared to n-type devices, and improve performance by applying unique structures and technologies. Recently, applying compressive strain has

reported high hole mobility of 1500 cm^2/Vs in GaSb/AlAsSb heterostructures [14]. The realization of high-performance n- and p-type MOSFETs requires technology boosters such as high-mobility channel materials, GAA structures, and strain effects. From the viewpoint of industrial applications, heterogeneous integration technology on Si is also important, and vertical III-V nanowires on Si play a major role as channels.

1.4 Objective

Based on the background described in the previous section, the objective of this study was to improve the performance of InAs nanowire vertical GAA-FETs as n-type FETs, establish growth technology for InGaAs/GaSb CS nanowires as p-type channels, and simultaneously integrate n-type and p-type FETs. Therefore, this thesis aims to realize three-dimensional integrated circuits composed of III-V compound semiconductor nanowires. The specific objective of this thesis is as follows;

i. to suppress off-state leakage current and to enhance on-state current of InAs nanowire vertical GAA-FETs,

ii. to investigate a growth condition dependence of InGaAs/GaSb CS nanowires,

iii. to characterize InGaAs/GaSb CS nanowire vertical GAA-FETs as n- and p-type FETs.

1.5 Outline of This Thesis

This chapter describes the background and objectives of this study and provides an overview of the chapters. This thesis is divided into eight chapters.

Chapter 2 describes the history, features, and fabrication methods of semiconductor nanowires. In addition, the basic principle, structure, and performance of MOSFET are explained.

Chapter 3 describes the fundamental growth mechanism of the metal-organic vapor-phase epitaxy method used in this study, as well as the process technology used for device fabrication and the equipment used for characterization.

Chapter 4 discusses InAs nanowire vertical transistors improving off-leakage characteristics and switching by forming a pseudo-true layer with compensating doping and a contact layer with high-concentration doping. The minimum subthreshold slope (SS) of 68 mV/decade was achieved, close to the minimum theoretical limit of SS for FETs (60 mV/digit). The introduction of the pseudo-true layer reduces the off-leakage current, revealing that the SS can be significantly reduced. Transmission electron microscopy observation confirmed that the facets of InAs nanowires are flat at the atomic layer level, and the InAs nanowire/oxide film interface exhibits good interfacial properties.

Chapter 5 investigates the crystal structure of InAs/InP core-shell nanowires and the electrical properties of vertical gate-all-around field-effect transistors using InAs/InP core-shell nanowires. We estimated the strain between InAs nanowires and InP shells using X-ray diffraction in the core-shell nanowire growth. Next, we investigated the formation of a two-dimensional electron gas for the vertical transistor by introducing a core-shell structure and found that the on-current increased with increasing the shell thickness. We also calculated the band structure and wavefunction of InAs/InP heterointerface by solving the one-dimensional Poisson-Schrödinger equation and confirmed that carrier confinement occurs near the heterointerface. Based on these results, we discussed the effect of the core-shell structure on device performance and showed that thicker InP shell films result in smaller oxide film capacitance and SS degradation, indicating a tradeoff between SS and on-current increase.

Chapter 6 investigates the growth temperature dependence and growth time dependence of InGaAs/GaSb core-shell nanowires. We focus on forming smooth GaSb layers by using the atomically smooth surfaces of the selectively grown nanowires as templates. At 500°C, a two-dimensional island grows on the top of the nanowire. At 540°C, the roughness of the facets increases. Next, the electrical characteristics of the InGaAs/GaSb heterojunction were characterized by fabricating a two-terminal device, and devices exhibit good rectification properties.

Chapter 7 described vertical transistors using InGaAs/GaSb core-shell nanowires on Si and their electrical characteristics. The drain current is modulated by gate voltage, and the transistor showed p-type switching operation with an on/off ratio of two orders of magnitude under negative gate voltage and n-type switching operation with an on/off ratio of three orders of magnitude under positive gate voltage. Under negative gate voltage, the barrier of InGaAs nanowires is modulated, and carrier conduction occurs due to hole diffusion. On the other hand, the carrier conduction is due to tunneling at the InGaAs/Si heterojunction under positive gate voltages. These results show n-type and p-type FET operation in a single device. The device provides fundamental knowledge for realizing three-dimensional integrated circuits using III-V nanowires.

Finally, conclusions and prospects for next-generation technology are described in Chapter 8.

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Chapter 2

Semiconductor Nanowires and MOSFET Theory

The bottom-up creation of semiconductor nanowires has opened up entirely new avenues for nanofabrication and the design and realization of various devices. Semiconductor nanowires are a new type of semiconductor whose cross-sectional area can be tuned from 1 to 100 nm and whose length spans from several hundred nm to millimeters. The "nanowire" was variously referred to as "nano-pillar," "nano-rods," or "nano-column." The study of nanowires represents the forefront of solid-state physics and technology today. Because of their unique and attractive physical properties, nanowires increasingly attract attention as the basic building blocks for new nanoscale devices and circuits.

2.1 History of Nanowire Growth

Historically, the first important milestone in nanowire vapor phase growth was Wagner and Ellis's work on the vapor-liquid-solid mechanism (VLS) in 1964 [1]. Wagner demonstrated that adding gold particles to silicon wafers with <111> oriented surfaces forms millimeter-sized silicon whiskers. Silicon tetrachloride, $SiCl_4$, was provided as a source material for silicon growth. Wagner's work in the 1960s laid the foundation for today's nanowire research. The free-standing semiconductor nanowires were used for nanoscale field-effect transistors, bipolar junction transistors, light-emitting diodes, nanoscale lasers, complementary inverters, and complex logic gates. This achievement is

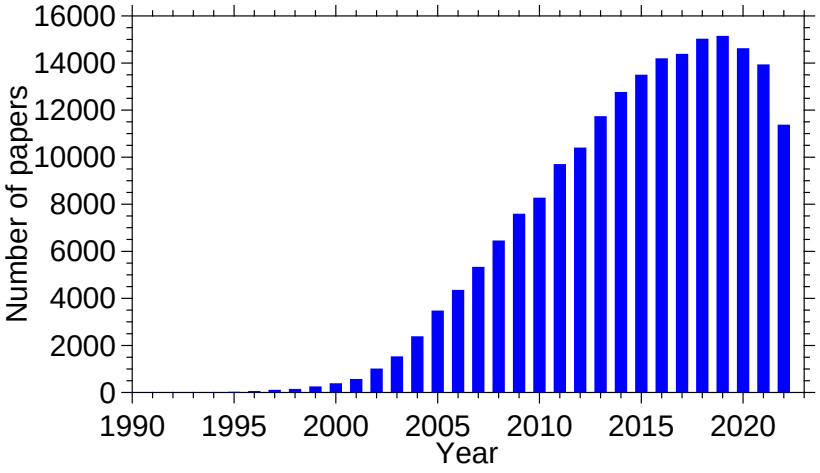


Figure 2-1: The number of papers published by year during the 1990-2022 period.

due to the first pioneering work done by K. Hiruma in the mid-1990s and by C. M. Lieber and P. Yang in the USA by the end of the 1990s and by L. Samuelson in Sweden and T. Fukui in Japan in the early 2000s.

Givargizov reported on VLS growth of compound semiconductors [2], and later, Hiruma's group at Central Research Laboratory, Hitachi Ltd., demonstrated the nucleation and growth with diameter below 100 nm, called whiskers, of III-V compound semiconductors such as InAs and GaAs [3–6]. This effort led to the first successful demonstration of the functionality of GaAs nanowire light-emitting devices [7] and the realization of heterostructures by combining InAs and GaAs [8]. Lieber's group from Harvard University has fabricated the first diode structure using p- and n-type crossed nanowires, assembling an active bipolar transistor that exhibits commutation transport similar to that of a planar p-n junction and increases emitter current, and has successfully assembled a complementary inverter that exhibits key elements of logic using p- and n-type nanowires [9]. Yang's group from the University of California, Berkeley, has demonstrated room-temperature ultraviolet lasing in zinc oxide nanowire arrays on sapphire substrates [10]. Samuelson's group has reported on the growth of one-dimensional InAs nanowhiskers containing segments of InP [11]. While all of these nanowires were fabricated by the VLS growth method, the first fabrication of InGaAs nanowire arrays using the catalyst-free selective-area growth method was reported in 2003 by Fukui's group from Hokkaido University. The successful demonstration of such

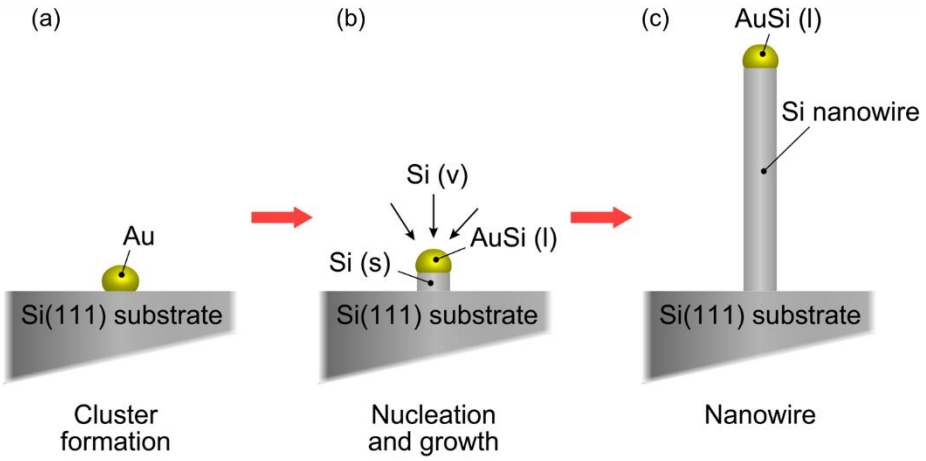
a wide variety of functional devices has led to a rapid increase in interest in nanowire research worldwide and a sharp rise in the annual number of publications ("Web of Science" database reports on papers published in 2022 that use "topic = nanowire OR nanowhisker OR nanorod OR nanocolumn OR nanopillar" and their plural forms as keywords).

2.2 Nanowire Growth Method

There are three basic approaches to forming nanowires. First is the top-down approach. This method takes a high-quality bulk material as a starting point from which the material is selectively etched to form the final structure. For this technique to be valid, it is essential to consider the effects of etching on exposed surfaces, as etching damage can degrade the intrinsic quality of the material. There are several examples where top-down approaches have been successful in fabricating nanowire structures that can improve device performance or add new functionality [12,13]. The second is the bottom-up approach. This approach does not rely on bulk starting materials to assemble nanowires, allowing the growth of materials or combinations of materials that are difficult or impossible to form in bulk. The third is the hybrid approach. This approach combines various patterning and selective growth processes. This section deals with nanowires fabricated by bottom-up or hybrid approaches such as catalyst-assisted VLS growth, selective-area growth (SAG), and template-assisted growth.

2.2.1 Catalyst-Assisted Vapor-Liquid-Solid Growth

The use of metal seeds to form elongated semiconductor crystals now dates back more than 50 years. Metal seed particles were used in microwires by Wagner and Ellis in the 1960s and nanowires by Hiruma *et al.* in the 1990s. This technology is often referred to as VLS because of the presence of three phases. The role of the metal seed particles is to provide a location where the growth rate is locally enhanced. The reduced nucleation



Figures 2-2: Schematic illustrations of VLS growth of Si nanowire. (a) A liquid droplet of Au is first formed on substrate. (b) Nucleation and growth from the liquid-solid interface. (c) Nanowire growth due to continuous incorporation of gaseous precursors.

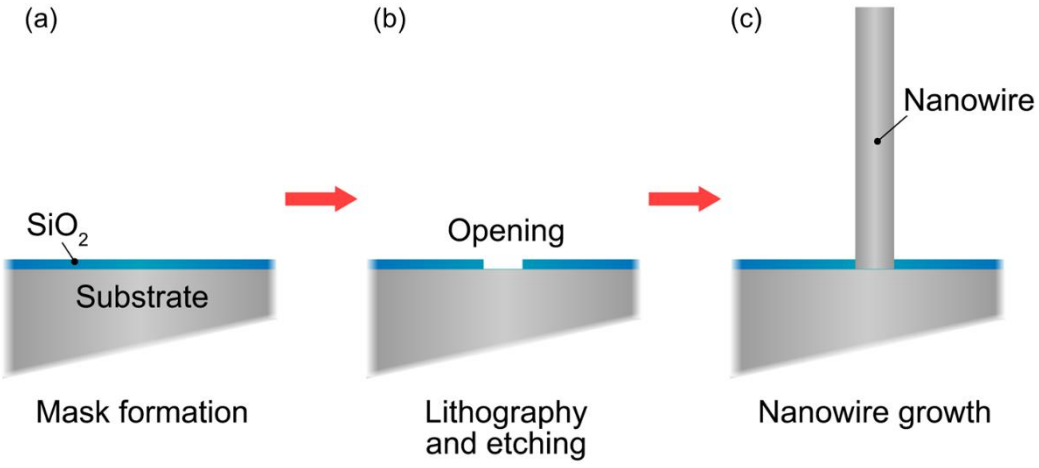
barrier under the seed particle compared to the substrate and nanowire side increases the growth rate. The wide process parameter space for Au-seeded nanowire growth makes it possible to grow and control nanowire structures using molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE).

Semiconductor nanowires are typically synthesized in a vapor-liquid-solid phase process. Figs. 2-2 (a)-(c) show a schematic illustration of catalyst-assisted VLS procedure of nanowire growth. This process is divided into three main steps: a) formation of tiny droplets on the substrate surface. b) supersaturation of the liquid by incorporating gaseous precursors and c) subsequent nucleation and growth of nanowires from the liquid-solid interface. Catalyst nanoclusters are deposited on the substrate surface by various methods. The precursor deposits to the liquid surface to form an alloy as the appropriate precursor gas flows through the reactor and encounters the metal droplet. The continuous incorporation of the precursors leads to the supersaturation of the desired compound, resulting in the growth of nanowires at the solid-liquid interface. However, the use of Au is incompatible with CMOS technology; given the unsuitability of Au for Si technology, a metal that would be a suitable catalyst for VLS growth is being explored. Criteria to be considered in the selection of a catalyst are (i) the solubility of the precursor in the metal, (ii) the solubility of the catalyst in the material to be grown, and (iii) the surface tension

of the catalyst. In other growth techniques, nanowires can be realized without metal catalysts on the substrate by thermal evaporation of appropriate source materials near their melting points and subsequent deposition at low temperatures. This method is often called “self-catalyzed growth” because one component of the source materials may serve as a catalyst.

2.2.2 Selective-Area Growth

SAG can grow vertically oriented nanowire arrays; in contrast to the VLS method, SAG does not use metal seed dots. Instead, SAG uses an amorphous mask such as SiO_2 and SiN_x to prevent nucleation in unwanted areas. Mask openings are formed by lithographic methods to expose the surface of the underlying semiconductor substrate (usually in the (111) direction). As shown in Fig. 2-3(c), vertical nanowires grow through these mask openings, and no materials are deposited in the area protected by the mask. SAG is usually performed in MOCVD systems to maintain growth selectivity. The diameter of SAG nanowires is determined mainly by the mask opening size. The selective epitaxial growth of Si was first reported by Joyce *et al.* in 1961 [14] and allowed for the growth of structures considerably larger than nanowires. Subsequently, the selective epitaxial growth of GaAs was first reported by Tausch *et al*., in 1965. In the late 1990s, nanowire



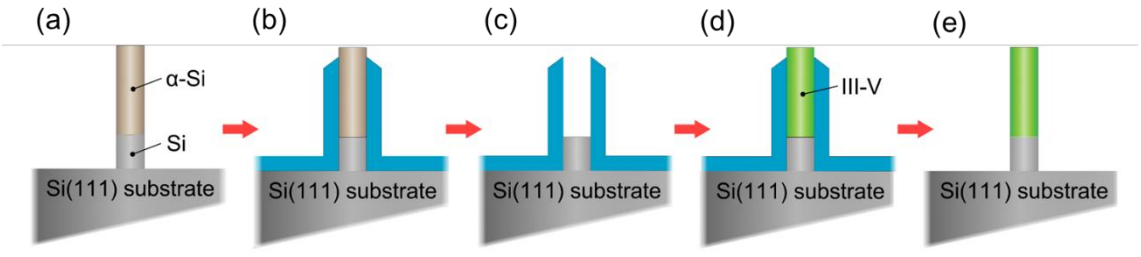
Figures 2-3: Schematic illustrations of SAG of nanowire. (a) Formation of mask to prevent nucleation in unwanted areas. (b) Formation of mask opening by lithography and etching. (c) Nanowire growth by nucleation on the mask opening area.

structures were fabricated for the first time using the SAG method by reducing the mask opening size [15]. The SAG of nanowires was greatly developed in the 2000s by Fukui's group, which grew materials such as GaAs[16,17], InAs[18,19], AlGaAs [20], InP [21], and InGaAs [22].

The SAG method has advantages such as the flexibility to incorporate heterogeneous integration of lattice-mismatched materials in the nanowires. A HEMT-like core-shell (CS) structure has been applied to these vertical SAG nanowires, improving carrier transport properties [23–27]. One of the critical issues with SAG III-V nanowires is that the as-grown nanowires exhibit a high density of stacking faults that act as scattering centers. Although phase-pure nanowires can be grown by VLS method, SAG nanowires without stacking defects have not been demonstrated to date.

2.2.3 Template-Assisted Growth

Recently, template-assisted growth has introduced nanowire growth. This method can grow nanowires vertically regardless of substrate orientation and demonstrated epitaxial growth of III-V homo- and heterostructure nanowires in various orientations [28–32]. Figs. 2-3 shows a schematic illustration of the template-assisted growth technique procedure of nanowire growth. In this method, nanotube templates made of oxides are fabricated on Si substrates and filled with III-V materials by selective epitaxy.



Figures 2-4: Schematic illustrations of template-assisted growth. (a) Etching of Si. (b) Formation of silicon dioxide mask template and top opening. (c) Back etching of α-Si. (d) III-V growth in a template. (e) Removal of the template.

2.3 Heterostructure Nanowires

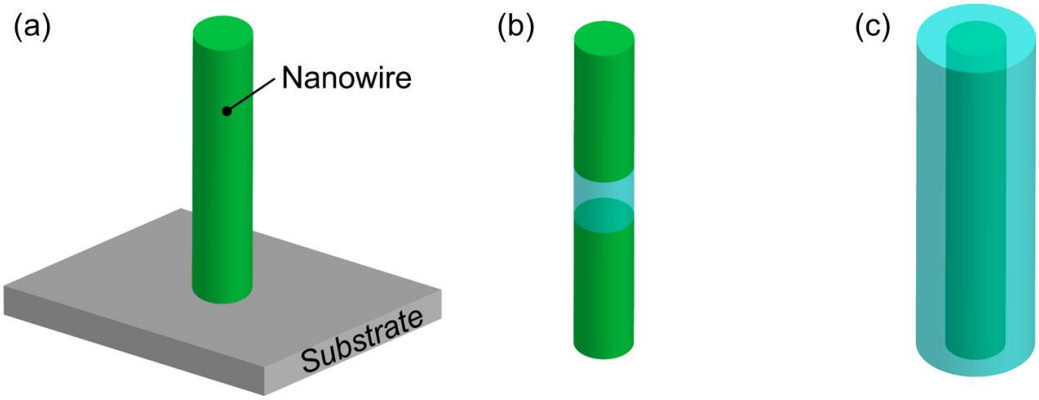
Compared to epitaxial films, one of the major advantages of nanowires is that there is unlimited potential for the formation of heterostructures in nanowires. Schematic illustrations of three related categories of heterostructures are shown in Fig. 2-5. Figs. 2-5(a)-(c) show heterostructures between the nanowires and substrate, axial (longitudinal) heterostructures, and radial (core-shell) heterostructures, respectively. The advantage of heterostructures is that different materials have different bandgaps, which are widely used in modern electronics and optoelectronics applications. The growth of complex nanostructures is the next step in developing functional materials with properly controlled interfaces. Heterostructures have provided unique properties and functionality that single-component materials cannot achieve. Nanowire-substrate, axial, and radial heterostructures will be explained.

2.3.1 Nanowire-Substrate Heterostructures

The simplest and most basic nanowire heterostructure is the integration of nanowires on a different material substrate (see Figure 1a). The most obvious motivation in this structure is the combination of III-V materials and silicon. The integration of III-V nanowires on Si substrate enables monolithic integration of highly specified optoelectronic and high-speed III-V devices. Tomioka *et al.* have fabricated tunnel field-effect transistors (TFETs) using III-V nanowire/Si heterojunction [33–39]. The heterojunction with Type-II band discontinuity is a promising tunnel junction for steep subthreshold swing (*SS*).

2.3.2 Axial Heterostructures

The ability to form axial heterostructures is one of the most critical advantages of nanowire geometry. Nanowires can relax perpendicular strains in the transverse direction. Because nanowires typically have less than 100 nm dimensions, they can mitigate strain



Figs 2-5: Schematic illustration of nanowire heterostructure. The different colors represent different materials. (a) Nanowire-substrate heterostructure. (b) Axial heterostructure. (c) Core-shell heterostructure.

without defect formation for much larger lattice mismatches than can be accommodated in bulk systems [40]. Therefore, as in planar technology, axial heterostructures are no longer limited to lattice-matched materials. Several defect-free axis heterostructure formations have been reported in Si/SiGe [41–44], InAs/InP [45–48], and GaAs/GaP [49–51] systems. Axial heterostructures are of particular interest in the field of electron transport. If layers of materials with sufficiently different bandgaps are formed thin enough, axial heterostructure can provide a variety of applications, including single-electron transistors [52,53], tunnel diodes [54,55], and TFETs [56–58]. In addition, controlling the steepness of axial heterojunctions has enabled the engineering of 1D superlattices [49,59,60].

2.3.3 Core-Shell Heterostructures

The core-shell heterostructures, in which the core nanowire is surrounded by radial heterostructure, have several advantages. The optical properties of nanowires can be significantly improved with proper surface passivation. Defects that usually occur on the surface or at the interface shorten the lifetime of minority carriers [61,62]. Nanowires have a high surface-to-volume ratio, resulting in a high surface recombination rate.

Moreover, charge carrier scattering occurs on the nanowire surface. Surface passivation in nanowire structures, therefore, plays an important role. Epitaxial growth of crystalline shells prevents these defects and scattering [63–66]. In addition, if the nanowire diameter is small enough, the electrons are confined to the potential well in the radial direction, resulting in quantized energy. The Bohr radius of excitons in bulk crystals indicates the length scale required for the quantum confinement effect to occur. For low-effective mass semiconductors such as InSb and InAs, quantum confinement effects can be observed with relatively thick nanowires, but for technically essential materials such as Si and GaAs, the diameter must be less than 20 nm. It is much easier to grow a shell of controllable thickness that behaves as a quantum well around a nanowire core than a single thin nanowire.

Core-shell structures, like HEMTs, allow modulation doping in the shell to spatially separate impurities and free carriers, reducing the scattering rate and improving carrier mobility [23]. Morkötter *et al.* fabricated delta-doped GaAs-AlGaAs CS nanowire transistors [26]. The device exhibits remarkable n-type performance with on-current saturation at zero gate voltage, indicating that electron gas accumulates in the GaAs/AlGaAs heterojunction due to modulation doping. Tomioka *et al.* fabricated FETs consisting of multiple InGaAs/InP/InAlAs/δ-doped InAlAs/InAlAs/InGaAs modulation-doped core-multishell (CMS) nanowires [27]. Compared to comparable devices formed with bare InGaAs nanowires, the modulation-doped nanowires showed considerably higher performance.

Recently, line-tunneling using CS structure has been proposed as attracted architecture for increasing the on-current in TFETs. TFETs using CS structure have a tunneling current along the gate-induced electric field, improving the on-current. Line-tunneling TFETs have been studied in IV [67] and III-V [68] material systems. Silicon-based TFETs suffer from low on-current due to their relatively large band gap. Therefore, a low bandgap is one of the most effective methods to increase the on-current. In particular, InAs/GaSb material system with low effective mass and narrow bandgaps is an ideal heterostructure for TFETs [69].

2.4 MOSFET Theory

2.4.1 Basic MOSFET Operation

The basic principle of MOSFET operation is that the voltage at the third terminal, the gate, controls the current between the two terminals, the source and drain, without flowing into or out of the gate itself. Fig. 2-6(a) shows a schematic of the device structure. The path between the source and the drain is called the channel. The gate structure is a MOS capacitor consisting of a metal electrode, a thin oxide dielectric, and a substrate. The gate control terminal is usually used as an input with the DC (direct) current flow blocked by the MOS capacitor, resulting in a highly efficient structure with extremely low power consumption. The operation of a MOSFET is illustrated in Fig. 2-6(b). N-type planar MOSFETs consist of highly n-doped regions implanted into a p-doped substrate as the source and drain contacts. A negative potential barrier is formed between the source and the channel, preventing electrons from flowing out of the source because the Fermi level is close to the edge of the balance band in p-doped channel regions. Thus, the current does not flow through the channel without an applied voltage, $V_{GS,}$ between the gate and the source, and the MOSFET is in the off-state. When a sufficiently high voltage is applied to the gate, the channel surface potential is high enough to lower the potential barrier at the source-channel pn junction. Electrons can pass from the source through the channel and into the drain for the positive drain bias. This is the on-state of the MOSFET. MOS device operation and derivations can be found in [70,71].

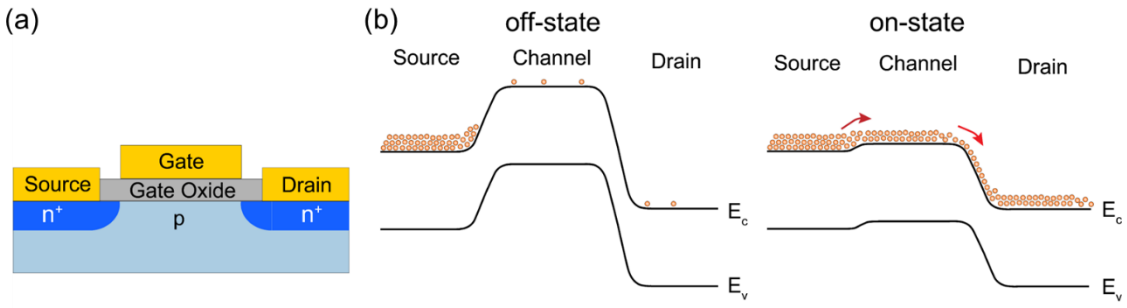


Figure 2-6: (a) Schematic illustration of a planar n-type MOSFET structure. (b) The corresponding energy band diagrams for the off- and the on-state.

2.4.2 MOSFET Characteristics

Transistor performance can be characterized by measuring transfer and output characteristics that quantify the relationship between current and voltage, as shown in Fig. 2-7. Some of these metrics are often normalized by the gate width of the transistor to be able to compare the transistor performance of different sizes. Fin or gate-all-around (GAA) structures are usually normalized by the perimeter of the gate. The transfer characteristics show the variation of drain current, I_D, as a function of gate-source voltage, V_{GS}. The transfer characteristics are divided into subthreshold (off-state) and on-state regions depending on the threshold voltage (V_{TH}). The subthreshold region is especially important when MOSFETs are used as low-power devices. An essential parameter in this region is the subthreshold slope (*SS*) defined as $(dlogI_D/dV_{GS})^{-1}$. The *SS* is a measure to capture the rapidity of this switching behavior, and for MOSFETs, 60 mV/decade is the basic lower limit. The important parameter in the on-state region is the transconductance (G_m) when MOSFETs are used for high-frequency applications. Transconductance is defined as dI_D/dV_{GS} in the on-state (linear scale). The low *SS* and high G_m enable high on-

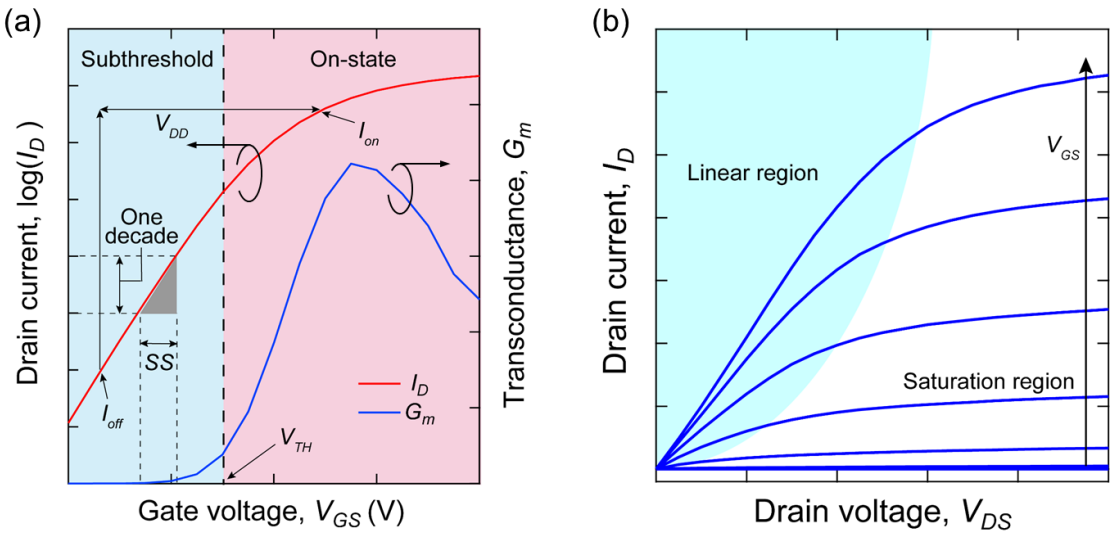


Figure 2-7: The most important *IV* curve characterizing the performance of MOSFETs. (a) Transfer characteristics, drain current as a function of gate voltage. (b) Output characteristics, drain current as a function of drain voltage.

state current I_{ON} at lower supply voltage V_{DD}. The relationship between drain current I_D, supply voltage V_{DD}, switching time t, and switching power p is given next:

$$t = \frac{CV_{DD}}{I_D} \tag{2.1}$$

$$p = \frac{CV_{DD}^2 f}{2} \tag{2.2}$$

where C is load capacitance, and f is the number of switching cycles per second or clock frequency. Thus, the low SS and high G_m contribute to high speed and low power consumption in digital applications of MOSFET.

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Chapter 3

Experimental Techniques

This chapter briefs experimental techniques for the formation and characterization of nanowires. III-V semiconductor nanowires are grown by selective-area growth using metalorganic vapor phase epitaxy (MOVPE). This growth method combines a top-down method, in which periodical openings are formed on a semiconductor substrate deposited in amorphous thin films, and a bottom-up method, in which crystals are selectively grown into the openings. This allows nanostructures of arbitrary size and shape to be formed at arbitrary locations. The principles of selective-area growth and the MOVPE system are described. Then, this chapter describes scanning electroscopy, electron beam lithography, reactive ion etching system, RCA cleaning, atomic layer deposition, and electron beam evaporation used in this study.

3.1 Principles of MOVPE

3.1.1 Overview

MOVPE is one of the techniques for growing homogeneous or heterogeneous crystals on a single-crystal substrate using chemical reactions and is widely utilized for growing thin films and bulk crystals. Other representative vapor phase epitaxy (VPE) growth techniques are hydride vapor phase epitaxy (HVPE) and molecular beam epitaxy (MBE). For MOVPE, crystals are grown at temperatures much lower than the melting point, resulting in high-purity crystals. In addition, MOVPE method can control growth rate, mixed composition, impurity concentration, and structures. Hence, MOVPE method has

already become an essential technology for semiconductor fabrication.

3.1.2 MOVPE System

Figure 3-1 shows a schematic illustration of the MOVPE system used in this study. The MOVPE system consists of a gas delivery system, a horizontal reactor system with a temperature controller, and an exhaust disposal system. The MOVPE system maintains a total flow of 5.75 standard liters per minute (SLM) and works at 0.1 atm. Gas sources supplied from gas cylinders and metalorganic (MO) sources supplied from bubblers are depressurized using pressure control valves (PCVs), and the flow rate is controlled by mass-flow controllers (MFCs). The MOVPE reactor is a horizontal quartz (SiO_2) tube. The sample is placed on a susceptor made of high-purity carbon that is heated by radio frequency induction. The susceptor temperature is measured by passing a thermocouple through the inside. The MOVPE system equipped Trimethylgalium (TMGa), trimethylindium (TMIn), tertiarybutylphosphine (TBP), trisdimethylaminoantimony (TDMASb), diethylzinc (DEZn), tetraethyltin (TESn), arsine (AsH_3), and monosilane (SiH_4) as MO and gas source materials.

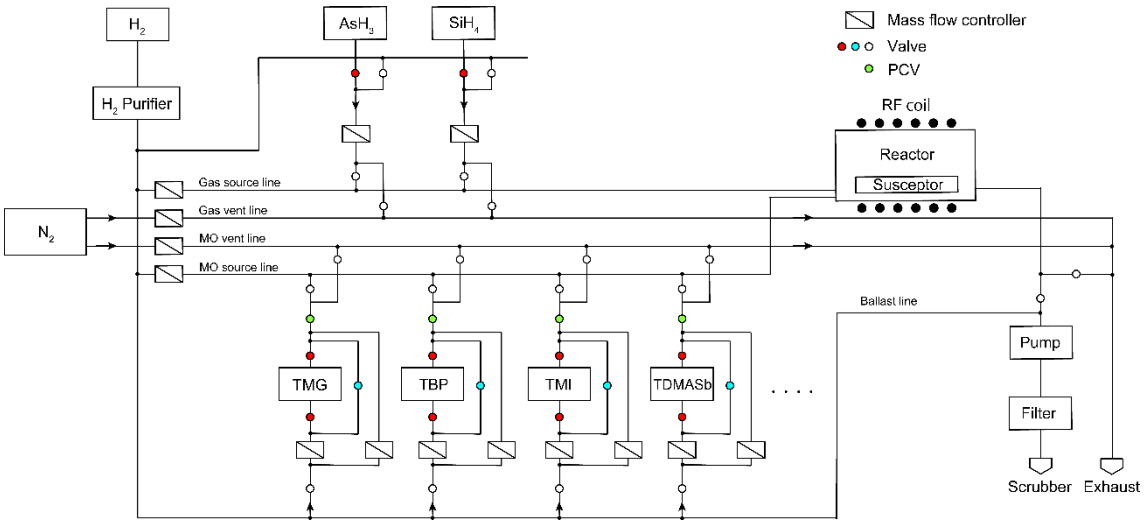

Figure 3-1: Schematic illustration of the MOVPE system used in this study.

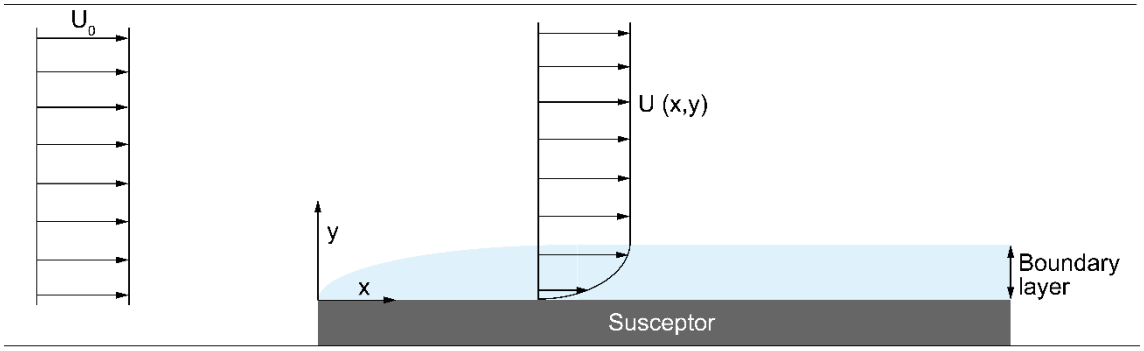

Figure 3-2: Schematic view of boundary layer for parallel flow over a susceptor in the reactor.

Fluid flow parallel to the wa ll slows down as it approaches the wall. This region of decreasing velocity is referred to as the boundary layer. A criterion of inertial relative to viscous effects is the Reynolds number, N_{Re}, $N_{Re} = U_0 L\rho/\mu$, where L is a characteristic linear dimension of the flow problem, U_0 is the free-stream velocity, μ is coefficient of viscosity, and ρ is density of gases. When N_{Re} is large, the entire region of fluid flow may be subdivided into regions of inviscid flow and regions of the viscous boundary layer. The case of parallel flow on a flat plate is clear, as in Fig. 3-2. The thickness of the boundary layer, δ, expands from zero at the starting point of the susceptor and increases with the square root of x, the distance measured from the starting point. The boundary layer thickness, defined as the distance from the interface at which the velocity component parallel to the wall becomes 99% of its free stream value, is

$$\delta = 4.64\left(\frac{\mu L}{\rho U_0}\right)^{1/2}. \tag{3.1}$$

As source materials are consumed during crystal growth, there is a difference in the concentration of source materials between the mainstream and the substrate surface. The source material diffuses through the boundary layer to the substrate due to this concentration difference.

3.1.3 MOVPE Growth Process

Fig. 3-3 shows a schematic illustration of the mechanisms of selective-area growth processes. The fundamental processes occurring during crystal growth are subdivided into (i) mass and heat transport, (ii) physical surface processes, (iii) chemical reactions, and (iv) thermodynamics [1].

(i) Mass and heat transfer due to diffusion and convection of the source material is directed to the substrate surface through the boundary layer. The mass transport process limits the growth rate since neither thermodynamics nor reaction rates depend on the total gas velocity.

(ii) Adatoms diffuse across the crystal surface and bind at suitable locations for incorporation into the crystal. Two- or three-dimensional nucleation occur at the substrate surface.

(iii) The rate of chemical reactions depends on the details of the surface structure (e.g., reconstruction and step structure). Each of these factors will dominate some aspect of the overall growth process.

(iv) Thermodynamics determines the driving force and the maximum growth rate of the epitaxy growth process.

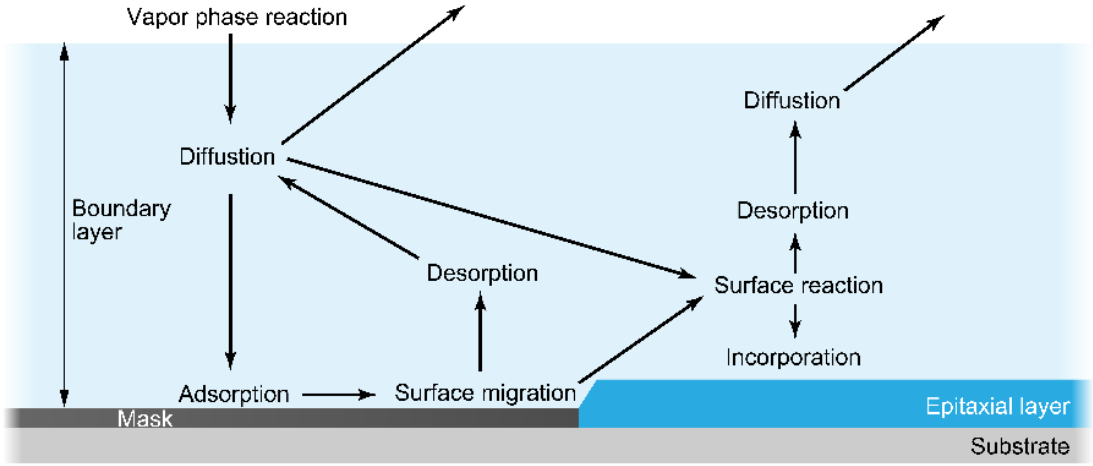

Figure 3-3: Schematic illustration of the mechanisms of selective-area growth in boundary layer.

3.2 Nanowire Fabrication Processes

The principles of selective-area growth for nanowire fabrication are described. This selective-area growth method combines a top-down method, in which periodical openings are formed on a semiconductor substrate deposited in amorphous thin films, and a bottom-up method, in which crystals are selectively grown into the openings, as shown in Fig. 3-4. First, 20-nm-thick SiO_2 films are formed by thermal oxidation. The thickness of SiO_2 film is measured by ellipsometry (ULVAC, ESM-1AT). Second, electron beam (EB) resist (Nippon Zeon: ZEP520A-7) is coated on the substrate by a spin coating technique. After the pre-bake at 170°C for 2 min and then 90°C for 10 min, EB lithography is carried out. EB lithography system (JEOL: JBX-6300SF) using ZrO/W field emitter with 100 kV of accelerating voltage was used. Periodical mask openings were formed using electron beam lithography, dry etching (reactive ion etching), and wet chemical etching (BHF). Next, EB resist is removed by methylethlketone (MEK) and 1165 remover (Rohm and Haas). Just before the nanowire growth, RCA cleaning was used to improve the surface quality of the Si substrate. Finally, the nanowire growth is carried out in the MOVPE system.

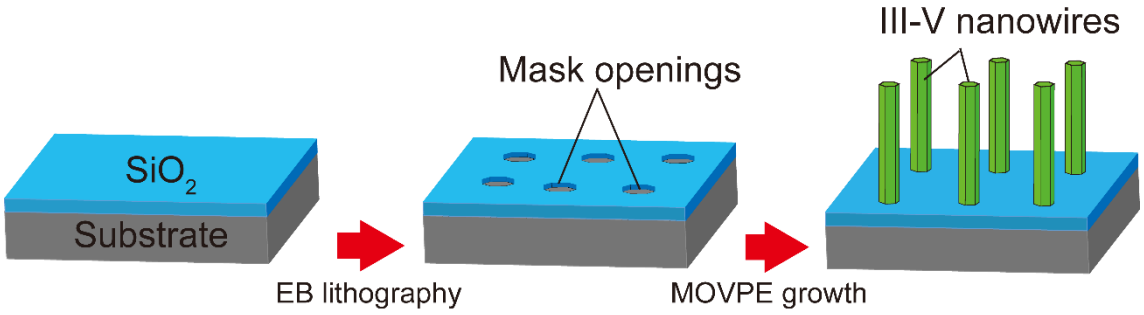

Figure 3-4: Fabrication process for III-V nanowire arrays by selective-area growth.

3.3 Experimental Method

3.3.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is used for the structural characterization of grown nanowires or fabricated devices (Hitachi High-Tech: S-4100). There are two types of electron guns: thermal electron emission type and field emission type. In this study, the SEM system with a field emission electron gun is used. The system consists of an electron gun, condenser lenses, scanning coils, an objective lens, and a detector for secondary electrons. SEM uses electron beams to observe minute surface structures clearly.

3.3.2 Electron Beam Lithography

Electron beam lithography (EBL) is used to form mask openings. The system consists of an electron gun, an electron gun column, a sample chamber, and an exhaust system. There are three types of electron guns: thermal electron emission electron guns, field emission electron guns, and thermal field emission electron guns. In this study, the EBL with thermal field emission electron gun is used (JEOL: JBX-6300SF). The column consists of an electron lens and deflector. The electron lens reduces the electron beam emitted from the electron gun, and blanking and position deflection are performed by the deflector to form the desired pattern in the exposure field on the substrate.

3.3.3 Reactive Ion Etching

Reactive ion etching (RIE) is one of the dry etching technologies. An electromagnetic field generates plasma under low-pressure conditions. In a RIE system, high-frequency power can be applied to the lower electrode on which the substrate is placed. The counter electrode is parallel to the lower electrode and is grounded. The etching gas is introduced into the chamber to generate plasma between the electrodes. Electrons, ions, and radicals are present in the plasma. In this study, RIE system (SAMCO Inc.: RIE-10NR) is used for the top-down method in selective-area growth and as etch back process in the device fabrication.

3.3.4 RCA Cleaning

RCA cleaning is a typical cleaning method for Si wafers [2]. The method is comprised of three steps. First, samples are cleaned by SC-1 solution (1NH_4OH: 1H_2O_2: 5H_2O) at 80°C for 10 min to remove the organic contaminates. The metallic contaminants were introduced in the SC-1 cleaning step. Second, buffered HF removes the thin oxide layer. Finally, samples are cleaned by SC-2 solution (1NH_4OH: 1H_2O_2: 5H_2O) at 80°C for 10 min to remove the metallic contaminants.

3.3.5 Atomic Layer Deposition

Atomic layer deposition (ALD) is a critical technique for depositing thin films for various applications [3]. This study uses ALD (Ultratech: Cambridge Nanotech Savannah S100) to form $Hf_{0.8}Al_{0.2}O$ in a field-effect transistor. General ALD processes are based on binary reaction sequences where two surface reactions occur and deposit a binary compound film. Since the number of surface sites is finite, only a finite number of surface species can be deposited in this reaction; if each of the two surface reactions is self-limiting, the two reactions can proceed sequentially, and thin films can be deposited with atomic-level control.

3.3.6 Electron Beam Evaporation

Electron Beam Evaporation is a physical vapor deposition method of forming thin films of a metal electrode by irradiating an electron beam in a vacuum onto an evaporating target to heat and evaporate. In this study, evaporating materials are used Au, Ni, Ge, Ti, Cr, and Al in the electron beam evaporation system (ULVAC: UEP-6000).

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Chapter 4

Growth of Pulse-Doped InAs Nanowires on Si and Vertical Transistors

III-V compound semiconductors are promising channel materials for the future low-power and high-performance transistor because of their high electron/hole mobility. Here, In this chapter, we report on the integration of vertical InAs nanowire channels on Si by selective-area metalorganic vapor phase epitaxy (MOVPE) with a pulse doping technique and demonstration of an InAs nanowire vertical surrounding-gate transistors. We formed junctions in III-V nanowires and characterized their vertical alignment and uniformity. Next, we investigated the possibility of improving off-leakage characteristics and increasing current in InAs nanowire vertical surround-gate transistors by forming a pseudo-intrinsic layer with compensating doping into the InAs nanowire channel and a contact layer with high impurity concentration. Transmission electron microscopy revealed that the InAs nanowire/oxide interface exhibited good interfacial characteristics. The device had a small subthreshold slope of 68 mV/decade, a normalized transconductance of 0.25 μS/μm, and on/off ratio of around 10^7. The axial junction with the pulse doping effectively suppressed off-state leakage current resulting in good electrostatic gate control. These results were published in 2018 [1].

4.1 Introduction

Silicon-based integrated circuits are facing growing problems with the size-scaling of field-effect transistors (FETs), such as increased off-state leakage current and power density per chip. Fast channel materials are expected to be alternatives for achieving FETs with high Ion and low off-state leakage current under low bias [2–12]. Meanwhile, the vertical surrounding-gate architecture realizes high packing density and good electrostatic gate control [13,14]. Vertical III-V compound semiconductor nanowires directly grown on Si platforms are promising channel materials because they have higher electron/hole mobilities than Si and can be used to implement the vertical surrounding-gate architecture. In addition, nanowires can relax stress originating from the lattice mismatch because of their small footprint[15].

We recently demonstrated the direct integration of vertical InAs nanowires on Si by selective-area metalorganic vapor phase epitaxy (SA-MOVPE) [16–18] and vertical gate-all-around (VGAA) FET [10]. Improvements to the electrostatic characteristics of the InAs nanowire channels, especially the subthreshold slope (*SS*) and off-state leakage current, are still inherent challenges because InAs has a narrow band gap and high electron mobility that would result in a very high off-leakage current. The dominant contribution to the off-state leakage is from source-drain band-to-band tunneling. In this study, we investigated the effect on the leakage current of adding Zn and Sn pulsed-doped layers to InAs nanowire VGAA FETs on Si. We observed a considerable improvement in the *SS* compared with undoped-InAs nanowire channel VGAA-FETs [10].

4.2 Experimental Procedure

InAs nanowires were grown on n-type Si(111) (resistivity of 1000 Ω·cm). First, 20-nm-thick SiO_2 film was formed on the substrates by thermal oxidation. Periodical mask openings were formed using electron beam lithography and dry and wet etchings. RCA cleaning was used to improve the surface quality of the SiO_2 film. Next, InAs nanowires

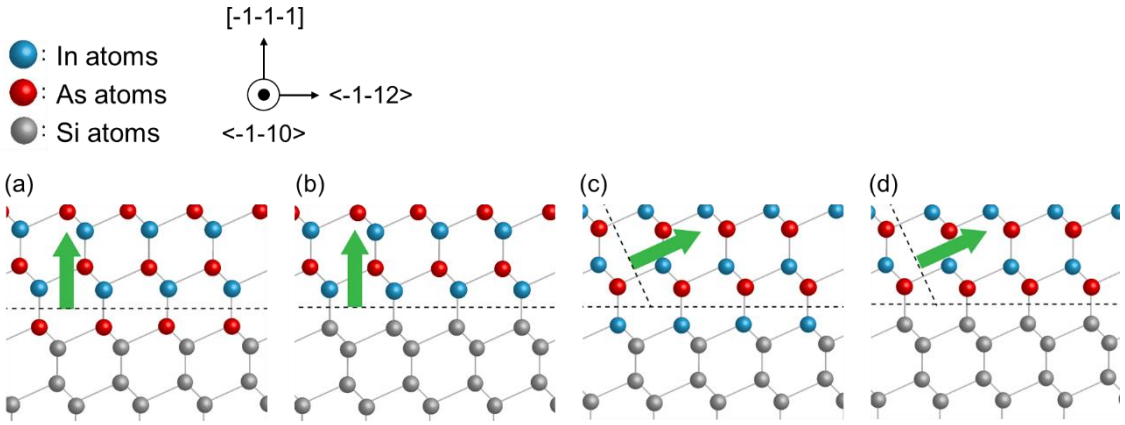


Figure 4-1: Shematic illustration of crystal structure of InAs/Si interface: (a) As-incorporated Si structure. (b) In-terminated Si surface. (c) In-incorporated Si structure. (d) As-terminated Si surface. Green arrows indicate direction of InAs nanowire growth.

were selectively grown on the partially masked substrate in a horizontal MOVPE system at a working pressure of 0.1 atm. Trimethylindium (TMIn) and arsine (AsH_3) were supplied as the source precursors. Diethlyzinc (DEZn) was used as the p-type dopant source, while monosilane (SiH_4) and tetraethyltin (TESn) were used as the n-type dopant sources. The partial pressures of TMIn and AsH_3 were respectively 9.7×10^{-7} and 2.5×10^{-4}. The growth temperature was 550 °C, and the V/III ratio was 256.

It is difficult to control the growth direction in III-V nanowire growth on Si(111) substrates. This is because III-V nanowires grow in vertical <111> and three equivalent tilted <111> directions on Si (111). Figs.4-1(a)-(d) show the crystal structures of the InAs/Si interface: the structure in which the outermost Si atoms are replaced by As atoms [Fig.4-1(a)] or terminated by In atoms [Fig. 4-1(b)] exhibit (111)B-oriented surface and thus grow vertically. On the other hand, the surface in which outermost Si atoms are replaced by In atoms [Fig. 4-1(c)] or terminated by As atoms [Fig. 4-1(d)] exhibit (111)A-oriented surface and thus grow diagonally. Therefore, in this study, AsH_3 surface treatment and pulse growth were used to control the growth direction of InAs nanowires. A thermal cleaning was performed at 910°C to remove the natural oxide film and form 1 ×1 reconstructed structure. Next, AsH_3 was supplied at 410°C to form the As-incorporated Si surface. Initial nucleations were grown using pulse growth with alternating TMIn and AsH_3 to maintain the (111)B-oriented surface [19].

We fabricated InAs nanowire VGAA-FET with high-*k*/metal surrounding gate

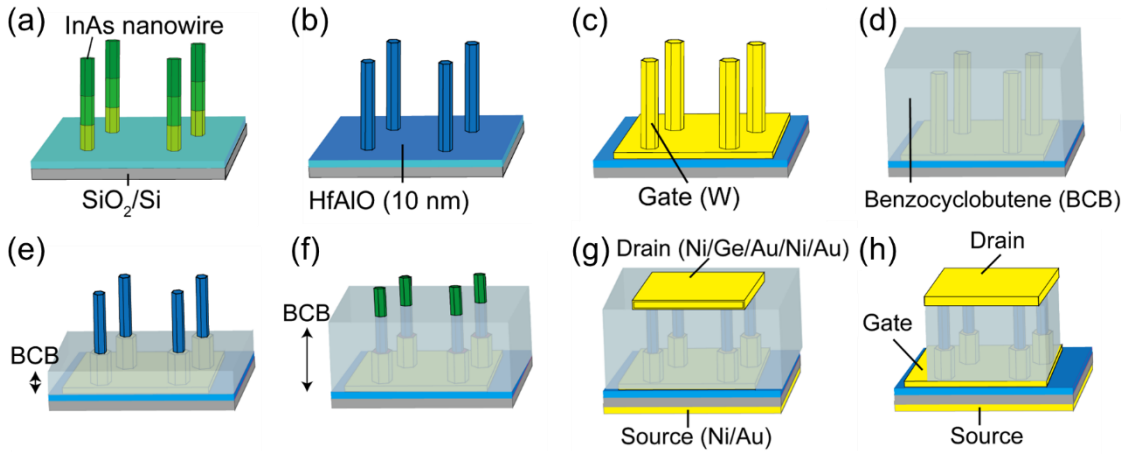


Figure 4-2: Device fabrication processes: (a) Growth of nanowires. (b) Atomic layer deposition. (c) Gate metal sputtering. (d) Coverage with benzocyclotene. (e) Etching benzocyclotene. (f) Formation of isolation layer between gate and drain. (g) Evaporation of drain and source metal. (h) Gate contacting-pads exposure and anneling.

[6,10,20]. After the growth, atomic layer deposition (ALD) was used to form a 10-nm-thick $Hf_{0.8}Al_{0.2}O$ layer on the whole surface of the nanowires. Second, gate metal (tungsten, W) was formed by radio frequency sputtering, and contact pads were made by photolithography and wet etching. The nanowires were then covered with benzocyclobutene (BCB) formed by spin-coating and etched back to the desired thickness by reactive ion etching (RIE). Next, an isolation layer between the gate and drain was formed by BCB. Drain and source metals were evaporated on the top of the nanowires and the back side of the substrate. The drain and source metals were Ni/Ge/Au/Ni/Au and Ni/Au, respectively. Finally, the InAs nanowire VGAA-FET was annealed at 350 °C in N_2 for Ohmic contacts in the source and drain regions.

4.3 Growth of Pulse-Doped InAs Nanowires on Si

SEM image of the nanowire array is shown in Figs. 4-2. The nanowires were aligned vertically relative to the <111> direction by using AsH_3 surface treatment and pulse growth as in previous reports [14]. This indicated Si(111) changed to having a (111)B polar nature. The diameter and height of the pulse-doped nanowires were 90 nm and 900

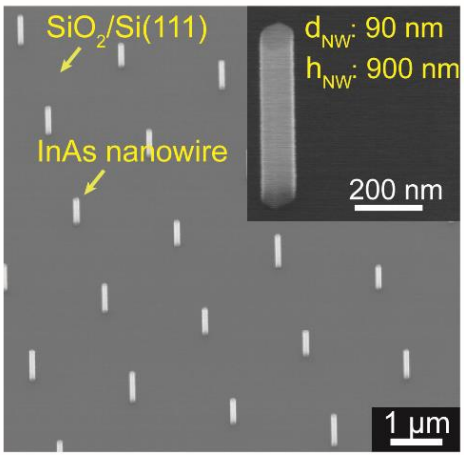
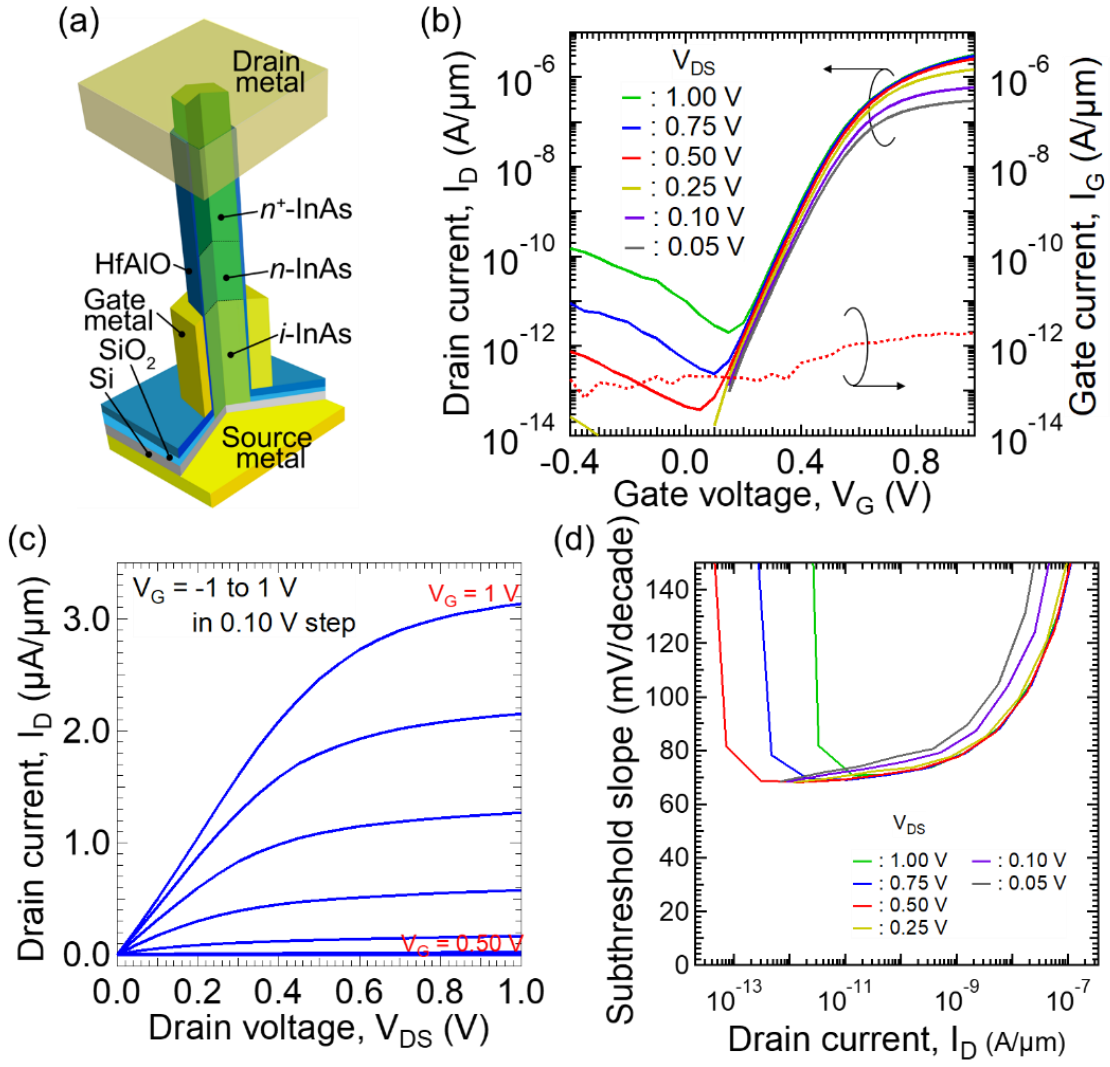


Figure 4-3: 30°-tilted SEM image of InAs nanowires array. Inset shows a representative nanowire.

nm, respectively. The InAs nanowires had hexagonal pillar shapes with {-110} vertical facets. InAs nanowires are unintentionally doped by carbon, with typical carrier concentrations of $10^{16}-10^{17}$ cm^{-3} [20,21]. The Zn-pulsed doping was used to compensate for the unintentional carbon dopants in the InAs nanowires, while the Sn-pulsed doping was used to form heavily doped n-type InAs nanowires and, at the same time, maintain the uniform shapes of the nanowire channels [22]. The InAs nanowire channel made with Zn-pulsed doping should shift the threshold voltage, while the n^+ contact layer made with Sn-pulsed doping would result in low contact resistance. It should be noted that lowering the effective carrier concentration by the compensation effect increases the channel series resistance. Regarding pulse doping, DEZn was supplied for 2 sec during the 10 sec undoped InAs growth period, and TESn was supplied for 1 sec during the 6 sec undoped InAs growth. The resulting nanowires grew vertically on Si without any lateral growth, similar to the undoped-InAs nanowires. The heights of the Zn-pulse-doped layer, Si-doped layer, and Sn-pulse-doped layer were 340 nm, 220 nm, and 340 nm, respectively. The segment heights were estimated from the growth rate of the nanowire.

4.4 Gate-All-Around Field-Effect Transistors Using Pulse-Doped InAs Nanowires

Fig. 4-3(a) shows the device structure of the pulse-doped InAs nanowire VGAA FET. Figs. 4-3(b) and 4-3(c) show the transfer and output characteristics of the device. The measured current was normalized by the perimeter and number of nanowires. The gate length (L_G) and the channel diameter were 200 and 90 nm, respectively. The device



Figures 4-4: (a) Schematic illustration of VGAA-FET. (b) Transfer characteristics. (c) Output characteristics. (d) Subthreshold solpe characteristics.

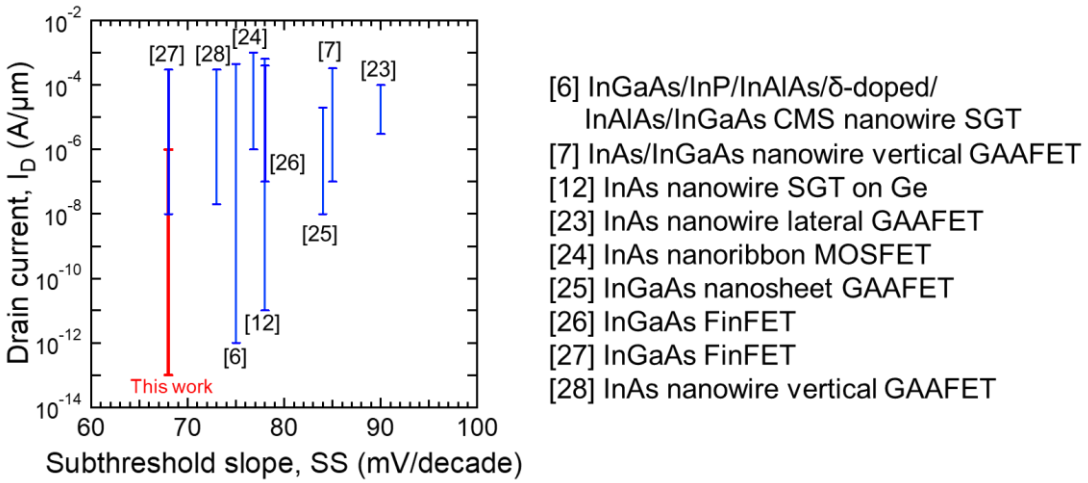


Figure 4-5: Comparison of projected drain current range versus minimum *SS* for III-V channels with multi-gate structure.

exhibited n-type enhancement-mode transistor characteristics with a threshold voltage V_{th} of 0.50 V. The threshold voltage was determined by linear extrapolation. The undoped InAs nanowire vertical surrounding-gate transistor (SGT) showed an off-leakage current of 1 nA/μm at V_{DS} = 1.00 V [10]. On the other hand, the nanowire with axial junction showed an off-state leakage current of ~10 pA/μm at V_{DS} = 1.00 V. The off-state leakage current between the source and gate was considerably decreased because the Zn-pulsed doping formed a junction in the nanowire channel. We believe that the reduction in off-state leakage current originated from the isolation of E_F between the source and gate. This phenomenon suppresses the band-to-band tunneling causing off-state leakage. The InAs nanowire VGAA-FET had a minimum *SS* (= $dV_G/d(\log I_{DS})$) of 68 mV/decade at V_{DS} = 0.50 V, as shown in Fig. 4-3(d). The drain-induced barrier lowering (DIBL) was estimated to be 27 mV/V, which was low, likely due to the suppression of short-channel effects by the GAA structure. The gate leakage current (I_G) was on the order of 10 pA/μm with a variation of V_G under V_{DS} = 0.50 V [Fig. 4-3(b)]. Compared with undoped InAs nanowire VGAA-FETs [10], the *SS* of the doped nanowire channel considerably improved. Fig. 4-4 compares projected drain current versus minimum *SS* for reports regarding III-V channels with multi-gate structure [6,7,12,23–28]. Compared with the other reports, this work has a tiny channel, the InAs nanowires reported here exhibit the smallest *SS*.

4.5 Characterization of InAs Nanowire/Oxide Interface

Although the InAs nanowire with the axial junction had the smallest *SS*, the *SS* was still higher than its physical limit (60 mV/decade at RT), which indicates the nanowires had a large diameter and high interface state density D_{it} between the InAs nanowires and high-*k* dielectric. Assuming that the cylindrical nanowires covered with Schottky gates and nanowires of diameter d_{NW} are fully depleted, the donor density N_d can be expressed as [29]:

$$N_d \approx \frac{4\varepsilon_0\varepsilon_{InAs}(V_{bi}-V_{th})}{q(d_{NW}/2)^2}, \tag{4.1}$$

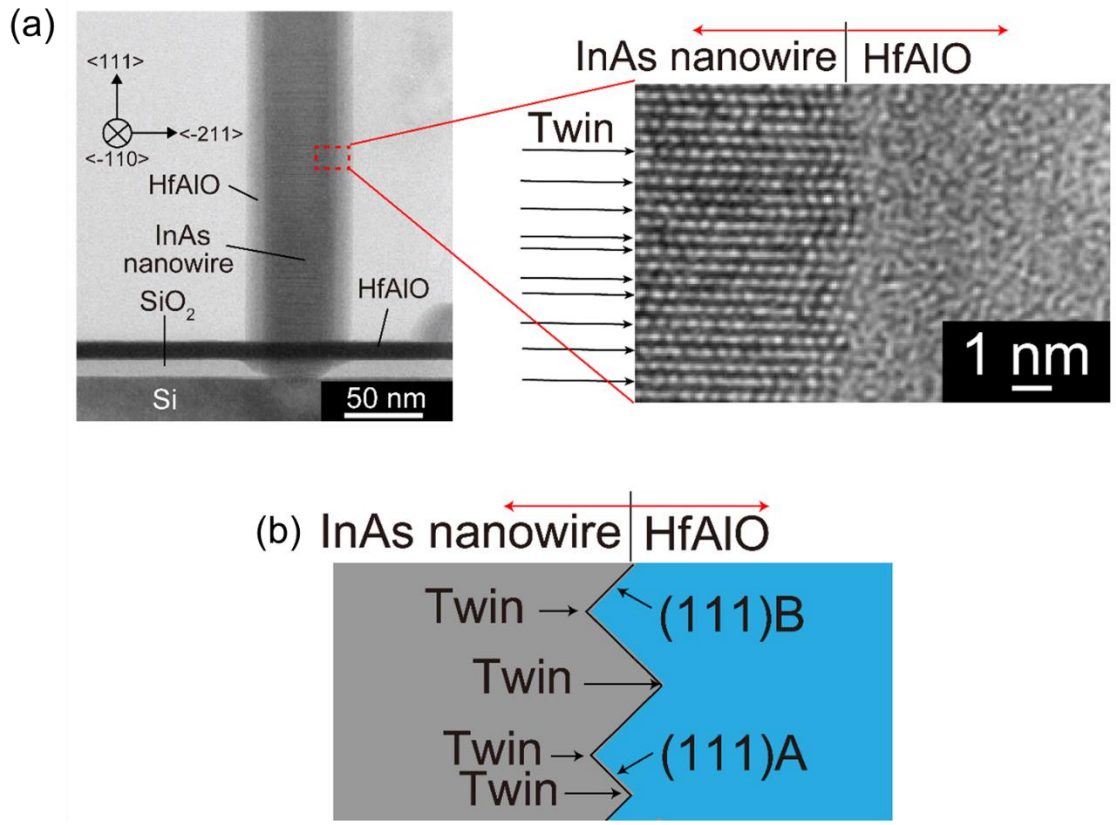
where V_{bi} is the built-in potential, V_{th} is the threshold voltage, and ε_{InAs} is the dielectric constant of InAs, ε_{InAs} = 12.3. V_{bi} is the applied voltage at the flat-band condition and can be considered the gate voltage when the gate current is lowest. The band would be the flat-band condition when the gate current is the slightest since Fowler-Nordheim Tunneling occurs at a triangular barrier layer. V_{bi} and V_{th} were estimated to be 0.65 V and 0.50 V, respectively. N_d was calculated to be 2.0 × 10^{17} cm^{-3}. The maximum depletion layer width $W_{d,max}$ was then deduced from N_d, $W_{d,max}$ = 36 nm. The depletion layer capacitance C_d of the nanowire was given by [13]:

$$C_d = \frac{\varepsilon_{NW}}{R\cdot\ln(R/(R-W_d))} \tag{4.2}$$

ε_{NW} is the dielectric constant of the nanowire and *R* is the radius of the nanowire. From (4.2) equation, we obtained C_d = 1.7×10^{-3} F/m^2. *SS* can be expressed as [30]:

$$SS = \frac{kT}{q}\cdot\ln 10\left(1+\frac{C_d+C_{it}}{C_{ox}}\right), \tag{4.3}$$

Where C_{it} is a capacitance of an interface level, C_{ox} is a capacitance of an oxide. The interface level density D_{it} (= qC_{it}) was calculated to be 2.2×10^{12} $cm^{-2}eV^{-1}$, which is a very low value for the III-V/oxide interface. Therefore, we investigated the crystallinity of InAs nanowire/gate oxide interface by transmission electron microscope (TEM). Fig. 4-5(a) shows TEM images of the HfAlO-covered InAs nanowires on Si. The HfAlO/InAs {-110} facet has an atomically flat surface, as shown in Fig. 4-5(a). On the other hand, the nanowire contains a number of twins with a period of 1 - 4 monolayers. Although the



Figures 4-6: (a) TEM image of HfAlO-covered InAs nanowires on Si (left). High-resolution TEM image of the InAs/HfAlO interface (red dashed line in Fig. 4-4(a)). Twins were introduced with a 1-4 monolayer period. (b) A Schematic illustration of InAs/HfAlO interface.

{-110} facet has a zigzag structure across the twin, this surface roughness converges with the period; that is, an atomically smooth surface is obtained. This smooth surface helps to lower the *SS*, and the cause is assumed to be the zigzag structure. The zigzag surface in Fig. 4-5(b) is composed of (111)A and (111)B microfacets. A recent report regarding InGaAs/Al_2O_3 interfaces [31] has revealed that (111)A/oxides interfaces are superior to (111)B and (100) surfaces. In our InAs nanowire channel, half of the whole {-110} facet [(111)A/B mixed facet] contained (111)A microfacets. Accordingly, this specific crystal phase in the InAs nanowire, which originated from many twins [shown in Fig. 4-5(b)], inherently formed an excellent interface. Surface roughness is the main reason for scattering. A possible approach to minimizing D_{it} is to make a core/shell structure during *in situ* MOVPE growth for passivation. Although the pulse-doped InAs nanowire VGAA-FET had a good I_{on}/I_{off} ratio of around 10^5 at V_{DS} = 1.00 V compared with undoped-InAs

nanowire VGAA-FETs [3], I_{on} was small despite an n^+ contact layer forming. This indicates that the series resistance was high because of the channel resistance. Moreover, the twins in the nanowire act as scattering centers which degrade carrier mobility. A possible approach to enhancing I_{on} is modulation-doping using a core-multishell structure.

4.6 Summary

The InAs nanowires were grown by selective-area growth. The InAs nanowires constructed Zn- and Sn-pulse-doped layers. The pulse-doped nanowires grew vertically on Si without any growth in the lateral direction, and a hexagonal pillar shape was maintained, similar to undoped-InAs nanowires. We demonstrated an InAs nanowire VGAA-FET with a pulse-doping technique. The device showed *SS* of 68 mV/decade and an off-leakage current of ~100 fA at V_{DS} = 0.50 V. The introduction of the pulse-doped layers significantly improved the *SS* and leakage current comparison with undoped-InAs nanowires. In addition, the device operated as a normally-off transistor because of the formation of a pseudo-intrinsic InAs channel by the Zn-pulse-doped layer.

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Chapter 5

Characterization of InAs/InP Core-Shell Nanowire Vertical Transistors

Among the III-V semiconductor materials, indium arsenide (InAs) nanowires with high carrier mobility are expected to be alternative channels for high-performance and low-power field-effect transistors (FETs). However, there is a challenge in enhancing the on-state current for the InAs nanowire channel vertical gate-all-around (VGAA) structure on Si. In this chapter, we explore vertical InAs/InP core-shell (CS) nanowire channels to enhance the current and demonstrate InAs/InP CS nanowire VGAA-FETs. The InAs/InP CS nanowire channel enhanced the on-state current while maintaining a small off-leakage current. The devices showed an on-state current of 10 μA/μm, off-state leakage current of 20 fA/μm, and a subthreshold slope of 93 mV/dec at V_{DS} = 0.50 V. The origin of the current enhancement suggested that there is a formation of two-dimensional electron gas (2DEG) in the InAs/InP CS nanowire channel, and the characteristics of the InAs/InP CS nanowire VGAA FET revealed that the InP interlayer at drain edge and low source resistivity are important parameters to take advantage of 2DEG for CS nanowire VGAA-FET. These results were published in 2020 [1].

5.1 Introduction

The III-V compound semiconductor nanowires are promising alternative channel materials for high-performance and low-power field-effect transistors (FETs) due to their high electron mobility and gate-all-around (GAA) structures [2–12]. Among the III-V channels, InAs channels have much higher electron mobility. However, InAs channel

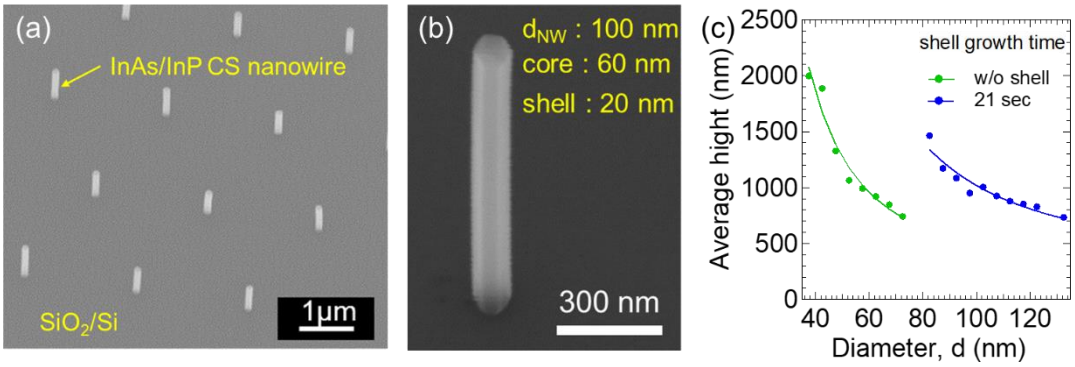
material has a problem regarding large off-state leakage current due to the narrow band gap with a small electron-effective mass. Moreover, InAs contains a large concentration of donor-type surface states resulting in reduced electron mobilities [13–15]. The core-shell (CS) structure, in which the core nanowire is surrounded by radial heterostructure, would provide the confinement carriers inside the core nanowire and would enhance the carrier mobility due to suppression of the carrier scattering process [16–20]. Another benefit of the CS structure is surface passivation [21]. Recently, we demonstrated an InAs nanowire channel for VGAA-FET on Si [22,23] and achieved a small subthreshold slope (*SS*) and off-leakage current. However, the challenge of obtaining a high on-state current for the InAs nanowires directly integrated into Si remains. In this paper, we investigated InAs/InP core-shell nanowire channels to confine carriers in the core nanowire.

5.2 Experimental Procedure

InAs/InP CS nanowires were integrated on Si(111) substrates by selective-area metalorganic vapor phase epitaxy (MOVPE). The details for integrating vertical InAs nanowires on Si were the same as in Chapter 4. Trimethylindium (TMIn), arsine (AsH3), and tertiarybutylphosphine (TBP) were used as source materials. Diethylzinc (DEZn), tetraethlytin (TESn), and monosilane (SiH4) were used as dopant sources. The InAs nanowires were composed of Zn pulse-doped layer, Si-doped layer, and Sn pulse-doped layer from the bottom of the nanowire. The carrier concentration of the Zn pulse-doped layer and Sn pulse-doped layer are of the order of 1×10^{16} cm^{-3} and 1×10^{19} cm^{-3}, respectively. The InP shell was grown on the sidewalls of the nanowires at 580°C. A Si δ-doped layer was inserted during InP shell growth. The device process flow for the VGAA-FET was similar to that of Chapter 4. The drain metal was non-alloy Ti/Pd/Au, and the source metal was Ni/Au. Finally, the VGAA-FETs were annealed at 350°C in N_2 atmosphere to achieve Ohmic contact.

5.3 Growth of InAs/InP Core-Shell Nanowires on Si

A SEM image of the InAs/InP CS nanowire is shown in Fig. 5-1(a). The nanowires had



Figures 5-1: (a) 30°-tilted view SEM image of InAs/InP CS nanowire array on a Si(111) substrate. (b) SEM image of representative InAs/InP CS nanowire. (c) Dependence of InAs nanowire and InAs/InP CS nanowire height on diameter.

hexagonal pillar shapes with {-110} vertical facets, indicating that InP shells were grown flat. As shown in Fig 5-1(b), the diameter and height of the CS nanowire were 120 nm and 800 nm, respectively. The CS nanowires are slightly bent due to the strain caused by lattice mismatch between InAs and InP (~3.1%). Fig. 5-1(c) shows average height, *h*, as a function of diameters, *d*, from SEM images of InAs nanowires and InAs/InP CS nanowires. InP shell thickness was estimated by comparing it to InAs nanowires, assuming a constant shell growth rate. Thus, the shell growth rate was deduced to be 1nm/sec.

We investigated the crystallinity of InAs/InP CS nanowires on Si by X-ray diffraction. The 2θ-ω scans of InAs/InP CS nanowires with different shell thicknesses, including 10 nm, 20 nm, and without the shell in Fig. 5-2 showed two peaks at 25.45 degrees and 26.27 degrees and a strong peak from Si observed at 28.4 degrees, indicating that the InAs/InP CS nanowires were directly integrated on Si. In the case of the 20 nm-thick InP shell layer, a distinct peak was observed between InAs and InP. This result indicated the formation of a distorted InP and/or InAsP layer. We interpret this as strained layers because the peaks between the InAs and InP peaks were double peaks. Fig. 5-3(a) showed the peak deconvolution of the XRD profile for InAs/InP CS nanowire with 20 nm- and 10 nm-thick InP shell layers. In the case of the 20 nm-thick InP shell layer, the peaks at 25.45 degrees and 26.27 degrees originated from unstrained InAs and InP. In the case of the 10 nm-thick InP shell layer, the peaks at 25.44 degrees and 26.20 degrees

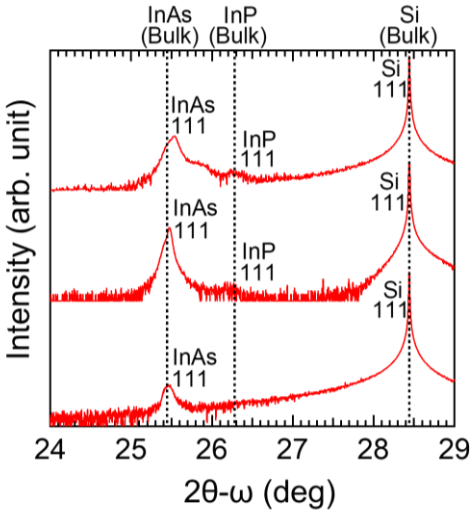
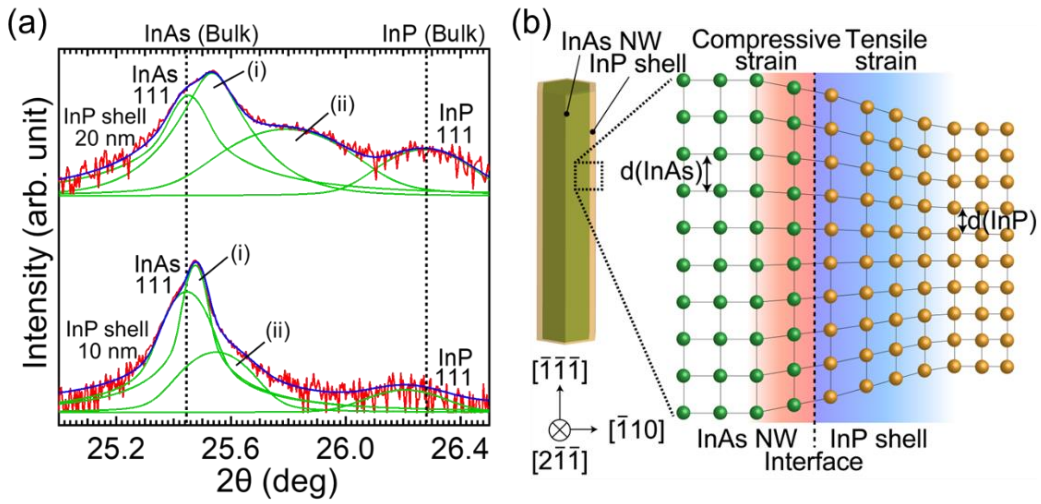


Figure 5-2: XRD profile of InAs nanowires and InAs/InP CS nanowires with 10 nm- and 20 nm-thick InP shell on Si(111) substrate. The diffraction intensity was 111 planes parallel to the substrate surface.



Figures 5-3: (a) The observed XRD profile (red line) and fitted profile (blue line) for InAs/InP CS nanowire with 10 nm- and 20 nm-thick InP shell. The deconvolution lines (green line) using the Voigt function. (b) Illustration of the lattice constant changes induced by the strain effects in the InAs/InP CS heterointerfaece.

originated from unstrained InAs and tensile strained InP (+0.302%). The peaks ascribe to the compressive strained InAs and tensile strained InP in the <111> direction. For the 20 nm-thick InP layer, the compressive strain in InAs and the tensile strain in InP were -

Table 5-1: Lattice constant and in-plane strain for InAs nanowire and InAs/InP CS nanowire.

	lattice constant (Å)				in-plane strain (%)	
	InAs NW	InP shell	(i)	(ii)	(i)	(ii)
without shell	6.0546	-	-	-	-	-
InP : 10 nm	6.0602	5.8864	6.0511	6.0342	-0.151	2.51
InP : 20 nm	6.0566	5.8703	6.0374	5.9780	-0.317	1.84

0.317% and +1.84%, respectively. For 10 nm-thick InP layer, the compressive strain in InAs and the tensile strain in InP were -0.151% and +2.51%, respectively. The calculation results are summarized in Table 1. The peak intensities of strained InAs and InP were stronger than that of unstrained InAs and InP because the inhomogeneous strain was introduced CS nanowire [24]. Misfit dislocation may be introduced at the heterointerface to reduce strain energy in heteroepitaxial growth when a critical thickness is exceeded. Misfit dislocation catches carriers, resulting in the degradation of carrier mobility. Therefore, it is important to design CS nanowires with a shell thickness that prevents misfit dislocation formation. We estimated the critical thickness in an InAs/InP heterojunction. The equation of People and Bean, which is calculated from the energy equilibrium theory, is given by [25].

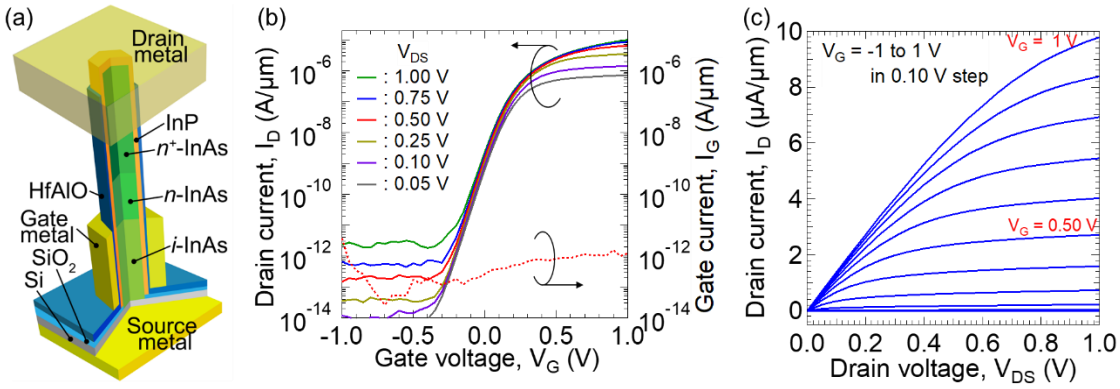
$$h_c = \frac{1-\nu}{1+\nu}\frac{1}{16\pi\sqrt{2}}\frac{b^2}{a}\frac{1}{f^2}ln\frac{h_c}{b}, \tag{5.1}$$

Where ν is a Poisson ratio, b is Burgers vector, a is the lattice constant, f is the lattice mismatch. From this equation, h_c is estimated to be 12 nm. According to this calculation, a 20 nm InP shell film thickness would introduce a misfit dislocation at the interface, but in InAs/InP core-shell nanowires, the actual critical film thickness would be thicker than 12 nm because the core InAs is also distorted. Therefore, direct observation of the presence or absence of misfit dislocations is necessary to determine the critical thickness accurately.

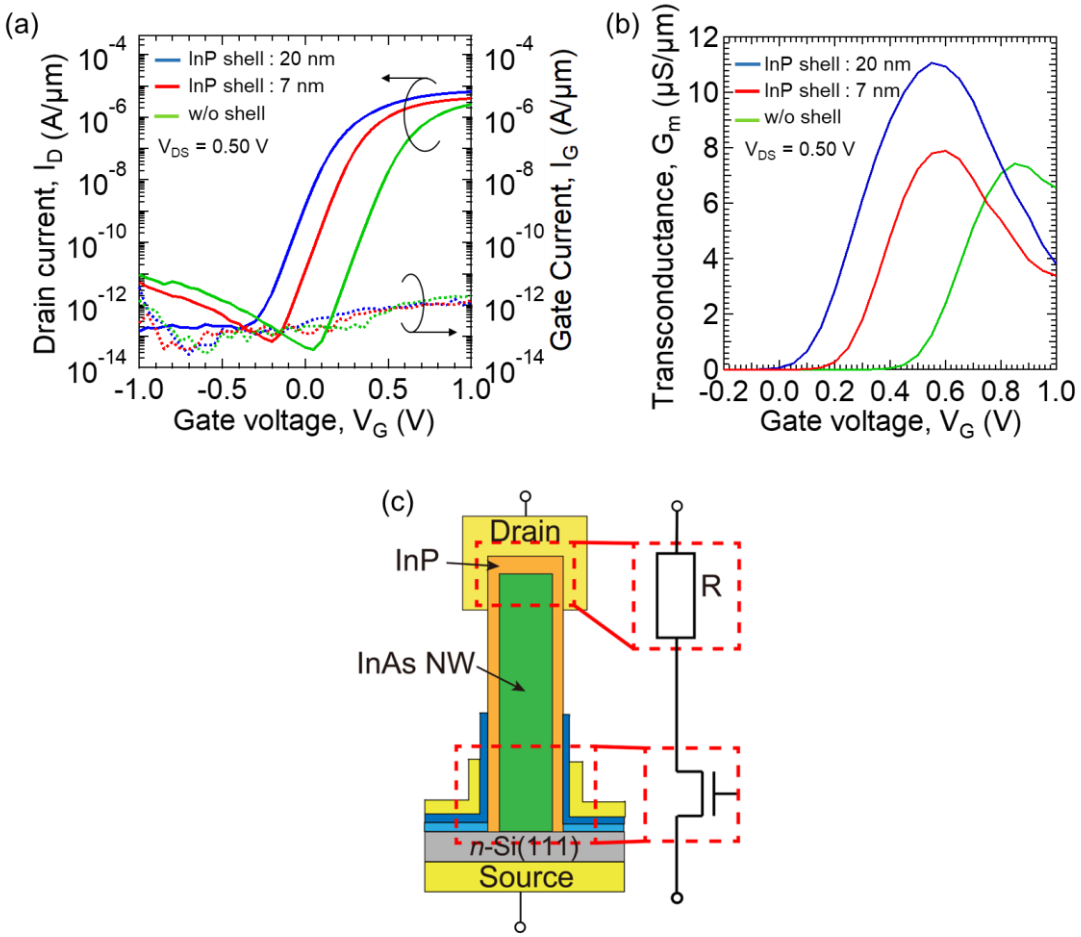
5.4 Gate-All-Around Field-Effect Transistors Using InAs/InP Core-Shell Nanowires on Si

The VGAA-FET structure is illustrated in Fig. 5-4(a). The transfer and output characteristics for the device with a gate length of 200 nm and a channel diameter of 120 nm, including a 20 nm-thick InP shell, are shown in Figs. 5-4(b) and 5-4(c). The drain current was modulated by the gate bias. The device exhibited n-type enhancement-mode behavior. The device with a source resistivities of 1000 Ωcm showed an on-state current (I_{on}) of 6 μA/μm, an off leakage current (I_{off}) of 200 fA/μm, a minimum *SS* of 70 mV/decade, a drain-induced barrier lowering (DIBL) of 29 mV/V. Figs. 5-4(a) and 5-4(b) compare the transfer and transconductance characteristics of InAs/InP CS nanowire and InAs nanowire channels with source resistivities of 1000 Ωcm at V_{DS} of 0.5 V. The I_{on} for the InAs/InP CS nanowire was about three times higher than that of the InAs nanowire channel VGAA-FET. The G_m for the InAs/InP CS nanowire was about 1.5 times higher than that of the InAs nanowire channel VGAA-FET. The *SS* was almost unchanged from 68 mV/decade to 70 mV/decade. The increment of the I_{on} originated from the increased carrier density inside the InAs nanowire channels caused by the InP shell layer. The small increment of the I_{on} was assumed to originate from the InP interlayer increased contact resistance of the drain region due to the conduction band offset of 0.52 eV across the InAs/InP interface, shown in Fig. 5-4(c). Next, Figs. 5-6(a) and 5-6(b) show transfer and transconductance characteristics for the InAs/InP CS nanowire and InAs nanowire channels with source resistivities of 1-3.5 Ωcm. The I_{on} for the InAs/InP CS nanowire VGAA-FET with the 20 nm-thick InP shell was about ten times higher than that of the InAs nanowire channel VGAA-FET. The G_m for the InAs/InP CS nanowire VGAA-FET was about five times higher than that of the InAs nanowire channel VGAA-FET. In addition, the reduction in source resistivity with higher I_{on} means that low source resistivity is an important factor to take advantage of the 2DEG in this CS nanowire VGAA-FET.

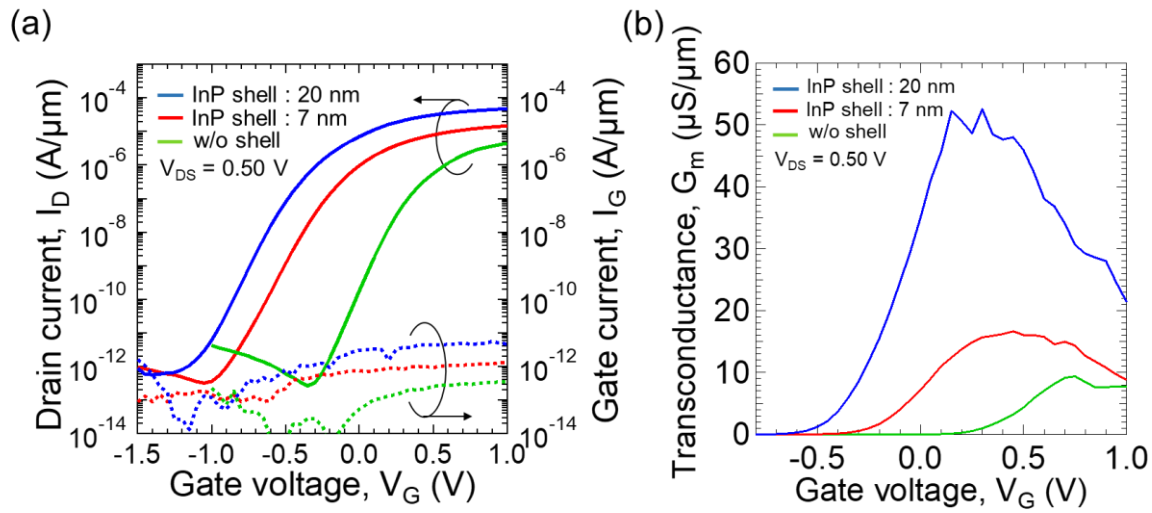
We calculated the band diagram and wavefunction for the InAs/InP heterostructure by solving the one-dimensional Poisson- Schrödinger equation to reveal the increment of I_{on} when using the InAs/InP CS nanowire structure. The strain effects



Figures 5-4: (a) Schematic cross-sectional structure of InAs/InP CS nanowire VGAA FET. (b) Transfer characteristics of InAs/InP CS nanowire VGAA-FET on Si of resistivity of 1-3.5 Ωcm. The measured current is normalized with the gate outer parameter and number of nanowires. (c) Output characteristics of the VGAA-FET. The gate voltage is changed from -1 V to 1 V in steps of 0.10 V.



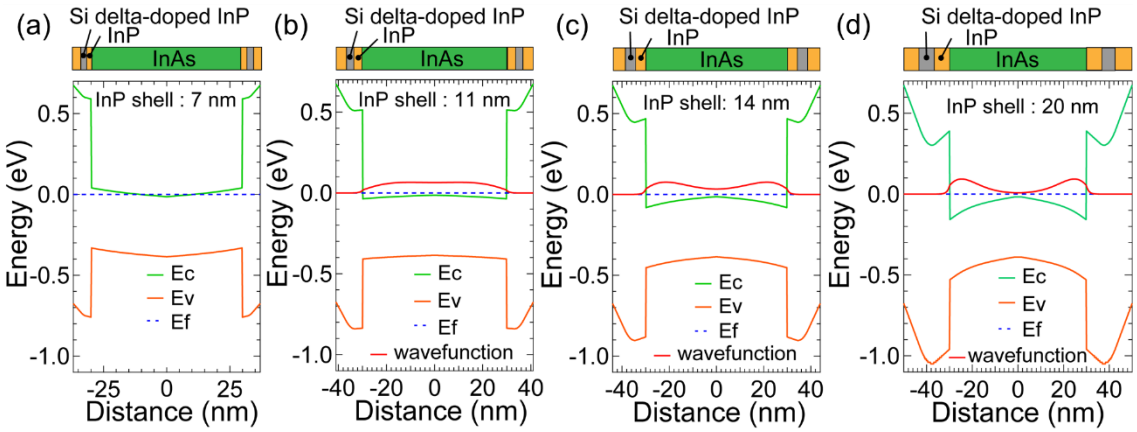
Figures 5-5: Comparison of electric characteristics at V_{DS} = 0.50 V between InAs/InP CS nanowire VGAA-FET with 7 nm-thick InP shell (red line) and 20 nm-thick InP shell (blue line) and InAs nanowire VGAA-FET without shell (green line): (a) transfer characteristics and (b) transconductance characteristics. (c) Schematic of the resistive components of the InP interlayer of InAs/InP core-shell nanowire VGAA-FETs.



Figures 5-6: Comparison of electric characteristics at V_{DS} = 0.50 V between InAs/InP CS nanowire VGAA-FET with 7 nm-thick InP shell (red line) and 20 nm-thick InP shell (blue line) and InAs nanowire VGAA-FET without shell (green line): (a) transfer characteristics and (b) transconductance characteristics.

were not included in these calculations. Figs. 5-7(a)-(d) exhibits the band diagram profile across the InAs/InP heterojunction and the wavefunction in the vicinity of the InAs/InP interface without bias. The InP layer had Si δ-doped layer and spacer layer. Different InP shell thicknesses were calculated. In the case of the 7 nm-thick InP shell layer, the carrier was not confined in the vicinity of the InAs/InP interface. Then, the carrier began to be confined in the InAs nanowire channel when the thickness was 11 nm. Eventually, the carrier was confined in the InAs nanowire channel when the thickness was 14 nm and 20 nm at V_G = 0. This means the carrier was accumulated in the vicinity of the InAs/InP heterointerface as the InP shell thickness was increased, and the threshold voltage was negatively shifted with increasing InP shell thickness, as shown in Fig. 5-8. In the case of 20 nm-thick InP, the threshold voltage is estimated to be -0.44 V from a sheet carrier of 9.9×10^{11} cm^{-2}. The calculation fits well with the experimental data of -0.41 V. Thus, the InP thickness is an important parameter of forming 2DEG and controlling the threshold voltage.

Note that the InP shell layer possibly degrades the device performance. It can be shown that the *SS* can be expressed by



Figures 5-7: Band diagram and the wavefunction (red curve) of InAs/InP heterojunction simulated using the one-dimensional Poisson-Schrödinger equation at zero bias. The blue dashed line denotes the Fermi level. (a) 7 nm-thick InP layer. (b) 11 nm-thick InP layer. (c) 14 nm-thick InP layer. (d) 20 nm-thick InP layer.

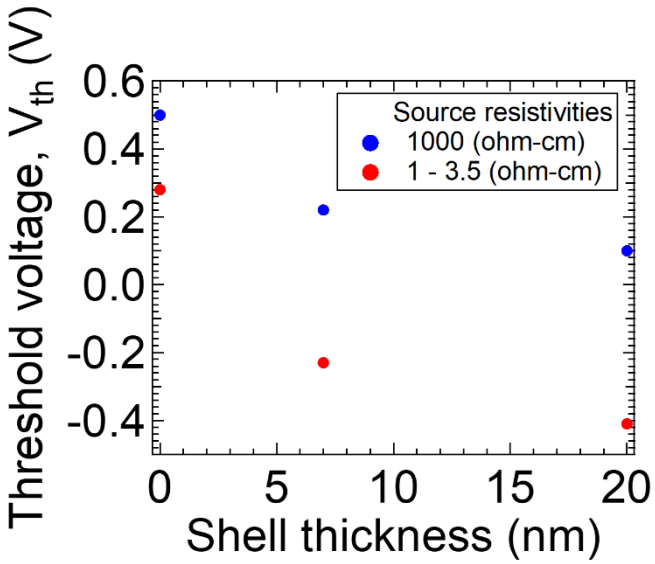


Figure 5-8: Dependence of threshold voltage for InAs/InP CS nanowire VGAA-FETs on Si with source resistivities of 1000 Ωcm (blue dot) and 1-3.5 Ωcm (red dot) on InP shell thickness.

$$SS = \frac{kT}{q} \ln 10 \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right), \tag{5.2}$$

where C_{ox} is the intrinsic capacitance of gate oxide, C_d is the depletion capacitance of the core InAs nanowire, and C_{it} is the interface trap capacitance. The small C_{ox} inherently

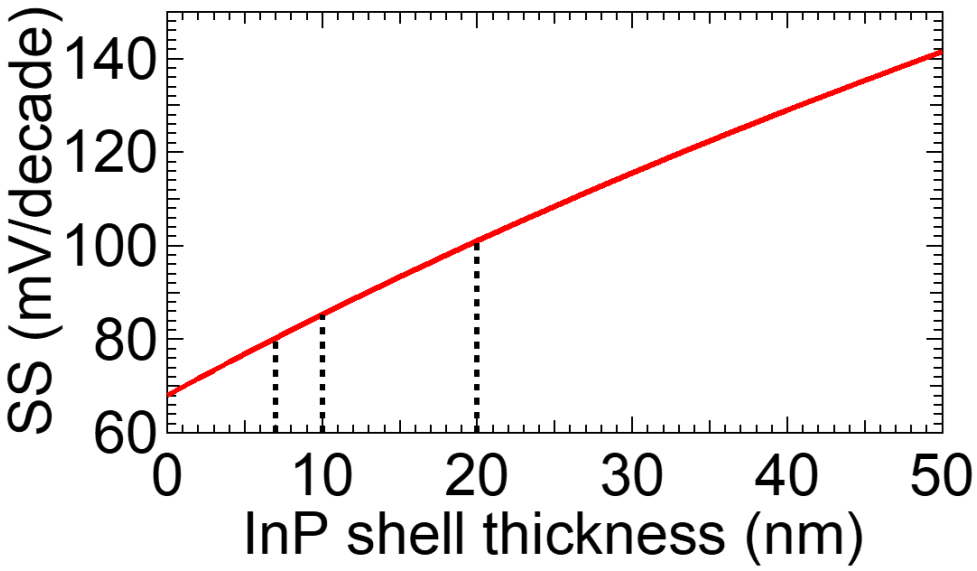


Figure 5-9: *SS* as a function of InP shell thickness in InAs/InP CS nanowire VGAA.

increases the *SS*. As for the InAs/InP CS nanowire VGAA-FET, the C_{ox} and depletion capacitance with the InP layer (C_{InP}) are connected in series. Thus, the *SS* is modified by

$$SS = \frac{kT}{q} \ln 10 \left(1 + \frac{C_d + C_{it}}{\frac{C_{ox} C_{InP}}{C_{ox} + C_{InP}}} \right). \tag{5.3}$$

The effective oxide capacitance decreases with increasing InP thickness; therefore, the *SS* is increased. Assuming that (C_d+C_{it}) is constant in equation (5.3), the increase in *SS* with increasing InP shell thickness is shown in Fig. 5-9. *SS* increased with increasing InP shell, and *SS* was 101 mV/decade at 20 nm InP shell thickness. However, the *SS* of InAs/InP CS nanowire VGAA-FETs on Si remained almost unchanged. This result is because InP/oxide exhibits better interfacial properties than InAs/oxide films. Therefore, the interface state density (D_{it}) of the InAs/InP CS nanowire VGAA-FETs is smaller than the 2.2×10^{12} $cm^{-2}eV^{-1}$ estimated in Chapter 4. On the other hand, the D_{it} of InAs/InP CS nanowire with 20 nm-thickness InP shell is estimated to be 2.9×10^{11} $cm^{-2}eV^{-1}$ from the *SS* of 70 mV/decade. This reduction in the interface state density offsets the increase in *SS* due to the reduction in effective oxide capacitance, and the thicker InP shell increases the on-current by forming 2DEGs. However, the thicker InP shell caused degradation factors such as lower carrier mobility and increased *SS* due to the formation of misfit

dislocations. We revealed an important tradeoff between the on-current increase and *SS* increase due to the core-shell structure.

5.5 Summary

We have investigated the improvement of I_{on} using the InAs/InP CS structure for nanowire VGAA-FETs. The VGAA-FETs demonstrated improvement of the I_{on} compared to the InAs nanowire VGAA-FET. The I_{on} was increased due to carrier confinement in the vicinity of the InAs/InP heterointerface, even if the InP shell increased the contact resistance. The calculation of the InAs/InP heterointerface using a one-dimensional Poisson-Schrödinger equation showed that carrier confinement and the threshold voltage can be modified by changing the InP shell thickness. The designed CS nanowire VGAA-FET is attractive for high-performance and low-power transistors because the confined carrier suppresses the scattering process, resulting in higher electron mobility.

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Chapter 6

Growth of InGaAs/GaSb Core-Shell Nanowires and Vertical Diode Application

Several research groups have actively explored antimonide-related III-V materials in recent years. The advantage of Sb-related materials with high carrier mobility is that it provides lower power consumption. However, the epitaxy of Sb-related materials is still challenging due to the surfactant effect of Sb atoms. In this chapter, we report on the dependence on growth temperatures and times for GaSb growth on InGaAs nanowires facet and investigate vertical diodes using InGaAs/GaSb core-shell nanowires on Si to characterize the InGaAs/GaSb heterojunction. The morphology of GaSb growth changed with growth temperatures, and We demonstrated GaSb growth with a smooth surface at a low temperature.

6.1 Introduction

The III-V compound semiconductor nanowires have attracted materials as next-generation nanoelectronics [1–6]. Among the III-V materials, InGaAs and GaSb are alternative materials expected as components in future electronic and optical devices because of their small effective mass and fast carrier mobilities [7–10]. In addition, the integration of III-V compound semiconductors on a Si platform has been of great interest

in optical interconnection and integrated circuits [11–15]. However, it is challenging to integrate III-V devices on Si due to mismatches in the lattice constant and thermal expansion coefficient between III-V materials and Si. In this regard, a small footprint of nanowire suppresses misfit dislocation and thereby permits the use of mismatched material systems [16]. The core-shell (CS) structure is essential to take advantage of material properties. The structure would reduce the surface states and provide confinement carriers [17,18]. The efficacy of the CS structures as tunneling field-effect transistors (TFETs) [19–21], Esaki diodes [22,23], and lasers [24,25] has been reported. For TFET applications, the subthreshold slope (*SS*) is less than the thermal limit (60 mV/dec at room temperature). However, TFETs intrinsically have a lower drive current than MOSFETs because the current is based on band-to-band tunneling (BTBT). TFET using a tunneling junction between core and shell increases BTBT current due to its large tunneling junction area [26]. The InGaAs/GaSb system provides the band alignment of a staggered and broken gap, depending on the In content of InGaAs. Thus, InGaAs/GaSb CS nanowire is a good candidate for high-performance TFET.

There is still difficulty in the versatile epitaxy of Sb-related III-Vs due to the surfactant effect of Sb atoms [27,28]. Sb atoms with high vapor pressure are prone to segregation, affecting the morphology and surface properties of the nanowire. The abrupt GaSb layer and interface between InGaAs and GaSb are essential to take advantage of device performance. The previous report regarding InAs nanowire facets has revealed that the surface roughness of nanowire facets converges with the period of 1-4 monolayers; hence, an atomically smooth surface is obtained. This smooth facet can be utilized for forming a smooth GaSb layer and a high-quality interface between InGaAs and GaSb. In this section, we investigated InGaAs/GaSb CS nanowires on Si(111) substrates using metal-organic vapor phase epitaxy (MOVPE) and compared the morphology of the nanowire by changing various growth temperatures of GaSb. A smooth GaSb shell was grown on the InGaAs nanowire sidewalls through low growth temperature (T_g). The vertical nanowire diode using InGaAs/GaSb CS nanowire exhibited rectifying properties.

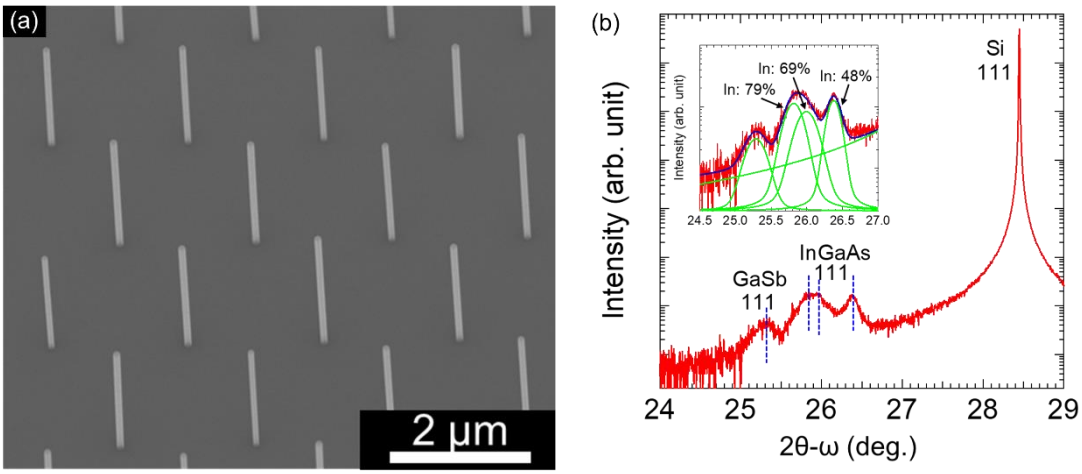
6.2 Experimental Procedure

InGaAs/GaSb CS nanowires were grown on Si by selective-area growth. Periodical mask openings were formed by electron beam lithography, dry etching, and wet etching processes. Trimethylindium (TMIn), trisdimethylaminoanitimony (TDMASb), arsine (AsH3), and trimethylgallium (TMGa) were used as source materials. Monosilane (SiH_4) and diethylzinc (DEZn) were used as n-type and p-type dopant sources, respectively. Si-doped InGaAs nanowires were grown for 15 min at 670°C. In content in vapor phase was 63%. Zn-doped GaSb layers were grown for 5-15 min at 450-540°C. The partial pressure of TMGa and TDMASb were 2×10^{-6} atm and 2×10^{-4} atm, respectively. The V/III ratio was 6.36.

For the fabrication of the vertical diode, the nanowires were buried with benzocyclobutene (BCB) as an interlayer dielectric by spin-coating, and the metal contact region was exposed by reactive ion etching. Ti/Au was evaporated on the top of the nanowires and the backside of the substrate. The vertical diodes were annealed at 380°C in N_2 for Ohmic contact.

6.3 Growth of InGaAs/GaSb Core-Shell Nanowires

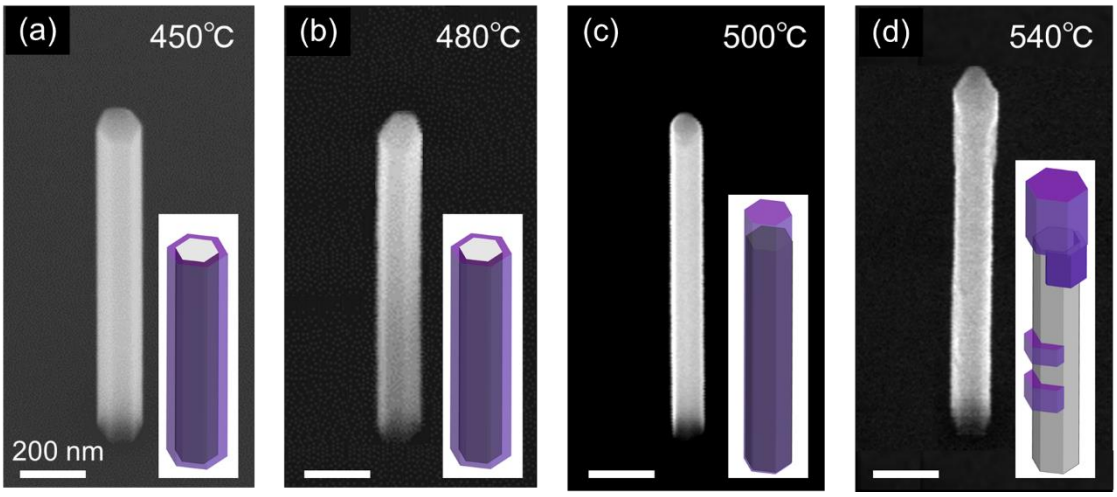
Figure 6-1(a) shows a scanning electron microscopy (SEM) image of representative growth results of InGaAs/GaSb CS nanowires array on Si(111). The nanowires were vertically aligned on Si(111). The morphology of InGaAs/GaSb CS nanowires with a similar mask opening diameter was investigated by SEM. The XRD profile of the grown nanowire array shown in Fig. 6-1(b) shows multiple diffraction peaks around 25.29°, 25.89°, 25.97°, and 26.49° in addition to the Si(111) diffraction peak. The peak deconvolution shown in the inset of Fig. 6-1(b) indicates that the InGaAs nanowires have various In compositions (48%, 69%, and 79%); the diffraction peaks with In compositions are attributed to the XRD measurements of the nanowire array containing different pitches. The diffraction peak at 25.29° originates from the GaSb layer and is roughly consistent with the lattice constant of GaSb (6.095 Å to 25.287°); the lattice mismatch



Figures 6-1: (a) 30°-tilted view SEM image of a integration of InGaAs/GaSb CS nanowire array on a Si(111) substrate. (b) XRD profile for the InGaA CS nanowires. Inset shows the peak deconvolution of the XRD spectra.

between the GaSb epilayer and $In_{0.79}Ga_{0.21}As$ is estimated to be 2%, indicating that the lattice distortion of the epitaxial GaSb layer is relaxed.

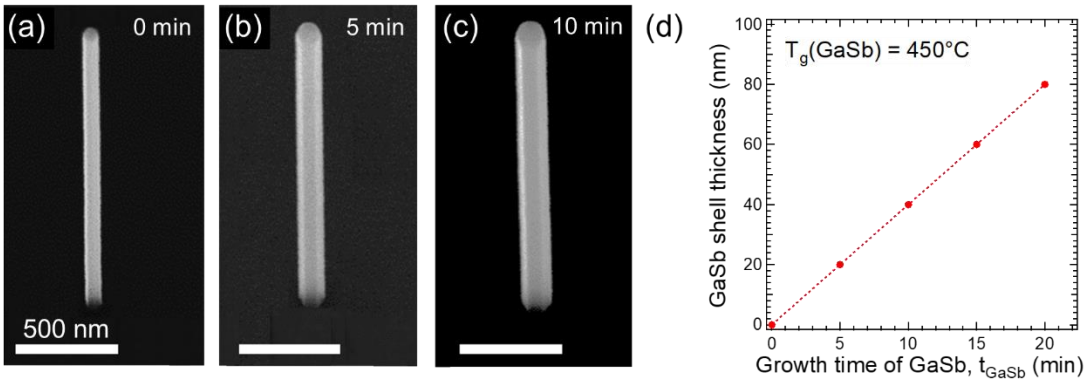
Fig. 6-2(a) shows the nanowires at different growth temperatures of GaSb, along with schematics of each case as insets. At the T_G of 450°C and 480°C, the GaSb layer was grown n along <-110> directions, and the axial growth along [111]B direction was suppressed. The vertical {-110} sidewalls maintained a smooth surface. This result indicated that the GaSb shell was uniformly grown on the InGaAs nanowire sidewalls. This is because the coverage of Sb increases at low T_g, and the adsorption and crystallization of Ga are promoted. For nanowire growth, one of the major contributions is adatom surface diffusion from the sidewalls and substrate surface to the nanowire top. The surface diffusion of Ga atoms from the nanowire sidewalls to the top is eliminated by promoted crystallization of Ga atoms in lateral growth. In addition, Sb is less likely to be adsorbed on the As-atom-exposed (111) plane. Thus, the growth of GaSb on the top facet was suppressed. At T_g of 500°C, the GaSb were grown on the top facet of the nanowires. At T_g of 540°C, GaSb was grown preferentially in the axial [111]B direction. Furthermore, GaSb were grown on the sidewalls of the nanowire partly. Thus, surface morphology for the GaSb roughened at T_g > 500°C. The morphology of nanowire sidewalls is because layer-by-layer growth and desorption processes of Sb atoms on the



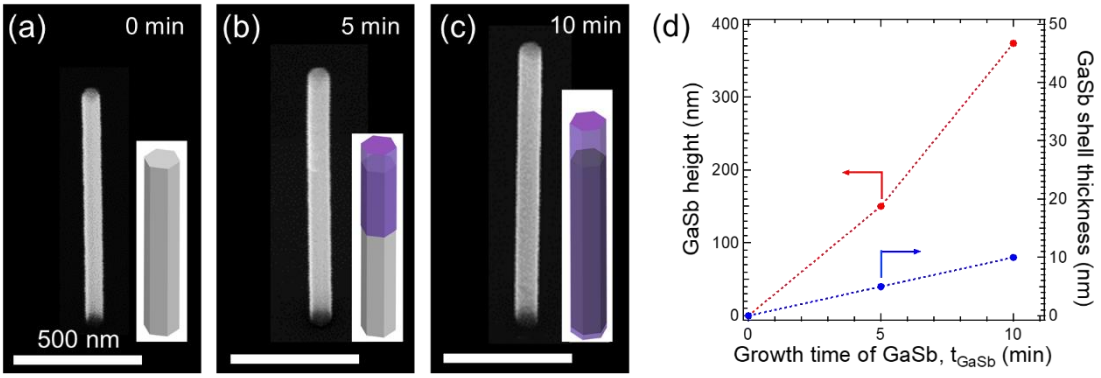
Figures 6-2: SEM images of representative InGaAs/GaSb CS nanowires at different growth temperature of GaSb. GaSb grown at: (a) 450℃, (b) 480℃, (c) 500℃, and (d) 540℃. The insets are schematic illustrations of nanowires, with InGaAs shown in gray and GaSb in purple.

nanowires sidewalls are competed due to high T_G, resulting in the inhomogeneity of the coverage of Sb adatoms.

Figures 6-3 and 6-4 show growth time dependence for InGaAs/GaSb CS nanowires at T_g of 450°C and 500°C, respectively. We compared the nanowires with a similar mask opening diameter. A SEM images in Fig 6-3(a) and 6-4(a) show bare InGaAs nanowires with a diameter of 80 nm. At T_g of 480°C, the diameter of nanowires increased as the growth time, while the nanowire height was almost constant. The lateral growth was grown linearly with 2 nm/min. The vapor pressure of Sb is extremely low, and hence the driving force for crystallization is low, resulting in a slow growth rate. At T_g of 500°C, The nanowire height linearly increased as the growth time, and the lateral growth rate was slower than that of T_g of 480°C. The axial growth rate was about 34 nm/min. In the case of a growth time of 5 min, the GaSb shell was grown downward from the nanowire top as following the illustration in Figs 6-5(a)-6-5(d). Figures 6-5(e)-6-5(h) show a schematic cross-section of the down-step-flow growth. The down-step-flow growth occurs because the nucleation on GaSb sidewalls axially grown is faster than nucleation on InGaAs sidewalls. First, GaSb axially grew on InGaAs nanowire top facet, as shown in Fig. 6-5(f). And then, lateral over-growth of GaSb occurs only on axially grown GaSb,

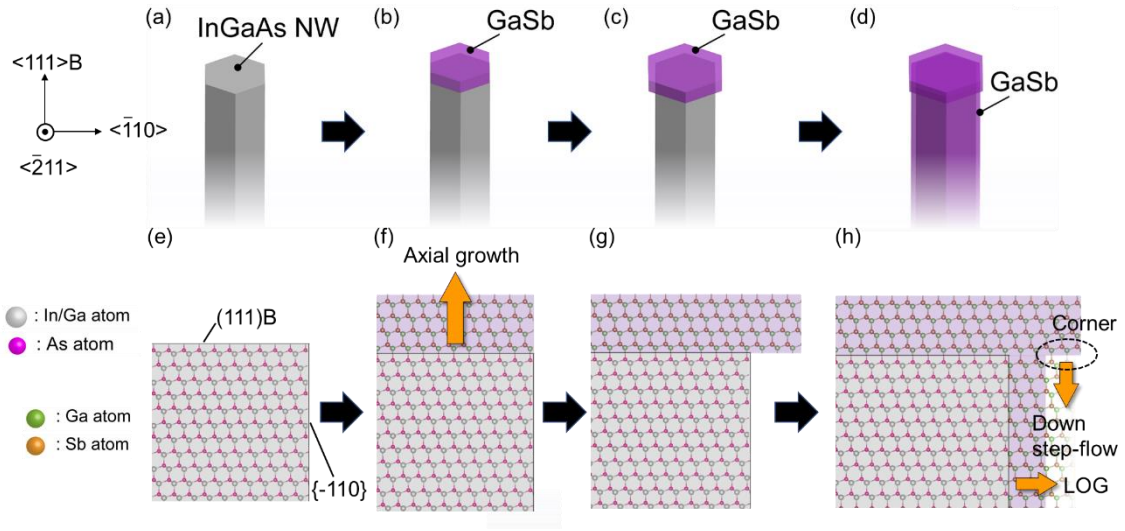


Figures 6-3: SEM images of representative bare InGaAs nanowire and InGaAs/GaSb CS nanowires with GaSb growth time of (a) 0 min (bare InGaAs nanowire), (b) 5 min, and (c) 10 min at growth temperature of 480°C. (d) GaSb shell growth thickness as a function of the growth time of GaSb.



Figures 6-4: SEM images of representative bare InGaAs nanowire and InGaAs/GaSb CS nanowires with GaSb growth time of (a) 0 min(bare InGaAs nanowire), (b) 5 min, and (c) 10 min at growth temperature of 500°C. The insets are schematic illustrations of nanowires, with InGaAs shown in gray and GaSb in purple. (d) GaSb height and shell growth thickness as a function of the GaSb growth time.

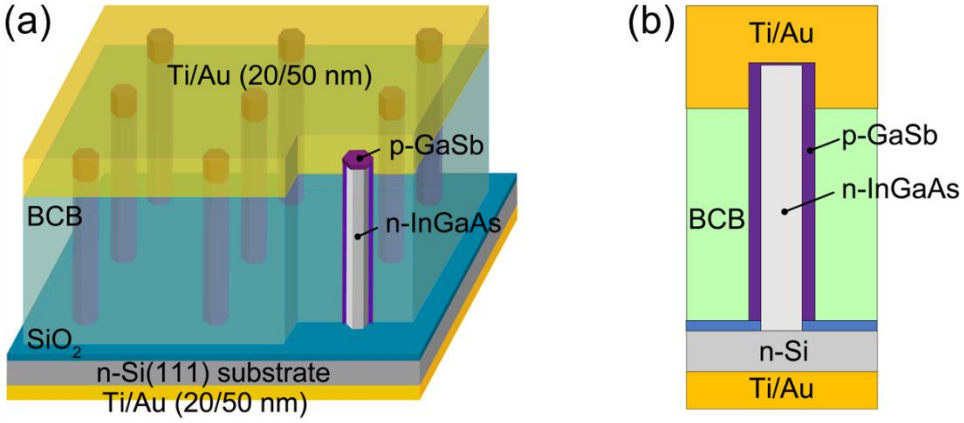
as shown in Fig. 6-5(g). The nucleation rate of GaSb on InGaAs nanowire sidewalls is slow due to the large lattice mismatch between GaSb and InGaAs. In addition, crystallization progressed preferentially along the <111>B direction in the downward direction since there were three more dangling bonds in the corners than in the {-110} facet, as shown in Fig. 6-5(h). These results indicate that the optimum T_g for forming the high-quality GaSb shell layer was 450°C.



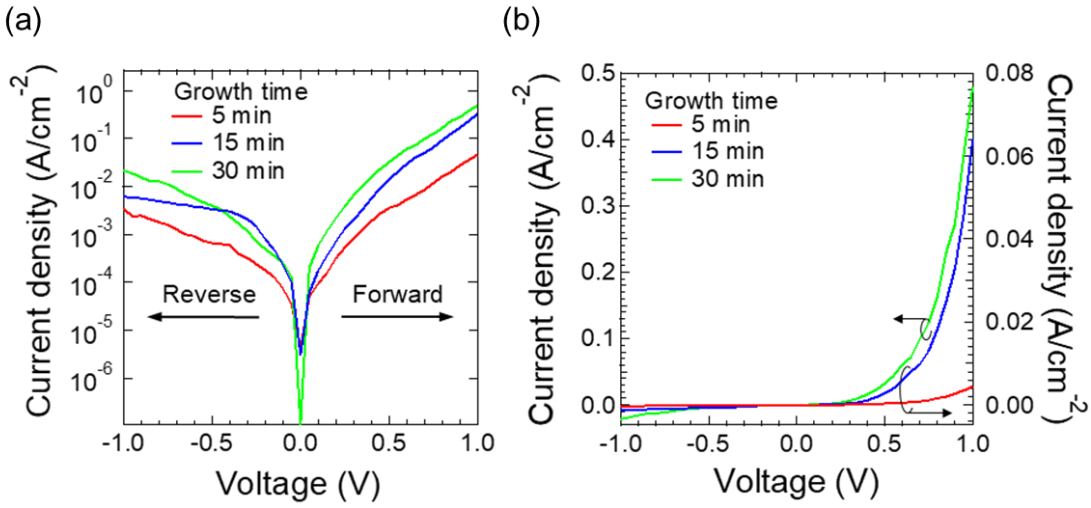
Figures 6-5: (a)-(d) Schematic illustration of the GaSb growth process on the InGaAs nanowire at T_g = 500°C. (e)-(h) Illustration of cross-section of GaSb growth process on InGaAs nanowire along the <-211> view. Crystallographic images were illustrated using Visualization for Electronic and Structural Analysis (VESTA) program [29].

6.4 InGaAs/GaSb Core-Shell Nanowires-Based Vertical Diodes

Figures 6-5(a) and 6-5(b) illustrate the nanowire-based vertical diode and schematic cross-sectional structure, respectively. Zn-doped GaSb layers were grown on InGaAs nanowires at the GaSb growth temperature of 450°C to characterize InGaAs/GaSb heterojunction. The diode connects five nanowires in parallel. The current density-voltage curve of semi-logarithmic and linear plots for the device for different GaSb growth times, as shown in Figs. 6-6(a) and 6-6(b), respectively. Measured currents were normalized by the metal contact area of the nanowires. The current density increased with increasing the growth time of GaSb. The current increment originated from the increased carrier concentration inside the GaSb shell as GaSb thickness increased. A depletion layer width of GaSb was calculated from an impurity concentration of GaSb, as shown in Fig. 6-7(a).



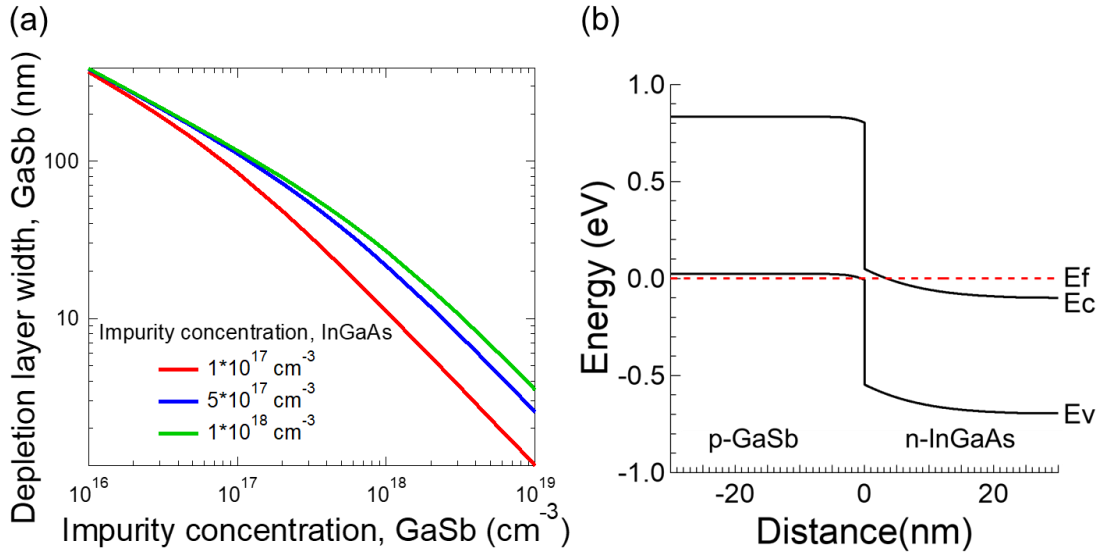
Figures 6-6: (a) Schematic structure of InGaAs/GaSb CS nanowire diode. (b) Schematic cross-sectional structure.



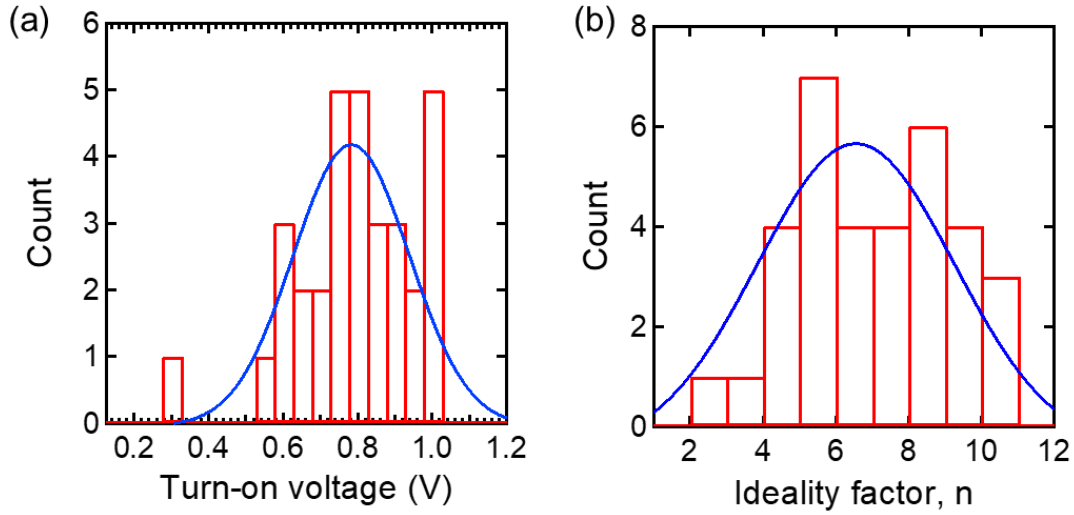
Figures 6-7: (a) Linear plot and (b) semilogarithmic of *J-V* curves of the InGaAs/GaSb CS nanowire veritical diode for different growth time of GaSb at growth temperature of 450℃.

The thickness of the GaSb layer for the growth time of 5 min was below the depletion layer width under the thermal equilibrium. Therefore, the current density for GaSb growth time of 5 min decreased because a p-type neutral region was not formed. Fig. 6-7(b) exhibits the band diagram profile across the InGaAs/GaSb heterojunction under the thermal equilibrium conditions. The calculated band discontinuity exhibited staggered Type-II.

Next, to accurately characterize the InGaAs/GaSb heterojunction, InGaAs/GaSb CS nanowires were grown at 450°C for 15 min and then at 500°C for 10 min, and the nanowire-based vertical diodes were fabricated. The histogram of the observed turn-on



Figures 6-8: (a) Depletion layer width of GaSb for different impurity concentration of InGaAs nanowire as a function of the impurity concentration of GaSb. (b) Band diagram of InGaAs/GaSb heterojunction simulated using the one-dimensional Poisson-Schrödinger equation under the thermal equilibrium conditions.



Figures 6-9: Histogram of properties of InGaAs/GaSb CS nanowire-based vertical diodes for 32 devices; the solid line corresponds to a Gaussian fit: (a) Trun-on voltage. (b) Ideality factor.

voltage for 32 devices was plotted in Fig. 6-8(a) with an average turn-on voltage of 0.78 V. The average turn-on voltage corresponded to the conduction band offset (about 0.70 V) calculated by the one-dimensional Poisson-Schrödinger equation. The turn-on voltage was estimated by linearly extrapolating current versus voltage in the forward bias. Figure

6-8(b) shows the histogram of the calculated ideality factor (n). We calculated using the current equation $J(n) = J_0\, exp[(V - R_s I)/nkT]$. Most nanowire-based p-n junctions reported an ideality factor of n > 2. The large ideality factor for the device originated from the carrier tunneling across the junction and the device fluctuation. The large ideality factor indicated misfit dislocation between the InGaAs/GaSb heterointerface.

6.5 Summary

Selective area growth of InGaAs/GaSb core-shell nanowires is demonstrated, revealing the morphology of GaSb shell growth. The lateral growth of the GaSb shell layer was dominant at T_G < 480°C. At T_G > 500°C, the axial and radial growth of GaSb competed. We find that these growth contributions can be separated by varying the GaSb growth temperature. In particular, we found that a low T_G(GaSb) on the nanowire top surface promotes the lateral over-growth process and the formation of an atomically thin GaSb shell layer. The vertical diode structure using the InGaAs/GaSb CS nanowires on Si exhibited moderate rectifying properties with a turn-on voltage of 0.78 V. The turn-on voltage corresponded to the conduction band offset of the n-InGaAs/p-GaSb heterojunction.

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Chapter 7

Vertical Gate-All-Around Field-Effect Transistors Using InGaAs/GaSb Core-Shell Nanowires

This chapter report on vertical gate-all-around transistor using the InGaAs/GaSb core-shell nanowires on Si. We found that the device can operate in both n-tunnel field-effect transistor (TFET) and p-MOSFET, depending upon the polarity of V_{DS}. The drain current was modulated by gate bias under negative V_{DS} in MOSFET switching mode. The MOSFET mode had a minimum subthreshold slope (*SS*) of 115 mV/decade and I_{on}/I_{off} ratio of around 10^2 at V_{DS} = -1.00 V. We obtained TFET switching mode in the same structure because this drain current originated from tunnel transport across the n-InGaAs nanowire/p-Si junction. The drain current was modulated by gate bias under the positive V_{DS} in TFET switching mode. The TFET mode showed *SS* of 105 mV/decade at V_{DS} = 0.50 V. The *SS* was still higher than 60 mV/decade, which indicates the effective electrical field was decreased at the InGaAs/Si interface due to the thick GaSb shell and high contact resistance of GaSb/InGaAs.

7.1 Introduction

The integration of III-V semiconductor devices on silicon is a major challenge in current electronic materials research due to the material properties difference between III-V and Si, which introduces a high density of defects. In this regard, III-V semiconductor

nanowires have a lot to offer because their small footprint enables suppression of misfit dislocation [1,2]. A significant body of work has recently emerged on III-V field-effect transistors (FETs) with InGaAs and GaSb, channel material candidates for future CMOS devices [3–9]. InGaAs for n-type FET and GaSb for p-type FET satisfy many requirements on a channel material: high carrier mobility, low effective mass, low contact resistance, and good interfacial quality with high-*k* dielectrics [10,11]. However, a severe issue in the co-integration of n- and p-type channels on the same substrate remain and hinder the development of III-V digital CMOS logic circuits. Several research groups have reported on the co-integration of III-V materials. Wernersson's group from Lund University demonstrated n- and p-type III-V MOSFETs monolithically integrated on Si substrate using both InAs and InAs/GaSb vertical nanowires [12,13]. In addition, Takagi's group from the University of Tokyo has demonstrated a single channel III-V complementary metal-oxide-semiconductor transistors by ultrathin body InAs/GaSb-on-insulator channels on Si [14,15]. These device structures and fabrication processes, however, are increasingly complex. In this chapter, we suggest that the core-shell (CS) structure of n-InGaAs nanowire and p-GaSb shell enable the co-integration of n- and p-type channels. We demonstrate dual switching properties using InGaAs/GaSb CS nanowires on Si as a channel of vertical gate-all-around FET (VGAA-FET).

7.2 Experimental Procedure

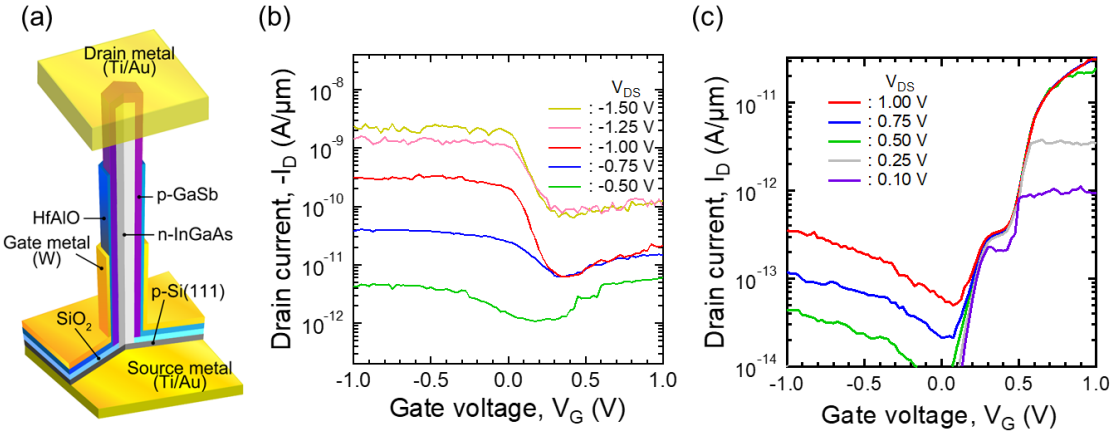
InGaAs/GaSb CS nanowires were grown on Si by selective-area growth. Periodical mask openings were formed by electron beam lithography, dry etching, and wet etching processes. Trimethylindium (TMIn), trisdimethylaminoantimony (TDMASb), arsine (AsH3), and trimethylgallium (TMGa) were used as source materials. Monosilane (SiH_4) and diethylzinc (DEZn) were used as n-type and p-type dopant sources, respectively. Si-doped InGaAs nanowires were grown for 15 min at 670°C. Zn-doped GaSb layers were grown at 450°C. The V/III ratio was 6.36.

We fabricated vertical gate-all-around (VGAA) FETs. First, a 10-nm-thick $Hf_{0.8}Al_{0.2}O_2$ film was deposited on the surface of the nanowires by atomic layer deposition. Next, 200 nm-thick gate metal (tungsten, W) was sputtered. The nanowires were buried

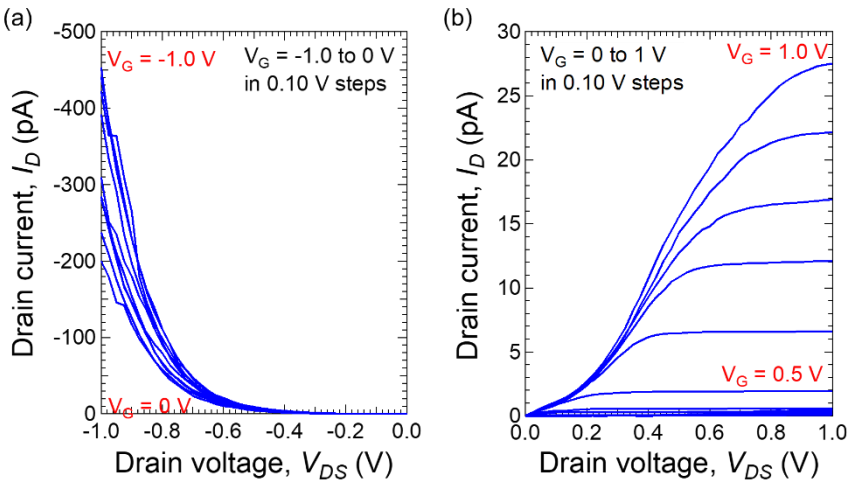
with benzocyclobutene (BCB) by spin-coating, and the BCB was etched to desired thickness. An isolation layer between gate and drain was formed by repeating the BCB and reactive ion etching processes. Drain (Ti/Au) and source (Ti/Au) metals were evaporated on the top of the nanowires and backside of the substrate, respectively. Finally, the VGAA-FETs were annealed at 400°C in N_2 for Ohmic contact in the drain and source metals.

7.3 Vertical Gate-All-Around Field-Effect Transistors Using the InGaAs/GaSb Core-Shell Nanowires

Figure 7-1(a) illustrates the schematics of the VGAA-FET structure consisting of p-Si (source)/n-InGaAs nanowire (channel)/p-GaSb shell (drain). Figs. 7-1(b) and 7-1(c) show the transfer characteristics for the VGAA-FET with a 30 nm thick GaSb shell under the negative and positive V_{DS}, respectively. The measured current was normalized with the gate outer perimeter and number of nanowires. The transfer characteristics indicated that the drain current was modulated by gate bias. Interestingly, the VGAA-FET using the InGaAs/GaSb CS nanowires exhibited dual switching behavior depending on the polarity of V_{DS}. The VGAA-FET showed p-type FET behavior under the negative V_{DS}, as shown in Fig. 7-1(b). The device in the p-type behavior showed a minimum subthreshold slope (*SS*) of 115 mV/decade and an on/off ratio of 10^2. Meanwhile, the VGAA-FET demonstrated n-type TFET behavior in the same structure under the positive V_{DS}, as shown in Fig. 7-1(c). And the tunnel current originated from the InGaAs nanowire/p-Si heterojunction. The device in the n-type TFET behavior showed a minimum *SS* of 105 mV/decade and on/off ratio of 10^3. The *SS* of the TFET mode was higher than the thermal limits of 60 mV/decade. This result indicated that the GaSb shell layer slightly interrupted the gate modulation at the InGaAs nanowire/Si junction. The effective electrical field was decreased at the InGaAs nanowire/Si because the distance between the gate electrode and the InGaAs nanowire/Si interface increased, and the electric field was dispersed by InGaAs/GaSb heterojunction. The output characteristics showed nonlinear characteristics because of high contact resistance of drain region. Figs. 7-2(a) and 7-2(b) show the output



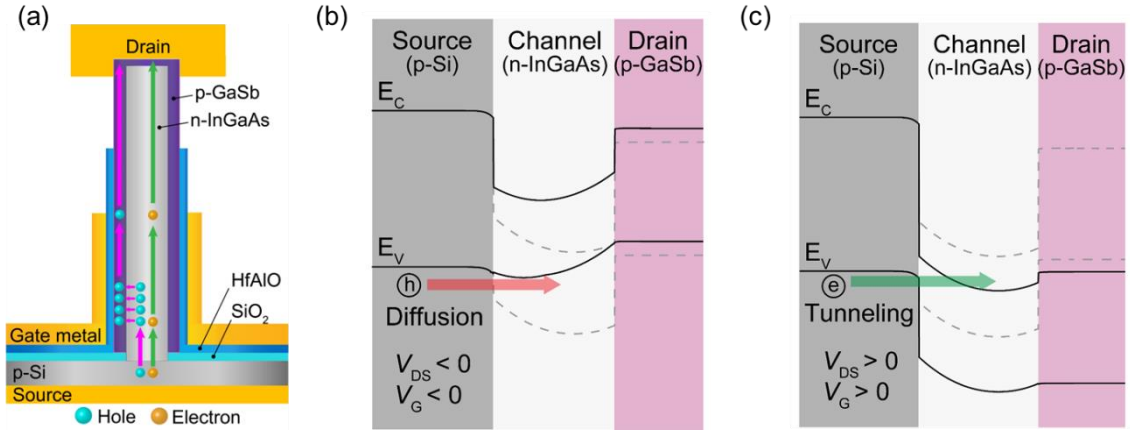
Figures 7-1: (a) Illustration of the InGaAs/GaSb CS nanowire VGAA-FET. (b) Transfer characteristics of InGaAs/GaSb CS nanowire VGAA-FET on Si under the negative V_{DS}. (c) Transfer characteristics of InGaAs/GaSb CS nanowire VGAA-FET on Si under the positive V_{DS}.



Figures 7-2: Output characteristics of InGaAs/GaSb CS nanowire VGAA-FET on Si. (a) Applying the negative V_{DS}. (b) Applying the positive V_{DS}.

characteristics for the device under the negative and positive V_{DS}, respectively. The output characteristics showed nonlinear characteristics because of high contact resistance of drain region.

Fig. 7-3(a) represents a schematic illustration of the device operation,



Figures 7-3: (a) Schematic illustration displaying the carrier conduction in the n- and p-type FET behavior. (b) Band diagram of the p-type behavior in on-state (black line) and off-state (gray dashed line). (c) Band diagram of the n-type behavior in on-state (black line) and off-state (gray dashed line).

incorporating hole (radial) and tunneling electron (axial) transports. Under the positive V_{DS}, holes transport to the GaSb shell layer from the p-Si substrate across the core InGaAs nanowire channel. On the other hand, under the negative V_{DS}, tunneling electrons transport from the p-Si substrate into InGaAs nanowire channel via BTBT process reached the drain edge of the p-GaSb layer. Figures 7-3(b) and 7-3(c) illustrate the band diagram in the on-state (black lines) and the off-state (black dashed lines) for the p-MOSFET and n-TFET behavior. Note that these carrier injection and transport mechanisms are caused by the difference in the gate bias modulation of the potential inside the InGaAs nanowire layer. Applying the negative gate voltage under negative V_{DS} upwards the potential of InGaAs nanowire channel against holes transport. Thus, holes diffused into p-GaSb shell through the InGaAs nanowire. Applying the positive gate bias under positive V_{DS} downward the potential in the InGaAs nanowire layer resulting in BTBT a cross the n-InGaAs nanowire/p-Si junction. The increased positive V_{DS} eventually decreases the depletion region width across the InGaAs nanowire/top GaSb junction at the drain edge, and the electron reaches the drain edge. Further improvements, for example, reduction in drain contact resistance and design of carrier concentrations in each layer, are required for the high-performance GaSb p-MOSFETs and TFET with steep

SS. We suggested that the unique device performance for the InGaAs/GaSb CS nanowire on Si would provide a new approach to integrating a complementary switch by a single transistor structure.

7.4 Summary

InGaAs and GaSb are alternative fast channel materials for future n-channel and p-channel FETs. However, there is a severe issue in integrating these different III-V channels as building blocks for CMOS on the same Si platforms. The InGaAs/GaSb CS nanowire on Si demonstrated co-integration of n- and p-channel materials. The transfer and output characteristics for the VGAA-FETs using the InGaAs/GaSb CS nanowire on Si indicated that the drain current was modulated by gate bias. The carrier conduction of p-type MOSFET mode occurred by diffusion of holes from the source into the channel under the negative V_{DS}. The conduction of n-type TFET mode occurred by the tunneling transports of electrons across the InGaAs nanowire channel/Si interface under the positive V_{DS}. The VGAA-FETs using the InGaAs/GaSb CS nanowire channel demonstrated n- and p-type switching behavior in the same structure and have the potential to realize vertical complementary integration circuits on the Si platform.

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Chapter 8

Conclusion

In this study, vertically aligned III-V nanowires on Si by selective-area growth are demonstrated. Additionally, field-effect transistors (FETs) using III-V compound semiconductor nanowire heterostructure achieved high-performance device and n- and p-type switching behavior.

8.1 Summary

In chapter 4, the InAs nanowires were grown by selective-area growth. The InAs nanowires constructed Zn- and Sn-pulse-doped layers. The pulse-doped nanowires grew vertically on Si without any growth in the lateral direction, and a hexagonal pillar shape was maintained, similar to undoped-InAs nanowires. We demonstrated an InAs nanowire vertical gate-all-around (VGAA) FET with a pulse-doping technique. The device showed subthreshold slope (*SS*) of 68 mV/decade and an off-leakage current of ~100 fA at V_{DS} = 0.50 V. The introduction of the pulse-doped layers significantly improved the *SS* and leakage current comparison with undoped-InAs nanowires. In addition, the device operated as a normally-off transistor because of the formation of a pseudo-intrinsic InAs channel by the Zn-pulse-doped layer.

In chapter 5, we investigated the improvement of on-state current (I_{on}) using the InAs/InP core-shell (CS) structure for nanowire VGAA-FETs. The VGAA-FETs demonstrated improvement of the I_{on} compared to the InAs nanowire VGAA-FET. The I_{on} was increased due to carrier confinement in the vicinity of the InAs/InP heterointerface, even if the InP shell increased the contact resistance. The calculation of the InAs/InP

heterointerface using a one-dimensional Poisson-Schrödinger equation showed that carrier confinement and the threshold voltage can be modified by changing the InP shell thickness. The designed CS nanowire VGAA-FET is attractive for high-performance and low-power transistors because the confined carrier suppresses the scattering process, resulting in higher electron mobility

In chapter 6, selective area growth of InGaAs/GaSb core-shell nanowires is demonstrated, revealing the morphology of GaSb shell growth. The lateral growth of the GaSb shell layer was dominant at the growth temperature of GaSb less than 480°C. At the growth temperature of GaSb above 500°C, the axial and radial growth of GaSb competed. We found that these growth contributions can be separated by varying the GaSb growth temperature. In particular, we find that a low T_G(GaSb) on the nanowire top surface promotes the lateral over-growth process and the formation of an atomically thin GaSb shell layer. The vertical diode structure using the InGaAs/GaSb CS nanowires on Si exhibited moderate rectifying properties with a turn-on voltage of 0.78 V. The turn-on voltage corresponded to the conduction band offset of the n-InGaAs/p-GaSb heterojunction.

In chapter 7, InGaAs and GaSb are alternative fast channel materials for future n-channel and p-channel FETs. However, there is a severe issue in integrating these different III-V channels as building blocks for CMOS on the same Si platforms. The InGaAs/GaSb CS nanowire on Si demonstrated co-integration of n- and p-channel materials. The transfer and output characteristics for the VGAA-FETs using the InGaAs/GaSb CS nanowire on Si indicated that the drain current was modulated by gate bias. The carrier conduction of p-type MOSFET mode occurred by diffusion of holes from the source into the channel under the negative V_{DS}. The conduction of n-type TFET mode occurred by the tunneling transports of electrons across the InGaAs nanowire channel/Si interface under the positive V_{DS}. The VGAA-FETs using the InGaAs/GaSb CS nanowire channel demonstrated n- and p-type switching behavior in the same structure and have the potential to realize vertical complementary integration circuits on the Si platform.

8.2 Outlook for Nanowire Transistors

In recent years, technological advances such as the IoT and computational algorithms have led to high expectations for CMOS that can achieve high-speed processing of big data with low power consumption. However, as the limits of FET miniaturization have begun to be reached, there is a growing need for alternative technologies that can support future improvements in computer performance. For this issue, it is being investigated to increase the on-current by replacing the Si-based semiconductor channel material with III-V compound semiconductors or Ge, which have high mobility, and to suppress the leakage current by introducing a three-dimensional gate structure.

In future work, we will integrate channels on silicon-on-insulator(111) fin wires to realize three-dimensional integrated circuits consisting of III-V nanowires. Therefore, it is important to clarify the mechanism of nanowire growth on silicon-on-insulator fin wires. Based on these findings, we will fabricate a prototype three-dimensional integrated circuit and demonstrate the current density matching of n-type and p-type FETs and circuit operation. We will also fabricate an inverter circuit and a ring oscillator circuit and evaluate the delay time and power consumption of the circuits, aiming for high-speed operation and low voltage.

List of Publications/Conferences/Awards

1. Pubilication related to this work

[1]. Hironori Gamo, Katsuhiro Tomioka: "Selective-area growth of pulsed-doped InAs nanowires on Si and vertical transistor application" J. Cryst. Growth, Vol. 500, pp. 58 – 62 (2018) (IF = 1.797, T.C.=4)

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2. Publication related to other works

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[1]. H. Gamo, K. Tomioka, A. Yoshida, J. Motohisa, "Selective-area growth of pulse-doped InAs related nanowire-channels on Si" 19th International Conference on Metalorganic Vapor Phase Epitaxy (ICMOVPE-XIX), Nara, Japan, June 3 – 8 (2018).

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4. Presentations related to other work

International conference

[1]. K. Tomioka, A. Yoshida, H. Gamo, “Heteroepitaxial growth of InGaAs/InP/InAlAs/InP core-multishell nanowires on Si for a complementary tunnel FETs” Compound Semiconductor Week 2019 (CSW 2019), Nara, Japan, May 19 – May 23 (2019).

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[11]. 木村峻、蒲生浩憲、勝見悠、本久順一、冨岡克広、「代替ナノ光源に向けた異なる pn 接合構造を持つウルツ鉱 InP ナノワイヤ発光ダイオード」、The 38th Electronic Materials Symposium (EMS 41), 橿原 2022 年 10 月.

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5. Awards

[1]. 令和 2 年度電子情報通信学会北海道支部学生奨励賞

6. Patents

特許特願2022-48567 「マルチモードスイッチ素子」 発明者: 蒲生浩憲, 冨岡克広, 出願日:2022年3 月24 日.