Ring-VCO-based ADC design for low-energy smart sensing devices

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Abstract

The rise of IoT sensor nodes enables continuous background monitoring of our internal physiological (blood oxygen, electrocardiography) and various external (surrounding) environmental (air quality, humidity, moisture, pressure, sound, and temperature) signals. In recent years, Internet of Things (IoT) sensors are being powered using energy harvesters, motivated by mobile and battery-less operation in remote areas. Additionally, key to smart sensing is embedding or integrating IoT sensors with artificial intelligence, and it is a significant challenge due to their energy and resource requirements. In this thesis we report the development of a novel ring VCO-based ADC architecture suitable for ultra-low energy smart IoT sensors. Analog-to-digital converters (ADCs) are a necessary part of the data acquisition in IoT sensors, and we designed a voltage-controlled oscillator-based ADC using all digital circuits. Our motivation is based on the theory that VCO-based ADCs can be implemented very efficiently with a ring oscillator, which is a simple digital circuit.

Fundamentally, a ring-VCO can generate digital code by counting its pulse frequency. Low energy IoT devices can benefit from scaling down the CMOS technology, this can reduce the operating voltage, therefore, minimizing power dissipation. Although the operating voltage is scaled down, the threshold voltage of transistors is not significantly reduced. VCO-based ADCs have been widely studied in a great deal of papers and it is known that one of its main drawbacks is the non-linearity of voltage-to-frequency (V-to-F) tuning characteristics it presents. Furthermore, operating at a lower voltage could adversely affect the linearity of the V-to-F tuning characteristic. One of the objectives of this thesis is to improve the linear V-to-F characteristic of the ring-VCO, in which IoT systems are constrained in their supply voltage by ambient energy sources.

We approach the new linearity improvement technique called complementary bias voltage control to achieve linear V-to-F characteristics of fully pseudo-differential current-starved inverter-based delay elements without using body bias. The complementary bias voltage control consists of the independent voltage-to-current (V-to-I) conversion, which provides the linear bias current source and sinks matching for the current-starved transistor of delay elements. Additionally, the best nonlinearity error can be optimized by selecting an optimal transistor size. The second

contribution of this thesis will facilitate reducing the size and area costs of future IoT sensor devices. By simplifying the development of fully pseudo-differential current- starved ring oscillators as observed in our first contribution. From our studies, reducing the number of transistors will not adversely affect the linearity of the V-to-F tuning characteristic.

Finally, inspired by AI-enabled intelligent sensing networks, we propose a pulse neuron circuit in which fully pseudo-differential current-starved inverter-based delay elements with linearity technique are served as ReLU linear activation functions using their V-to-F tuning characteristic.

Furthermore, our experiments and studies show the nonlinearity effect of process variation, and we propose a compensation technique. All the three proposed circuit contributions have been proven by using Cadence Spectre (Virtuoso Design Environment version IC6.1.8-64b). The simulation results with a 0.5V power supply circuit designed in TSMC 180nm CMOS technology are observed as follows:

- The measured maximum nonlinearity error is below 0.24% for 4-stage and below 0.49% for 8-stage ring-VCO.
- Only 4-stage ring VCO can generate 8 phase signal, and it normally requires more than 9 numbers of delay cells.
- The designed pulsed neuron circuit which can be used in DNN is benchmarked by MNIST performance, and we report average validation accuracy among ve possible corners at approximately over 97%.

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Contents

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List of Abbreviations

ADCs . . . . . Analog-to-digital converters

AIoT . . . . . Artificial intelligence of things

Amp . . . . . Amplifier

CT $\Delta\Sigma$ ADC . Continuous-time delta sigma analog-to-digital converter

C3PU . . . . . Cross-coupling capacitor processing unit

CLK . . . . . Clock

CMOS . . . . . Complementary metal oxide semiconductor

CMRR . . . . Common-mode rejection ratio

CPG . . . . . Central pattern generator

DSP . . . . . Digital signal processing

DNN . . . . . Deep neural network

FD-SOI . . . . Fully Depleted Silicon on Insulator

FF . . . . . Fast-Fast Conner

FS . . . . . Fast-Slow Conner

FOM . . . . . Figure-of-merits

IoT . . . . . Internet-of-Things

LC- VCO . . . inductor-capacitor-voltage-controlled oscillator

LSB . . . . . Least Significant Bit

MAC . . . . . Multiply-and-accumulate

MNIST . . . . Mixed National Institute of Standards and Technology

NMOS . . . . N-channel metal oxide semiconductor

PMOS . . . . . P-channel metal oxide semiconductor

PMAC . . . . Phase-encoded MAC circuit

PWM . . . . . Pulse-width modulated

ReLU . . . . . Rectifier linear Unit

Ring-VCO . . Ring voltage-controlled oscillator

RO . . . . . Ring oscillator

RMS jitter . . description]

SF . . . . . Slow-Fast Conner

SS . . . . . Slow-Slow Conner

SNR . . . . . Signal-to-noise-ratio

SNDR . . . . . Signal-to-noise-distortion-ratio

VACs . . . . . Voltage accumulators

VCO . . . . . Voltage-controlled oscillator

VDD(V_{DD}) . . Supply voltage

Vin(V_{in}) . . . . Input voltage

VTC . . . . . Voltage-to-Time Converter

VTH(V_{Th}) . . . Threshold voltage of transistor

V/I . . . . . Voltage-to-current

V-to-I . . . . . Voltage-to-current

V-to-F . . . . . Voltage-to-Frequency

1 Introduction

1.1 Motivation

Recently there is an increased interest in smart devices, and it has resulted in development of embedded sensing applications for healthcare, home automation and transportation. The smart sensors used in the IoT devices are known as Artificial intelligence of things (AIoT). In future AIoT devices may connect billions of edge devices in the multidisciplinary paradigm via wireless communication. Additionally, these IoT devices are expected to have long operational lifetime; hence, IoT device consume energy from batteries or energy harvester of which the open circuit (OC) voltage (<0.5 V) is mandatory to operate in sub- threshold and at the lowest operating voltage. (e.g. $V_{DD} < 0.5$ V) as evident in figure 1.1 [1]. Ideal design objective when developing such sensors are ultra-low-power operation which is realized by using energy-efficient circuits for both communication and computing part. For data acquisition, analog-to-digital converter (ADC) is indispensable and is utilized in the preprocessing stage as analog interface circuits.

Conventional voltage domain ADC fundamental relies on the analog domain, thereby utilizing preprocessing circuits such as an analog amplifier, filters, etc., as shown in figure 1.2[2]. Continuous time (CT) $\Delta\Sigma$ ADC as proven to be a great

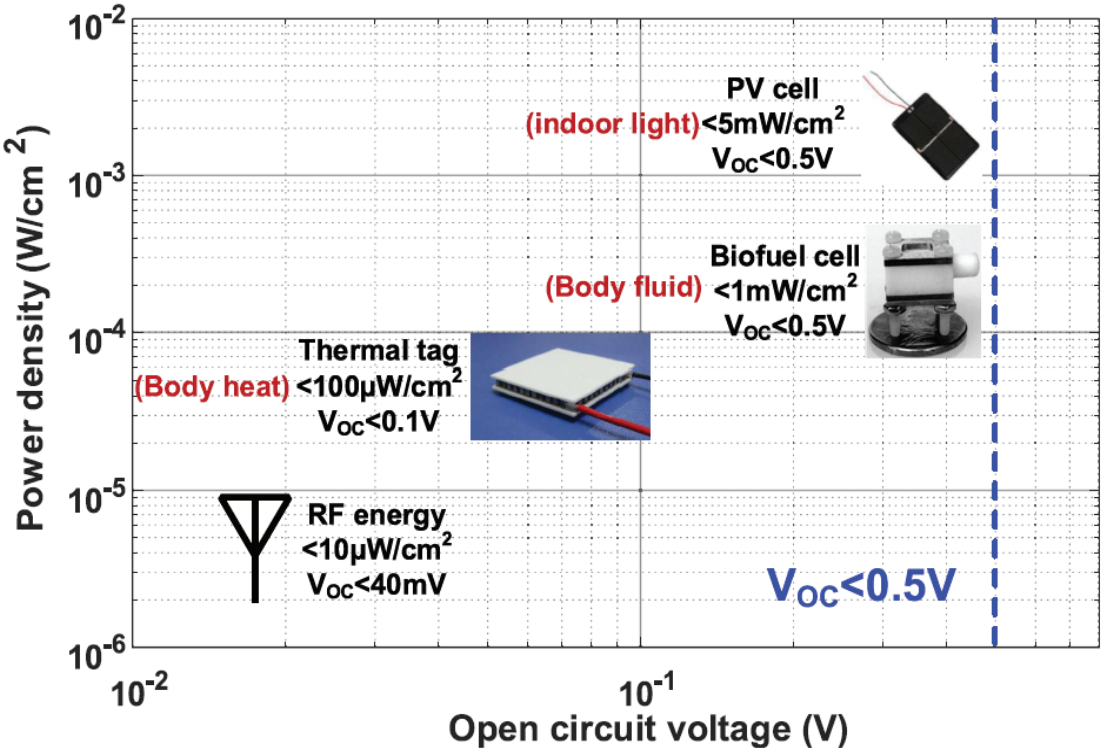

Figure 1.1: Power density and open circuit voltage range of various energy harvester that can be potentially integrated into a wearable or implantable sensor[1].

candidate for IoT edge devices; consequently, it benefits from CMOS scaling technology. Their advantageous properties include simplicity in circuit implementation by removing the sample/hold circuit with continuous sampling in each sampling period. Furthermore, this continuous sampling generates anti-aliasing characteristics and can even make analog pre-filter dispensable. Ring-VCO based ADC is one of the CT $\Delta\Sigma$ ADC, because the ring-VCO and the counter performs continuous integrating pulse density in each sampling period while frequency counting and reuse phase condition of the VCO as the quantization error for the following conversion. Ring-VCO based ADC is fundamental construction of chain of CMOS inverters or delay elements, where an analog input is continuously converted from voltage to frequency.

In ring-VCO based ADCs, non-linearity is an issue, because high linearity can directly achieve lower harmonic distortion with high signal-to-noise-ratio (SNR) and signal-to-noise-distortion-ratio (SNDR). IoT applications strongly require smaller-

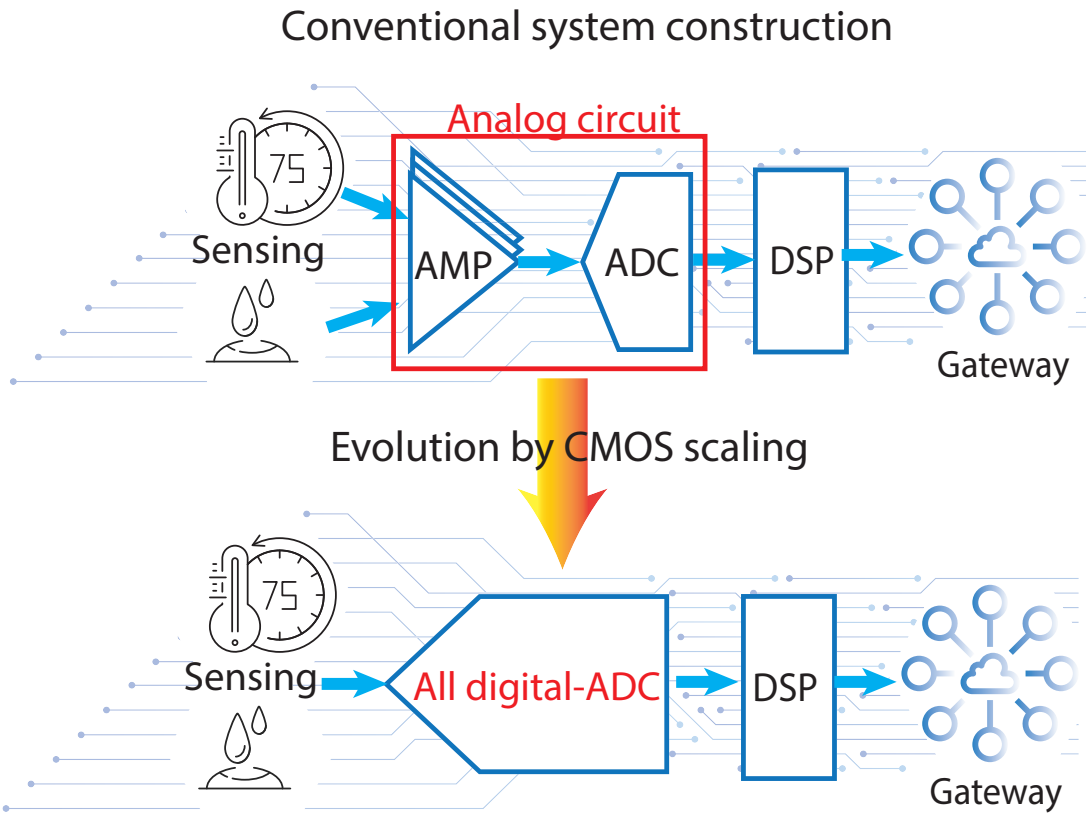

Figure 1.2: The comparison of IoT device in which conventional system construction and all digital sensor achievement in mixed signal circuit[2].

area and lower-supply-voltage. Although ring-VCO benefits from CMOS scaling by reducing the supply voltage(V_{DD}), Threshold voltage of MOSFET(V_{th}) is not significantly scaled down due to avoid high static power consumption from increasing leakage current of the scaled device [3]. Therefore, the challenge is to improve the linearity of ring VCO, which is characteristic of conventional delay elements and further degrades linearity at low operating voltage. Moreover, ring-VCO is implemented based on an inverter that cannot produce frequency from input voltage below the threshold voltage of the MOS transistor.

Our study expands AI algorithm on IoT device which is engaged with deep neural network (DNN). A deep neural network is fundamental to the architecture, and the Multiply-and-accumulate (MAC) operations are dominant which consumes nearly 99% energy in the DNNs. Approximating multiplier units are alleviating

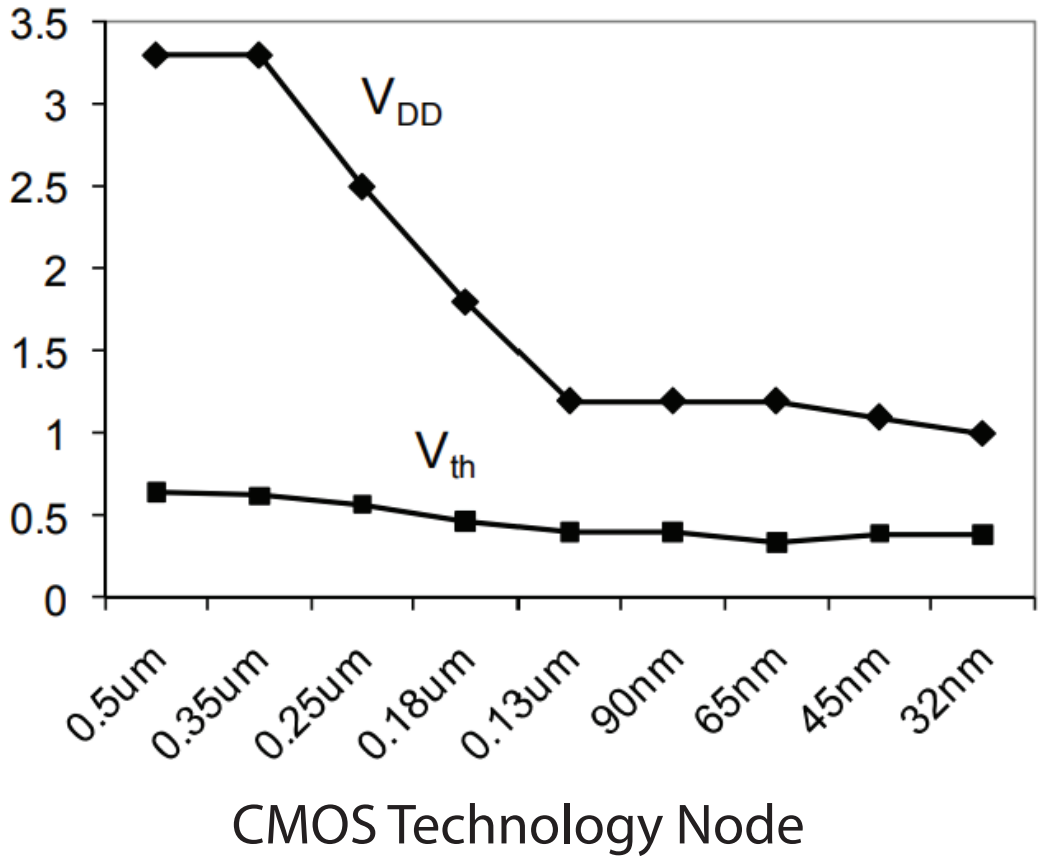

Figure 1.3: VDD and Vth scaling across various CMOS technology nodes[3].

energy-hungry and latency. The stochastic computing technology is one of the approximate computing strategies which represent data by the probability of 1 appearance in a long bit-stream as pulse. Therefore, Pulse-based information construct at DNN can alleviate power consumption in MAC operation.

1.2 Contribution

The main contribution of this thesis are shown in figure 1.4. In this work, we propose a novel voltage-to-current (V/I) conversion to improve the linearity of V-to-F tuning curve under low power supply condition. This provides for driving even-stage of the differential current-starved inverter-based ring-VCO-based ADC. We expand ring-VCO to establish the pulsed neural network. The merit of ring-VCO is that it performs analog-to-digital conversion along with classification by

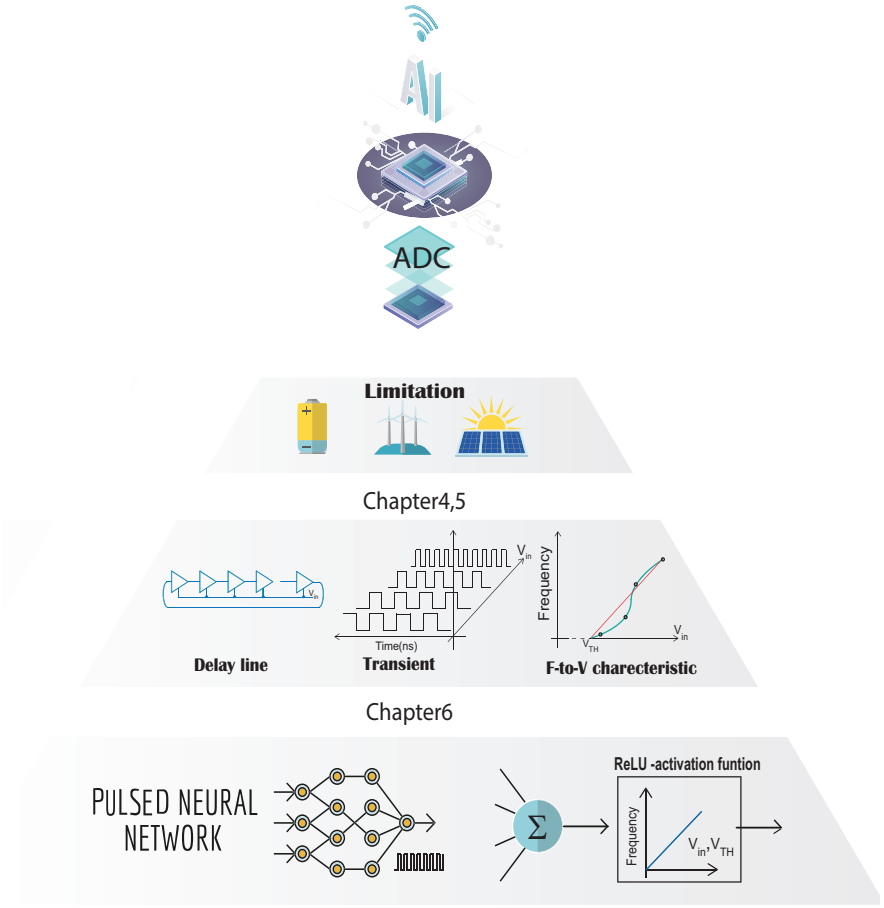

Figure 1.4: Overview contribution of thesis

Voltage-to-Frequency (V-to-F) tuning characteristics representing the ReLU activation function. The ReLU activation function is used for the mid-layer and the output layer of the pulsed neural network. Hence, the linearized technique is crucial for ring-VCOs' V-to-F tuning characteristics. Moreover, the pulsed neural network is adopted as AIoT, which has led the ring-VCO to operate at the lowest supply voltage in order to reduce its overall power consumption. The contributions are summarized as follows.

- A novel voltage-to-current (V/I) conversion to improve the linearity V-to-F tuning curve under low power supply condition. Which provides for driving even-stage of the differential current starved inverter-based ring VCO-based ADC.

- A novel current-starved pseudo differential delay element for ring-VCO with the objective of a simplified number of transistors.
- We explain detailed circuit implementation of the pulsed neuron circuit in which ring-VCO is applied in A/D converter data and its linearity of the ring VCO's V-to-F characteristic serving as ReLU activation function.
- Pulse-based multiply-and-accumulate (MAC) operations unit consists of AND gate and counter, which can perform positive and negative weight computation.
- We propose a compensation technique due to sub-threshold or near-threshold operation, the linearity of the ring VCO's V-to-F characteristics can be affected by the process variation.
- The pulsed neuron circuits are assembled as neural network to validate ring-VCO-based ReLU activation function and benchmark using the MNIST handwritten digits for classification.

1.3 Thesis Organization

The thesis is organized as follows:

Chapter-1 This chapter briefly discusses the background and motivation for the thesis and summarizes its contributions.

Chapter-2 Overviews of ring-VCO based ADC, linearity of V-to-F tuning characteristic, and pulse neural network are presented in this chapter.

Chapter-3 This chapter briefly discusses the related work which is involved in ring-VCO-based ADCs at low operating voltage, Linearity improvement technique and pulse neural network.

Chapter-4 This chapter presents a complementary bias voltage control approach to attain a linear V-to-F characteristics with low-power dissipation. The novel voltage-to-current (V-to-I) conversion provides the linear bias current source and sink matching for current-starved inverter-based delay elements. Furthermore,

the proposed circuit can be extended to optimize nonlinearity error by selecting an optimal transistor size.

Chapter-5 The ring-VCO relies on the current-starved pseudo-differential ring-VCO configuration in which a huge number of transistors occupy one delay element. This paper presents the novel current-starved pseudo-differential delay element, which has a decreased overhead transistor by 37.5% and sizing by 44.88% when compared with to previous work while not adversely affecting the linearity of V-to-F tuning characteristic.

Chapter-6 This chapter present a low power ReLU activation function for pulsed neural network. The proposed rectifier is based-on our linearity improved ring-VCO. Furthermore, our studies shows that nonlinearity is affected by process variation, and we discuss a compensation technique. These improvements are illustrated using simulation results of the proposed neuron circuit which is designed in 0.18-μm CMOS technology. The designed pulsed neuron circuit which can be used in DNN is benchmarked by MNIST performance.

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2
Background

This work involves in continuous-time (CT) $\Delta\Sigma$ VCO-based ADC. One of the key circuits for time domain analog processing is a voltage-controlled oscillator (VCO). Ring oscillator (RO) has emerged as a preferred building block for highly digital $\Delta\Sigma$ ADC and pulse neural network. An RO is built using inverters in a chain which generates binary pulse, which is then integrated to phase of its tuning analog voltage/current in time domain, but the limitation of ring oscillator is nonlinear. This chapter explains essential knowledge for three of our research topics. We describe ring oscillator, linearity and pulse neural network and get into more practical and relevant issues.

2.1 VCO-based ADC

The VCO-based ADC shown in figure 2.1 converts analog input to an output frequency. This frequency is converted to digital representation using the register and counter as determined by the total number of frequency pulse in the sampling period.

A VCO-based ADC in open loop is also known as Frequency Delta Sigma Modulator (FDSM) and VCO-based quantizer since the noise shaping takes place. The general structure of a VCO quantizer is illustrated in figure 2.2 (b) and (c) its

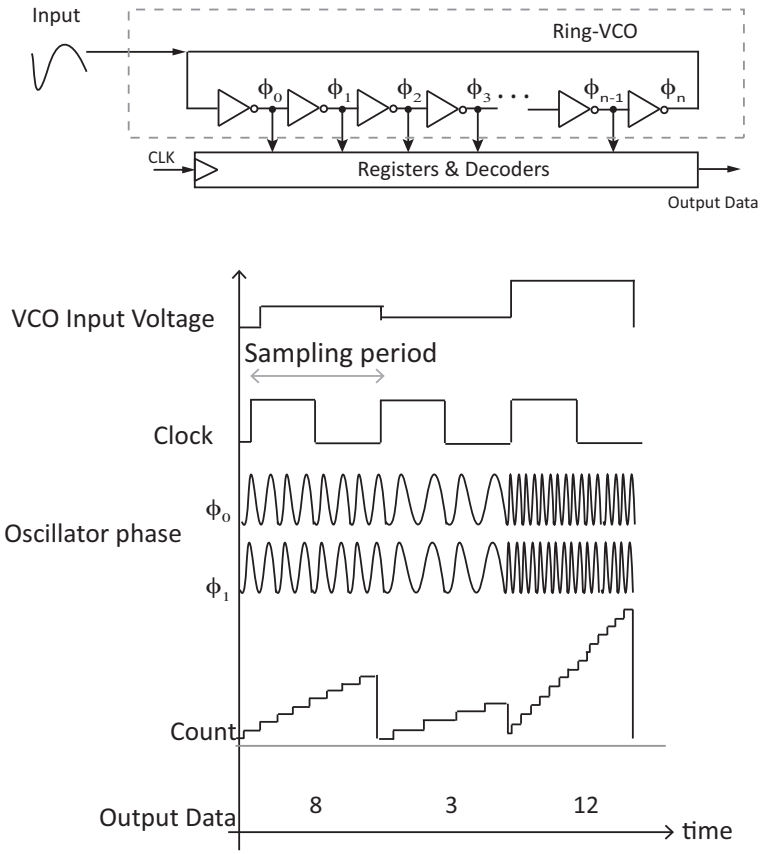

Figure 2.1: Block diagram of VCO-based ADC [1].

operation in detail is given in reference [1]. The VCO generate output binary pulse by the input voltage of X(z) conversion when the internal phase value of P(z) is equivalent to value 2πn including initial phase of P(o). The VCO output pulses of Y(z) are counted during a sampling period with reset pulse. A residual phase shift of final sampling period is the quantization noise Q(z), which is expressed by equation 2.1.

$$Q(\mathrm{z}) = P(\mathrm{z}) - 2\pi \mathrm{Y}(z) \tag{2.1}$$

Q(z) is assumed to be the initial phase shift for the following sample period, which is express by equation 2.2

$$Q(\mathrm{z}) = z^{-1} - Q(\mathrm{z}) \tag{2.2}$$

With initial phase shift, minus next phase shift for the succeeding sampling period,

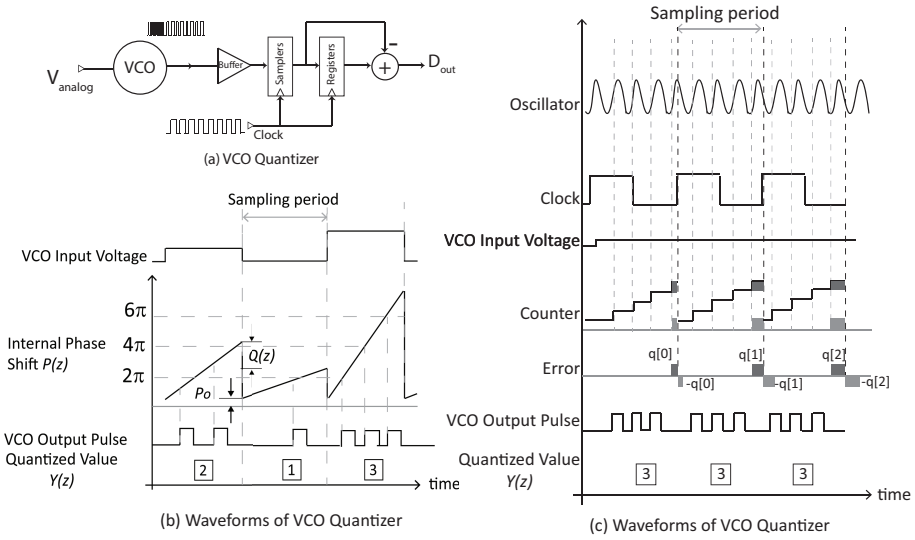

Figure 2.2: (a)Block diagram of VCO quantization and (b) its fundamental operation (c)its quantization[1].

we can obtain the quantization noise Q(z) which is shaped by the first order noise shaping filter as express by equation 2.3.

$$Y(\mathrm{o}) = (2\pi)^{-1} G\mathrm{v} X(\mathrm{z}) + (1 - z^{-1}) Q(\mathrm{z}) \tag{2.3}$$

where Gv is gain constant.

Figure 2.2(c) shows the principle in simplified form by examining the counting process of one phase of the oscillator with a constant input (V_{in}), the key point here is that the truncation error $q[k]$ at the end of a clock period boundary is not lost, but rather it is accounted for in the following measurement. Therefore, we find that the overall quantization error signal can be described by $Error[k] = q[k] - q[k-1]$ which reveals first-order noise shape.

2.2 Ring-VCO based ADC

The ring-VCO based ADC we have presented is an all-digital analog-to-digital converter (Time A/D converter: TAD) [2] which is a method of measuring both voltage signals and frequency signals (time interval signals). In other words, it combines both a voltage to digital converter and an ADC. A ring-VCO based ADC

consists of a ring delay-line (RDL) as shown in the pulse delay circuit within the figure 2.1(a) along with frequency counter, latch and encoder. This subsection explains essential knowledge and basic structure of ring oscillator and its linearity of V-To-F characteristics.

2.2.1 Ring-VCO topology

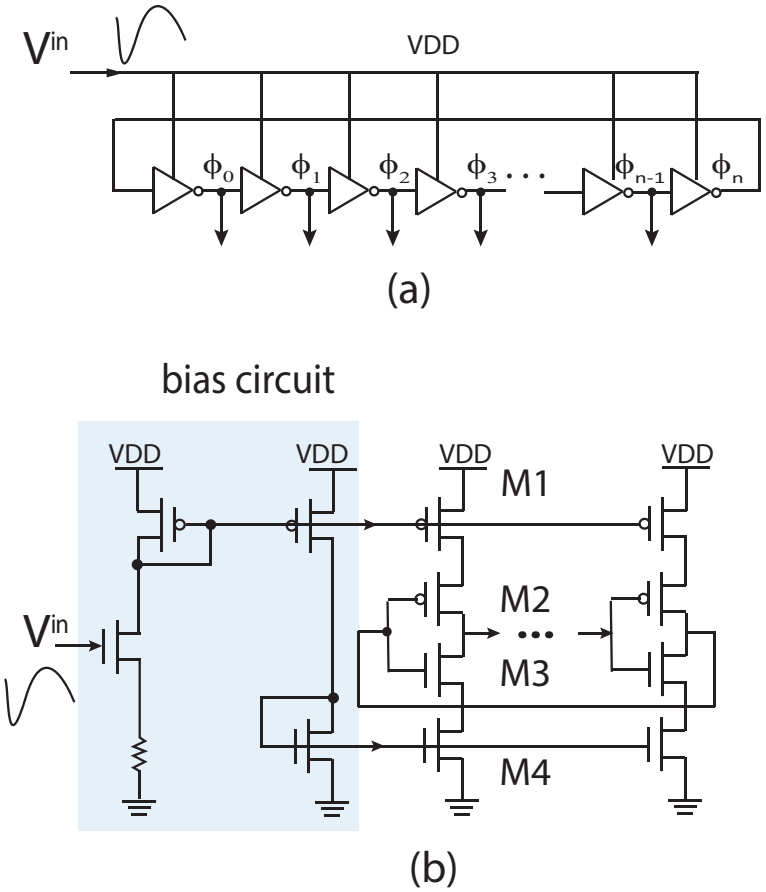

Figure 2.3: Block diagram showing the basic structure of a ring-OSC (a) inverter-based ring (b) current starved ring.

Inverter-based ring-VCO

Since the delay of an inverter is fed by the supply voltage (V_{DD}), the oscillation frequency f(o) is inversely proportional to V_{DD} in the inverter-based delay cell as shown in figure 2.3(a). This supply sensitivity, K(V_{DD}), is significant as noise on V_{DD} changes the output frequency directly. By utilizing differential rings, the issue

of supply noise can be significantly mitigated. The propagation time t_d of transition of signal through the complete chain determines the period of ring oscillator and is given by the equation (2.4) as

$$T = 2 \times N \times t(\mathrm{d}) \tag{2.4}$$

where N is the number of inverters in the chain. Therefore, the oscillation frequency is given by the equation (2.5) as

$$f_o = \frac{1}{T} = \frac{1}{2 \times N \times t_d} \tag{2.5}$$

Current starved ring-VCO

With reference to a current starved ring VCO the input voltage V_{in} modulates the pull-down resistor and pull-up transistor through a current mirror as shown in figure 2.3(b). A large input voltage allows large current flow. Current starved ring-VCO requires a bias NMOS current sink and PMOS current source to control its oscillation frequency. The advantage of this topology is that the oscillation frequency can be tuned for a wide range of input voltage.

The variation of input voltage (V_{in}) determines the frequency range and linearity of the VCO. However, a major drawback of this stage is longer rise/fall time when bias current is quite small because the voltage swing of the VCO becomes slower. The total capacitance on the drains of M1 and M4 is given as in equation (2.6).

$$C_{total} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n) \tag{2.6}$$

The oscillation frequency is determined by the bias current t_d, number of stages N, total capacitance C_{total} and input voltage $\mathrm{V}(in)$ as

$$f_{osc} = \frac{I_d}{2 \times N \times C_{total} \times V_{in}} \tag{2.7}$$

2.3 Linearity V-to-F characteristic of VCO-based ADC

The ring-VCO based ADC replaces the conventional analogue domain to all digital domain, and then the digital output is generated by frequency to digital converter (FDC). However, VCO has the disadvantage of nonlinearity VCO tuning curve. Voltage-to-Frequency relationship of VCO can be represented as

$$f_{osc} = K_{vco}V_{in}(t) + f_o \tag{2.8}$$

where VCO gain sensitivity K_{vco} is define as

$$K_{vco} = \frac{\delta f_{vco}}{\delta V_{in}} = \frac{f_{high} - f_{low}}{Vin_{high} - Vin_{low}} \tag{2.9}$$

Nonlinearity in the VCO tuning curve will result in harmonic spurs in the output spectrum due to nonlinearity of VCO gain sensitivity K_{vco} as shown in figure 2.4. These spurs will degrade the SNDR depending on the amount on nonlinearity of V-to-F characteristic [5].

The frequency of the VCO is directly related to gain sensitivity K_{vco}. If the gain or voltage-to-frequency relationship is nonlinear, which usually is the case, it will be described by higher order polynomial. Figure 2.5 shows an example of non-linearity behavior which obtains a small linearity range compared to their the rail-to-rail (0-VDD) input voltage. As the non-linearity is more severe in outermost section of K_{vco} curve one can maximize the linearity by using a limited range at the expense of a reduced SNR which is given by the equation (2.10).

$$f_{osc} \approx f_o + K_{vco}V_{in}(t) + kV_{in}^2 + ... \tag{2.10}$$

2.4 Pulse encoding

A *pulsed-based computation in VLSI Neural network* is defined as the usage of pulsed coding technique to represent the neural state and a weight value. Pulse

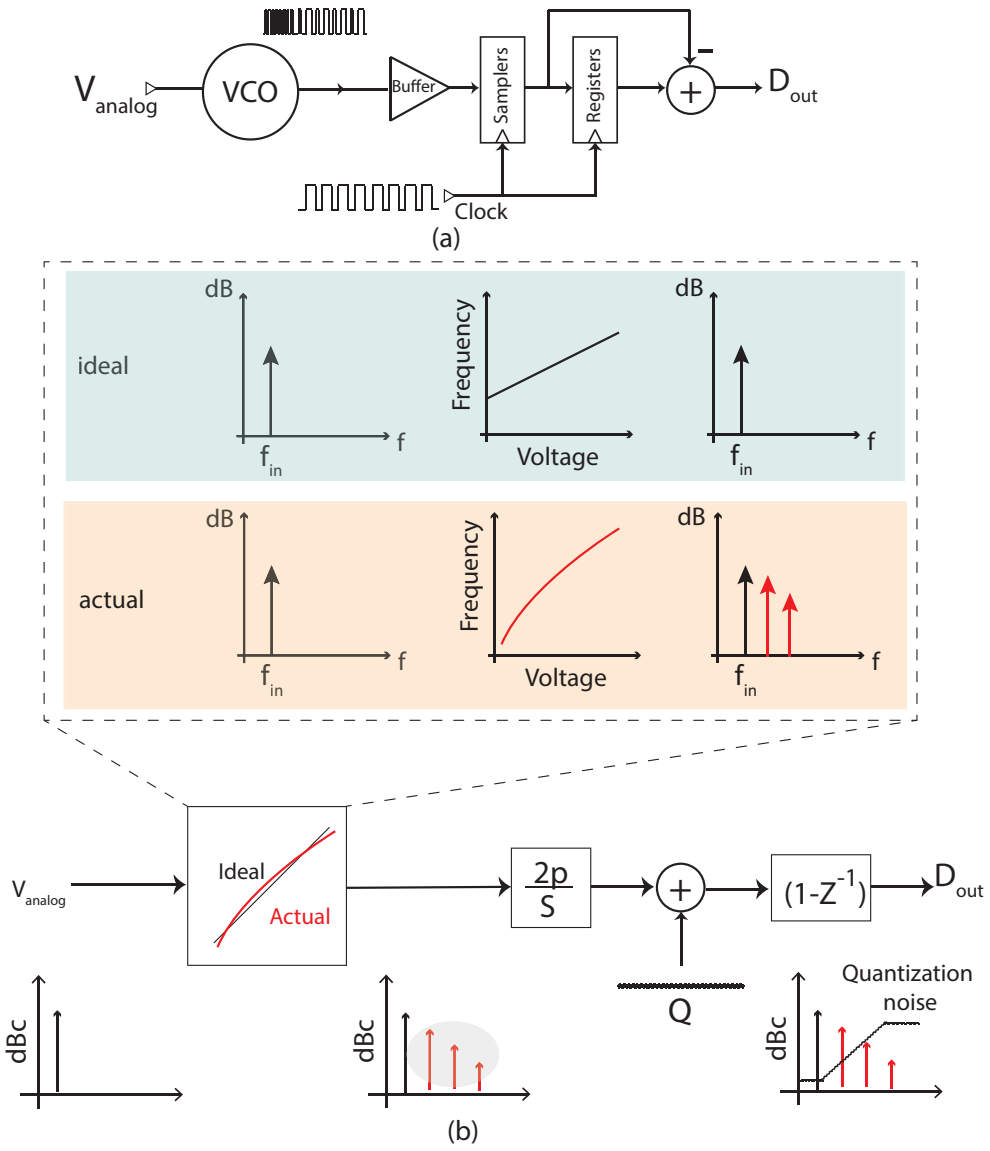

Figure 2.4: (a) Block diagram of VCO quantization (b) VCO nonlinearity in the output spectrum of the VCO-based quantizer [5].

stream encoding in the time domain is show in figure 2.8, it can be represented using several methods like

- Pulse Amplitude Modulation (PAM)
- Pulse width Modulation (PWM)
- Pulse Frequency Modulation(PFM) [6].

Next, we will describe them briefly.

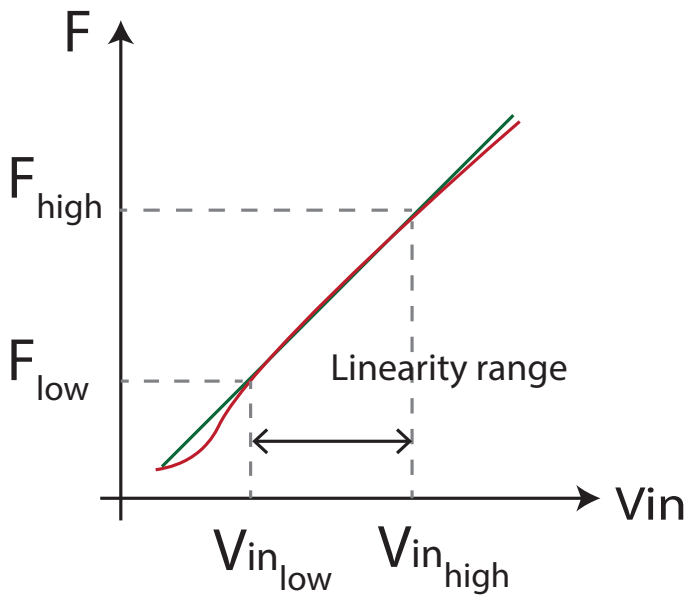

Figure 2.5: Voltage-to-Frequency characteristic of VCO.

Pulse Amplitude Modulation

Pulsed waveform amplitude represents the reflection of variation in V_i when V_i equivalent to amplitude of A_i multiply a constant frequency pulsed signal. This pulse encoding is not robust for long-range signaling in neural net.

Pulse width Modulation

The value of state V_i represents width of individual digital pulses in V_i. In this technique, no analog voltage signal is involved in the signal; thus, information is coded as described along the time axis. This pulse encoding is robust but complex. Some research notes that the PWM is equivalent to "time-to-first spike-code".

Pulse frequency Modulation

Pulse frequency modulation is the average pulse repetition rate. V_i represents the frequency of instantaneous digital pulses. Variable signaling frequency distorts both the leading and trailing edges of brain status signals and prevents excessive transient demand on supply lines. Therefore, the power requirement is averaged throughout time.

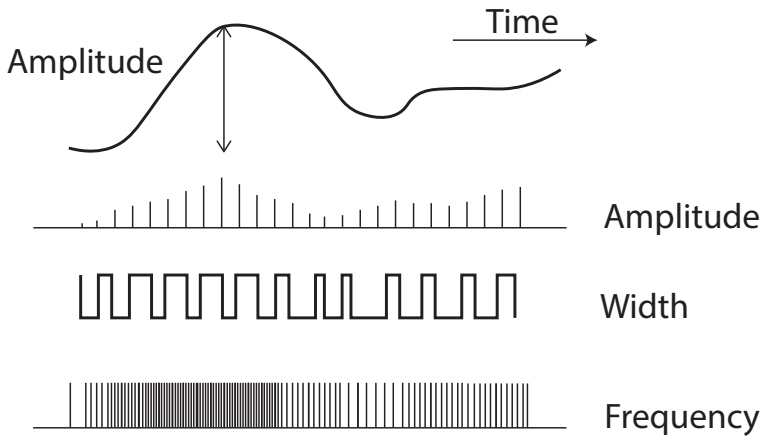

Figure 2.6: Modulation schemes that encode analog values as pulsed waveform[4].

2.5 Pulse neural network

In neuro-informatics[6] its fundamental has been represented by a set of elementary devices: adders, synapses, neurons, which are combined into networks for solving specific tasks. Pulse neuron models are an alternative to binary neuron models. The basic elements of the basis is the addition and multiplication operations.

Addition of Pulse signal

Pulse addition functions are represented by two technique which are (1) voltage pulse addition and (2) current pulse addition, and they are described as follows:

Voltage Pulse Addition This technique is based on logical OR between two uncorrelated pulse stream of fixed-width pulse or their density in time which is equivalent to addition of signal representations. This OR-based add function are thus distorted by pulse overlap, which can be estimated by very simple neural OR-based accumulator with N inputs. OR'ing pulsed signals together to form the add function assumes that the probability P_{out} given by the equation (2.11), i.e., the output of the OR gate is logical high, is given by the sum of the probabilities that the individual pulsed inputs are each high.

$$P_{out}(ideal) = \quad \sum_0^N p_n \tag{2.11}$$

Current Pulse Addition Current pulse addition is fully analogue, and it requires a simpler circuitry. The same consideration relating to the rate of occurrence of pulse overlap apply here. It is their consequence that are different. Current may be accumulated either as charge on a capacitor or via an active integrator, based on an operational amplifier circuit.

Multiplication of pulse stream signal

There are two generic approaches- pulse width modulation, and pulse height modulation. We will therefore discuss the surrounding issues within this framework. Synaptic gating was achieved by dividing time artificially into periods representing "chopping clock" in which synchronous form one to another but asynchronous to neural activation. In other words, clocks are introduced with the ratios between pulse width and period equal to 1:1, 1:2, 1:4, etc., to define time intervals during which input pulses may be passed or blocked. Multiplication takes place when the presynaptic pulse stream is logically AND gated with each of chopping clock enabled by the bits of weight and resultant pulse bursts OR gate together [6,7].

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3
Related work

In this section, we briefly overview recently related work that regards Analog CMOS implementation of ReLU activation on which analog circuit implementation and pulsed neural network implementation. This paper presents the VCO serving as ReLU activation; thus, linearity technique reveals our work.

3.1 Linearity improvement technique

atanabe et al. proposed basic VCO based ADC which consists of a ring-delay-line (RDL). The ADC circuits were implemented using digital circuit components only, and the supply voltage to the delay line were directly controlled [1]. Applying 2^n stage delay elements for RDL, pulse position in the RDL, which corresponds to phase of the oscillation, directly indicates additional lower bits. However, since the delay was controlled using supply voltage, non-linearity was not essentially improved.

For the delay control of RDL in the VCO, a current-starved inverter is used which is a well-known technique to realize delay elements with current tuning by transconductance. However, the delay elements rely on stacking MOSFETs, whose structure decrease the input voltage range, resulting in difficult low voltage operation. Therefore, the design of current-starved delay element at low nominal

voltage supply degrades its linearity in the sub-threshold region. In contrast, linear operation of the current-starved inverter is challenging, which is related to both the linearity in V-to-F conversion and the wide tuning range of the current-starved inverter-based ring-VCO. In general, an inverter-based delay element suffers from non-linearity due to the relationship between input voltage (i.e., either the source voltage as its power supply voltage or gate voltage) and delay. Moreover, if a VCO-based ADC is designed as an open-loop architecture, where there is no need for DACs, it may result in poorer VCO linearity. Thus, the researchers developing VCO-based ADCs using open-loop architecture, in addition try to suppress non-linearity. Different approaches have been proposed both at an architecture level, for instance, digital calibration [2] and two identical pseudo- differential VCO-based ADCs, and a digital subtraction for distortion cancellation [3].

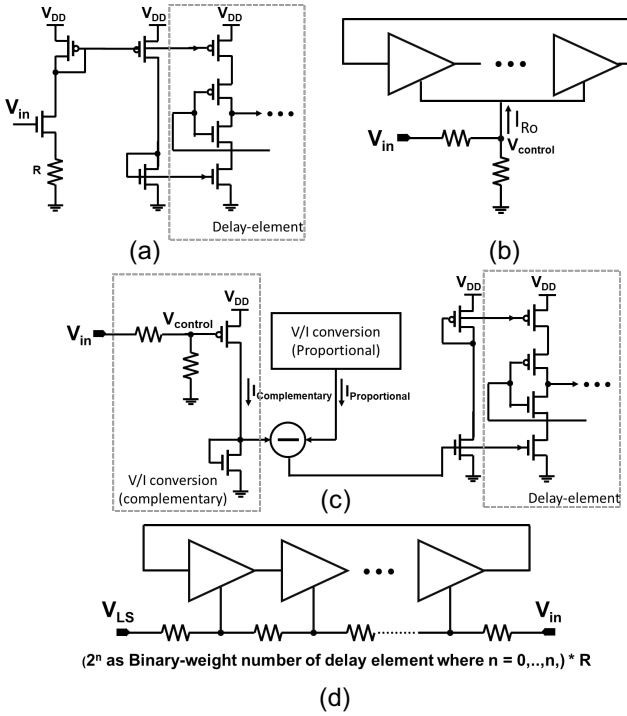

Figure 3.1: Linearity improvement techniques: (a) Conventional voltage-to-current converter for current-starved inverter [6]. (b) Voltage-to-current conversion by using resistance [7, 8]. (c) Linearized current control mechanism [9]. (d) Scaled resistance network at their input [10].

The proposed linearization technique at the circuit level tends to mitigate additional circuits, resulting in small area realization. With reference to circuit

approach, researchers have been exploring several techniques based on the controllable current ring oscillator. The preliminary approaches can be categorized into two groups according to the modified inverter-based delay element and additional resistance. Voelker et al., presented a break-before-make delay cell using five-stacked series transistors [4]. The modified delay elements generate synchronized waveform using controller signal and are applicable to reduce the short current for linearity improvement. Alvero-Gonzalez et al. [5] proposed a new delay model consisting of two parts. In their proposed design, first, the supply-controlled inverter-based delay element requires to increase voltage-controlled current source. Therefore, they use the second part which consists of two inverters-based delay elements as the buffer with nominal supply voltage in cascade. Additionally, their study has further discussed about obtaining higher linearity in V-to-F characteristic of their modified delay model depending on the highly linear input current. To generate the linear current, they apply additional resistance-based method, and this is beneficial for differential inverter-based delay elements and current-starved delay elements in nominal supply voltage. The baseline case of a conventional linearity in voltage to frequency conversion of the current-starved VCO whose ring-VCO requires a highly linearized biasing current source for its supplement due to characteristically degrading linearity of the delay cell. The current-starved VCO [6] compensated its linearity of V-to-F characteristic by using a resistor, as shown in figure 3.1(a), and the current is related to the input voltage. However, this operation neglects input voltage range in the sub-threshold region. References [7, 8], discuss a compromised current control and voltage control technique which enables the current source in the ring oscillator to be linear. Figure 3.1(b) shows the proportional resistive input circuit which converts the input voltage to current depending on bias current. Likewise, [14] played a role in determining non-linearity, which affects the current source flowing through the ring oscillator. Consequently, the linearized control mechanism has been established, as shown in figure 3.1 (c), by subtracting proportional resistive voltage-to-current (V/I) conversion with complementary behavior. The bias current serves the current mirror technique,

which may affect the phase noise performance of the current amplifier. However, many linearity enhancement strategies have been motivated by the current-starved circuit in which bias current is served based on the current-mirrored technique, as shown in figure 2 (a) and (c). Considering the bias circuit is affected by various transistor operations with the input voltage, the nMOSFET could perform inefficiently in the triode region. In contrast, the pMOSFET maintains operation in the saturation region by the given high input voltage. At the same time, the nMOSFET requires to relieve the saturation region until input voltage is corresponding to the supply voltage. Thus, the operation region of those transistors could influence the linearity of ring-VCO. As far as we know, no approaches have been presented apart from serving the biased current source and sink realization using a current mirror.

AL-Tamimi et al., in contradiction to [9], presented a binary pre-weighted resistor network connected between the input which adjusted the voltage at every delay element [10]. Figure 3.1(d) shows the circuit where resistance values are increased exponentially based on the number of stages. Hence, accumulating different time delays are attained to correct the amount of time delay, using which linearity transfer curve can be expanded over rail-to-rail input. This circuit suffered from a huge area and power consumption; however, the author presented an alternative pre-weighted resistance network called inverse R-2R [11]. The topology is equivalent to a prior art [10] with some modifications, which have resistors with constant value. Although this approach improved power consumption efficiency and the area when compared to prior art, but it increased the nonlinearity error percentages. A.Steven et al. [12] presented a method which would increase the linear frequency range of the current-starved ring-oscillator by adding a floating-gate transistor at the input stage. The floating-gate transistor can extend the linear current starved region, whose saturation region limits current to be zero or negative voltage. According to the existing literature on current starved ring-oscillator, the identical bias current throughout the stages is served by the current mirror for

the current source and the sink, which may affect the phase noise performance of the current amplifier.

Unlike above methods, reference [13] utilized a simple current-starved VCO with current sink, i.e., NMOS-starving transistor. In their proposed approach, the limitation of linear voltage range for current sink transistor is caused by less current flowing through the ring-oscillator in the ohmic region in which oscillator gain is limited because of the transconductor. Thus, it cannot remain the oscillator frequency with the same slope as in the saturation region, as shown in figure 3.2(a). Their configuration is realized by several NMOS-starving transistors connected in parallel with different bias conditions, as shown in figure 3.2(b).

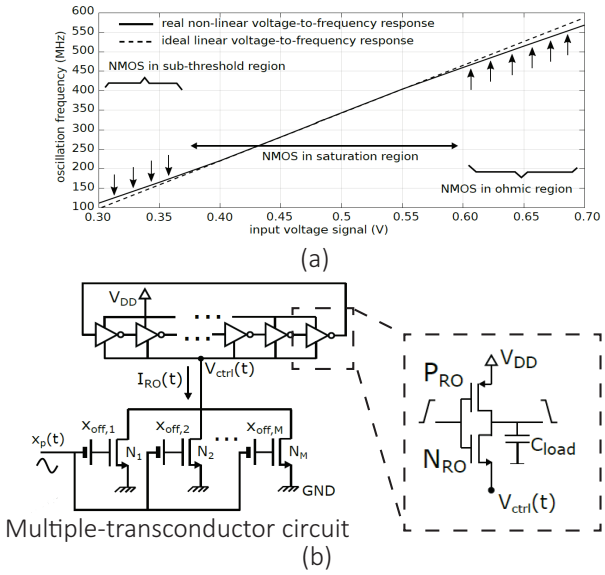

Figure 3.2: (a) Voltage-to-frequency conversion function (b) multiple-transconductor circuit for a linear ring-oscillator-based analog-to-digital conversion.[13].

G. Rui et al. [14] proposed a conventional LC-VCO with a varactor resonant tank composed of four identical MOS varactor pairs whose proper input bias voltages are optimized linearly by multilayer perceptron (MLP) algorithm. In their design, the MLP algorithm utilized the ReLU function as an activation function to improve the linearity of VCO. Due to the requirement of ultra-low-power consumption, the ring oscillator supply voltage is reduced by technology downscaling below 1V.

A-F. Javad et al. [15] proposed the design of a ring oscillator in 28-nm Fully Depleted-Silicon-On-Insulator (FD-SOI) CMOS technology. FD-SOI MOS devices provide a back-gate in order to enhance the body effect in bulk-CMOS. Moreover, FD-SOI results in a higher linear relationship between the threshold voltage and the bulk (body) voltage MOS transistors. Hence, their proposed ring oscillator, implemented using current-starved inverters that provide an input voltage as body bias, they achieve a wider linear tuning curve of the V-F characteristic in the threshold region.

The studies of ring-VCO, as mentioned above, have focused only on one established linearization technique. Some of these works suffer from the area and power consumption from a low power device point of view. Furthermore, those proposed techniques cannot provide ring-VCO for operation at a supply voltage below 1V. Our approach proposes a solution that can be categorized as a circuit technique for linearity improvement of ring-VCO at low power supply voltage, and it is suitable for serving as a ReLU activation function unit.

3.2 pulse neuron circuit

In recent years, pulsed neuron circuits have been presented using an analog-mixed-signal technique to improve energy efficiency and latency on neural network circuits. Whilst some research has been carried out on pulsed neural network with sigmoid-shape nonlinear function, there are a few published studies that present pulsed neural networks comprising ReLU activation circuits.

According to Sigmoid activation function, R.Zhang et al. [16] proposed Neuron-MOS mechanism. Input of neuron circuit is input voltage then generated oscillation frequency by VCO. The pulse frequency was turned to current by chopper circuit along with multiply current weight from current mirror part then whole current accumulate with the connected point. The result from MAC will be input to the continue state machine for Sigmoid function as shown in figure 3.4 (a). Their proposed continued state machine provide Sigmoid function programable which can adjust the nonlinearity curve.

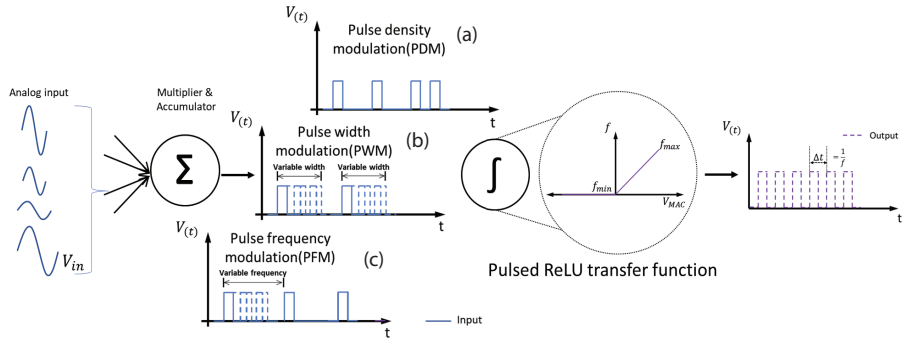

Figure 3.3: Characteristic of (a) pulse density neuron, (b) pulse width neuron, (c) pulse frequency neuron with operation of pulsed ReLU activation circuit, and its transfer function curve.

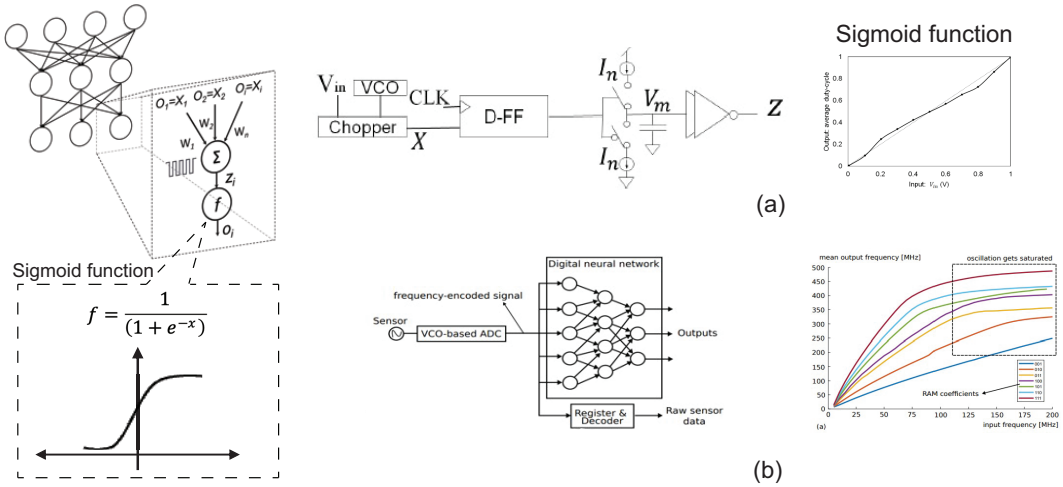

Figure 3.4: Pulse neuron circuit with sigmoid activation function by (a) continue state machine[16], and(b) PMAC architecture[17].

E.Gutierrez et al.[17] proposed phase-encoded MAC circuit (PMAC) in which provide by VCO-based ADC as shown in figure 3.4 (b). And Their proposed activation function of neuron circuit is benefit non-linear frequency response from ring-VCO characteristic in PMAC circuit serving as Sigmoid function.

B. Mohammad et al. [18] proposed a timed-based perceptron, which consists of the four-quadrant vector-by-matrix multiplier to perform Multiplication-and-Accumulation (MAC) operations realized by capacitance matrix. Those capacitors continuously integrate the current charge and produce the capacitor voltage until it reaches the maximum threshold voltage. Consequently, the voltage crossing

threshold converts the pulse-duration-encoded output. Their proposed pulse code generation scheme is like the pulse width modulation technique, as shown in figure 3.3 (b). The maximum weight value is assigned by the corresponding maximum current, while the smallest currents specify the weight value to zero. Therefore, the ReLU activation circuit determines frequency output from converting a pair of different pulse width output voltage into a pulse frequency output by two S-R latches. However, their work has not discussed on linearity characteristic of the ReLU function. In addition, the configuration was implemented on the 55-nm process with embedded NOR flash memory technology to achieve the pipeline operation.

In 2020, a new approach of PWM (pulse-width modulated)-based perceptron was presented by M. Sergey et al.[19],as shown in figure 3.5(a), to overcome the dynamic supply variation in an analog implementation operated under unreliable power supplies. Their configuration consists of weighted PWM accumulation and voltage to PWM converter serving as ReLU activation function. Their proposed weighted PWM accumulation is realized with a NAND gate, resistance, and output capacitance for resulting in voltage accumulators (VACs) to be PWM's input voltage on which the size of passive components affecting their energy efficiency. Their proposed ReLU activation circuit is realized with a single-ended ring oscillator. The variant of duty cycle value depending on voltage accumulation is provided by different supply voltages. The duty-cycle to-voltage transfer characteristic are discussed on ReLU function. In addition, R-square is used to estimate the linearity error of the ring oscillator.

X. Zhang et al.[20] presents the current controlled oscillator (CCO) with the time-to-digital converter (TDC) to function as a neuron. Figure 3.5(b) shown oscillation frequency of the CCO which feed by the current input from the synapse array. The current-to-frequency tuning characteristic, like the ReLU activation function, serves as custom activation. Their proposed study is emphasized on low-power and low-area CCO circuits for neuromorphic applications than linearity improvement.

The previous related work indicated the voltage-to-pulse transfer characteristic. One study has not discussed the transfer characteristic of the ReLU function, which

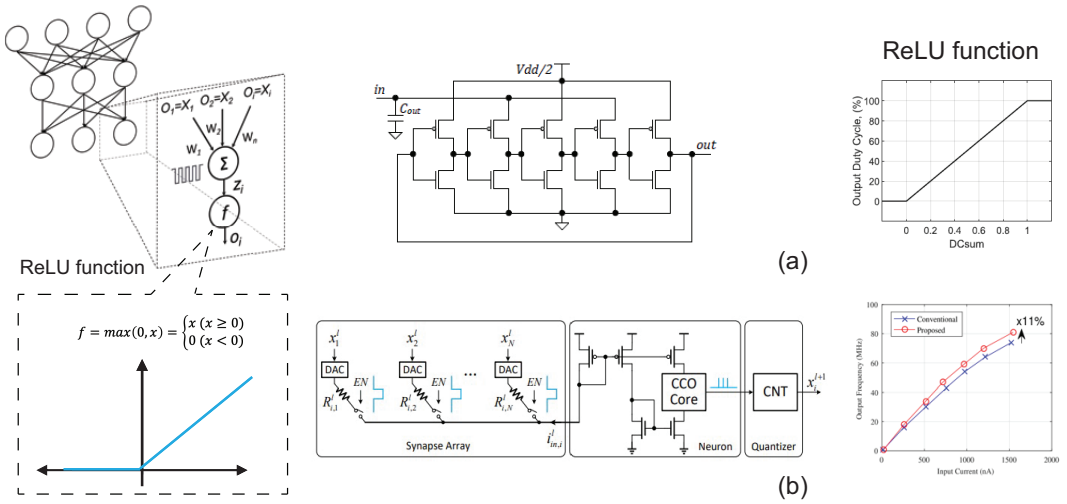

Figure 3.5: Pulse neuron circuit with ReLU activation function by (a) PWM-based perceptron[19], and(b) current controlled oscillator[20].

is PWM (pulse-width modulated)-based perceptron implementation proposed by D. Kilani et al.[21]. Their proposed Multiply-and-Accumulate (MAC) units rely on an analog-mixed signal in-memory computing approach that utilizes a cross-coupling capacitor processing unit (C3PU). The output voltage of C3PU is transferred into the pulse width signal by the voltage-to-time converter (VTC) circuit, then determined output by the ReLU function. The ReLU function circuit consists of the conventional logic gate, which determines pulse widths of the output signal, either positive or zero, by its pulse width subtraction.

In all the pulse neuron studies reviewed here, MAC operations provided by PWM technique, and ReLU circuit is distinguished output value by the pulsed frequency value. Although the linearity is important for ReLU activation implementation, it is apparent that a few studies concentrate on linearity improvement of the ReLU activation circuit. In addition, the ReLU activation circuits of previous works operate in nominal supply voltage.

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4

Linearity Improvement of Ring-VCO by using Complementary Bias Voltage Control

4.1 Introduction

Recently there is an increased interest in smart devices, and this has resulted in development of embedded sensing applications for healthcare, home automation and transportation. The smart sensors used in the IoT devices, rely on energy provided by batteries or energy harvesters, and connect billions of edge devices in a multidisciplinary paradigm via wireless communication. Additionally, IoT devices are expected to have long operational lifetime. An ideal design objective when developing such a sensor is ultra-low-power operation, and at an implementation level this is realized by using energy-efficient circuits for both communication and computing part [1]. For data acquisition, analog-to-digital converter (ADC) is indispensable, and is utilized in the preprocessing stages as analog interface circuits[2].

Continuous-time (CT) $\Delta\Sigma$ ADC has proven to be a great candidate for IoT edge devices [3]. Their advantageous properties include simplicity in circuit implementation by removing the sample/hold circuit with continuous sampling in each sampling period. Furthermore, this continuous sampling generates anti-aliasing

characteristics, and it can even make analog pre-filter dispensable. VCO based ADC is one of the CT $\Delta\Sigma$ ADC, because the VCO and the counter performs continuous integrating pulse density in each sampling period while frequency counting, and reuse phase condition of the VCO as the quantization error for the next conversion. Ring-VCO is important part of VCO-based ADC and is composed of a chain of inverters or delay elements, where an analog input is continuously converted from voltage to frequency.

In VCO based ADCs, power dissipation is an issue, because high frequency oscillation increases power dissipation of its delay elements and counter. Also, the linear V-to-F tuning characteristic is important for VCO based ADC design because high linearity can directly achieve lower harmonic distortion with high signal-to-noise-ratio (SNR) and signal-to-noise-distortion-ratio (SNDR). However, V-to-F tuning gain of ring-VCO has some non-linearity. Particularly, for low power operation with low voltage supply, the linearity further degrades because of characteristics of delay elements. The current-starved delay element is well-known as part of the VCO for the frequency tuning by transconductance. Optimal current control in low-voltage supplies may improve the linearity of VCOs with low power operation. Therefore, in this thesis we propose a novel voltage-to-current (V-to-I) conversion to improve the linearity V-to-F tuning curve under low power supply condition. This provides for driving an even-stage of the differential current starved inverter-based ring VCO-based ADC. Following are our main contributions:

- Low power supply and low leak-current V/I converters for current source/sink using a negative-feedback transconductance amplifier without body-bias technique.
- Linear bias current sink and source matching for ring-VCO replacing the current-mirrors with bias current mismatch due to its variable gain in sub-threshold operation.
- Simplify the methodology for optimization of transistor sizing in the proposed circuit.

4.2 Proposed ring-VCO with linearity improvement

4.2.1 Linearity improvement under ultra-low supply voltage

The ring-VCO which is voltage-controlled delay cell, may not be substantially improved linearity of V-to-F tuning characteristic. The current-starved ring-VCO is current-controlled delay cell which input voltage is converted to current by voltage-to-current converter. The current starved VCO in which oscillation frequency linearly varied with linearized biasing current source for its supplement.

By this motivation, many design strategies have been served with bias current based on the current-mirrored technique. Considering the bias circuit is affected by various transistor operations with the input voltage, the nMOSFET could perform inefficiently in the triode region. In contrast, the pMOSFET maintains operation in the saturation region by the given high input voltage. At the same time, the nMOSFET requires to relieve the saturation region until input voltage is corresponding to supply voltage. Thus, the operation region of those transistors could influence the linearity of ring-VCO[5]. As far as we know, no approaches have been presented apart from serving the biased current source and sink realization using a current mirror.

With the demand for low-power (battery-operated) applications, there is a dilemma between linearity improvement and power dissipation reduction. Since input voltage in weak and moderate inversion leads to non-linear bias current. The bias current yields the drain current which is computed exponentially as shown in equation 1[6].

$$I_D = I_{bias} = \frac{2K'W}{L} \cdot \left(\frac{nkT}{qe}\right)^2 \cdot exp\left(\frac{q(V_{GS}-V_{th})}{nkT}\right) \tag{4.1}$$

Where, n is the sub-threshold slope factor, k is the Boltzman constant, q is the electronic charge, V_{th} is the threshold voltage and T is the temperature.

To realize linearity improvement in low supply voltage operation, we propose a novel complementary biasing voltage technique for current-starved inverter-based ring-VCO, as conceptually shown in the block diagram of figure4.1. The complementary bias voltage control scheme combines two V/I conversion circuits for the current source and the current sink; which is described in section 4.2.1 provides the required linear biased current matching. Furthermore, both V/I conversion circuits simultaneously convey input voltage (V_{in}), i.e., control voltage, to current, preventing nonidentical region operation. The proposed current-starved inverter-based delay element configuration is described in section 4.2.2 Besides, emphasizing linear bias current can improve the linearity of V-to-F characteristics. The bias input voltage of the V/I converter can minimize nonlinearity error by finding the optimal size of the transistor as described in section 4.3.

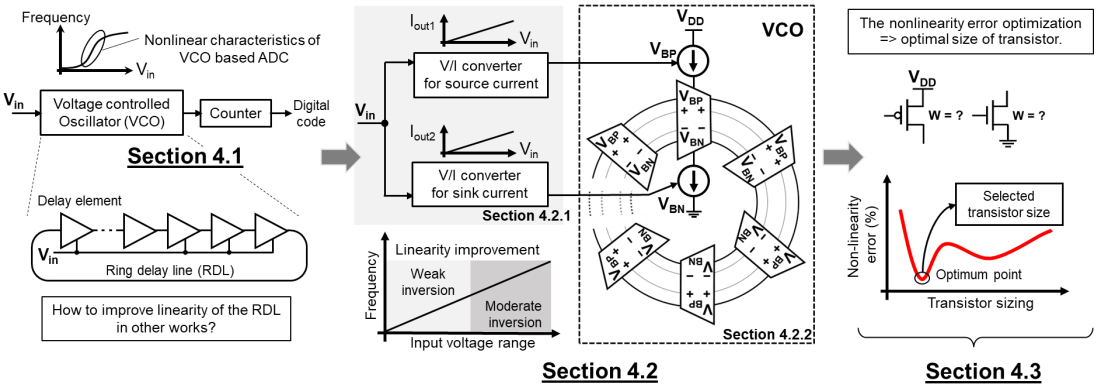

Figure 4.1: Conceptual block diagram of complementary bias voltage controls for linearity in voltage-to-frequency tuning characteristic improvement in weak and moderate inversion input range.

4.2.2 V/I conversion topology and its operation

The schematic of the proposed complementary bias voltage control approach is shown in figure 4.2. The main circuit relies on a transconductance amplifier with

a negative-feedback loop through a common-source amplifier. However, the ultra-low-power supply restricts circuit configuration due to its current flow limitation. We apply a pseudo-differential amplifier which simplifies the number of transistors and minimizes power dissipation resulting in a low supply voltage operability. This configuration lacks a tail current; it degrades common-mode rejection ratio (CMRR) by increasing common-mode gain of pseudo-differential circuits. However, our designed amplifiers maintain negative common-mode gains (maximum common-mode gain, in figure 4.2(a) $-8.7dB$, (b) $-30dB$). Thus, we can ignore the disadvantages of pseudo-differential amplifier.

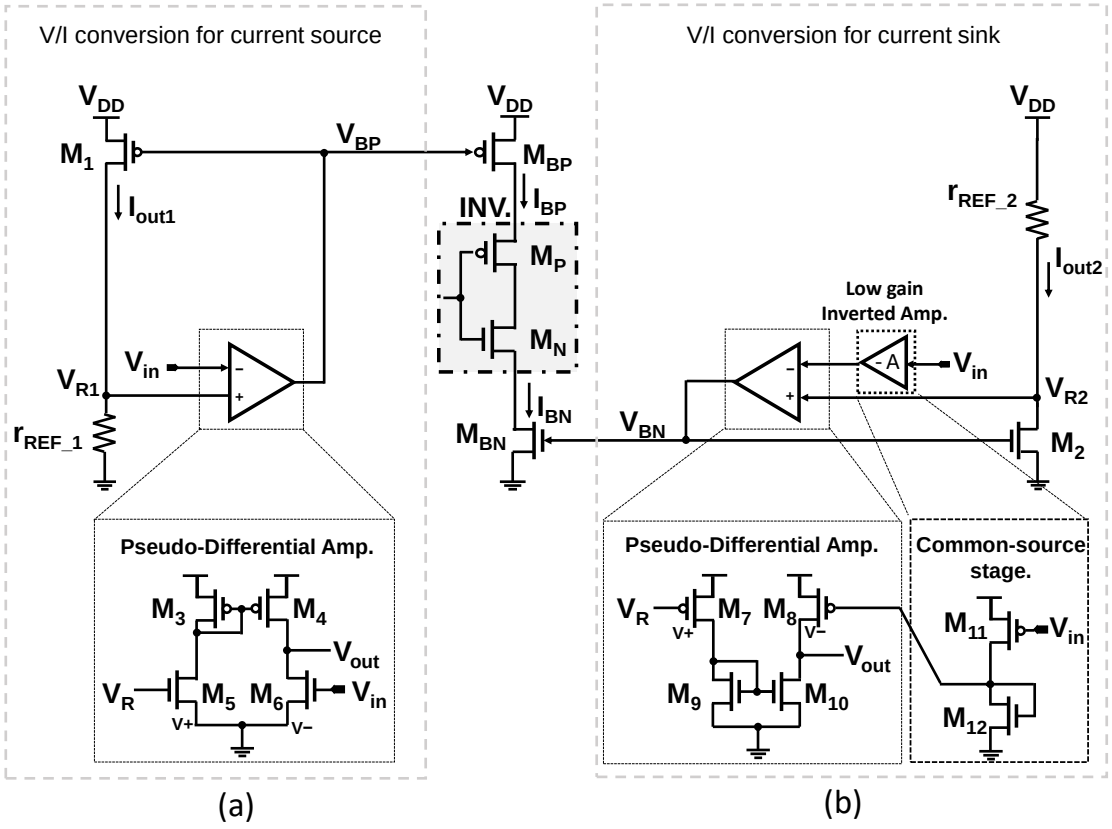

Figure 4.2: Schematics for the proposed V/I, (a) Current source and (b) Current sink: Generate bias voltage and replica- biased current for current-starved inverter-based ring-VCO.

In the source-side V/I converter (in figure 4.2(a)), negative feedback loop controls gate voltage of M_1 for leading V_{R1} is close to V_{in}. Thus V_{R1}, which is nearly equal to V_{in}, is given to r_{REF_1}; I_{out1} along with the V_{in} can flow. On the other

hand, in the sink-side V/I converter (in figure 4.2(b)), since I_{out2} is based on the current of r_{REF_2} with $V_{DD} - V_{R2}$, if V_{R2} is along with V_{in}, will result in reverse current. Therefore, in our sink-side V/I converter design, we apply the low gain inverted amplifier with diode-connected nMOSFET for inverting V_{in}. This is not reverse current but also reverse the output voltage of pseudo-differential amplifier. The simulated result of output voltage of V/I current sink which are defined as V_N and output voltage of V/I current source as V_P, respectively, and illustrated in figure 4.3. Before adding the inverted amplifier, output current V_N decreases along with the V_{in} like V_P. However, after inverting V_N increase along with the V_{in} and reverse direction with V_P.

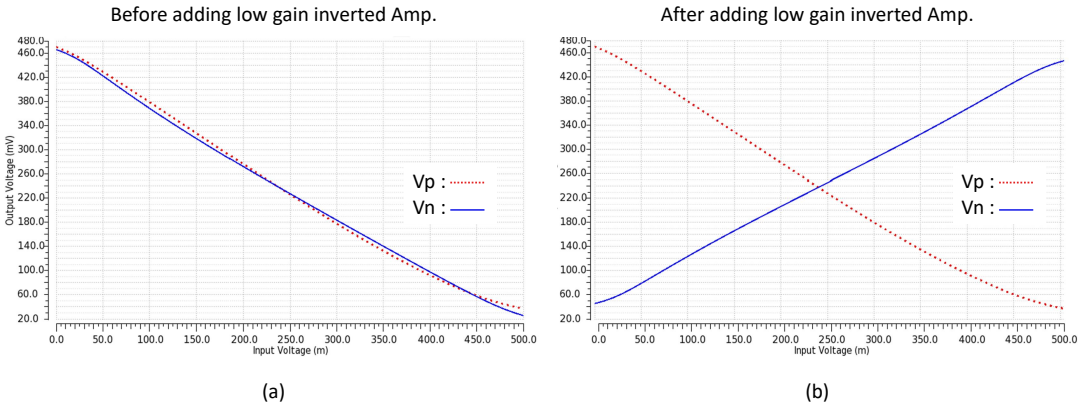

Figure 4.3: Simulation results of output voltage characteristic of $I_{P,N}$ variation over input voltage range. (a) Before adding low gain inverted amplifier and (b) after adding low gain inverted amplifier.

On the other hand, in case of output current, the simulated result of absolute current (I_{out1}) with a corresponding current value of I_{out2} illustrated in figure 4.4. Before adding the inverted amplifier, absolute current I_{out2} decreases along with the V_{in}. However, after inverting V_{in}, I_{out2} increases along with the V_{in} like I_{out1}. Proportional V_R can cause a linearized current through r_{REF}, which is approximately given by equation 4.2.

$$I_{out1,2} \approx \frac{V_{R1,2}}{r_{REF\_1,2}} \tag{4.2}$$

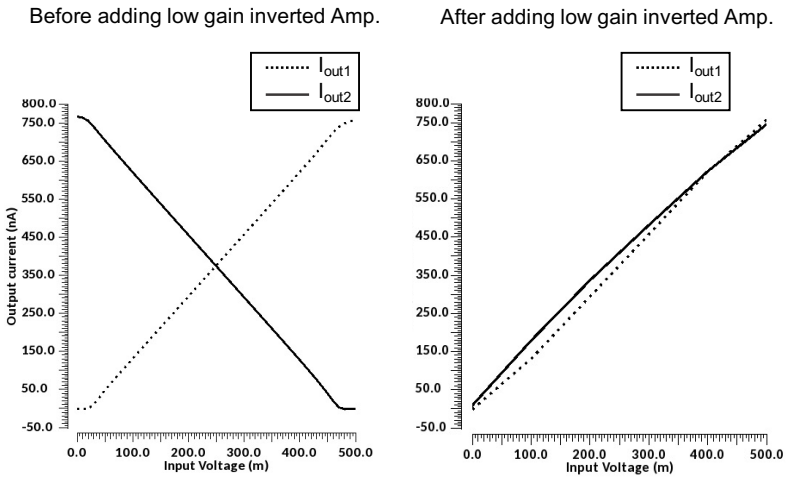

Figure 4.4: Simulation results of output current characteristic of $I_{out1,2}$ variation over input voltage range, (a) Before adding low gain inverted Amp. and (b) After adding low gain inverted Amp.

Relationship between V/I conversion and delay time

The operation of those V/I conversions can be performed as a replica-biasing circuit. The conceptual operation and the schematic of the single current-starved inverter are illustrated in figure 4.4, V_{BP} and V_{BN}, which are generated by negative feedback networks, are given to current source (M_{BP}) and sink (M_{BN}). Consequently, I_{out1} (I_{out2}) behaves identical to current source. In particular, the values of both sides are similar; thus, the load of M_{BP} (M_{BN}) is the equivalent value of $r_{REF\_1,2}$. The inverter sandwiched between M_{BP} and M_{BN} behaves like a switch limiting the current I_{BP} (I_{BN}).

The propagation delay of the delay element is controlled low-to-high (T_{plh}) and high-to-low (T_{phl}) transient times by a current source and sink [[12]], and can be expressed as:

$$\begin{aligned} T_{plh} &= \frac{C_{eff} V_{trp}}{I_{BP}} \\ T_{phl} &= \frac{C_{eff}(V_{DD} - V_{trp})}{I_{BN}} \end{aligned} \tag{4.3}$$

Where C_{eff} is the effective load capacitance of each inverter stage, V_{DD} is the supply voltage, and V_{trp} is the inverter trip voltage.

Even though we apply the constraints of ultra-low-power supply, the proposed V/I conversion can provide sufficient current source and current sink (in other words

$I_{BP} = I_{BN}$=I_{Bias} (bias current)); and therefore, the overall propagation delays can nullify V_{trp}. This can be expressed as:

$$T_{plh} + T_{phl} = \frac{C_{eff} V_{DD}}{I_{Bias}} \tag{4.4}$$

Hence, the frequency oscillator of ring-VCO is inversely proportional to sum of propagation delay of n-stage delay elements and is given by

$$F_{osc} = \frac{I_{Bias}}{n(C_{eff} V_{DD})} \tag{4.5}$$

As far as near-threshold voltage condition is concerned, the current-starved inverter operates in the sub-threshold region; therefore, the delay is assumed by corresponding to the resistance of the current source (R_{BP}) and current sink (R_{BN}) along with the inverter ($R_{P,N}$) in each stage, which can be written [8] by

$$T_d \propto (R_{BP,BN} + R_{P,N}) * C_{eff} \tag{4.6}$$

In particular, the nonlinearity of V-to-F tuning characteristics caused by bias current is inefficient in the sub-threshold operation. As mentioned earlier, the proposed V/I converters replicate their linearized output current as biasing current of current-starved delay elements, where the transistors are approximately equivalent as corresponding reference resistors $r_{REF\_1,2}$ which are constructed as feedback network. Therefore, this study has utilized this characteristic and the resistance behavior of current-starved delay element in sub-threshold operation to improve the linearity V-to-F tuning characteristics of ring-VCO.

4.2.3 Pseudo-differential ring-VCO

Figure 4.5 shows circuit configuration of the proposed ring-VCO, which consists of two main current-starved inverters and two auxiliary current-starved inverters which adjust delay time, as shown in figure 4.5 (a). The current source (sink) of these inverters are controlled by the V/I converters explained in section 4.2.1. This configuration has efficient linearity in the current to frequency conversion rather than voltage [6].

Generally, in an inverter-based delay line, odd number of inverter stages are required. However, applying differential delay elements, oscillator can be implemented using even number of stages (in figure 4.5 (b)). Furthermore, using differential outputs, the oscillator can increase phase resolution twice that of a single-ended delay element. When we apply 2^n stages to the ring-VCO, our ADC has the capability to add more lower bits by picking up the pulse edge position in the RDL, which is like Watanabe et al s method [4].

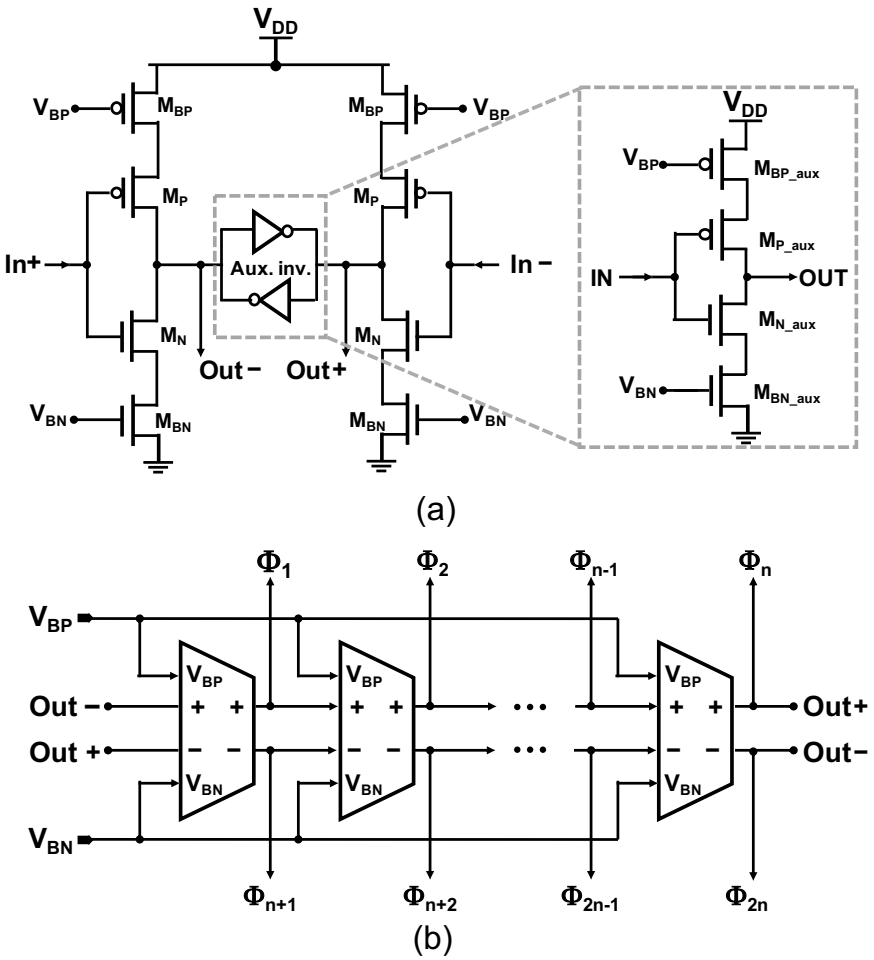

Figure 4.5: Block diagram of proposed (a) current-starved cross-coupled inverter-based delay element with the auxiliary inverters (schematic). (b) Even-stage pseudo-differential delay elements.

4.3 Ring-VCO circuit simulation experiments

The proposed current-starved ring VCO-based ADC is implemented to confirm the proposed conceptual linearity improvement. The implementation of this circuit is simulated in 180-nm TSMC process technology at 0.5 V supply voltage. Table 1 demonstrates the optimal transistors sizing of the proposed V/I converters and differential delay elements, which are implemented as 4-stage and 8-stage. The resistance reference of V/I converters has value of r_{REF_1} = 640 KΩ and r_{REF_2} = 560 KΩ in 4-stage, whereas in 8-stage, the resistance reference of V/I converters has value of $r_{REF\_1,2}$ = 640 KΩ. The transistor sizing and resistor values are optimally determined by considering the minimal nonlinearity error, which can be observed from the linearity curve of V-to-F tuning characteristic results. Cadence Spectre (Virtuoso® Design Environment version IC6.1.8-64b) has been used to perform the following experiments:

- Output waveform as a transient response
- Voltage-to-frequency tuning characteristics
- Curve fitting
- Frequency error curve
- Phase noise analysis

The simulation results are based on typical process corner and temperature of 27 ℃. Furthermore, a discussion on performance results compared to other techniques provides in the following section.

4.3.1 Transient analysis

The transient analysis was simulated to confirm corresponding output waveform of proposed ring-VCO as shown in figure 4.6; here, figure 4.6 (a) shows a single

Table 4.1: The size of the transistors

V/I conversion for current source		V/I conversion for current sink	
Transistor	W (um)	Transistor	W (um)
M_1	5.4	M_2	1.55/2.7†
M_3/M_4	2.7	$M_7/M_8/M_{11}$	2.7
M_5/M_6	0.33	$M_9/M_{10}/M_{12}$	0.33
Inverter		Aux. inverter	
Transistor	W (um)	Transistor	W (um)
M_{BP}	5.4	M_{BP_aux}	1.35
M_{BN}	1.55/2.7†	M_{BN_aux}	0.38/0.675†
M_P	1.76	M_{P_aux}	0.44
M_N	1.34	M_{N_aux}	0.335

†size of transistors for 8-stage

output waveform of 4-stage ring-VCO, and figure 4.6 (b) shows the waveform of 8-stage ring-VCO for four different input voltage (V_{in}) as 0.1V, 0.2V, 0.3V, and 0.4V respectively.

The ring-VCO implemented by the proposed technique generates a square wave as the transient response with an the output rail-to-rail swing. Moreover, the waveform as the transient response is utilized to convert the delay time (Δt) to the oscillating frequency by tuning the input voltage (V_{in}), then those frequency values are transformed to the V-to-F tuning characteristic.

4.3.2 Linearity of V-to-F tuning characteristic

The linearity of the V-to-F tuning characteristics is directly related to INL (integral non-linearity) of VCO-based ADC and can represent how harmonic distortion limits obtaining high resolution of this ADC. Thereby, the V-to-F tuning curve of ring-VCO can be expressed using equation 4.7.

$$\begin{aligned} F_{vco} &= K_{vco}V_{in} + f_o \\ where, K_{vco} &= \frac{\delta f_{vco}}{\delta V_{in}} \end{aligned} \tag{4.7}$$

Here, ring-VCO sensitivity or gain (K_{vco}) is defined as derivative of transfer function with respect to input signal, and the free-running frequency of ring-VCO is defined as f_o.

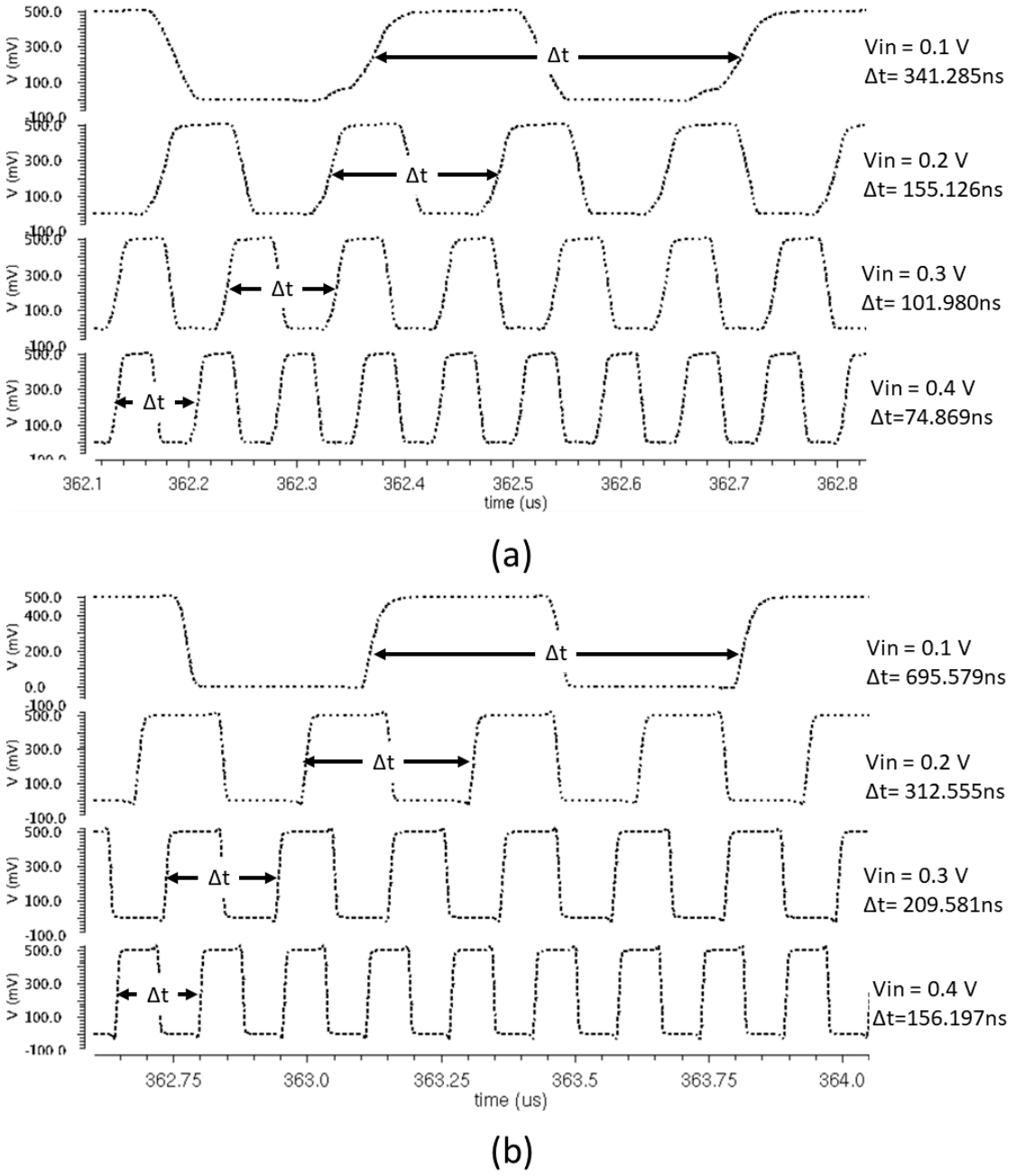

Figure 4.6: Transient response of a single output phase, (a) 4-stage and (b) 8-stage ring-VCO with the coarse tuning input voltage range (0.1 -0.4 V).

The V-to-F tuning characteristics of our proposed ring-VCO for 4-stage and 8-stage designs are presented in figure 4.7(a). The actual value refers to simulation result of output frequency over the input voltage range along with its ideal value, which fits the curve of actual value which is obtained from equation 4.8. The difference between the actual value and the ideal value is called the frequency

error, and it is shown in figure 4.7(b).

The linearity performance can be evaluated using the nonlinearity error or relative error given by equation 4.8. The maximum nonlinearity error of our proposed 4-stage and 8-stage ring-VCOs are 0.2325% and 0.4898%, respectively.

$$Nonlinearity\_error[\%] = \left\{\frac{F_{actual} - F_{ideal}}{F_{ideal}}\right\} \times 100 \tag{4.8}$$

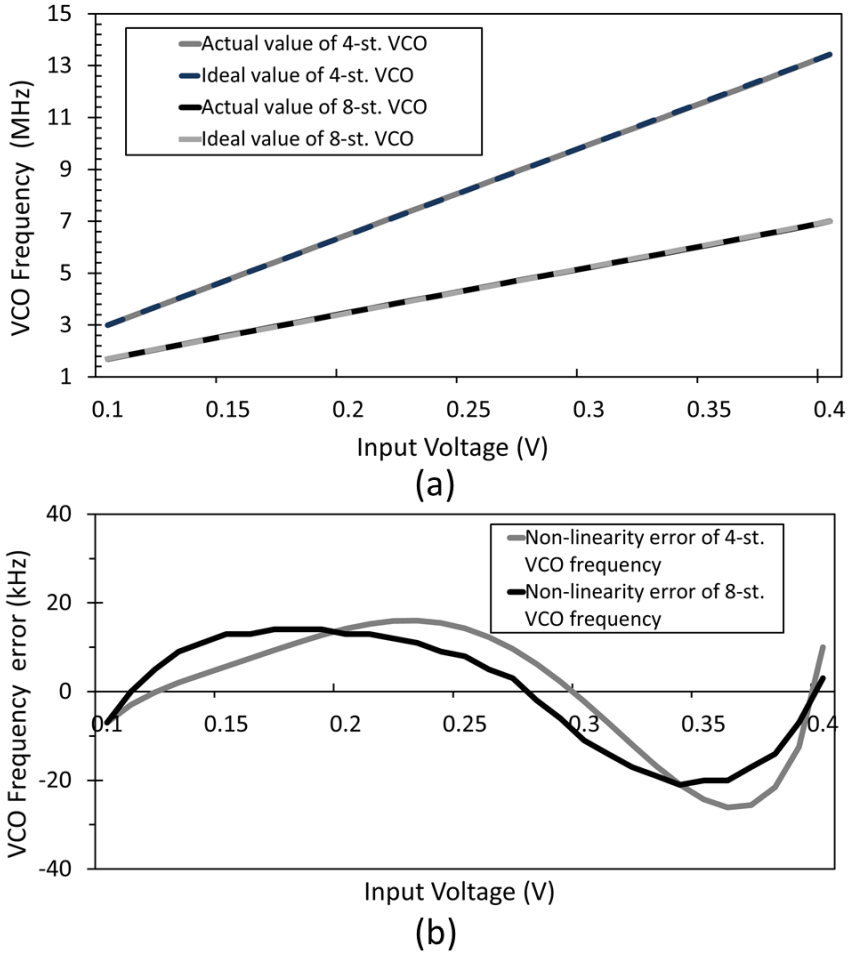

Figure 4.7: Voltage-to-frequency tuning characteristic of (a) Proposed ring-VCO comparison of the actual and ideal value of 4-stage and 8-stage with (b) Its frequency error.

Additionally, linear regression coefficient are utilized to estimate the linearity V-to-F characteristics, i.e., for r-square, linearity error is 1-R^2 [10]. The output frequency and input value is normalized to calculate the linear regression coefficient. Our proposed 4-stage and 8-stage ring-VCO results are shown in figure 4.8 (a) and

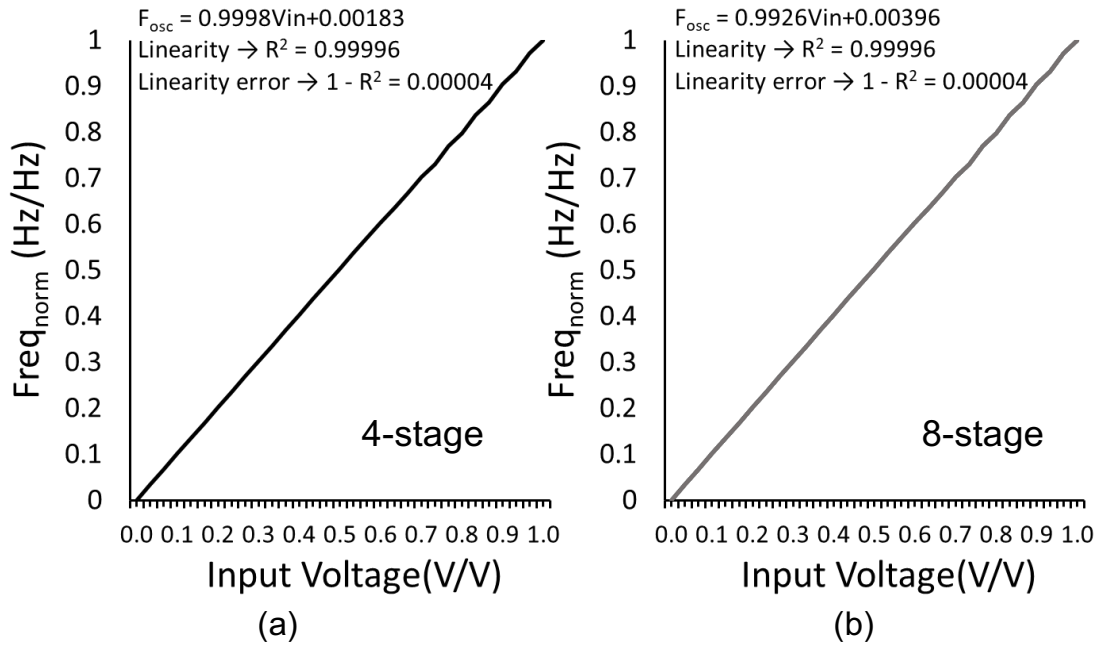

Figure 4.8: Linearity error of V-to-F tuning characteristics, (a) Proposed 4-stage ring-VCO and (b) 8-stage ring-VCO determines normalized output frequency and normalized input voltage to compute the
r-square value (R^2).

figure 4.8 (b), respectively. The linearity error computed by Python programming for our proposed ring VCOs are 0.004%.

As mentioned previously, the transistor sizing listed in Table 4.1, is determined by optimized nonlinearity error. Even though a proper resistor value of proposed V/I converter can generate linear current source and sink matching, and actual fine tuning of the bias voltages control of current sink and source (V_{BP} and V_{BN}) are optimized by nonlinearity error adjusted using transistor sizing.

Figure 4.9 shows bias voltage control variation on input voltage along with different transistor sizing. The transistor sizing of current sink from 1 to 4 of the $\beta 1$ value, referred to as the pMOS (M_1, M_{BP})-to-nMOS (M_2, M_{BN}) width ratio scenario over an input voltage of 4-stage ring-VCO. The value of bias voltage control for each $\beta 1$ is significantly different in output voltage value, as shown in figure 4.10; whereas, output current variation of I_{out1}(current source) and I_{out2} (current sink) is not significant different in output current value.

Additionally, figure 4.11 shows the results of $\beta 1$ value versus nonlinearity error. As far as nonlinearity error as defined in equation 4.8 was used to compare the frequency error among variations for the $\beta 1$ value, this metric indicates a significant difference error value between 4-stage and 8-stage ring-VCO. Therefore, the optimal nonlinearity error obtained from $\beta 1$ is 3.5, in which the current-source width is applied on 5.4 μm, and current-sink width is applied on 1.55 μm. This optimization method is analogous to implementing current sink on the 8-stage ring-VCO.

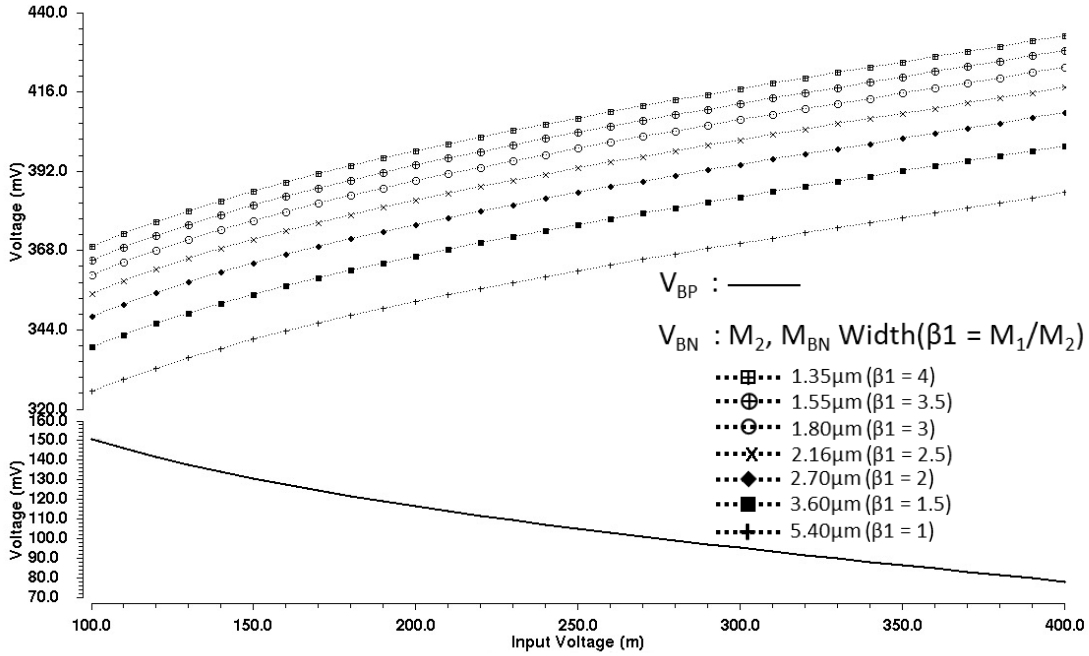

Figure 4.9: Bias voltage control variation of V_{BP} (current source) and V_{BN} (current sink) on input voltage with difference transistor sizing M_2, M_{BN} (current sink) of 4-stage ring-VCO, and shows current source(M_1, M_{BP})-to-current sink width ratio by $\beta 1$.

Subsequently, the optimal inverter sizing selected by comparing output frequency over the variation of the $\beta 2$ referred to as the pMOS (M_p, M_{p_aux})-to-nMOS (M_n, M_{n_aux}) width ratio scenario of 4-stage and 8-stage ring-VCO at 0.25V input voltage is shown in figure 4.12. In this case, the value of 0.25V is selected as input voltage by the majority of overlapping nonlinearity error from figure 4.11, even though the minimized $\beta 2$ obtained the best output frequency; this ratio has a higher nonlinearity error. Therefore, inverter sizing is selected as one with high output frequency, and at the same time with minimum of the

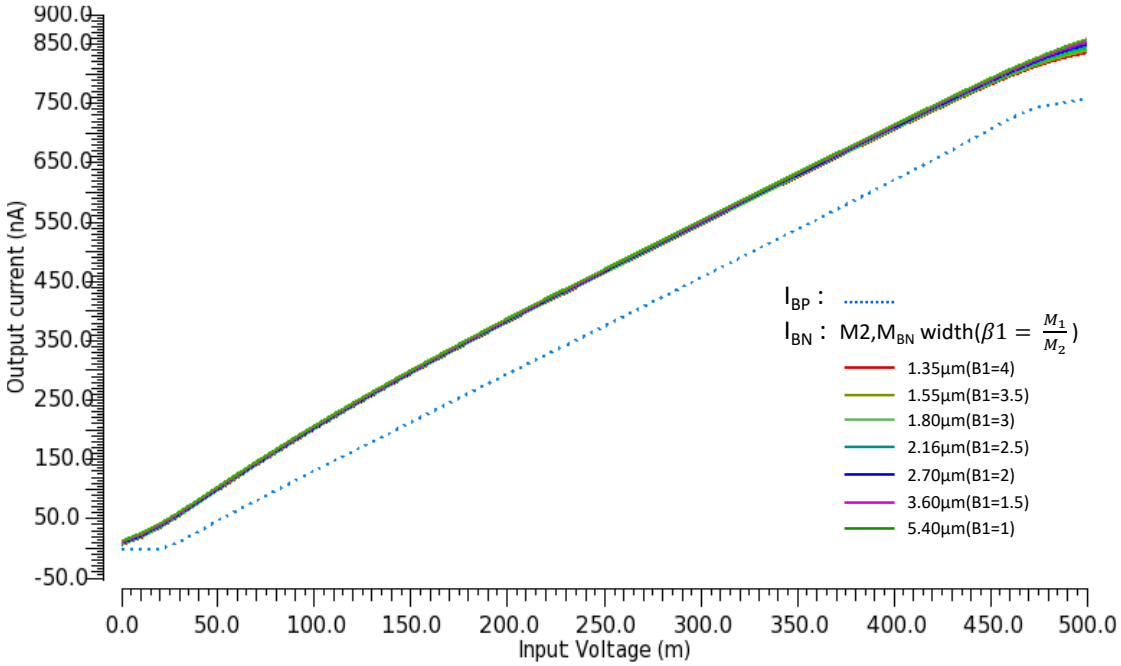

Figure 4.10: Output current variation of I_{out1}(current source) and I_{out2} (current sink) on input voltage with difference transistor sizing M_2, M_{BN} (current sink) of 4-stage ring-VCO, and shows current source(M_1, M_{BP})-to-current sink width ratio by $\beta 1$.

maximum nonlinearity error value. With this constraint $\beta 2$ ratio = 1.3 is the chosen value and this result is shown in figure 4.13.

4.3.3 Phase noise analysis

The ring-VCO-based ADC produces non-ideal output waveforms in the time domain due to jitter corresponding to phase noise in the frequency domain. Phase noise is caused by active/passive-device noises such as thermal and flicker noise. The phase noise refers to the power ratio at a specified offset from the carrier frequency to the power at the center frequency. In this study the phase noise simulation results are obtained from the periodic steady-state analysis (PSS) on Cadence simulation.

Figure 4.14 shows the simulated phase noise performance of the 4-stage ring-VCO with, output phase noise of -50.85dBc/Hz, - 72.49dBc/Hz, and -92.71dBc/Hz at 10kHz, 100kHz, and 1MHz offset frequency, respectively. Concurrently, the simulation results showed phase noise performance of the 8-stage ring-VCO with

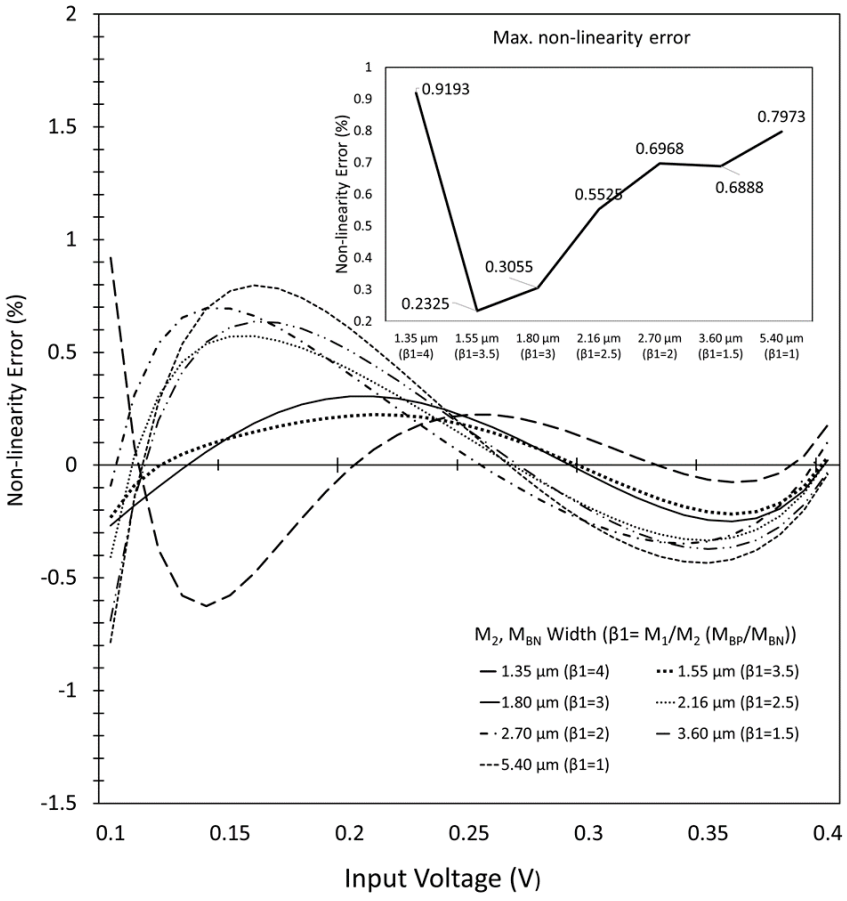

Figure 4.11: Nonlinearity error variation of dependence output frequency on input voltage with difference transistor sizing M_2, M_{BN} (current sink) of 4-stage ring-VCO, and shows current source (M_1, M_{BP})-to-current sink width ratio by $\beta 1$, Besides, insert a graph to summarize maximum nonlinearity error versus those sizing design scenarios.

output phase noise of -53.06dBc/Hz, -73.43dBc/Hz, and - 93.1dBc/Hz at 10kHz, 100kHz, and 1MHz offset frequency, respectively. The offset frequency of 1MHz is selected to compare the performance with results in other related works, as shown in Table 4.2.

Maezawa et al., has mentioned that offset frequency depends on -20dB/dec, and phase noise performance was difficult to evaluate under 1kHz [21]. In actual use of our ADC (e.g., 2kS/s), the effect of low frequency noise is important. Thus we evaluate the effect of phase noise within range from 1kHz to 1MHz. The phase noise in this range can be converted to RMS jitter [22]. The obtained RMS jitter are 0.77 ns and 1.1 ns for 4-stage and 8-stage ring-VCO, respectively. Thus, The jitter

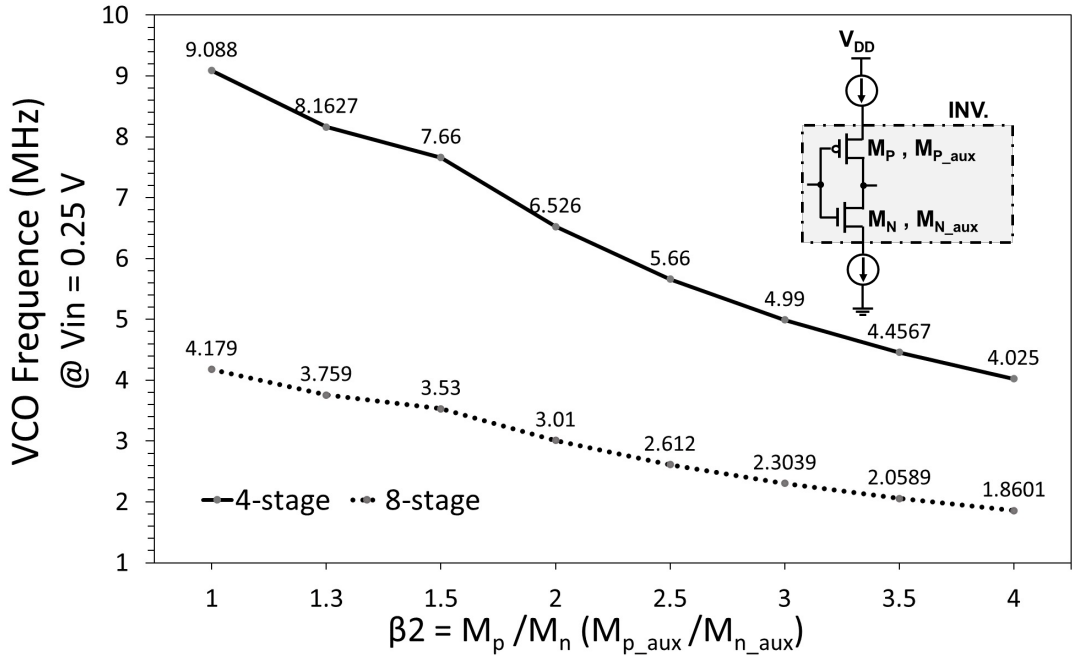

Figure 4.12: The comparison between pMOS-to-nMOS width ratio by $\beta 2$ of 4-stage and 8-stage ring-VCO versus its output frequency at 0.25 input voltage.

yields in our ADC are ±2 LSB and ±3 LSB fluctuation at 10 bit ADC operation (V_{in} = 0.25V, 2kS/s sampling rate).

4.3.4 Comparisons with results in other work

The proposed ring-VCO is targeted for IoT devices which are to be operated at low supply voltage. Therefore, the nonlinearity error of our ring-VCO is compared with other works which may not feature in high frequency application. The related works are emphasized on low-frequency and low power consumption improvement in addition to bulk-driven technique. Thus, comparison with other works are categorized by dominant performance into three groups. The other works that reported the phase noise result are listed in Table 4.2, whereas Table 4.3 lists those related works that did not reveal the phase noise analysis. According to the ring-VCO, linearity improvement is crucial for evaluating the wide frequency tuning range and their stability in output waveform. Thus, in Table 4.2 the results of [7], [5], and [17] have been evaluated by power-frequency-turning-normalized (FOM_{TR}) [13] which ss dominant in the tuning range of ring-VCO as given by equation4.9.

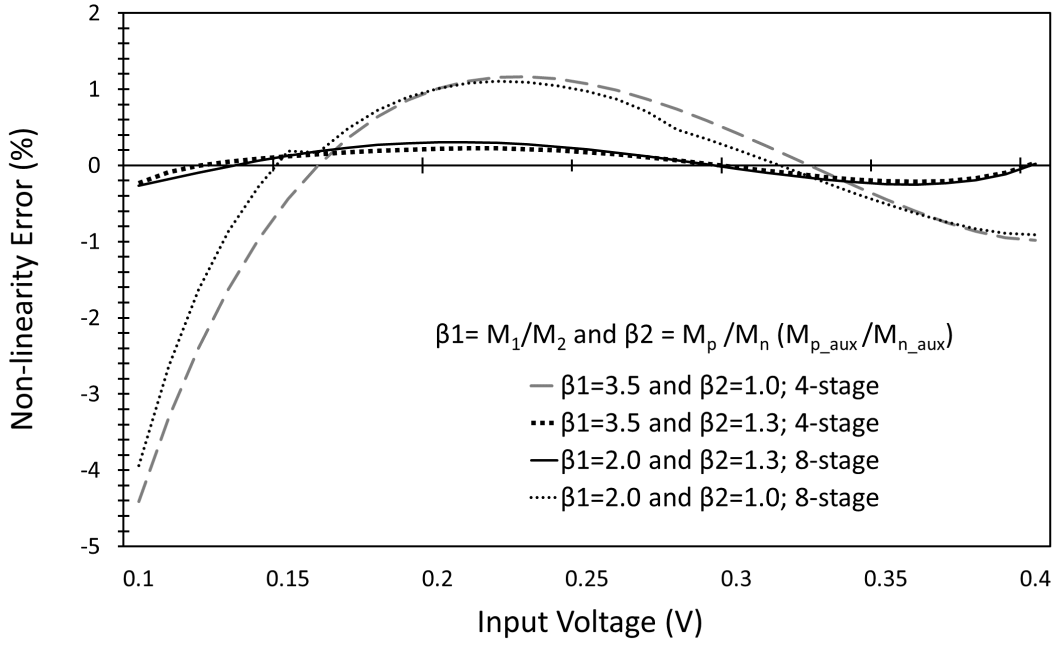

Figure 4.13: The comparison of nonlinearity error variation of dependence output frequency on input voltage between 1 and 1.3 of pMOS-to-nMOS width ratio $\beta 2$ on 4-stage and 8-stage ring-VCO.

$$FOM_{TR} = 10 \log \left[\left(\frac{F_{max} - F_{min}}{F_m} \right)^2 \frac{1}{P_{(mW)}} \right] - L\{F_m\} \tag{4.9}$$

where $L\{F_m\}$ is phase noise of an oscillator at F_m, F_{max} and F_{min} that are offset, the maximum and minimum frequency oscillator, respectively, and P is the total dissipated power.

The power dissipation in [5] is prominent in a ring-VCO that was operated over nominal supply voltage group. It is worth noting that its design methodology is based on conventional current-starved ring-VCO, whereas in [7], [8], and [9] they achieved the high linearity owing to a resultant resistance network at their inputs despite huge power consumption. However, the variation of linearity error in [7] depends on the process corner and temperature condition. The comparison with [7] and [5] reveals that resistance at their input could be limited by the phase noise performance and wide frequency tuning range as according to FOM_{TR}.

Alternately linearity improvement is achieved by bulk-driven control or bulk input technique, while operating at ultra-low supply voltage. The performance in

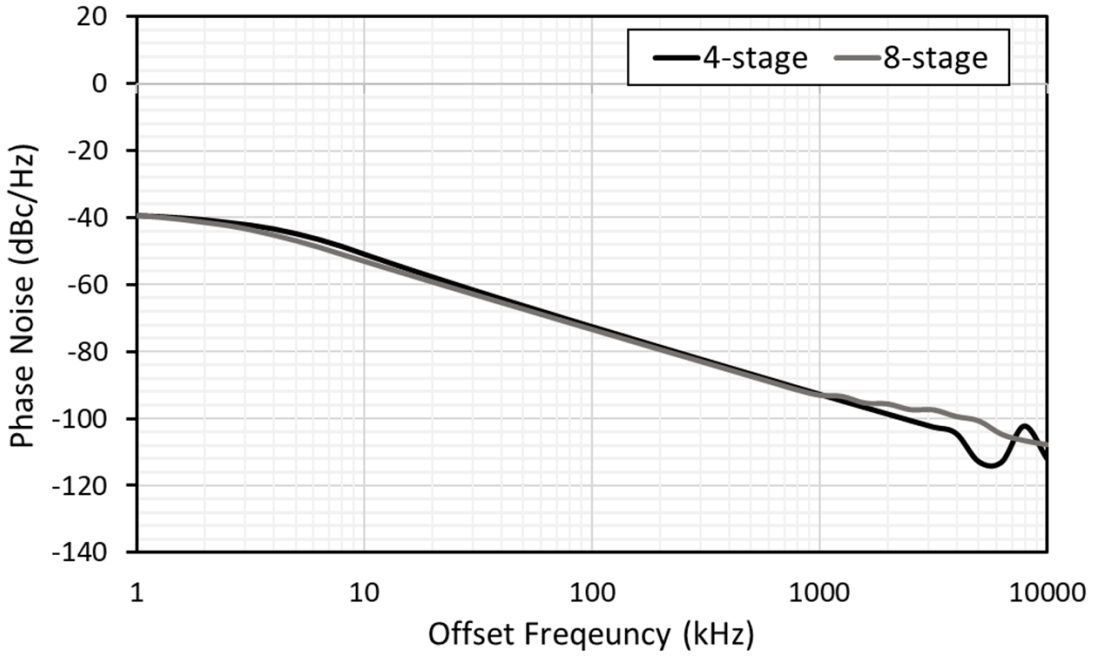

Figure 4.14: Simulated phase noise results for proposed 4-stage and 8-stage ring-VCO.

[14], [15], and [16] obtained a lower tuning input range than other works. The nonlinearity error metrics of [14] and [15] were evaluated by their proposed metric, whereas other works in Table 4.2 and Table 4.3 were evaluated by equation 4.8. However, a limitation of the bulk-input voltage is that it may cause leakage current.

Ring-VCOs in low frequency application are ideally low power devices. Even though those works [18]-[20] are remarkable in low power consumption, their non-linearity error could be significant. In [17], the phase noise is dominant due to the inclusion of a phase detector and other reported ring-VCOs were not evaluated for their phase noise performance. In [21] ring-VCO is utilized in machine learning applications, and linearity is essential for this application. Thus, they propose to extend the input voltage range technique to preserve the ring-VCO in linear operating range and then obtain accurate digital code.

According to the comparison with other works, the proposed scheme satisfies with high linear V-to-F characteristics. The frequency tuning range and power consumption results reveal that our proposed ring-VCO based ADC can operate in low-power, and is suitable for low-frequency applications like AI-enabled IoT

Table 4.2: Comparison of results and FOM_{TR} with other works

Ref.	Tech.	Supply	Input Range	Number of Stages	Error	Power (mW)	Output Freq.	Phase Noise	FOM_{TR}
	nm	V	V		%	mW	MHz	@1 MHz dBc/Hz	
Linearity improvement at nominal supply voltage									
[7]	180	1.8	0 - 1.8	5	0.02-0.9	0.965	574-852.8	-77‡	126
[5]	180	1.8	0.6 - 1.8	N/A	5.567	0.26	66-875	-82.25‡	146
Ring-VCO for Ultra-low-power application									
[17]	65	0.9	N/A	13	N/A	0.09	0.001 - 3	-106.8§ @0.43 MHz	161
Our proposed technique									
Our	180	0.5	0.1 - 0.4	4	0.24	0.000465	2.99 - 13.44	-92.71‡	146
				8	0.49	0.000466	1.69 - 7	-93.1‡	140

‡: Phase Noise from simulated results
§: Phase Noise from measurement results

Table 4.3: Comparison of results with other works

Ref.	Tech.	Supply	Input Range	Number of Stages	Error	Power	Output Freq.
	nm	V	V		%	mW	MHz
Linearity improvement at nominal supply voltage							
[8]	65	1	0 - 1.0	8	0.50	N/A	4000-5000†
[9]	65	1	0 - 1.0	8	1	3.1	340 - 460†
Linearity improvement by bulk-driven controlled technique							
[14]	N/A	0.6	-0.6 - 0	5	0.50	N/A	580 - 860
		0.2	-0.2 - 0		2.40		1 - 1.4†
[15]	130	0.25	0.1 - 0.15	3	0.33	0.000590	0.37- 0.55
[16]	130	0.4	0 - 0.1	N/A	2.7	0.078	0.033 - 3.48
Ring-VCO for ultra-low-power application							
[18]	180	0.5	0 - 0.5	N/A	N/A	0.000152	6.3 - 12.5†
[19]	180	0.4	0 - 0.4	N/A	N/A	0.000011	0.0000975 - 0.0004285
[20]	130	0.14	0.09-0.16	N/A	N/A	0.0000036	0.45-9.2
Our proposed circuits							
Our	180	0.5	0.1 - 0.4	4	0.24	0.000465	2.99 - 13.44
				8	0.49	0.000466	1.69 - 7

†: Approximate from frequency tuning curve

devices. Furthermore, 4-stage and 8-stage ring-VCO-based ADC achieve 12 bits and 13 bits of resolution with the sampling frequency of 1kS/s, respectively.

4.4 Conclusion

Linearized bias current plays an essential part in linearity improvement in ring-VCO-based ADC, relying on current-starved inverter-based delay elements. With

the proposed V/I converter for the current source and sink, we find that the bias voltage control is practical to improve its linearity at 0.5 supply voltage. The evaluation results based on TSMC 180nm CMOS technology show that maximum nonlinearity error is below 0.24% for 4-stage ring-VCO and below 0.49% for 8-stage ring-VCO which were obtained from the optimized error based on adapted transistor sizing. Furthermore, the proposed ring- VCO performs low power consumption; therefore, it applies to a wide range of ring-VCO applications from IoT-device to machine learning.

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5

Modified Pseudo-differential Current-Starved ring-VCO

In recent years, existing Internet of Things (IoT) sensor has shown a new tendency to consume energy excessively from energy harvesters [1]. IoT sensors collect energy from the environment and convert it to electricity. IoT devices are among the billions of edge devices connected through wireless communication in the multidisciplinary paradigm. IoT devices are operated with limited power consumption as well as are expected to have a long service life. Hence, an ultra-low-voltage solution can extend the lifespan of IoT devices. IoT devices can benefit from scaling down the CMOS technology, which can reduce the operating voltage, thus, minimizing power dissipation. Although the operating voltage is scaled down, the threshold voltage of transistors is not significantly scaled down[2].

Analog-to-digital converter (ADC, A/D, or A-to-D) plays an essential role in data acquisition in IoT sensors. In recent years, Voltage Control Oscillator (VCO)-based ADC has been developed to rely on ADC circuits based on all digital circuits [3]. The ring oscillator based VCO is gaining popularity since it can employ the simple delay elements connected in a chain. However, the nonlinearity

of ring-VCO restricts the performance of the Signal-to-Noise and Distortion Ratio (SNDR) of the ADC. The linearity of the V-to-F tuning characteristic can represent how harmonic distortion limits the SNDR and ADC performance.

The current-starved ring-VCO approaches have been proposed to alleviate the nonlinearity of the V-to-F tuning characteristic [4] -[6]. The conventional circuit of the current-starved ring-VCO [6] performs an oscillator by converting the input voltage to a bias current through mirrors to the oscillator core inverters, as shown in figure 5.1(a). The linearity of the V-to-F tuning characteristic is shown in figure 5.1(b), in which the oscillator cannot be operated in the sub-or near-threshold region when operating at a nominal supply voltage. Moreover, the current mirrors always deliver current source and sink to the entire inverter; thus, This function could be caused high static power consumption which conclude that the configuration of conventional current-starved ring-VCO may not be suitable for IoT applications [7],[8].

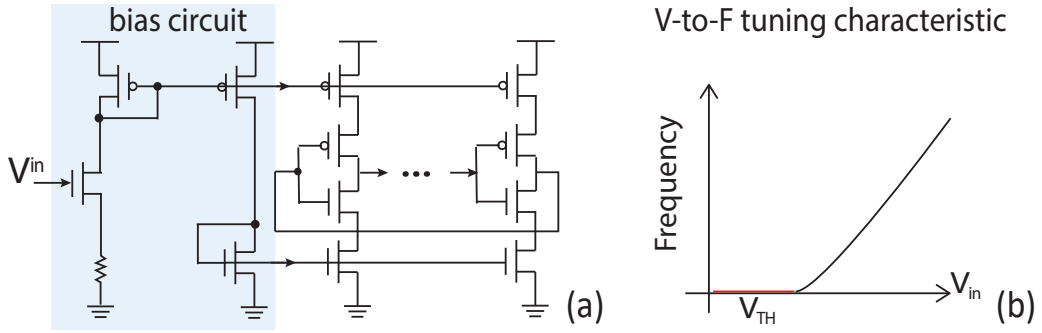

Figure 5.1: Conventional voltage-to-current converter for current starved inverter with linearized improvement technique[6] and (b) V-to-F tuning characteristic.

The separate current source and sink circuits, called the complementary bias voltage control technique, have been presented in [9]. The proposed delay element configuration relies on the current-starved pseudo differential ring VCO, with the current-starved auxiliary inverters comprising 16 transistors. Since IoT devices will not only be developed to minimize operating voltage but also reduce their size.

In this thesis chapter, we propose a novel current-starved pseudo differential delay element for ring-VCO with the objective of a simplified number of transistors. The reduced number of transistor methods is decided based on the pulsed signal transition of fully current-starved pseudo differential delay element while maintaining the linearity of the V-to-F tuning characteristic. The design of circuit is simulated in 0.18μm TSMC process technology under 0.5 V supply voltage in Cadence Virtuoso analog design environment.

The rest of this chapter is organized as follows. Section 5.1 briefly introduce complementary bias voltage control technique. Section 5.2 describes the proposed pseudo-differential current-starved delay element for ring-VCO. Section 5.3 discusses the experimental results with comparative results with other work. Finally, Section 5.4 describes conclusion.

5.1 Complementary bias voltage control technique

Figure 5.2 (a) shows the complementary bias voltage control technique, which has been presented in [9] to separate the current source and sink due to the inadequately linearized biasing current sink by the current mirror. In this independent V/I conversion of current source and sink, the frequency of the current-starved ring-VCO is adjusted by controlling both biasing currents matching as well as simultaneous operation within the change input voltage (i.e., control voltage). Consequently, The current-starved ring-VCO can achieve high linearity in the V-to-F tuning curve at sub-/near-threshold operating voltage without body bias and bulk-controlled technique.

Figure 5.2 (b) shows V/I converter of current source in which the main circuit is implemented using a pseudo-differential amplifier that reduces the number of stacked transistors in order to achieve low operating voltage. On the sink-side V/I converter design, we apply the low gain inverted amplifier with diode-connected

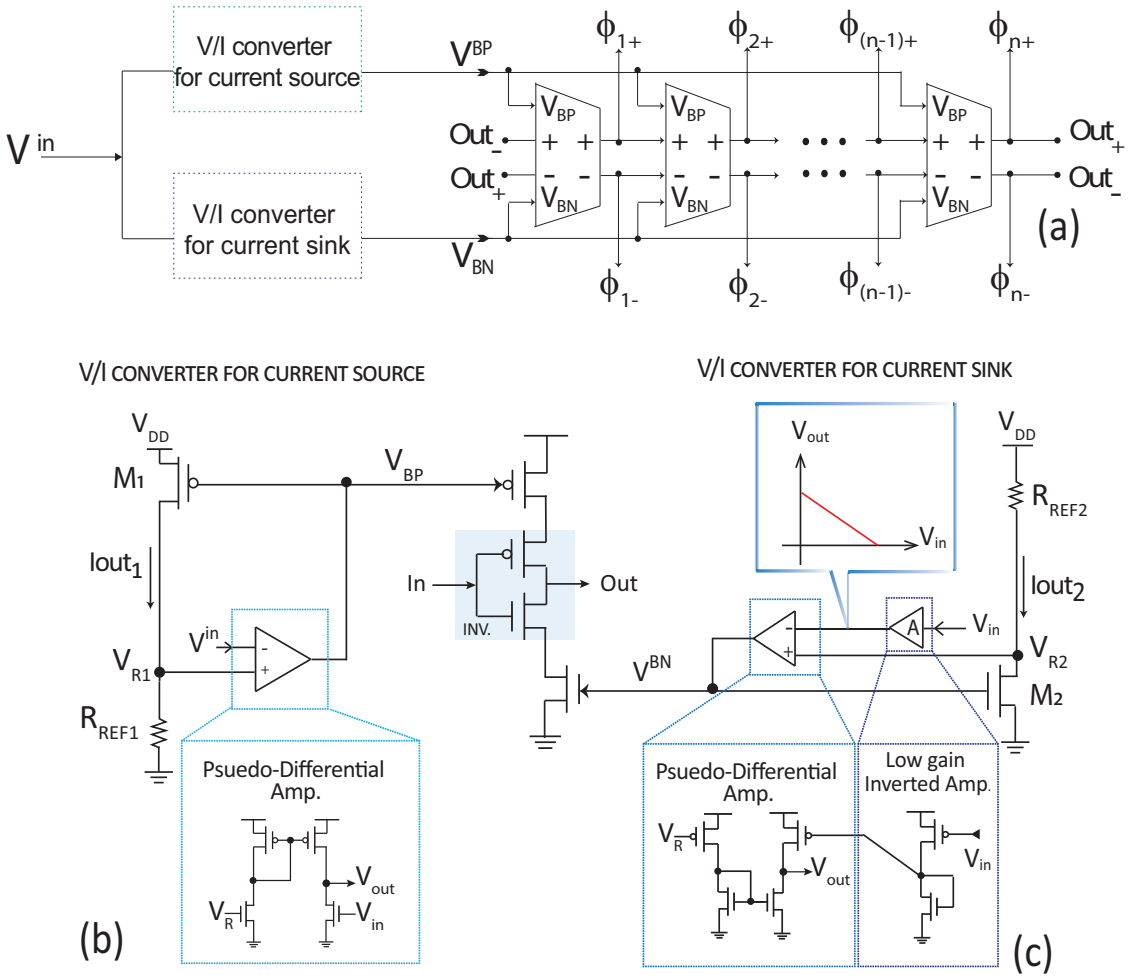

Figure 5.2: (a) Conceptual block diagram of complementary bias voltage controls [9] which is (b) schematic of V/I converter for the current source and (c) for the current sink inverters.

nMOSFET for inverting V_{in}, as shown in figure 5.2(c). The V_{out} with a negative-feedback loop connecting generates the bias voltage to control the current source transistor M_1 and current sink transistor M_2, called V_{BP} and V_{BN}, respectively. The output M_1 and M_2 are delivered as current through a resistor $r_{REF1,2}$. It is then conveyed as $I_{out1,2}$ where I_{out1} corresponds to the source current of V/I converter, and I_{out2} corresponds to the sink current to the internal input voltage $V_{R1,2}$. The voltage at $V_{R1,2}$ are approximately equivalent to the input voltage (V_{in}). The reference resistor R_{REF} can be caused linearized current I_{out1} (I_{out2}) by proportional V_R, as given by equation (1).

$$I_{out1,2} \approx \frac{V_{R1,2}}{r_{REF1,2}} \tag{5.1}$$

Due to V/I conversions serving as replica-biasing circuit to each stage of inverter, current-starved transistors have approximately equivalent resistance to the corresponding $r_{REF1,2}$;thus, designing this configuration often requires the current-starved transistor for the entire inverter circuit to feature low operating voltage as well as linearity improvement.

5.2 The proposed pseudo-differential current-staved ring-VCO

The pseudo-differential ring-VCO architecture is constructed as the cross-coupled current starved inverter-based ring VCO, in which delay element coupled by the main inverter and auxiliary inverter. The output of each inverter is denoted as Φ_i(i=1,2,..n), thereby n is defined as the number of stages, as shown in Fig. 5.2(a). In this section briefly introduce the fully pseudo-differential current-starved delay element which was utilized in [9] comprising 16 transistors which is the baseline delay element.

The fully pseudo-differential current-starved delay element shown in figure 5.3, which the current source (sink) represented by M_{BP} (M_{BN}), and M_P and M_N represent the inverter. According to the auxiliary parts, the cross-coupled inverter is used to guaranteed the opposite edge of the two main inverters at the identical time (e.g. Out_+ and Out_-) in which current source (sink) represented by M_{BP_aux} (M_{BN_aux}), and M_{P_aux} and M_{N_aux} represent the inverter. Consequently, minimizing its number of transistors approach is proposed to devise the new pseudo-differential current-starved delay element.

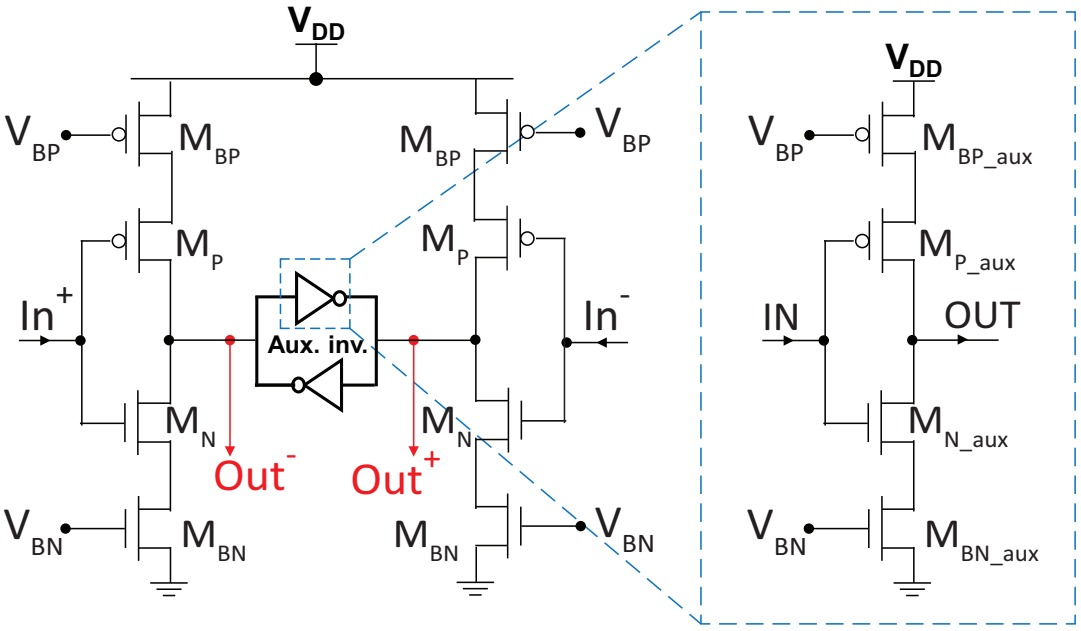

Figure 5.3: Schematic of fully pseudo-differential current starved inverter-based ring VCO with cross-coupled auxiliary inverter.

5.2.1 The procedure of modified baseline delay element

As mentioned earlier, the proposed V/I converters replicate their linearized output current to be a biased current of current-starved delay elements. All transistors functions are approximately controlled according to their corresponding on-resistance (R_{on}). Therefore, this study has utilized the resistance behavior of the current-starved delay element to the reduced number of the transistor and then established the new delay element. Our proposed method is decided based on the pulsed signal transition of baseline circuit. The procedure is divided into two parts depending on the rising transition edge and falling transition edge corresponding to the input of the inverter. We describe the procedure by illustrating the half-cell of the pseudo-differential current-starved delay element. According to the rising transition edge, the nMOS transistor of the main inverter is off-state; consequently nMOS auxiliary transistor which was on-state as well as can be formed to its on-resistance (R_{aux}), as shown in figure 5.4(a). Therefore, we can eliminate the pMOS auxiliary transistors which results shows in figure 5.4(b).

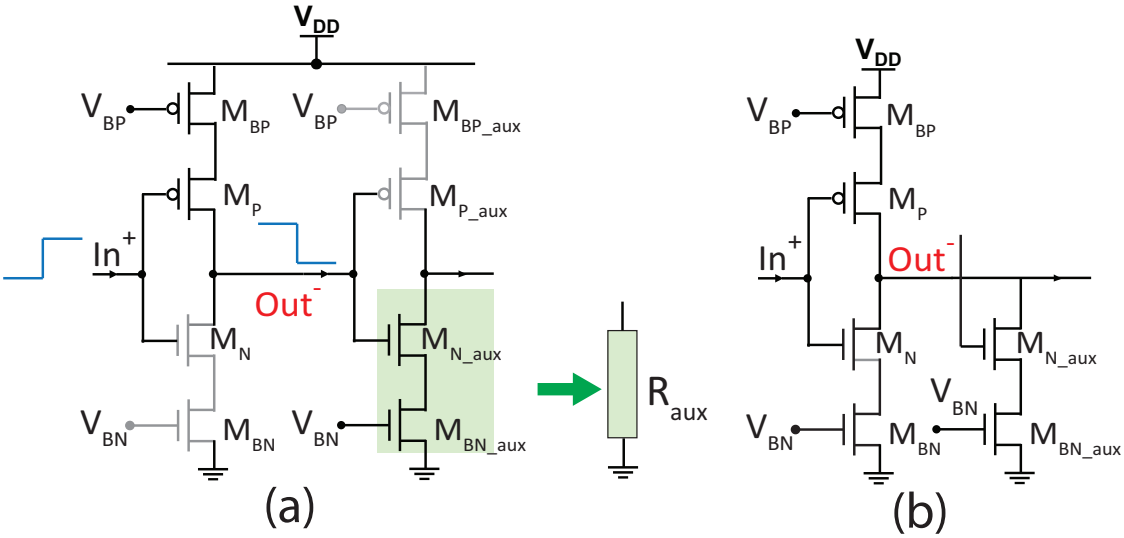

Figure 5.4: Behavior of half delay element for rising transition edge: (a)before eliminated pMOS auxiliary transistors and (b) its results.

Considering the falling transition edge, the pMOS transistor of the main inverter is in off-state; consequently, pMOS auxiliary transistors are in on-state. The pMOS auxiliary transistor can be formed to its on-resistance (R_{aux}), as shown in figure 5.5. Therefore, we can eliminate the nMOS auxiliary transistors.

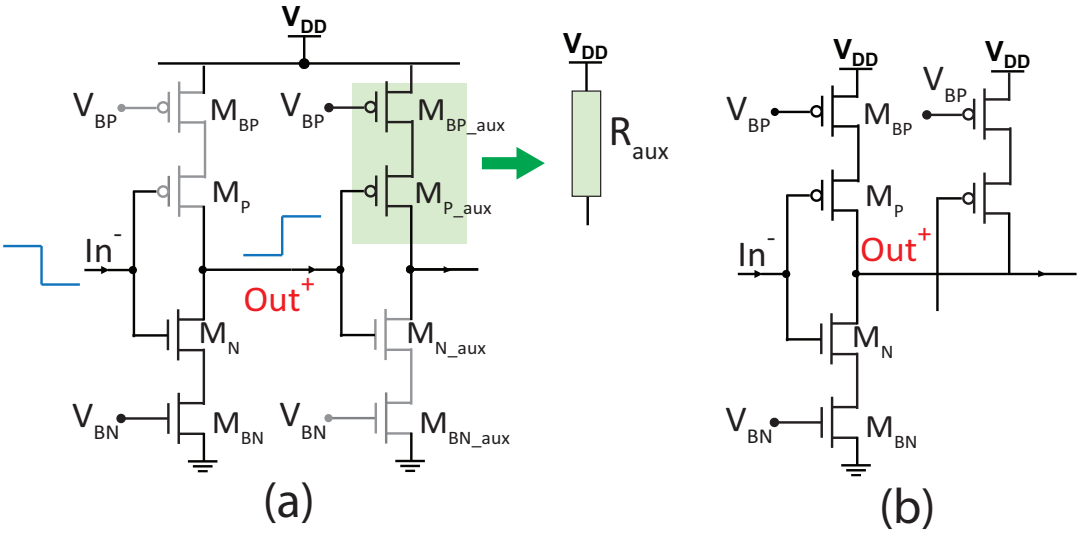

Figure 5.5: Behavior of half delay element for falling transition edge: (a)before eliminated nMOS auxiliary transistors and (b) its results.

5.2.2 The proposed pseudo-differential current-staved delay element

In figure 5.6 (a) we show the results of the minimized number of transistor of baseline delay element(5.3); however, the main inverter can be minimized by shared current staved current source and sink transistor, as shown in 5.6 (b).

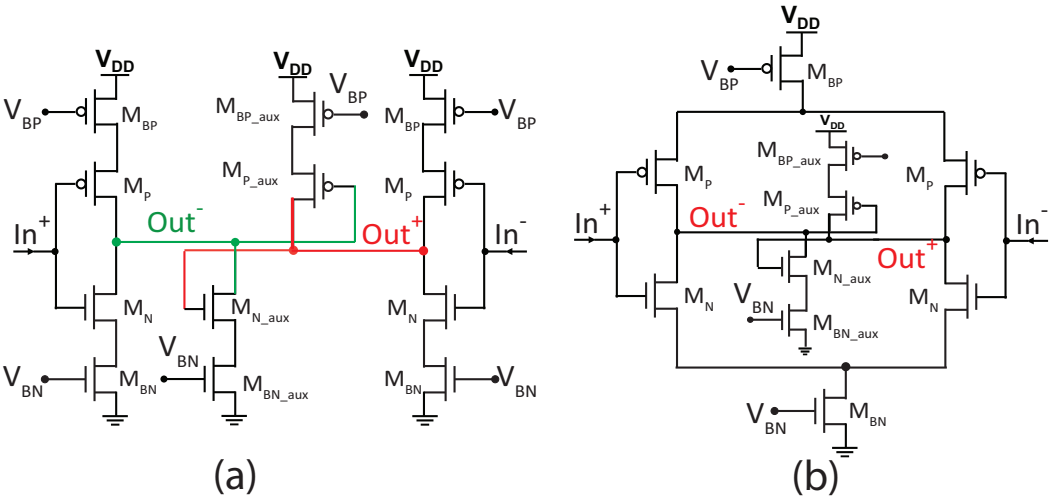

Figure 5.6: Schematic of proposed current starved pseudo-differential delay elements and (b) finally results by main inverter shared current source and sink.

The delay is assumed by corresponding to the on-resistance of the current source (R_{BP}, $R_{BP_{aux}}$) and current sink (R_{BN}, $R_{BN_{aux}}$) along with the inverter ($R_{P,N}$, $R_{P_{aux},N_{aux}}$) in each stage, which can be expressed as

$$T_d \propto (R_{BP,BN} + R_{BP,BN_{aux}} + R_{P,N} + R_{P,N_{aux}}) * C_{eff} \tag{5.2}$$

C_{eff} is defined as the effective load capacitance of each inverter stage. The value of any transistor's on-resistance(R_{on}) in equation(2) can be expressed by equation(3).

$$T_d \propto R_{on} * C_{eff} \propto \frac{(V_{DD}-V_{in})C_{eff}}{I_{ss}} \tag{5.3}$$

where, I_{ss} is defined as its bias current. When V_{in} is approximately equivalent to $V_{R1,2}$; therefore, $V_{BP,BN}$ can be expressed by equation(4).

$$\mid V_{BP,BN} \mid \approx V_{DD} - V_{in} \tag{5.4}$$

The propagation delay of the delay element is controlled as low-to-high (T_{plh}), and high-to-low (T_{phl}) transient times by a current source and sink. Therefore, we can rewrite the expression of the propagation delay by equations (4) and (5), which can be expressed as:

$$\begin{aligned} T_{plh} &= \frac{C_{eff}V_{BP}}{I_{BP}+I_{BP\_aux}} \\ T_{phl} &= \frac{C_{eff}(V_{BN}-V_{trp})}{I_{BN}+I_{BN\_aux}} \end{aligned} \tag{5.5}$$

Where C_{eff} is the effective load capacitance of each inverter stage. Even though the limitation of ultra-low-power supply, the proposed V/I conversion can provide the sufficient current source and current sink for main inverter and auxiliary part (where $I_{BP}+I_{BP\_aux} = I_{BN}+I_{BN\_aux} = I_{Bias}$ (bias current)); and therefore, the overall propagation delays can nullify V_{trp}. This can be expressed as:

$$T_{plh} + T_{phl} = \frac{C_{eff}(V_{BP}+V_{BN})}{I_{Bias}} \tag{5.6}$$

Hence, the frequency oscillator of ring-VCO is inversely proportional to sum of propagation delay of n-stage delay elements and is given by

$$F_{osc} = \frac{I_{Bias}}{n(C_{eff}(V_{BP}+V_{BN}))} \tag{5.7}$$

5.3 Simulation results and discussions

The proposed current-starved pseudo-differential ring-VCO was designed and simulated to confirm operation and performance by Cadence Spectre (Virtuosoő Design Environment version IC6.1.8-64b). The simulation results are based on typical process corner and temperature of 27℃. The circuit is designed in TSMC 0.18μm process technology at 0.5 V operating voltage. The size of transistors are shown in Table 1, and compared with the previous works.

The transistors sizing PMOS source M_1 and NMOS sink M_2 were used in the proposed V/I converters with the $r_{REF\_1,2}$ = 640KΩ compared with previous

Table 5.1: Comparison of transistor size used in prior work and this work.

Previous work [9]		This work	
V/I conversion		V/I conversion	
Transistor	W (um)	Transistor	W (um)
M1	5.4	M1	2.7
M2	1.55	M2	2.1
Inverter		Inverter	
Transistor	W (um)	Transistor	W (um)
MBP	5.4	MBP	2.7
MBN	1.55	MBN	2.1
Mp	1.76	Mp	1.74
Mn	1.34	Mn	1.74
MBP_aux	1.35	MBP_aux	0.675
MBN_aux	0.38	MBN_aux	0.525
Mp_aux	0.44	Mp_aux	0.44
Mn_aux	0.335	Mn_aux	0.44

work produced the $I_{out1,2}$ as shown in figure 5.7. The novel current-starved pseudo-differential delay element occupied transistor sizing more undersized than the previous work by 44.88%, which is total transistor sizing in one delay element.

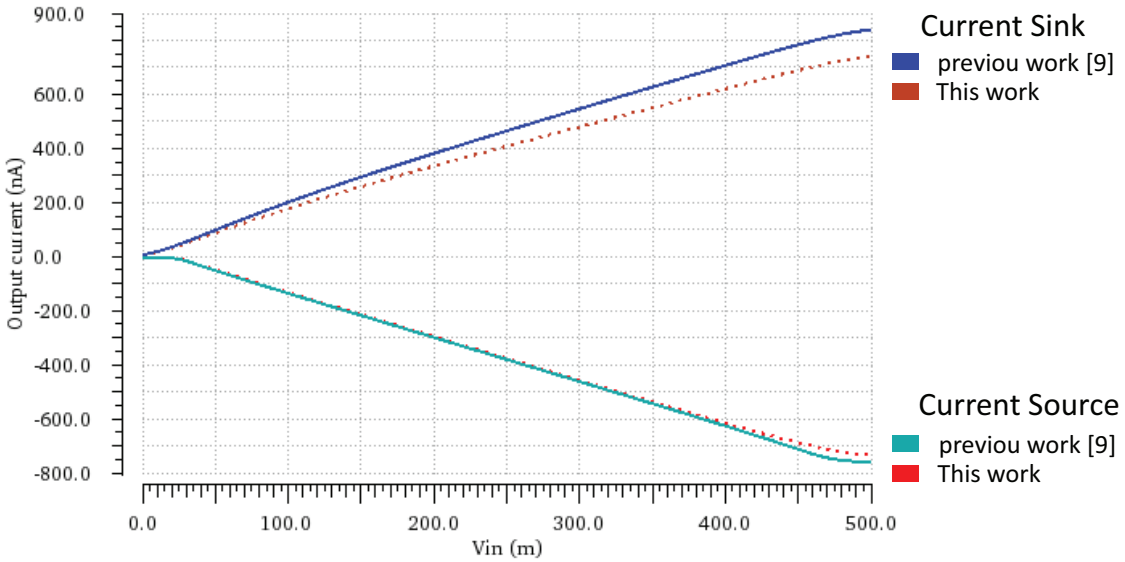

Figure 5.7: Output voltage is generated corresponding to $I_{out1,2}$ by V/I converter for current source(sink) compared with the baseline ring-VCO.

5.3.1 Transient analysis and V-to-F tuning characteristic

The transient analysis was simulated to confirm the corresponding output waveform of the proposed 4-staged pseudo-differential ring-VCO as well as confirm properties that output can generate inverse with a phase delay of 180° N each other. Figure 5.8 shows a cross-coupled output waveform of the third-stage (e.g., Φ_{3+}, Φ_{3-}); thereby, four different input voltages (Vin) as 0.1V, 0.2V, 0.3V, and 0.4V, respectively.

Consequently, we can determine the transient frequency over input voltage to form the V-to-F tuning characteristics as an actual curve. We evaluated the ideal curve by fitting the actual curve. The V-to-F tuning curve of ring-VCO can be expressed using equation (8), a difference in percentage actual frequency value (F_{actual}) and ideal frequency (F_{ideal}) value. The tuning range of input voltage is 0.1-0.4 V with a fine resolution of 0.01 V, and it results below 1.3% of maximum nonlinearity error.

$$Nonlinearity\_error[\%] = \left(\frac{F_{actual}-F_{ideal}}{F_{ideal}}\right) \times 100 \tag{5.8}$$

Table 5.2: Performance comparison of other works

Ref.	Tech.	Supply	Turning Range	Stages	Error	Power	Output Freq.	Phase Noise
	nm	V	V		%	[mW]	MHz	@1 MHz dBc/Hz
[3]	180	1.8	0 - 1.8	5	0.02 - 0.9	0.965	574 - 852.8	-77
[4]	180	1.8	0.6 - 1.8	N/A	5.567	0.26	66 - 875	-82.25
[9]	180	0.5	0.1 - 0.4	4	0.24	0.000465	2.99 - 13.44	-94.36
[10]	180	N/A	-0.2 - 0.2	N/A	2	N/A	∼27 - 94	N/A
Our 9	180	0.5	0.1 - 0.4	4	1.24	0.000221	3.59 - 13.74	-95.01

5.3.2 Phase noise analysis

The phase noise refers to the power ratio at a specified offset from the carrier frequency to the power at the center frequency. The phase noise simulation of the proposed ring-VCO results from the periodic steady-state analysis (PSS) on

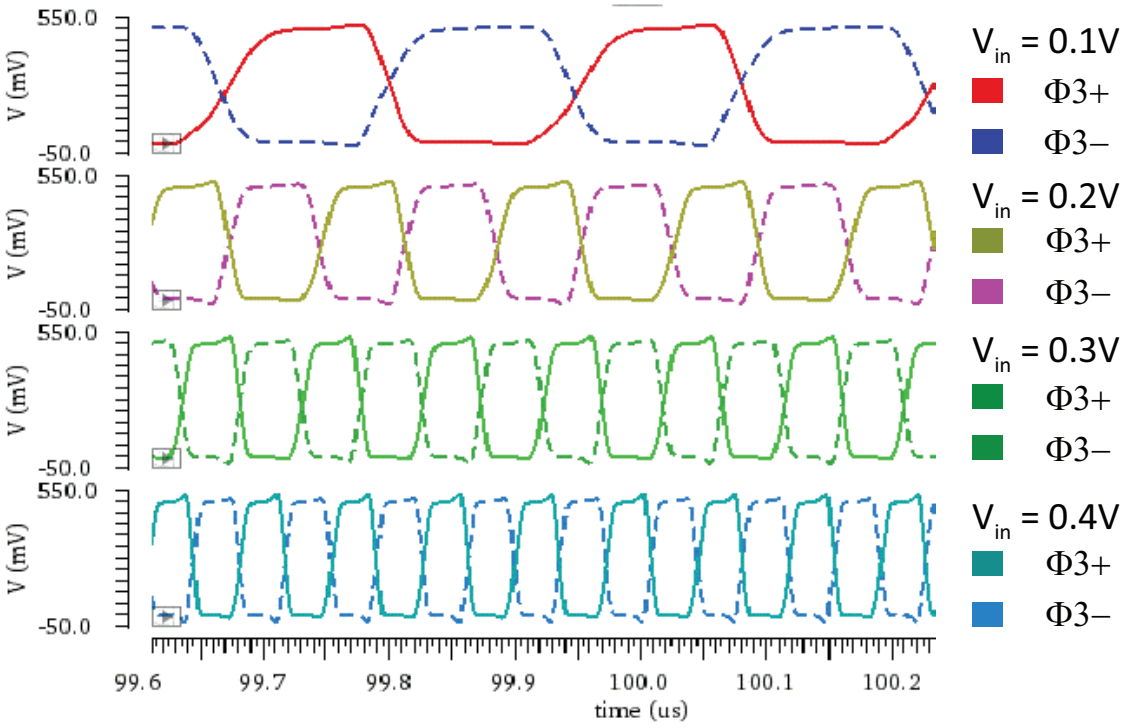

Figure 5.8: Transient response of a cross-coupled output phase of third stage of the proposed 4-stage ring-VCO with input voltage range (0.1, ... ,0.4 V).

Cadence simulation. Figure 5.10 shows the simulated phase noise of -54.2dBc/Hz, -75.6dBc/Hz, and -95.01dBc/Hz at 10kHz, 100kHz, and 1MHz offset frequency, respectively. The negative maximum value number refers to high performance.

5.3.3 Comparison with other work

The proposed ring-VCO is emphasized on a minimized number of transistor and their size, which can be operated at 0.5 V supply voltage. Table 2 lists the results of our ring-VCO compared with previous work and other work in which the current-starved ring-VCO was designed on 0.18μm CMOS technology. Since the output frequency is expressed by equation (7), in which the bias current is included auxiliary part due to eliminated overhead transistor. In addition, reducing the size of the transistor can decrease effective load capacitance. Our ring-VCO is dominant in output frequency and phase noise compared with the previous work in [8] which is sub/near-threshold operating voltage even though the bias current (fig.5.7) and the transistor sizing (Table 1) are smaller than

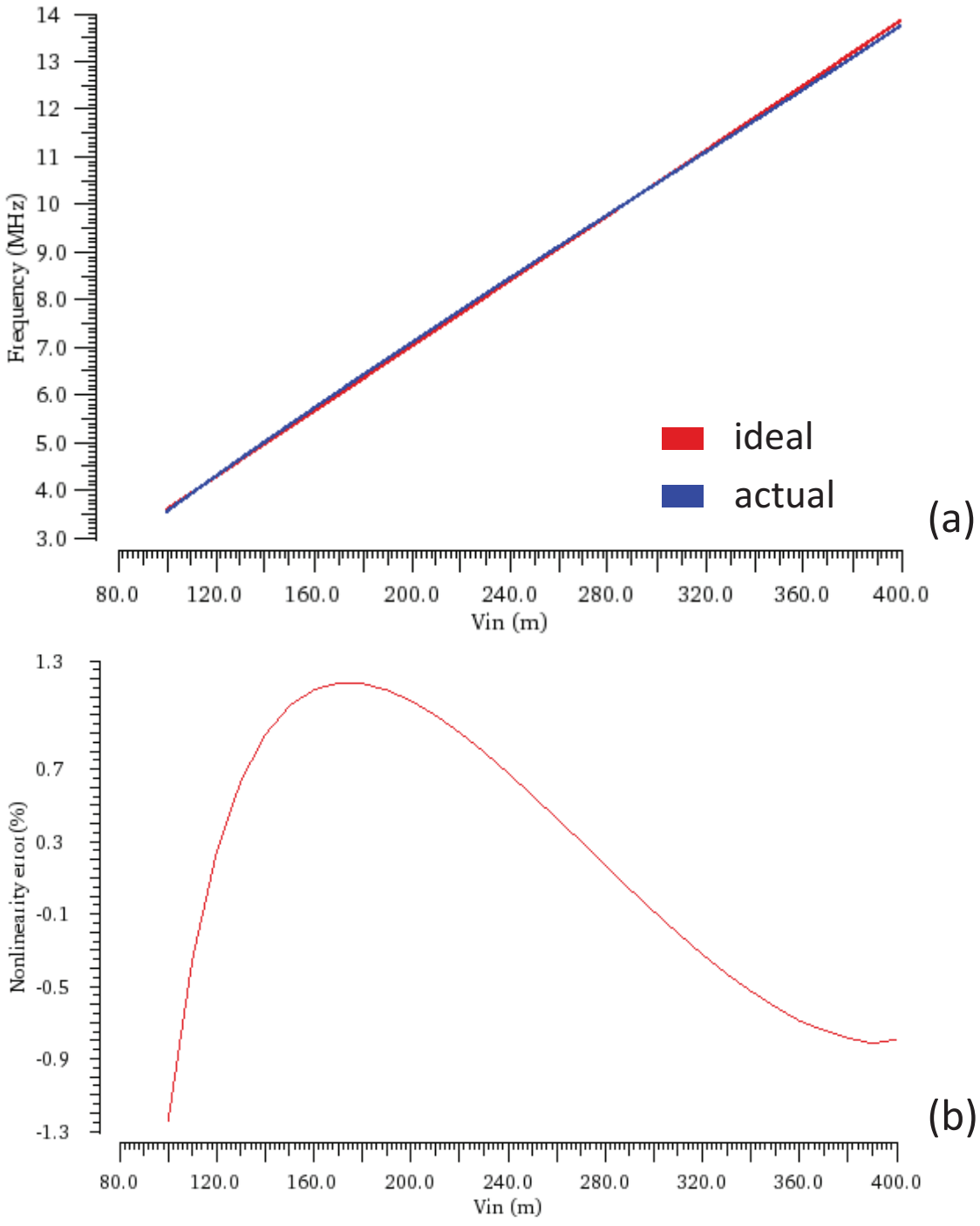

Figure 5.9: Simulation results of (a) V-to-F tuning characteristic and (b) percentage nonlinearity error.

in the previous work. The error refers maximum nonlinearity of the V-to-F characteristic. Our ring-VCO obtained the acceptable nonlinearity value, which can rank in the middle range among ring-VCO with linearity improvement. The ring-VCO in [3],[4] are operated at nominal supply voltage while ring-VCO in

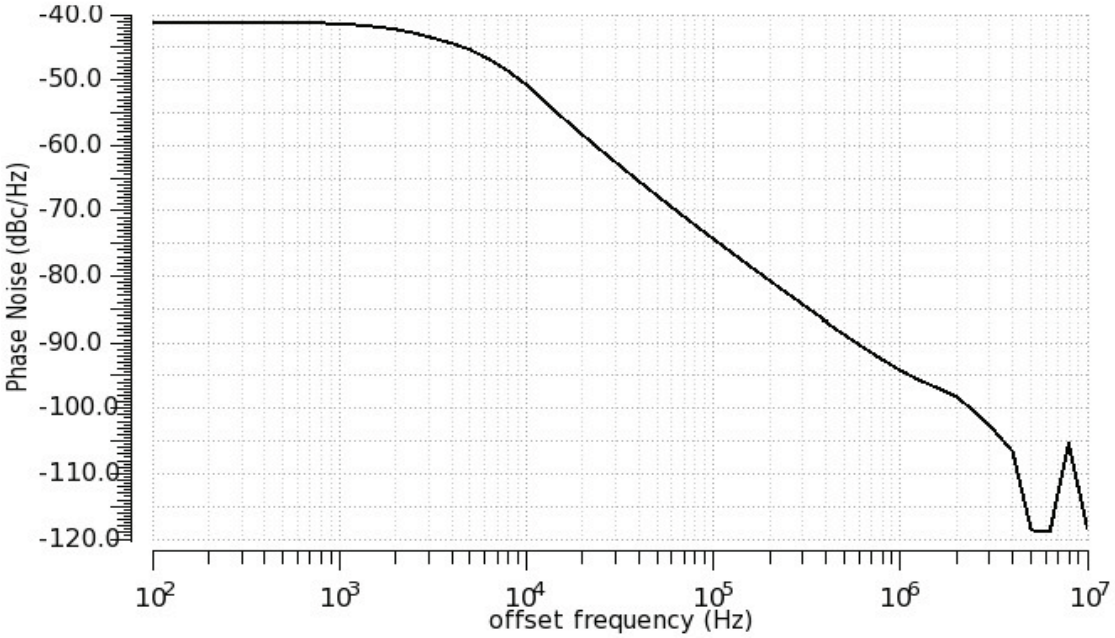

Figure 5.10: Phase noise performance of proposed 4-stage pseudo-differential Current-Starved ring-VCO.

[10] generated frequency by bulk technique.

5.4 Conclusion

In this chapter, we present the novel current-starved pseudo-differential delay element, which has decreased overhead transistors along with the size of the transistor. Therefore, power consumption was reduced by using this scheme while the frequency was higher than the baseline. Although there is a tread-off between transistor sizing, the number of transistors, and linearity, this configuration is not adversely affecting the linearity of the V-to-F tuning characteristic.

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6

Case study: ring-VCO as ReLU function on Pulsed neuron circuit

6.1 Introduction

With an increased interest for intelligent sensing devices, deep learning is being applied for internet-of-things (IoT) sensor. Ideally, the IoT devices are expected to operate on batteries or energy harvesters; thus, realizing analog neuron circuits can mitigate high power consumption and area constraints.

In the past decades pulsed neuron circuits were used as one of the ways to design analog neural networks. Their operation offers good advantage in terms of noise robustness (using binary pulse sequences) [1, 2]. Ring oscillators were investigated for energy efficiency in the pulsed neuron design [3]. Recently, the Rectified Linear Units (ReLU) activation function has been widely used in the hidden layer of Deep Neural Network (DNN) due to its vanishing gradient problems and high classification accuracy. Its function generates output to be zero when input is less than the threshold value, whereas it generates output as a linear function [4].

To implement practical ReLU activation circuit, linearity property is an essential feature. In this paper, we focus on the linear V-to-F tuning curve of our ring

VCO to design ReLU activation function, and then apply it to implement pulsed neural network.

The recent linearity improvement of VCOs have been based on various techniques such as; linearized current controlled mechanism [5], current-starved ring-oscillator by adding a floating-gate transistor at its input stage [6], simple current-starved VCO with NMOS-starving transistor[7], LC-VCO with varactor resonant tank and its linearity optimized by a multilayer perceptron (MLP) algorithm [8].

A ring-VCO can be implemented using a simple delay chain configuration, which can benefit from CMOS down-scaling technology. Although the supply voltage is scaled down, the threshold voltage (V_{th}) of transistors are not significantly scaled down [9]. A-F. Javad et al. [10] proposed the design of a ring oscillator designed in back-gate 28-nm FD-SOI CMOS technology which increases the body effect; thus, their ring-VCO has wider tuning range. However, they cannot guarantee linearity improvement when operating below 1V. The proposed design can operate at 0.5 supply voltage without using body bias technique or bulk-controlled inverter. Our main contributions are:

- To propose a ring-VCO-based ReLU activation circuit with linearity improvement. The ring-VCO can be operated in sub-threshold or near-threshold regions without using body bias technique or bulk-controlled inverter.
- Due to sub-threshold or near-threshold operation, the linearity of the ring VCO's V-to-F characteristics can be affected by the process variation, therefore, we propose a compensation technique.
- Pulse-based multiplication using an AND gate and PWM system which can perform negative weight calculation.
- The pulsed neuron circuits are assembled as neural network to validate ring-VCO-based ReLU activation function and benchmark using the MNIST handwritten digits for classification.

6.2 Proposed pulsed neuron circuit with ReLU activation function

6.2.1 Pulse-based multiplication using AND gate

Pulse multiplication circuit consists of a VCO with linearity improvement and an AND gate. Our ring-VCO [11] is based on a current-starved inverter with complementary bias voltage control. They provide linearly biased current source and sink matching, as shown in figure 6.1 (a) and (b).

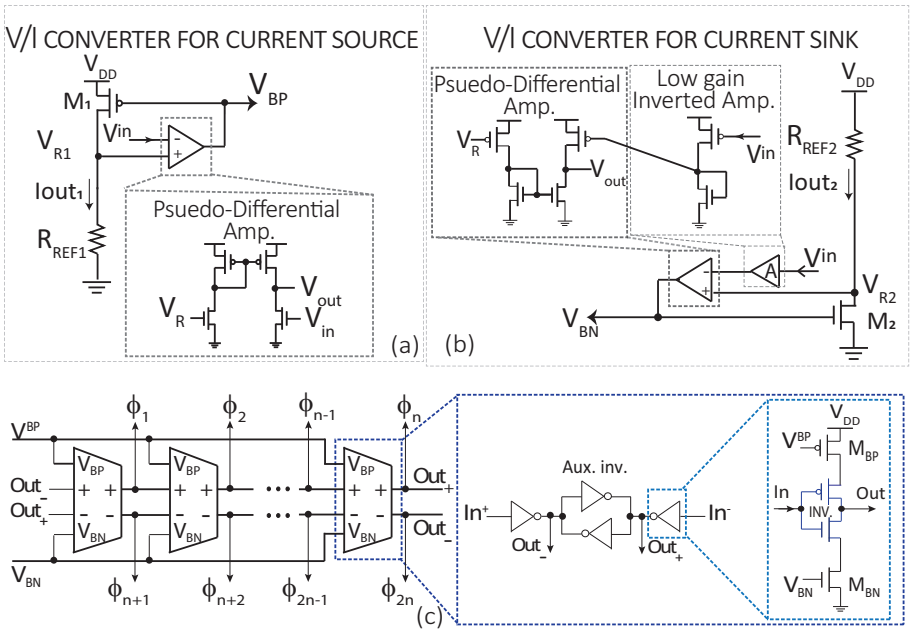

Figure 6.1: Block diagram of VCO-based ReLU activation circuit comprising V/I converter, and schematic of (a) V/I converter for source current,(b) V/I converter for sink current, and (c) current-starved cross-coupled inverter-based delay element with auxiliary inverters.

On the other hand, in our sink-side V/I converter design, we apply the low gain inverted amplifier with diode-connected nMOSFET for inverting V_{in}. The V_{out} generates the bias voltage control for the M_1 and M_2. The output M_1 current source and M_2 sink are delivered as current through a resistor $r_{REF1,2}$. It is then conveyed as $I_{out1,2}$ where I_{out1} corresponds to the source current of V/I converter, and I_{out2} corresponds to the sink current to the internal input voltage $V_{R1,2}$. Which is then approximately equivalent to the input voltage (V_{in}). The

linearized current through r_{REF} can be caused by proportional V_R, as given by equation (1).

$$I_{out1,2} \approx \frac{V_{R1,2}}{r_{REF1,2}} \tag{6.1}$$

Consequently, I_{out1} (I_{out2}) behaves identically to the linear current source I_{BP} (sink (I_{BN})) of current-starved inverters. Moreover, the transistors in current-starved delay elements have approximately equivalent resistance to the corresponding $r_{REF1,2}$. For the massive input of the neural network, the differential delay element of the ring-delay configuration can provide a double output per stage (2^n stages). The cross-coupled delay element with auxiliary inverters configuration was selected to be implemented as a current-starved ring-oscillator as shown in figure 6.1(c).

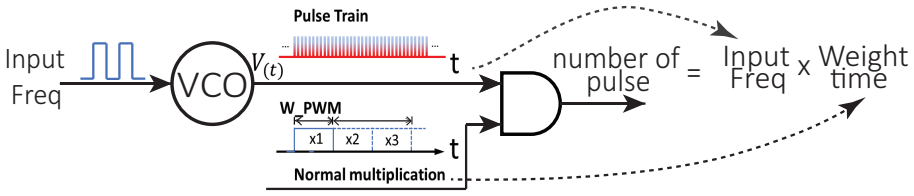

Figure 6.2: Block diagram of pulse multiplication circuit with a VCO and an AND gate.

According to the operation of our pulse multiplication circuit shown in figure 6.2, we can observe that the number of output pulse is determined from the multiplication operation (AND gate) between frequency (VCO) and weight PWM as time window. The PWM signal, whose value is modulated by time, can be directly multiplied by an AND operation with the output of the VCO. For example, an AND operation with a duration of PWM signal(W_PWM) as n seconds on a VCO output with a frequency of 2^8 Hz will generate $n \times 2^8$ digital pulses.

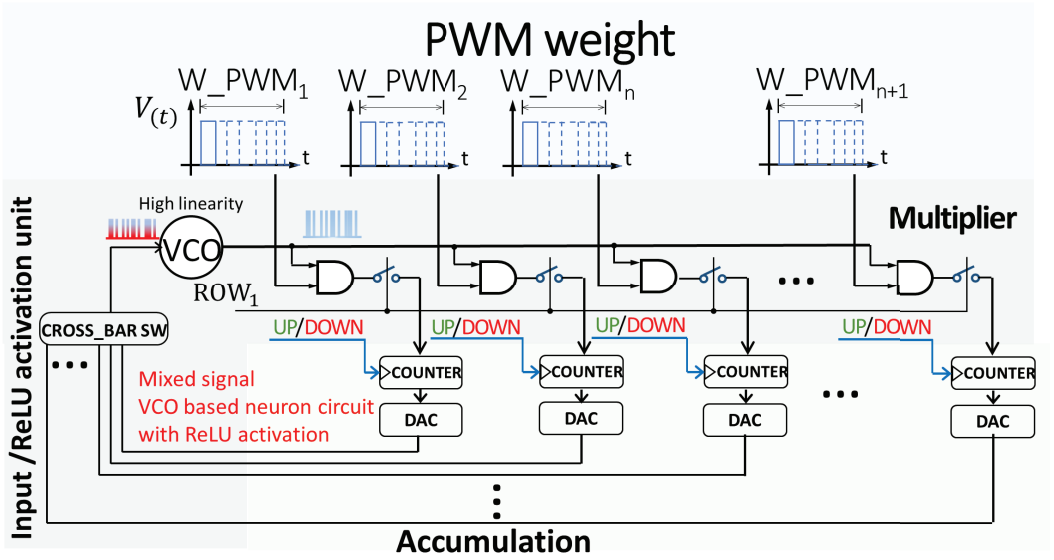

Figure 6.3: The neuron processing circuit incorporating our ring-VCO-based ReLU activation circuit.

6.2.2 Neural network design using our neuron circuit

The neuron processing circuit incorporating our ring-VCO-based ReLU activation circuit is shown in figure 6.3. The configuration is similar to the neuron processing circuit with pulse density modulation that has been studied for many years [12][13]. The ring-VCO is multiplied by a PWM signal at its output and the number of pulses is counted by a counter. An up-down counter is used to switch the up-down operation depending on a sign signal to achieve a negative weight. The output is converted to an analog voltage that is used as the input to the VCO using a DA converter. This process does not require a two-dimensional matrix configuration since the addition of pulses is expanded in a time series approach; one synaptic operation for a multi-neuron circuit group is performed in parallel by multiplying one ring-VCO output with a parallel set of weight signals using PWM signals. Consequently, the realization of a series processing of ReLU activation operations by the neuron processing circuit using VCOs requires high-precision linearization of the VCOs.

6.3 Results and discussion

The proposed pulsed neuron circuit was designed and simulated using 0.18-μm TSMC process technology @ 0.5 V supply voltage. Cadence Spectre (Virtuoso® Design Environment version IC6.1.8-64b) was used to simulate the following experiments:

- output waveform as transient response
- voltage-to-frequency tuning characteristics
- curve fitting for linear analysis, and
- process variation analysis

6.3.1 Linearity of ReLU transfer characteristic

Our ring-VCO serving as a ReLU activation function for typical-typical (TT) corner at room temperature is shown in V-to-F tuning characteristics in figure 6.4(a), and its transient analysis is shown in figure 6.4(b). The percentage of nonlinear error is expressed by equation (6.2), which is a difference in percentage actual and ideal frequency values. The tuning range of input voltage is 0.075-0.4 V with a resolution of 0.005 V, and it results in 0.2264% of maximum nonlinearity error.

$$Nonlinearity\_error[\%] = \left(\frac{F_{actual} - F_{ideal}}{F_{ideal}}\right) \times 100 \tag{6.2}$$

From the perspective of V-to-F characteristics non-linearity, the frequency of ring-VCO is also essentially nonlinear; therefore, the V-to-F tuning curve is coupled with the exponential coefficient value. We use the polynomial Taylor expansion to express the total frequency of ring-VCO as given in the frequency expression in equation (6.3).

$$F_{osc}(V_{in}) = K_{vco}V_{in} + f_o + \sum_{i=1}^{\infty} Y_i \cdot V_{in} \tag{6.3}$$

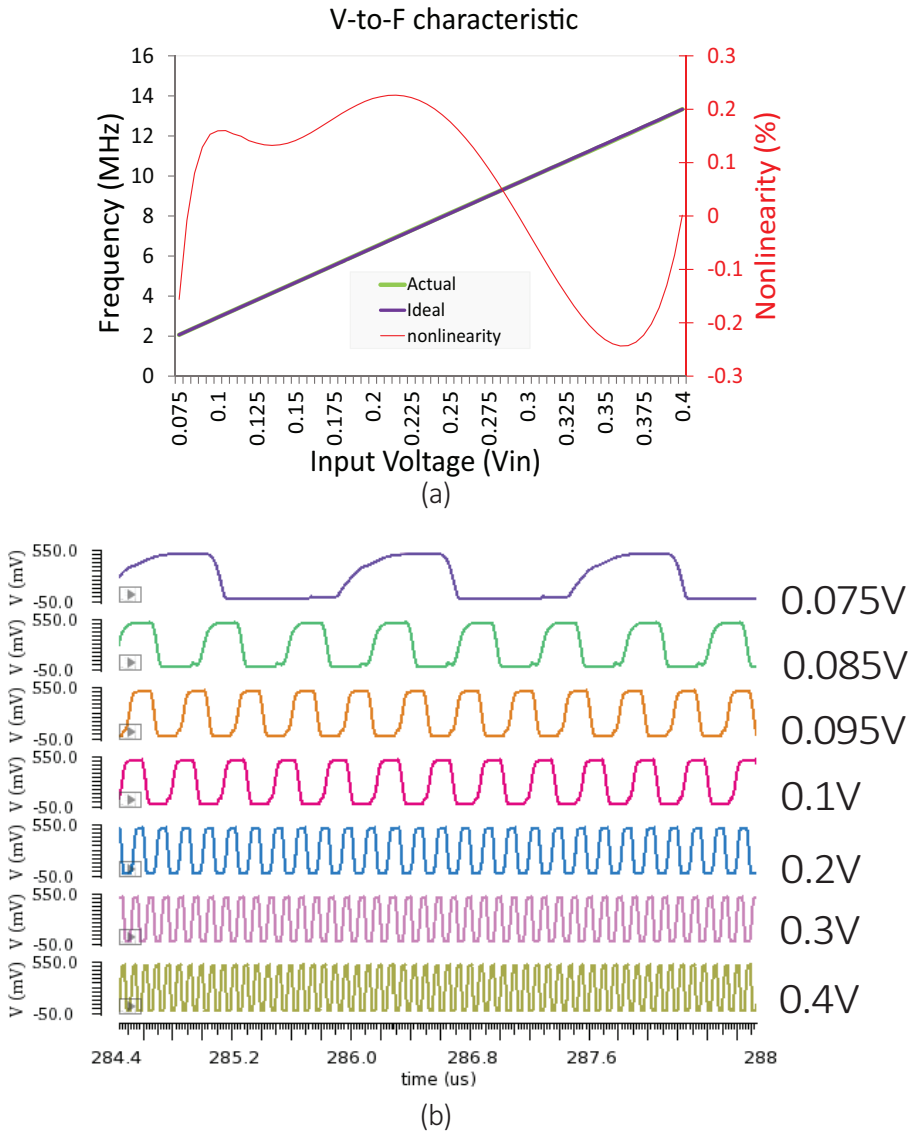

Figure 6.4: The simulation results of (a) voltage-to-frequency tuning characteristic and (b)its transient response of a single output phase.

where Y_i is i-th frequency coefficient. Therefore, G. Rui et. al. proposed equation (6.4) called non-linear error δ to evaluated their linearity of V-to-F characteristic along with indicated error value by the nonlinearity term which is based on equation (6.3).

Table 6.1: Comparison with other works

Ref.	Type	Tech	Supply	Power	Output Freq	Linearity			
		nm	V	mW	MHz	nonlinearity (%)	R-square	δ(%) [8]	FOM Linearity[6]
[3]	PWM	65	2.5	-	-	-	0.99	-	-
[5]	ring-VCO	180	1.8	0.965	574-852.8	0.22	-	-	4.51x10^{-3}
[6]	ring-VCO	350	2.5	-	4-97	0.84	-	-	3.6x10^{-4}
[8]	LC-VCO	130	-	-	1980-2120	-	0.99	0.253	-
[10]	ring-VCO	28 (FD-SOI)	1	0.23	-	0.6	-	-	-
Our	ring-VCO	180	0.5	0.000465	2.0 - 13.32	0.2264	0.99	0.13	3.99x10^{-4}

$$\begin{gathered}\delta[\%] = \left(\frac{\Delta Y_{max}}{Y}\right) \times 100 \\ where, \;\; \Delta Y = Y_{3rd\ drgree\ polynomial} \\ - Y_{1st\ degree\ polynomial}\end{gathered} \tag{6.4}$$

where Y is frequency of ring-VCO. A. Steven et. al.[7] proposed the Figure of merit(FoM) to make apparent how the frequency tuning of ring-VOC improves along with its linearity V-to-F tuning improvement as expressed in equation (6.5). Their proposed FoM is a benefit to the ring-VCO, which provides widen frequency tuning whose given a smaller value to indicate the high performance.

$$\begin{gathered}FoM_{\,linearity} = \left(\frac{Nonlinearity\_error\ [\%]}{Percent\ \ Change\ \ in\ \ Frequency\ [\%]}\right) \\ where, \;\; Percent\ \ Change\ \ in\ \ Frequency\ [\%] = \\ \left(\frac{F_{Max} - F_{Min}}{F_{Min}}\right) \times 100\end{gathered} \tag{6.5}$$

The comparison of linearity improvement with related works are given in Table 1. The VCOs in [6] and [8] have estimated their linearity using Figure of merit (FoM) of linearity, and nonlinear error ($\delta[\%]$), respectively. We also calculated the linearity of our ring-VCO by their equations. Besides R-square, the linearity metrics which has a smaller value indicates higher performance.

6.3.2 Transient analysis of overall system

Figure 6.5 shows the overall system operation. The ring-VCO generates pulses along with the input voltage. When the ring-VCO output and the PWM signal from the external input are given to the AND gate, it results in a

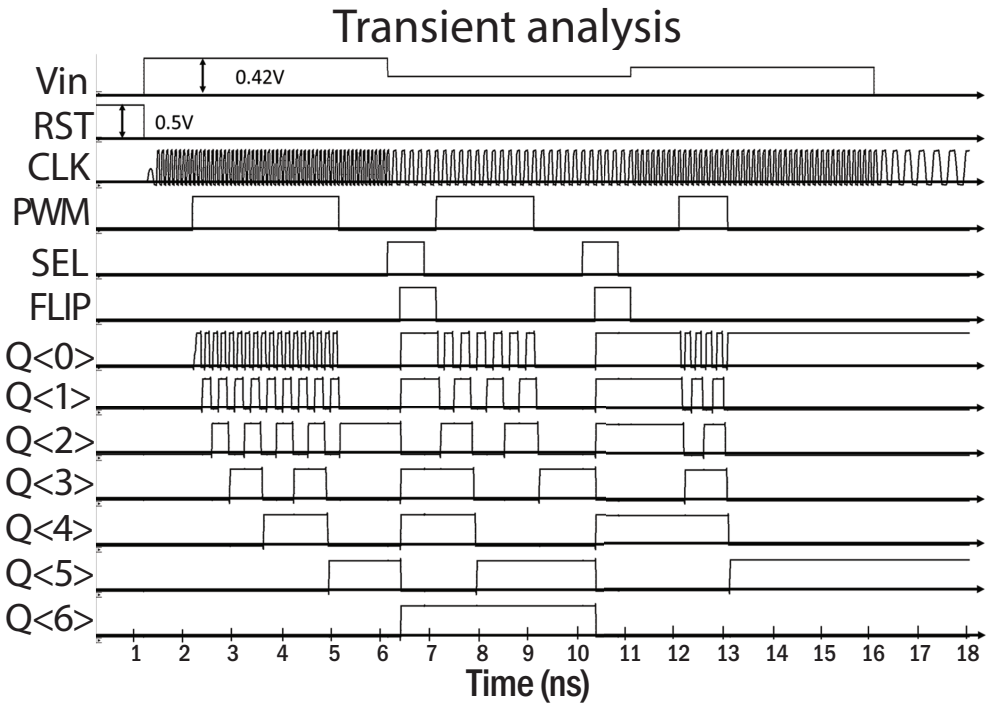

Figure 6.5: Simulation: Transient response of the neuron processing circuit incorporating our ring-VCO-based ReLU circuit by the amplitude of signal PWM, SEL, $FLIP$ and $Q < 6 : 0 >$ at 0.5V.

multiplication like operation and the output are number of pulses. The counter counts these pulses. In case of operation for negative weights, the counter generates complementary numbers by performing connection switching. The subtraction is then performed by up-counting the result of the multiplication between the VCO output and the PWM signal as shown in figure 6.6. The subtraction is completed by complementing the result obtained. Our counter uses a complement generation using two control signals SEL and FLIP. The signal SEL separates each D-FFs of the counter, and the FLIP turns over each D-FFs state simultaneously. The positive weight processing in sum-of-products operation follows the first operation sequence.

6.3.3 Compensation technique for process variations

Figure 6.7(a) shows the simulation result from the corner case, where nonlinearities are obviously observed in the Fast-Fast (FF) and Slow-Slow (SS) corners

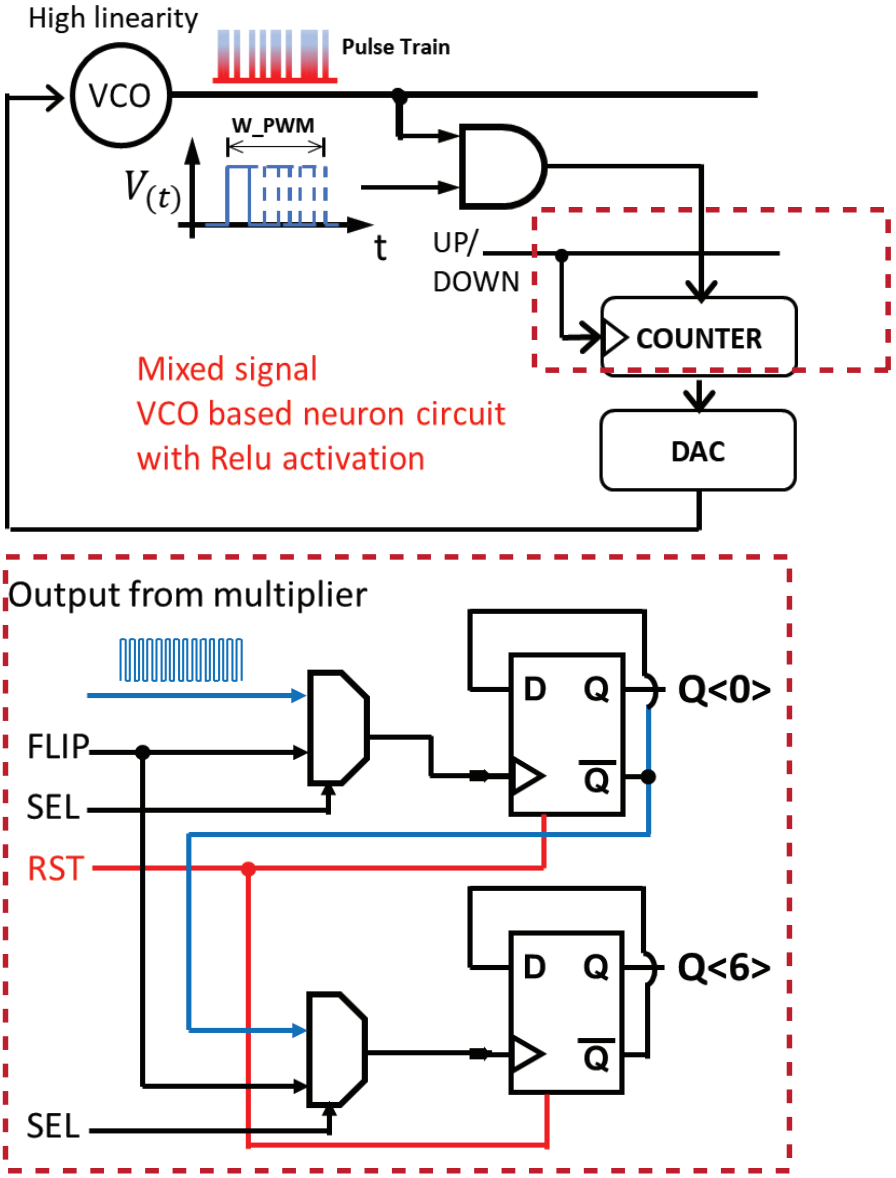

Figure 6.6: Our counter uses a complement generation using two control signals SEL and FLIP.

with linearity 97.8% and 91.8% respectively. These are due to the supply voltage dependence of the current source/sink circuit. Ring-VCO in the SS case is obtained with insufficient current bias; thus, the frequency drops compared to the other. The input offset in Slow-Fast (SF) corner is due to the offset of the current source/sink circuit. The input offset in Slow-Fast (SF) corner is due to the offset of the current source/sink circuit. Therefore, the linearity compensation operation is made with the following guidelines. This can be handled from the V_{IN} input by the DAC and the measurement of the counter value obtained.

1. VDD adjustment - provides adequate operation of the current source/sink circuit.
2. Gain and bias adjustment - gain can be treated as a multiplication factor of the overall weights. At the same time, the offset can be treated as the overall bias value. Therefore, the initial value of the counter should be given externally as a constant bias value.

In addition, gain compensation can be completed by generating PWM by multiplying all the weights by a certain factor. Therefore, the only analog adjustment is VDD. Figure 6.7(b) shows the simulation results of compensation by adjusting VDD. Although adjusting VDD can improve linearity from the corner case to 99%, the corner case of the implemented circuit might operate at the same supply voltage. Figure 6.7 (c) shows the gain and bias compensation results, and it can be observed that the same V-to-F characteristics and supply voltage operation are obtained. The other works which are related to ReLU activation function ([3],[8]), evaluated linearity of the V-to-F characteristics using R-squared metric. We also studied R-squared to evaluate whether the corner case in nonlinearities of the ring-VCO-based ReLU activation circuit is affected by the performance of the pulsed neural network. The comparison cases are for linearity improvement by VDD adjustment and gain and bias adjustment. The pulsed neural network is constructed in four (784/64/64/10) layers, simulating these systems with MNIST in Python programming through 100 epochs. MNIST

benchmark has been normalized training and testing data in the tuning range of ring-VCO operation (-0.4,0.4).

The validated accuracy results are shown in figure 6.8. Here, Fig. 6.8(a) indicates the best case (97.4%) and worst case (96.4%) of their average validation accuracy from five possible corners (in Fig. 6.7(a)). Figure 6.8(b) shows the validation accuracy of five possible corners with compensation by adjusting VDD. Average validation among five possible corners are approximately 97%, and figure 6.8(c) shows the gain and bias compensation results. It can be observed that the same characteristics are obtained. Moreover, we also determine accuracy results of our pulse ReLU by comparison with other activation function as shown in figure 6.8. The validated accuracy result is characteristic as similar as linear activation function.

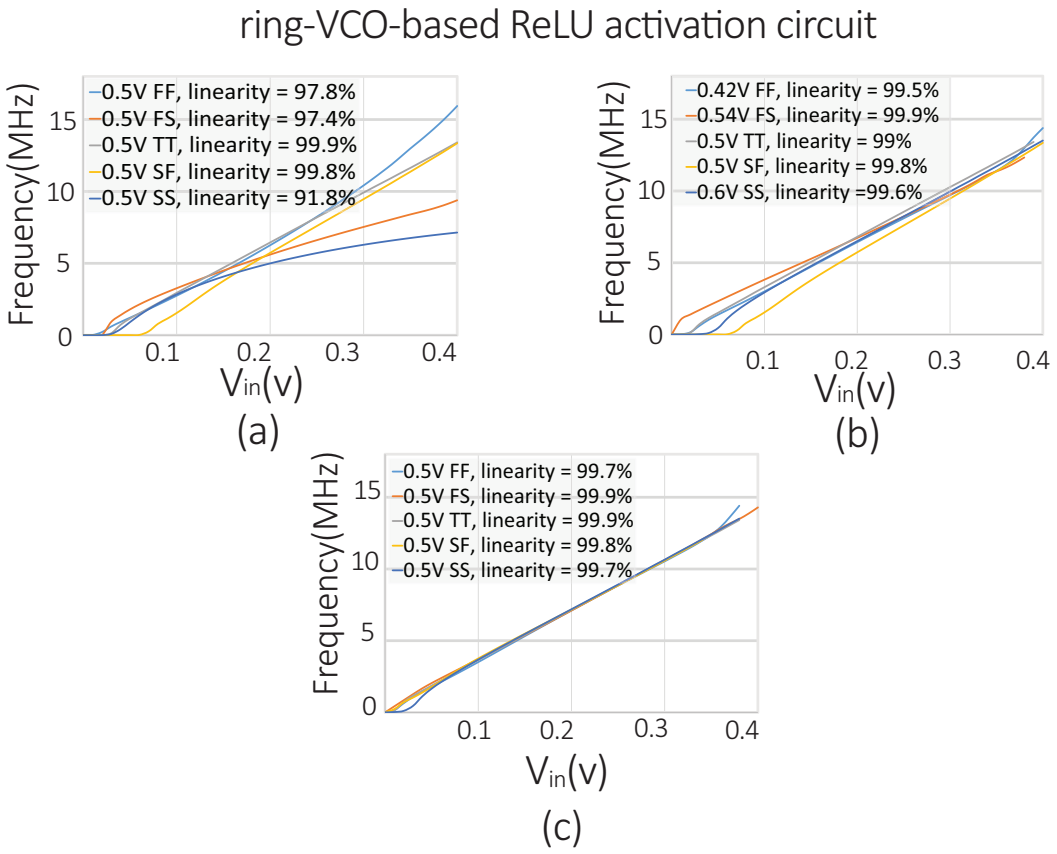

Figure 6.7: The simulation results (a) nonlinearity V-to-F characteristic from corner case with the result of (b) its compensation by VDD adjustment and (c) its gain and bias compensation.

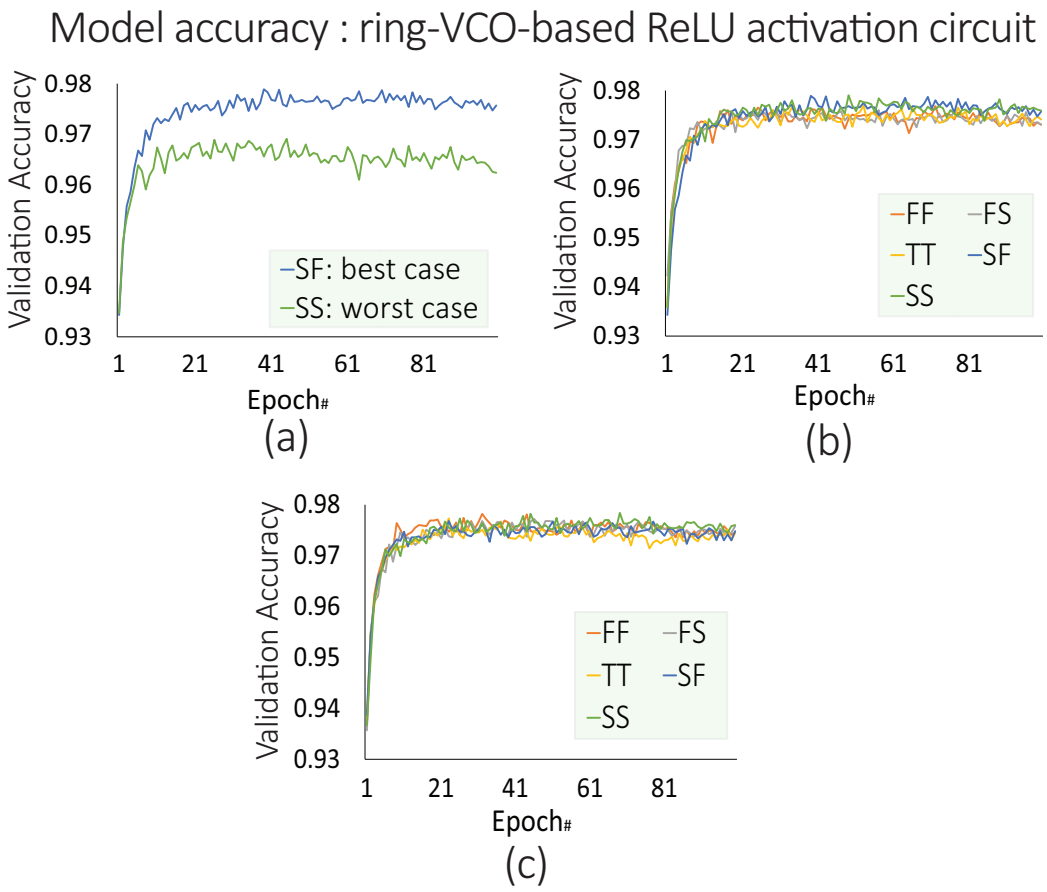

Figure 6.8: The model accuracy of ring-VCO-based ReLU activation circuit (a) from best and worst case of process corner with the result of (b) compensation by VDD adjustment and (c) its gain and bias compensation.

6.4 Conclusions

In this chapter we propose a low-power pulsed neural network with improved linearity characteristics that can realize ReLU linear activation function. Furthermore, we study and demonstrate nonlinearity effect by process variation and discuss its compensation technique with simulation results of a circuit-level implementation designed in TSMC 0.18-μm CMOS technology.

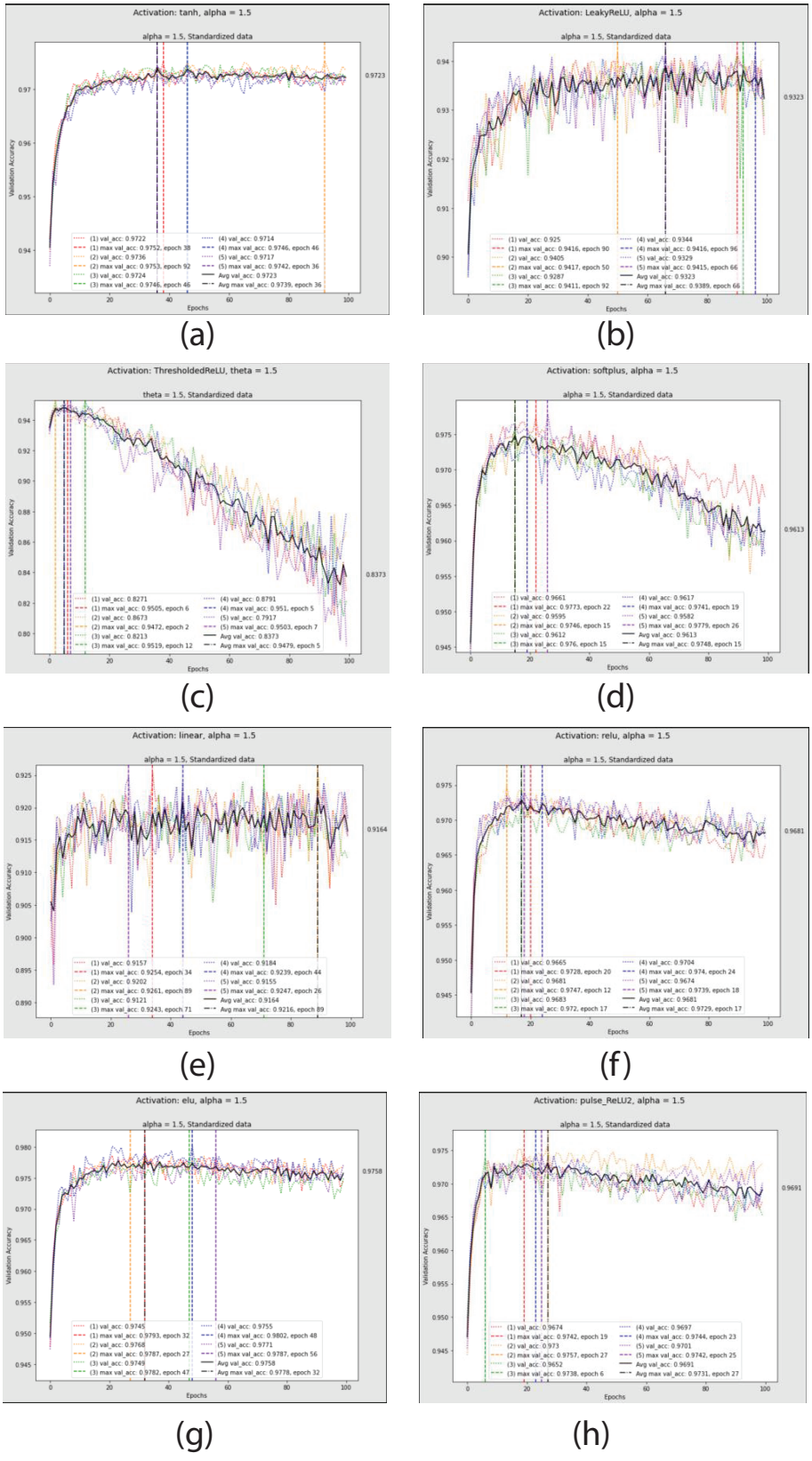

Figure 6.9: The comparision accuracy between (a) tanh function (b) LeakyReLU function (c) softpulse function (d) thresholdedReLU function (e) linear function (f) ReLU function (g) elu function and (h) pulsed ReLU function.

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7

Conclusion and future work

7.1 Thesis Summary

Our study tackles the problem of low energy smart device sensing in which the ADC circuit is fundamental component. We report ring-VCO-based ADC which can operate at low supply voltage or approximately sub-threshold voltage. Ring-VCO operate at a lower voltage that could adversely affect the linearity of the V-to-F tuning characteristic. We present the new linearity improvement technique called complementary bias voltage control to improve linearity of V-to-F characteristics. Our V-to-I converter circuit based on the proposed technique provides linear bias current source and sinks matching along with control voltage for current starved inverter-based delay elements without using body bias.

We present the fully pseudo-differential current-starved inverter-based delay. We also modified the fully pseudo-differential current-starved inverter-based delay to achieve smaller transistor count. Furthermore, our proposed delay element technique does not adversely affect the linearity of the V-to-F tuning characteristics. Besides, the modified ring-VCO generate higher frequency than the fully pseudo-differential one.

We applied the fully pseudo-differential current-starved inverter-based delay which is the high linearity of V-to-F characteristic for pulsed neural network serving as A/D converter along with ReLU activation function. The designed pulsed neuron circuit which can be used in DNN is benchmarked by MNIST performance, and we report average validation accuracy among ve possible corners at approximately over 97%.

7.2 Future work

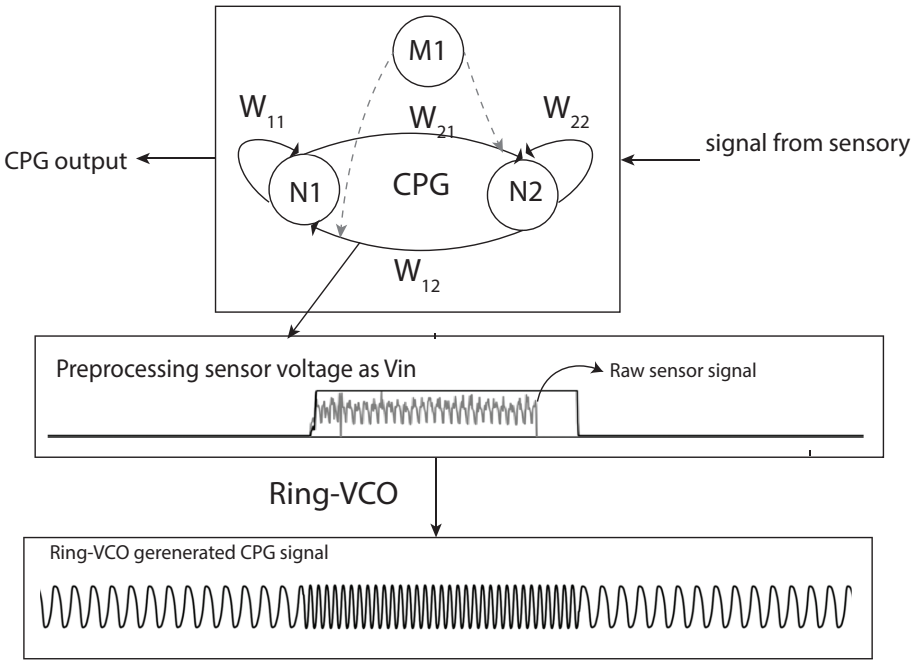

Figure 7.1: CPG-based neuron control with frequency adaptation

Currently, ring-VCO-based ADC has become a desired technique to represent pulse-based processing which is stochastic computation in machine learning. As a future perspective, we would like to apply our ring-VCO with linearity improvement to central pattern generator (CPG)-based neural control. CPG is an ensemble of neural oscillators found in vertebrate spinal cords and invertebrate ganglions that are intricately engaged in producing a variety of rhythmic patterns such as locomotion, breathing, and chewing [1], and might also use sensory

feedback to adapt their output. This section will explore the challenges and opportunities that systems have. Usually, CPG-based locomotion technology has relied on complicated CMOS analog or mixed-signal circuits to build on-chip artificial neurons and synapses with different levels of biological realism. The pulse-type hardware-based CPG requires a sub-threshold circuit technique with low power consumption and a small transistor count. We combine the CPG and CPG-based neural control [2] to explore the pulsed neural circuit for CPG-based neuron control with frequency adaptation as show in figure 7.1. Our future work will explore ring-VCO to generate CPG signal which is the raw sensor signal to regenerate the pulse signal of Vin. The CPG signal multiply pulse weight which is a form of pulse width modulation.

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Appendices

Appendix : Python code for Ring-VCO serving as ReLU function

In this appendix, we shown the python code that validated accuracy of MNIST benchmark. Those line is import the keres library, and tensorflow for the optimized the validation accuracy.

```
import keras
import keras.backend as K
from keras.datasets import mnist
from keras.models import Model, Sequential
from keras.layers import Input, Dense, Dropout, Activation
from tensorflow.keras.optimizers import RMSprop
from keras.callbacks import CSVLogger
import os
import keras.activations
import time
from keras.utils import np_utils
```

Listing 1: import necessary library

This line separated the training data set and testing data set then converter vector class to bineary class matrices.

```
(x_train, y_train), (x_test, y_test) = mnist.load_data()

num_classes = 10

x_train = x_train.reshape(60000, 784)
x_test = x_test.reshape(10000, 784)
x_train = x_train.astype('float32')
x_test = x_test.astype('float32')

print(x_train.shape[0], 'train samples')
print(x_test.shape[0], 'test samples')

# convert class vectors to binary class matrices
y_train = keras.utils.np_utils.to_categorical(y_train,
    num_classes)
y_test = keras.utils.np_utils.to_categorical(y_test, num_classes
    )
```

Listing 2: import mnist data set

This line assigned the relu activation with the custom value that we obtained from normalized curve fitting.We used the custom activation function;thus, the "$get\_custom\_object().update("name" : Activation(name))$" have been used in this code. There was a five possible process conner of Ring-VCO serving as ReLU activation function which have been evaluation their accuracy.

```
#Ring-VCO with TT process conner as ReLU activation function
def _pulse_ReLU_TT(a):
return K.maximum(0.0, ((a*1.037)- 0.0386))
get_custom_objects().update({'_pulse_ReLU_TT': Activation(
    _pulse_ReLU_TT)})

#Ring-VCO with SF process conner as ReLU activation function
def _pulse_ReLU_SF(a):
return K.maximum(0.0, ((a* 1.122)- 0.1641))
get_custom_objects().update({'_pulse_ReLU_SF': Activation(
    _pulse_ReLU_SF)})

#Ring-VCO with FS process conner as ReLU activation function
def _pulse_ReLU_FS(a):
return K.maximum(0.0, ((a* 0.968)+ 0.076))
get_custom_objects().update({'_pulse_ReLU_FS': Activation(
    _pulse_ReLU_FS)})

#Ring-VCO with FF process conner as ReLU activation function
def _pulse_ReLU_FF(a):
return K.maximum(0.0, ((a* 1.029)- 0.1125))
get_custom_objects().update({'_pulse_ReLU_FF': Activation(
    _pulse_ReLU_FF)})


#Ring-VCO with FF process conner as ReLU activation function
def _pulse_ReLU_SS(a):
return K.maximum(0.0, ((a* 1.044)+0.0889))
get_custom_objects().update({'_pulse_ReLU_SS': Activation(
    _pulse_ReLU_SS)})
```

Listing 3: Custom activation function

This line is normalized training data set and testing data set in -0.4-0.4 range corresponding to input value.

```
from scipy import stats
from sklearn import preprocessing
x_train = preprocessing.minmax_scale(x_train, feature_range
    =(-0.4, 0.4))
x_test  = preprocessing.minmax_scale(x_test, feature_range
    =(-0.4, 0.4))
print(x_train.max(),x_test.min())
print(stats.describe(x_train.reshape(60000 * 784, )))
print(stats.describe(x_test.reshape(10000 * 784, )))
```

Listing 4: Normalized training data set and testing data

This code is training and testing deep learning model for MNIST benchmark, and store the accuracy and lose value of training phase and testing phase in excel file.

```
batch_size = 64
epochs = 100
units = 64
experiments = 4
start = 0
activations = ['relu','_pulse_ReLU_TT','_pulse_ReLU_SF',
               '_pulse_ReLU_FF','_pulse_ReLU_FS','_pulse_ReLU_SS'
   ]

start_time = time.time()
counter = 0
total_items = len(activations)*experiments
num_classes = 10
for act in activations:
print("Training for activation " + act )

for i in range(experiments):

K.clear_session()
K.reset_uids()

act_dict = {
'sigmoid': Activation(keras.activations.sigmoid),
'tanh': Activation(keras.activations.tanh),
'relu': Activation(keras.activations.relu),
'linear': Activation(keras.activations.linear),
'elu': Activation(keras.activations.elu),
'softplus': Activation(keras.activations.softplus),
'softsign': Activation(keras.activations.softsign),
'hard_sigmoid': Activation(keras.activations.hard_sigmoid),
#'LeakyReLU': keras.layers.advanced_activations.LeakyReLU(alpha
   =1.5),
#'selu': Activation(keras.activations.selu),
#'ThresholdedReLU': keras.layers.advanced_activations.
   ThresholdedReLU(theta=1.0),
'_pulse_ReLU_TT':Activation(_pulse_ReLU_TT),
'_pulse_ReLU_FF':Activation(_pulse_ReLU_FF),
'_pulse_ReLU_FS':Activation(_pulse_ReLU_FS),
'_pulse_ReLU_SF':Activation(_pulse_ReLU_SF),
'_pulse_ReLU_SS':Activation(_pulse_ReLU_SS)


}

model_name = 'std_' + act + '_1.5_rmsp_' + str(i + start) + '_'
   + str(units)
inputs = Input(shape=(784,))
x = Dense(units)(inputs)
x = act_dict[act](x)
x = Dropout(0.2)(x)
x = Dense(units)(x)
x = act_dict[act](x)
x = Dropout(0.2)(x)

#the last layer is evaluated answer by Softmax funtion
```

```
predictions = Dense(num_classes, activation='softmax')(x)
model = Model(inputs=inputs, outputs=predictions)

model.compile(loss='categorical_crossentropy',metrics=['accuracy'])

#Save the accuracy value in Google Drive
csv_logger = CSVLogger('/gdrive/My Drive/7102023/%s.csv' %(model_name), append='False')
history = model.fit(x_train, y_train,
batch_size=batch_size,
epochs=epochs,
verbose=1,
validation_data=(x_test, y_test), callbacks=[csv_logger])

#indicate the evaluate value
score = model.evaluate(x_test, y_test, verbose=0)
print('Test loss:', score[0])
print('Test accuracy:', score[1])

t = time.time()
time_diff = t - start_time
counter +=1
rem_items = total_items - counter
total_time = round((total_items / counter) * time_diff)
rem_time = round(total_time - time_diff)
m, s = divmod(rem_time, 60)
h, m = divmod(m, 60)
d, h = divmod(h, 24)
print('Remaining time: %d days %d hours %02d minutes %02d seconds' % (d, h, m, s))
```

Listing 5: Training and testing deep learning model for MNIST benchmark

Python code for evaluated the r-square error

This code is evaluated the r-square error in which the actual frequency was normalized value in 0-1 range then passing though the linear regression.

```
1
2
3  import numpy as np
4  from sklearn.metrics import r2_score
5  from gekko import GEKKO
6  from scipy import stats
7  import numpy as np
8  from scipy import optimize
9  import matplotlib.pyplot as plt
10 from scipy.optimize import curve_fit
11
12 #from scipy.optimize import curve_fit
13 from pycse import deriv
14 #creating data
15 nx,ny = np.loadtxt('cfs05.txt', unpack=True)
16 x = (nx-min(nx))/(max(nx)-min(nx))
17 y = (ny-min(ny))/(max(ny)-min(ny))
18 for X in x:
19 print(X)
20 for Y in y:
21 print(Y)
22 #creating OLS regression
23 slope, intercept, r_value, p_value, std_err = stats.linregress(x
       ,y)
24 def linefitline(b):
25 return std_err+intercept + slope * b
26 line1 = linefitline(x)
27 print("stderre",std_err)
28 print("intercept",intercept)
29 print("slope",slope)
30
31 r2 = r2_score(y, linefitline(x))
32 ans = 1-r2
33 print('The rsquared value is: ' + str(r2))
34 print('The nonlinearity error is: ' + str(ans))
```

Listing 6: r-square error

Achievement

Journal publication:

- Srikram, P., Ikebe, M., and Motomura, M. (2022). Linearity Improvement of VCO-Based ADC via Complementary Bias Voltage Control for IoT Devices. Journal of Signal Pro- cessing, 26(1), pp. 1-12.

International Conference publication:

- Srikram, P., Ambalathankandy, P., Motomura, M., and Ikebe, M. A 0.5 V Modified Pseudo-Differential Current-Starved Ring-VCO with Linearity Improvement for IoT Devices. 2023 International Electrical Engineering Congress (iEECON), 2023,in press
- Srikram, P., Ambalathankandy, P., Kanazawa, Y., Motomura, M., and Ikebe, M. (2022, October). Ring-VCO-based ReLU activation function with linearity improvement for pulsed neuron circuits. In 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS) (pp. 1-4). IEEE.
- Srikram, P., and Thongtak, A. (2017, March). Distributed Lock Relation for Scalable-Delay-Insensitive Circuit Implementation Based on Signal Transition Graph Specification.In International MultiConference of Engineers and Computer Scientists (pp. 185-198). Springer, Singapore.
- Srikram, P., and Thongtak, A. (2015, June). Scalable-Delay-Insensitive Optimization based on Lock Relation. In ITC-CSCC: International Technical Conference on Circuits Systems, Computers and Communications (pp. 786-789).
- Srikram, P., and Thongtak, A. (2014). A Design of Asynchronous Control Circuit Based on SDI Model. In Proc. Proceedings of the International MultiConference of Engineers and Computer Scientists (pp. 728-732).