A study on sensitivity to an embedded nanostructure in a micrometer-channel-length Si MOSFET

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Abstract

Nano-artifact metrics is an information security technology that uses a nano-scale random structure as a unique identifier, expected to provide secure authentication in the IoT (Internet of Things) era. For electrical discrimination of the two-dimensional random nanostructure in terms of nano-artifact metrics, we investigated the sensitivity to the nanostructure in a Si MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) with a micrometer channel length in a simulation and experiment. The device simulation showed that the sensitivity was increased by decreasing channel length and increasing the height of the nano-convex structures. It also showed the device with a 10 μm channel length could detect a nano-convex. On the other hand, the fabricated Si MOSFET with a 50-nm-height nano-convex showed lower nanostructure sensitivity than that expected in the simulation. A detailed analysis indicated that the degradation of the sensitivity was attributed to the fabrication process issues including unintentional reduction of the convex size and high source and drain resistance.

1. Introduction

Toward Industry 4.0 and Society 5.0, in which a huge number of Internet of Thing (IoT) devices connect to the internet [1-5], highly secure authentication and identification technology must be developed. For strong authentication/identification preventing digital counterfeit, a physical unclonable function (PUF) technique has been attracted the attention recently [6,7]. Various physical properties in materials [8-10], devices [11-14], and circuits [15,16] have been investigated. Nano-artifact metrics (NAM) is a novel authentication technology that utilizes the physical characteristics of the nanometer-scale artifacts with randomness [17]. Because of the difficulty in counterfeiting a nano-scale structure, NAM can provide secure authentication and identification beyond the commercially available technology on the basis of the micro-scale fabrication and characterization techniques. As a feasible approach to produce a nano-scale identifier compatible with the Si chip fabrication process, two-dimensional (2D) random Si nano-patterns using resist collapse phenomena have been investigated [17,18].

A key issue in NAM is to develop a convenient way to read out the nano-scale pattern. For the practical application, the pattern observation using a scanning electron microscope (SEM) is not feasible. For a compact, fast, and low-cost approach, we proposed an electrical identification method using a Si metal-oxide-semiconductor field-effect transistor (MOSFET) [19,20]. A Si MOSFET possesses a high charge sensitivity that can detect the atomic level information [21]. In our approach, the nano-pattern is embedded in between the gate insulator and the channel in the Si MOSFET. The pattern information is transferred to the drain current. Prototype devices embedding nano-convex structures have been fabricated, and modulation of the drain current has been observed [22]. However, the fabricated device often showed smaller current modulation than that expected from the device simulation. Against this background, in this paper, we investigate the sensitivity to the nanostructures embedded in a micrometer-channel-length Si MOSFET in an experiment and device simulation.

2. Concept and Design for High Sensitivity

In nano-artifact metrics, a two-dimensional random nano-pattern as shown in the left-hand-side photograph in **Fig. 1(a)** is used as an identifier. This pattern is formed using the resist collapse phenomena [23,24]; 300-nm-high resist pillars with a square cross-section 60 nm on each side are formed on a Si substrate at intervals of 200 nm using electron-beam lithography. The pillars are collapsed during the rinsing process after development. Then, the collapsed resist pattern is transferred on the Si substrate by dry etching [17]. For electrical discrimination, the nano-pattern is embedded just below the gate of a Si MOSFET as shown in **Fig. 1(a)**. In this figure, the *y*-direction is along the channel and the *z*-direction is lateral to the channel. The discrimination/identification is carried out by measuring the drain current-voltage (I_{DS}–V_{DS}) curve; the I_{DS}-V_{DS} curve has a unique configuration correlated with the nano-pattern as shown in **Fig. 1(b)**.

For detecting the nano-pattern information in the *y*-direction, we use the V_{DS} dependence of the channel pinch-off position, L_P. Assuming that I_{DS} in the saturation region is independent on L_p, I_{DS} in an n-channel MOSFET is deduced from the gradual channel approximation as follows [22].

$$I_{DS} = We\mu_n n(L_p)E(L_p), \qquad (1)$$

where W is the channel width, e is the elementary charge, μ_n is the electron mobility, and $n(y)$ and $E(y)$ are the electron density and the electric field at position y, respectively. This equation indicates that I_{DS} in the saturation region is determined by the carrier density and the electric field along the channel at the pinch-off position. When the nanostructure is embedded in the gate area, the product of the charge density and the electric field becomes non-uniform in space. Taking into account that L_p is shifted from the drain to the source as V_{DS} increases, I_{DS} is expected to be perturbed from that in the device without the nanostructure. The spatial

resolution is considered to be given by the Debye length in the channel. On the other hand, the nano-pattern information in the *z*-direction is detected by the multiple narrow gates. By applying appropriate gate voltage at an arbitrary position z_i, the narrow gate can form an electrically isolated narrow inversion channel at z_i. The spatial resolution is determined by the physical gate width and interval.

We investigated the sensitivity to the nanostructure in the n-channel Si MOSFET using a 2D device simulator, Atlas/S-Pisces (Silvaco, Inc.). In this simulation, the drain current was calculated by using a conventional drift-diffusion current model under the field-dependent mobility based on the Lombardi model. The donor concentration in the n^+ source and drain wells was 10^{20} cm^{-3}, and their resistivity was 10^{-3} Ω·cm. The well area has a rectangular shape with an abrupt interface. The junction depth was 0.2 μm. No contact resistance was assumed for the source and drain in the simulation. Al having a work function of 4.10 eV was assumed for the gate metal. The simulated device had a nano-convex structure between the channel and the gate oxide as shown in **Fig. 2(a)**. The acceptor concentration of the p-Si substrate N_A was 10^{17} cm^{-3}, the channel width W was 1 μm, and the gate oxide thickness t_{ox} was 10 nm. **Figure 2(b)** shows simulated I_{DS}-V_{DS} curves for various channel length L. The nano-convex height H and width D were 10 and 100 nm, respectively. The position of the convex from the drain edge ΔD was 100 nm. In this figure, each I_{DS}-V_{DS} curve is normalized by the saturation current in the device without the convex. The result shows that the change in the drain current is increased by reducing L, indicating the high nanostructure sensitivity. It also shows that the nano-convex can be detected even in the 10-μm-channel-length MOSFET. The rate of change in I_{DS} at V_{DS} = 3 V as a function of L is plotted in **Fig. 2(c)**. The sensitivity to the embedded nanostructure is inversely proportional to L. This behavior is similar to the L dependence of the transconductance g_m. Here, it should be mentioned that a longer channel length is desired in terms of security, because the embedded nano-pattern can become more complicated as its area

becomes large, which helps to avoid counterfeiting. This means that there is a trade-off between the sensitivity and the secureness in terms of L.

Another important parameter involved in the sensitivity is the nano-convex height, H. It can be controlled by changing the etching depth for transferring the collapsed resist pattern to the substrate. **Figure 2(d)** shows the simulated I_{DS}-V_{DS} curves for various H. The change in the normalized drain current is increased by increasing H. On the other hand, the rate of change becomes small as H becomes high as shown in **Fig. 2(e)**. This means that the drain current becomes insensitive to the change in the convex height ΔH when H is large. If the variation in H is associated with the complexity of the identifier, H needs to be optimized. In addition, the nano-convex width also affects the I_{DS}-V_{DS} curve; the wider convex results in a wider drain voltage range where the drain current is decreased [20]. Thus, the convex width impacts the sensitivity less than the convex height.

To understand the effect of a nano-convex on the drain current, we checked inside the device using the device simulation. **Figure 3** shows the simulated spatial distribution of electrons in the device for various H. The current flow is also shown by small arrows. It is found that the electrons distribute along the SiO_2/Si interface and the current also flows along the interface. Accordingly, the convex twists the electron channel along the SiO_2/Si interface and disturbs the smooth current flow, resulting in the reduction of I_{DS}. However, when H is larger than 30 nm, the carriers come into flowing the entire convex in parallel with the interface, which makes the current less sensitive to the variation in H as shown in **Fig. 2(e)**. In this manner, the path of the carrier transport is made complicated by the embedded nano-convex. The one-dimensional model in **Eq. (1)** could not show this picture sufficiently. The complicated path exists even when V_{DS} is small, hence the drain current in the linear region is also decreased as shown in **Figs. 2(b)** and **2(d)**. Consequently, the sensitivity to the nanostructure in the device is available in a wide drain voltage range.

3. Experiment

We fabricated the n-channel Si MOSFETs with a nano-convex, characterized and compared with the results from the device simulation. **Figure 4** shows a photograph of the fabricated device with a schematic cross-sectional view. The devices were fabricated using standard photolithography on a (001) p-Si substrate with acceptor concentration N_A of 1×10^{17} cm^{-3} . The device mesa for isolation was formed by wet etching. Then n^+ wells for source and drain were formed by the phosphorus ion implantation. After RCA cleaning, a 30-nm gate oxide was formed by the thermal oxidation in dry O_2 at 950 ºC for 50 min. The source, drain, and gate metal electrodes were formed by the Al deposition and the lift-off technique. Annealing was made at 400 ºC for 10 min in the forming gas composed of 5% hydrogen in 95% nitrogen, to obtain ohmic contacts and to improve the SiO_2/Si interface characteristic. Before the RCA process, a nano-convex stripe across the channel was formed by using electron-beam lithography and dry etching. The channel length was L = 2 μm, which was smaller than that of the previously reported devices with L = 7 and 12 μm [22]. The channel width W was 10 μm. The nano-convex was placed at ΔD = 300 nm from the drain edge. The designed nano-convex height was H = 50 nm to clearly show the effect of the embedding nano-convex, which was larger than 30 nm in the previous device [22]. The electrical measurement was made on the fabricated devices at room temperature by using a conventional semiconductor parameter analyzer.

4. Results and Discussion

Figure 5 shows I_{DS}-V_{DS} characteristics of the MOSFETs with and without a nano-convex obtained from the simulation and experiment. All device dimensions were the same between the simulation and the experiment except W. The same gate voltages were applied in all plots. The simulation results showed that the current was greatly reduced by the nano-convex.

On the other hand, the overall change in the drain current in the fabricated device with a convex (**Figs. 5(b)**) was unclear compared with the simulation result in **Fig. 5(a)**. A slight increase of the drain conductance in the saturation region could be observed in the fabricated device with the convex, but this was not seen in the devices without the convex in **Fig. 5(d)**. Thus, the observed slight increase of the drain conductance may be attributed to the nano-convex. However, the drain current in the linear region behaved almost the same as that in the device without the convex. In addition, in the fabricated device without the nano-convex, the drain current was much smaller than the simulation result. The estimated saturation current at $V_G - V_{th} = 3$ V from the gradual channel approximation was 390 μA/μm, thus the simulation result was reasonable and the current in the fabricated device was unexpectedly small.

Figure 6 shows the transfer characteristics in the devices with and without a nano-convex. Estimated device parameters from the transfer characteristics are summarized in **Table I**. The curves were measured at $V_{DS} = 5$ V. We separately found on-chip V_{th} variation in the fabricated devices, although V_{th} in the fabricated device without the convex reasonably agreed with that from the simulation as shown in **Table I**. Therefore, to see the intrinsic effect of embedding the nano-convex avoiding such variation, we measured the drain current by switching the source and drain electrodes and compared the results. In the simulation result, V_{th} was greatly increased by the nano-convex and became larger than 3 V as shown in **Fig. 6(a)**. This large V_{th} shift made the drain current disappear in **Fig. 5(a)**. It was also found that V_{th} was changed by switching the source and drain electrodes. This shift was not seen in the device without the convex as shown in **Fig. 6(c)**. The fabricated device with the convex did not show such large V_{th} shift as shown in **Fig. 6(b)**, whereas the small shift was caused by switching the source and drain. This shift was not seen in the fabricated device without the convex as shown in **Fig. 6(d)**. The relationship among the source/drain electrodes and the V_{th} shift direction was the same between the simulation and the experiment. Therefore, the observed V_{th} shift in the

fabricated device was considered to arise from the convex. The V_{th} shift by switching the electrodes could be understood by the same mechanism as the drain induced barrier lowering [25]. When the convex was located in the drain side, the potential hill on the channel induced by the convex was pulled down by the drain voltage, resulting in the decrease of V_{th}. On the other hand, when the convex was located in the source side, the potential hill was not affected by the drain voltage, so V_{th} remained high.

It is known that the nano-scale effect of the carrier transport reflects well in the subthreshold current [26,27]. **Figure 7** shows the subthreshold currents obtained from the simulation and experiment. It was found that the nano-convex affected the subthreshold current in terms of the V_{th} shift. In addition, the subthreshold slope (*SS*) was increased by the nano-convex in both the simulation and experiment. The evaluated *SS* values are summarized in **Table I**. The *SS* values in the fabricated device were larger than those in the simulation, whereas they were not changed by switching the electrodes. We considered that the nano-convex-induced increase in *SS* was attributed to the V_G dependence of the convex-induced potential hill in the channel. Specifically, when the electrons in the channel are decreased by decreasing V_G, the electric field from the nano-convex portion can reach the channel without screening by the electrons. Then, the potential hill is reduced and the electron flow is increased, resulting in the increase of *SS*.

In **Fig. 8**, we compare the I_{DS}-V_{DS} curves when the convex is located at the drain side and the source side by exchanging the source and the drain. Here all curves were measured at $V_G - V_{th} = 3.2$ V. The configuration of the curve was changed by changing the nano-convex position as shown in **Figs. 8(a)** and **8(b)**. In both the simulation and experiment, the convex located at the drain side increased the drain conductance in the saturation region, whereas the currents in the linear region did not depend on the convex position. The nonlinear curve in the low V_{DS} region in **Fig. 8(a)** indicated the existence of the potential hill in the channel. When

V_{DS} was small, the potential hill was hardly affected by V_{DS} even when the hill position was changed. However, such reduction of the current did not appear in the fabricated devices with or without the convex as shown in **Figs. 8(b)** and **8(c)**. The almost normal current in the linear region suggested that the convex-induced potential barrier was small, with a height that might be comparable to or less than the thermal energy.

To understand the unexpectedly small effect of the nano-convex in the fabricated device, the configuration of the nano-convex is discussed. **Figure 9(a)** shows a SEM image of the convex cross-section in the test sample. In this sample, designed dimensions were D = 100 nm and H = 30 nm. The image indicated that the shape of the convex was changed from rectangle to trapezoid, and the size itself was reduced simultaneously. The observed structural change was possibly attributed to the RCA process for Si surface cleaning and the thermal oxidation for the gate insulator formation. It was reported that the latter process reduced the Si nanostructure size [27]. Then, we examined the effect of the change in the nano-convex shape on the drain current using the device simulation. As shown in **Fig. 9(b)**, when the nano-convex cross-section was trapezoid, the drain current increased compared with that in the device with the rectangular convex. The effect of the change in the cross-sectional shape of the convex was similar to the decrease in the convex height in **Fig. 2(d)**. This similarity was also seen in the potential landscape as shown in **Figs. 9(c)** and **9(d)**. From the discussion above, the weakened current modulation in the fabricated device was partly attributed to the change in the cross-section shape together with the reduction of the height of the nano-convex from those of the design. Although at present, we cannot observe the actual shape and size in the fabricated MOSFET, the observed current change suggested that the convex was smaller than that in **Fig. 9(a)**. To obtain the clear current modulation in the fabricated device, the fabrication process should be optimized to prevent the change in the cross-section shape of the embedded convex, such as using highly anisotropic etching and reducing the gate oxide thickness.

We also considered the unexpectedly small saturation I_{DS} and g_m in the fabricated device. The fabricated device without convex showed an effective mobility of 334 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which was one fifth of that from the simulation and the electron mobility in a bulk Si. Considering that the capacitance-voltage characteristics in the test MOS diode were normal, a possible reason was a large source resistance R_S. Assuming that the decrease in g_m is completely attributed to R_S, the effective g_m is given by $g_{m\_eff} = g_{m0}/(1+g_{m0} \cdot R_S)$, where g_{m0} is intrinsic transconductances [29,30]. Then R_S is estimated to be 20 kΩ by considering that g_{m_eff} and g_{m0} are given by the experimental and simulated values. This resistance value corresponds to the contact resistance of $4x10^{-2}$ $\Omega \cdot cm^2$, which is much larger than the conventional value less than 10^{-4} $\Omega \cdot cm^2$ [31,32]. This estimation suggests that the ohmic contact formation process also needs to be improved to achieve high sensitivity to the nanostructure as well as the high transconductance. There is still a possibility that the SiO_2/Si interface states caused the degradation of the gate controllability. Further study is necessary to identify the reason for the observed low g_m for achieving high nanostructure sensitivity.

6. Conclusions

For electrical discrimination of the two-dimensional random nanostructure in terms of nano-artifact metrics, we investigated the sensitivity to the embedded nano-convex in Si MOSFETs with micrometer channel lengths. From the device simulation study, the drain current was found to be modulated by embedding a nano-convex in the channel even with a channel length of 10 μm. The sensitivity to the nanostructure was increased by decreasing the channel length and/or by increasing the convex height up to 50 nm. However, the fabricated Si MOSFET with a 50-nm-height nano-convex showed smaller nanostructure sensitivity than that expected from the simulation. The analysis on the fabricated devices indicated that the degradation of the sensitivity was attributed to the fabrication process issues including

unintentional reduction of the convex size and high source and drain resistance. To achieve the high nanostructure sensitivity experimentally, the fabrication process needs to be optimized to form a convex with a sharp rectangular cross-section and low-resistance ohmic contacts. Our findings contribute to enabling the electrical discrimination of the nano-scale pattern, which will be indispensable for the practical use of nano-artifact metrics as a secure authentication and identification technology in the IoT era.

Acknowledgments

This research was supported by NEDO “Research and Development of Basic Technologies for Cross-sectional Security Evaluation of AI Edge Devices” (JPNP16007).

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Figure Captions

Fig. 1 Concept of electrical discrimination of 2D nano-pattern using Si MOSFET. (a) Device structure and (b) electrical structure detection in *y*-direction.

Fig. 2 Nanostructure sensitivity in n-channel Si MOSFET evaluated using 2D device simulation. (a) Device structure and dimensions, (b) simulated I_{DS} - V_{DS} curves with a nano-convex for various L at V_G = 3 V and H = 10 nm, and (c) rate of change in normalized I_{DS} vs. L at V_{DS} = 3 V. (d) Simulated I_{DS} for various convex heights at V_G = 3 V and L = 1 μm and (e) rate of change in normalized I_{DS} vs. H at V_{DS} = 3 V.

Fig. 3 Electron and current distributions in nano-convex-embedded MOSFETs at V_G = 3 V and V_{DS} = 3 V. (a) H = 0 nm (without convex), (b) H = 10 nm, (c) H = 30 nm, and (d) H = 50 nm.

Fig. 4 Photograph of fabricated device and its schematic cross-section.

Fig. 5 I_{DS}–V_{DS} characteristics of n-channel Si MOSFETs without and with a nano-convex. (a) Simulation with convex, (b) experiment with convex, (c) simulation without convex, and (d) experiment without convex.

Fig. 6 I_{DS}–V_G characteristics of n-channel Si MOSFETs without and with a nano-convex: (a) simulation with convex, (b) experiment device with convex, (c) simulation without convex, and (d) experiment device without convex.

Fig. 7 Subthreshold drain current in n-channel Si MOSFETs with a nano-convex by switching source and drain electrodes from (a) simulation and (b) fabricated devices. Current from the device without convex is also shown in each plot.

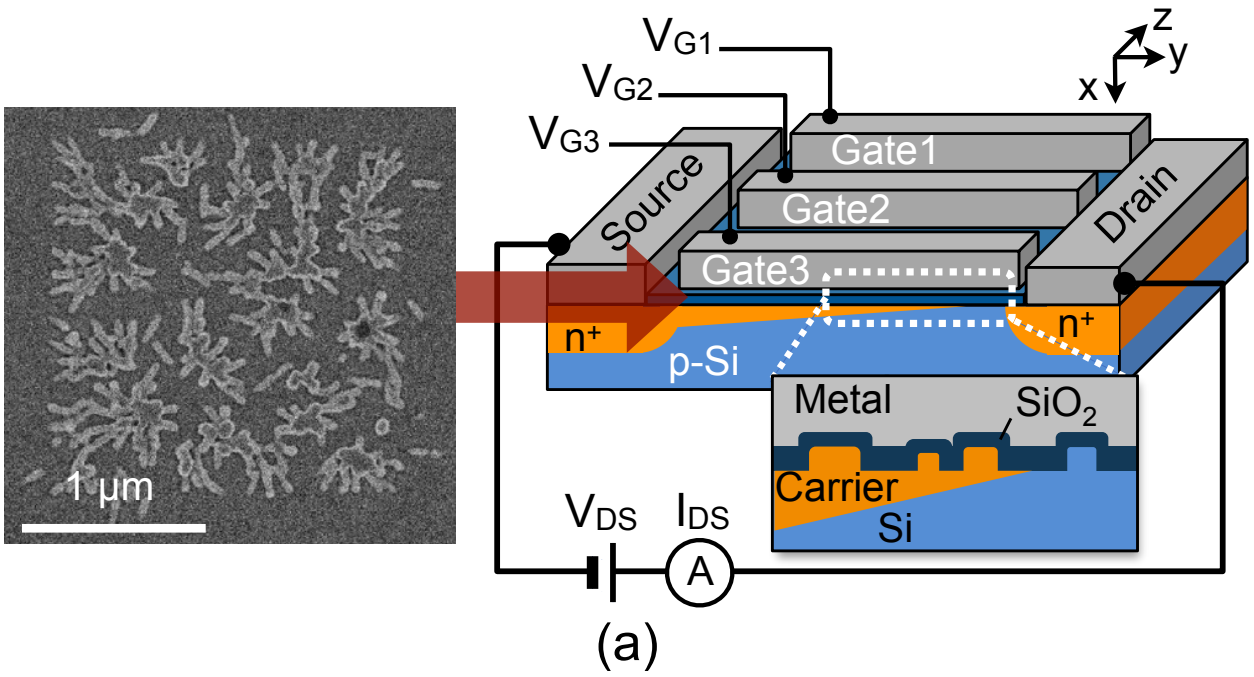
Fig. 8 I_{DS}–V_{DS} characteristics of n-channel Si MOSFETs measured by switching source and drain electrodes. (a) Simulation with convex, (b) experiment with convex, and (c) experiment device without convex. All measurements were carried out at V_G - V_{th} = 3.2 V.

Fig. 9 (a) Cross-sectional SEM image of nano-convex in a test device after thermal oxidation, (b) simulated I_{DS}–V_{DS} characteristics of n-channel Si MOSFETs with a trapezoidal and rectangular convexes, and simulated spatial distribution of electrons in devices with (c) a trapezoidal convex and (d) a rectangular convex.

Table I

Estimated device parameters from transfer characteristics in simulation and experiment.

	Simulation			Experiment		
Parameters at V_{DS} = 5 V	Convex drain side	Convex source side	Without convex	Convex drain side	Convex source side	Without convex
V_{th} (V)	3.2	4.0	0.18	-0.5	-0.2	0.19
ΔV_{th} from without convex (V)	+3.02	+3.82		-0.69	-0.39	
ΔV_{th} by switching S and D (V)	-0.8			-0.3		
Effective mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)			1760			334
g_m (mS/μm) at V_G-V_{th} = 3.2 V	0.026	0.030	0.161	0.046	0.048	0.050
SS (V/dec)	0.56	0.63	0.087	0.90	0.84	0.36



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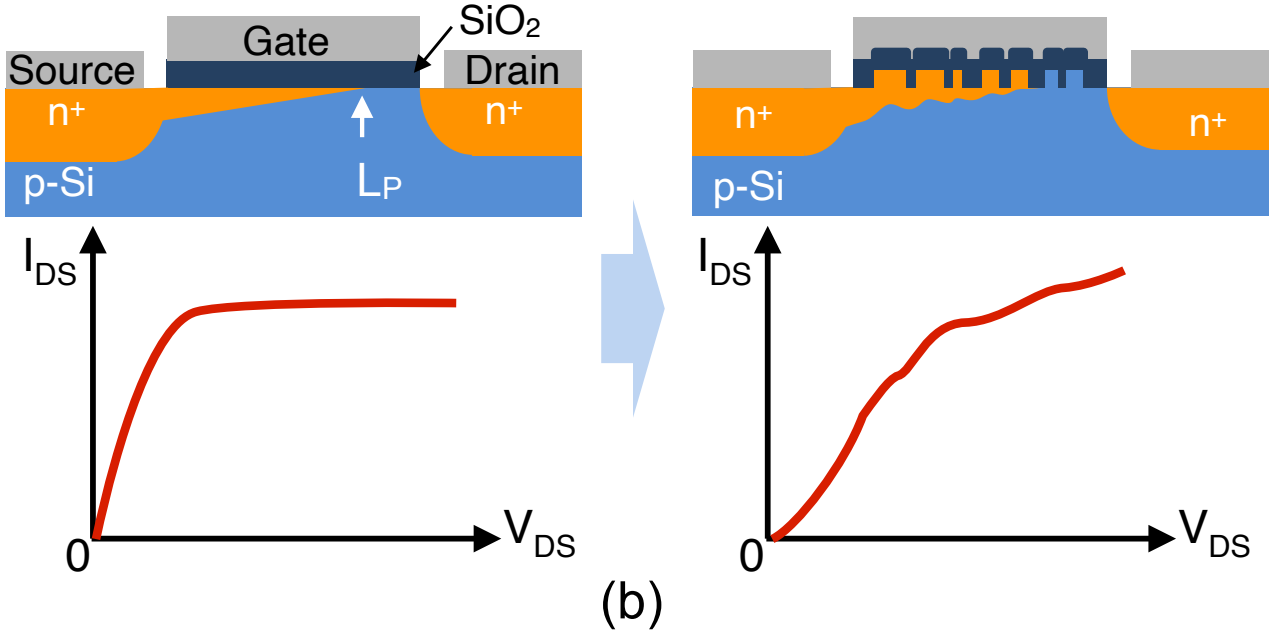

(b)

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Figure 1

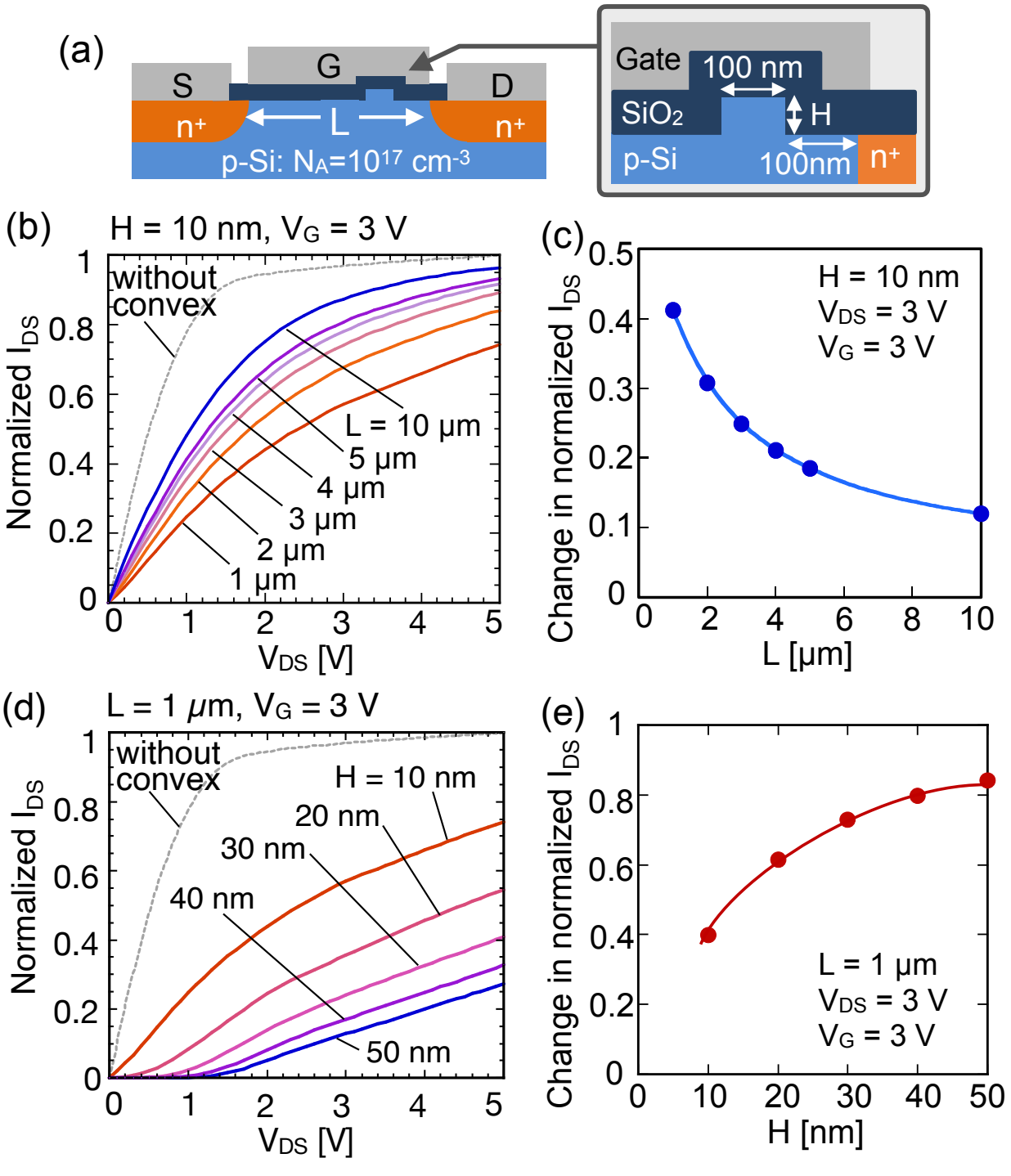

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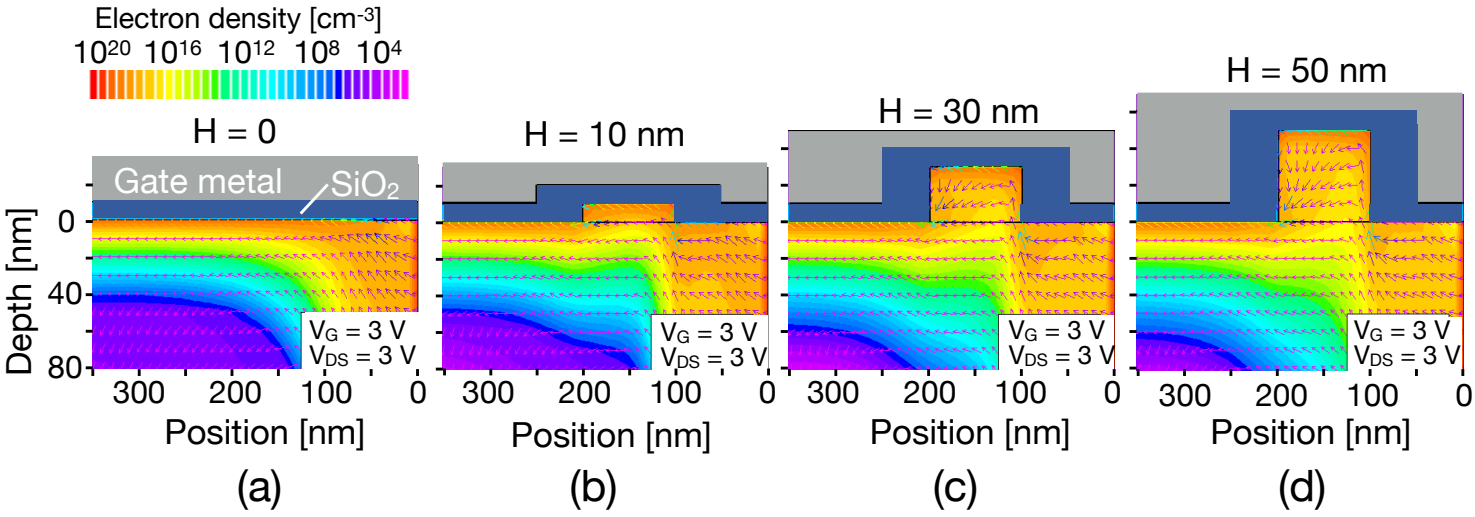
Figure 2



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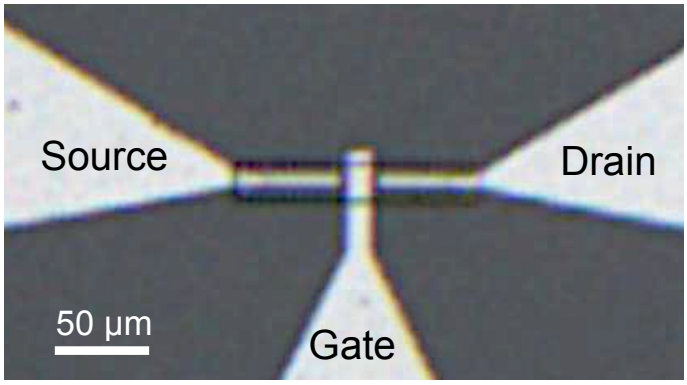

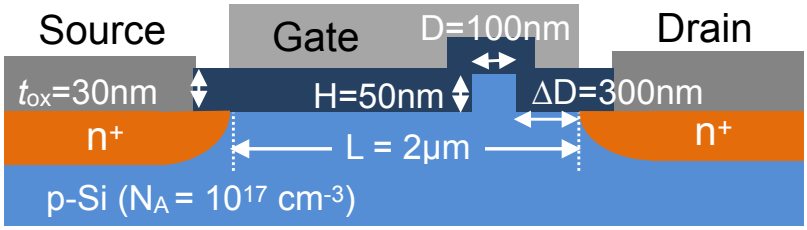

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Figure 4

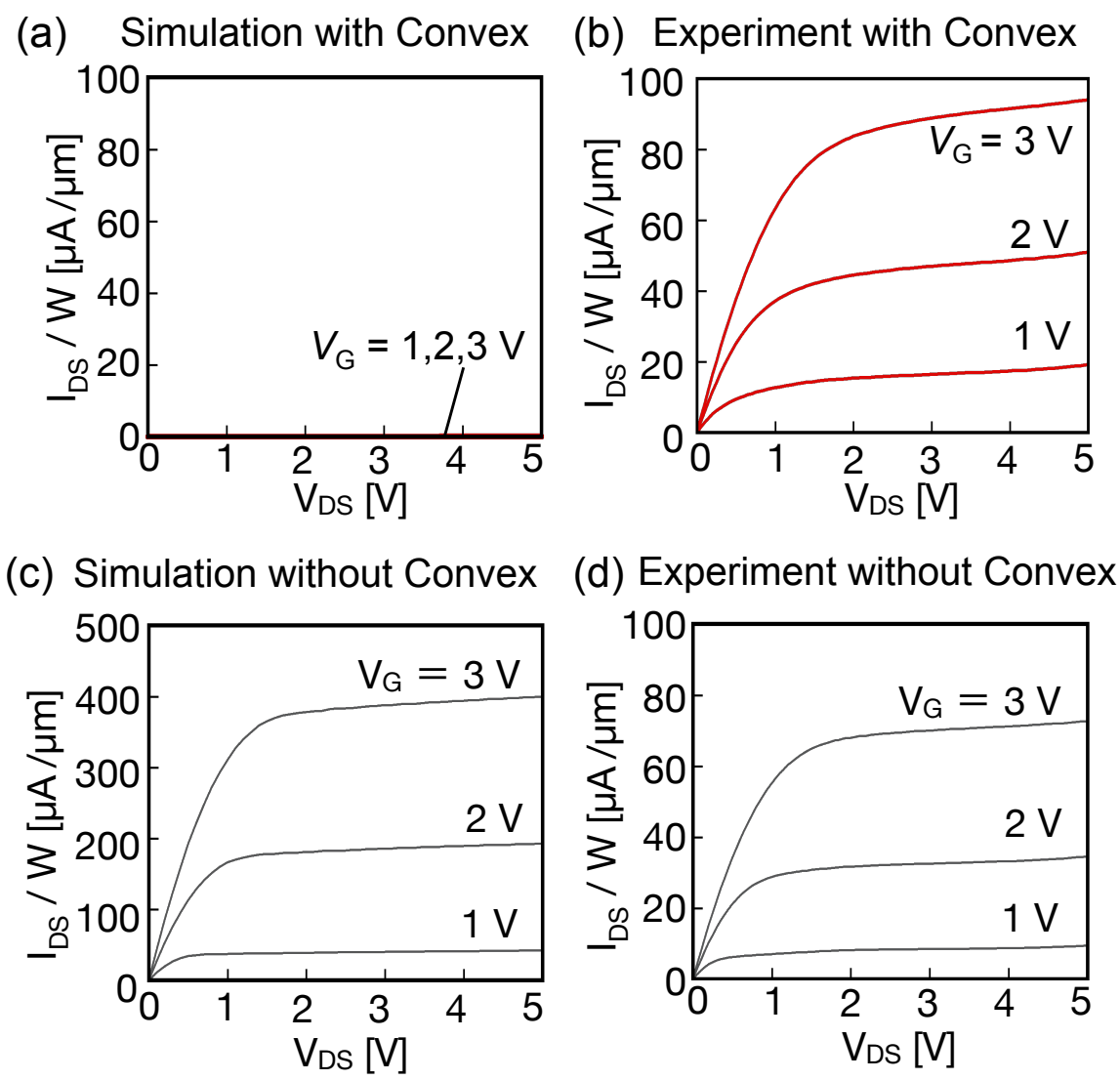

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Figure 5

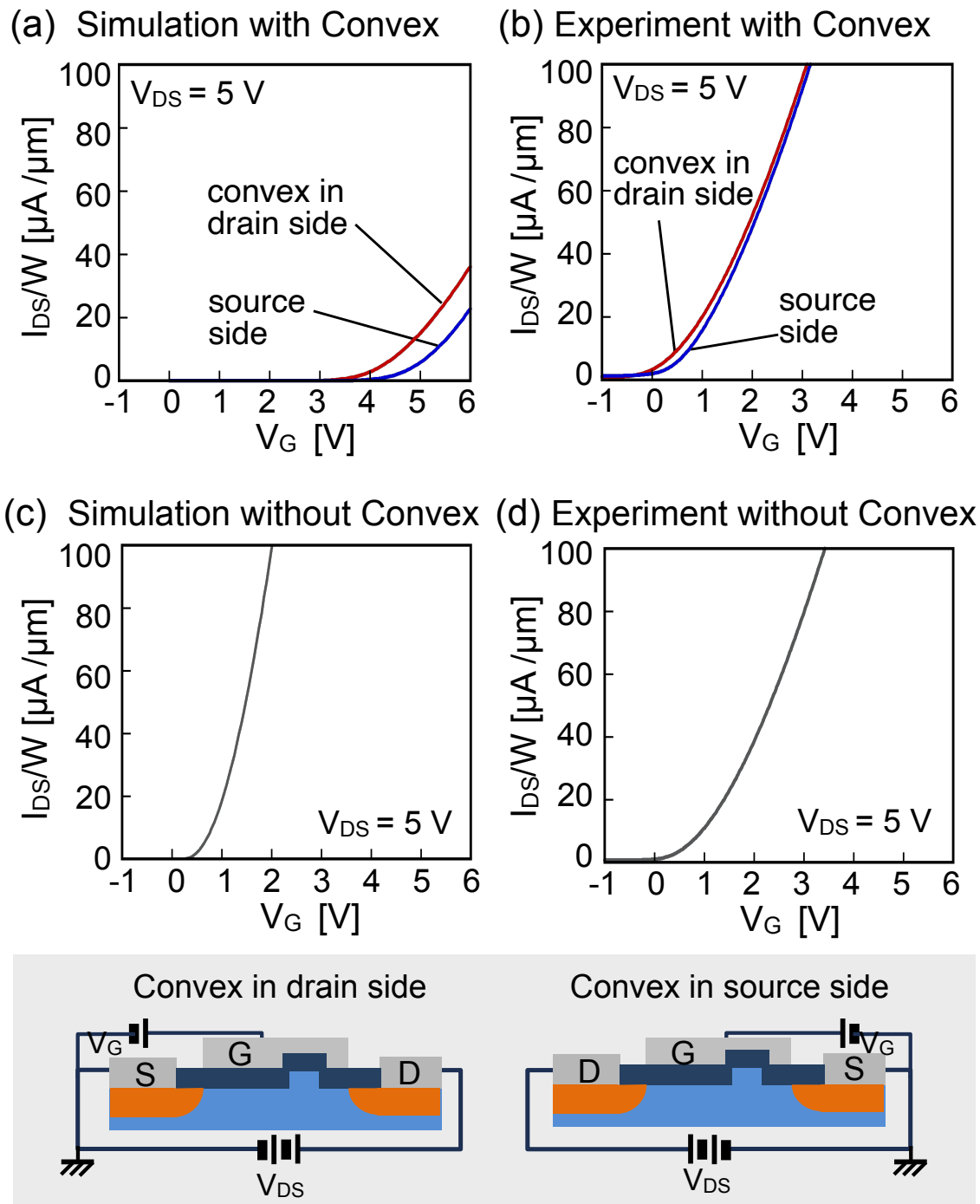

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Figure 6

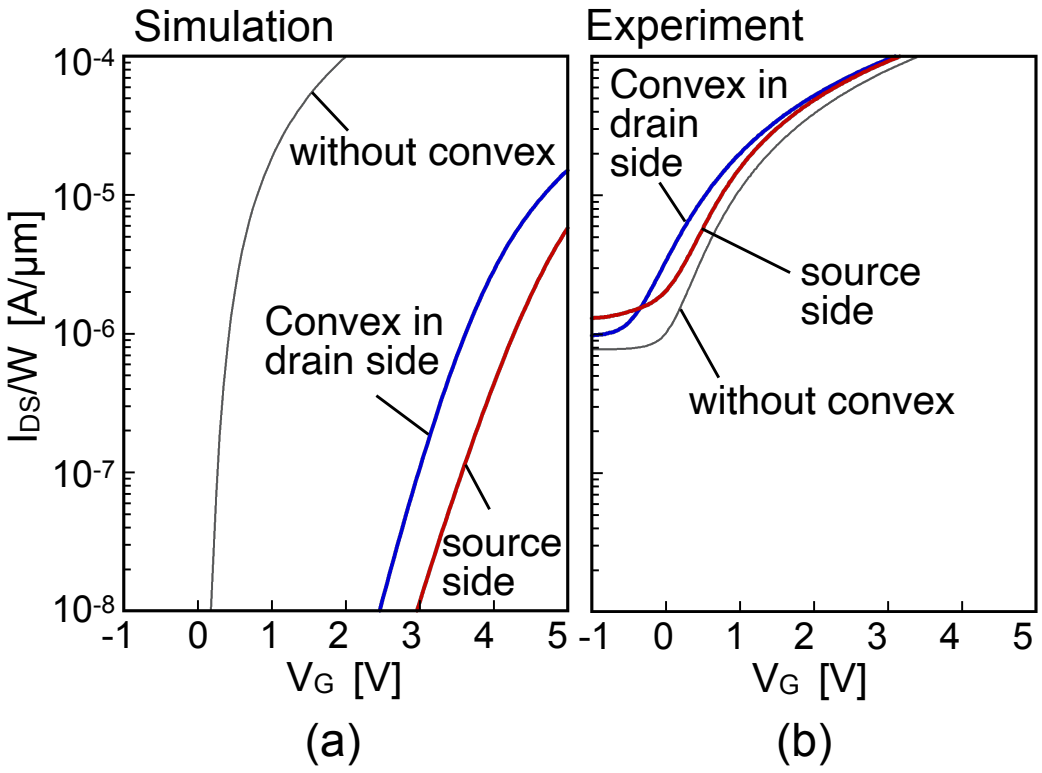

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Figure 7

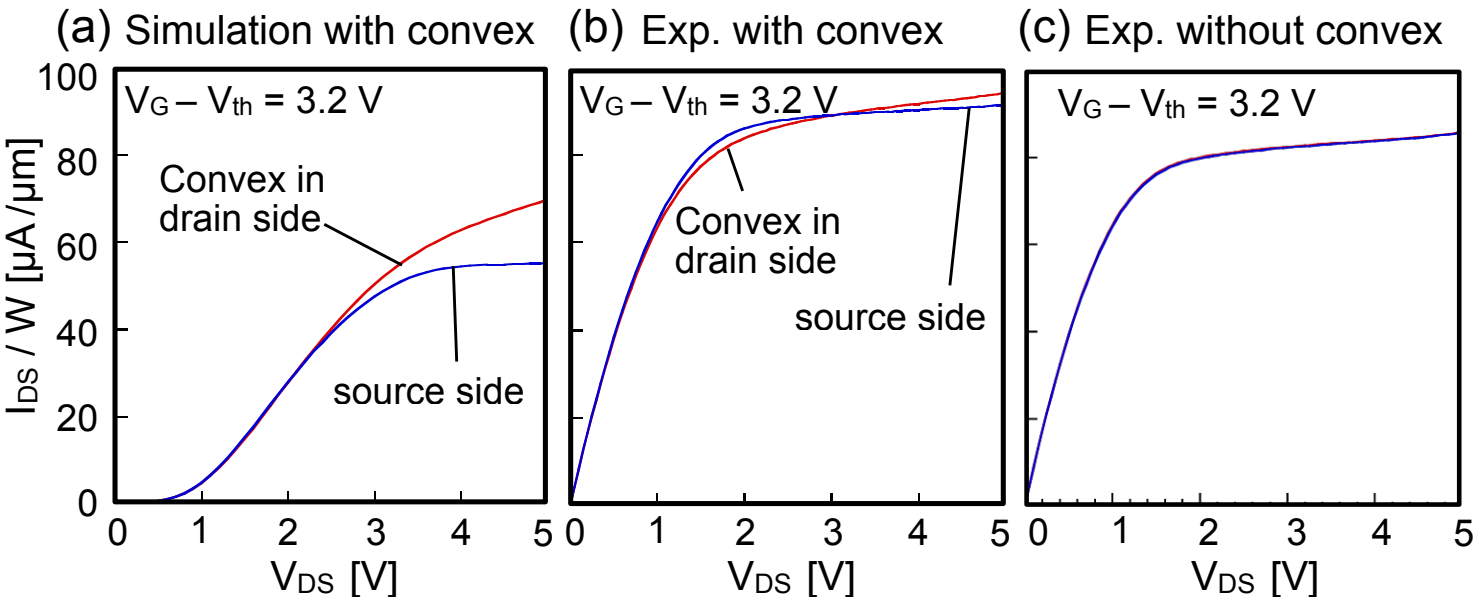

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Figure 8

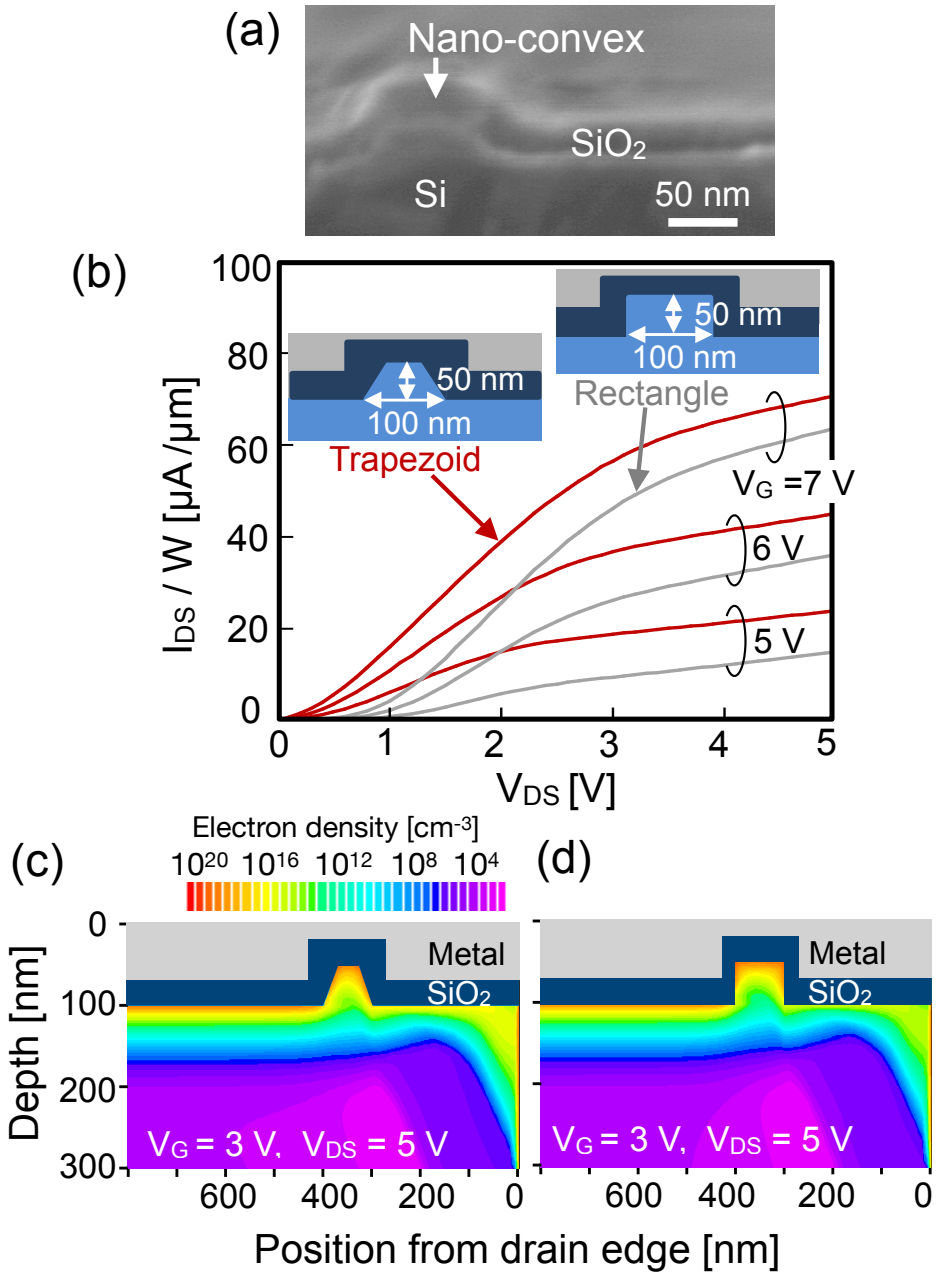

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Figure 9