Research on Ultra-Long Lifetime Development for Nano-Silicon Semiconductor Device Implementation

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Contents

Chapter 1 Introduction

1.1 Overview

Electronic device technology has evolved not only to improve high-speed switching, but also to improve device lifetime. The improvement of high-speed switching plays an important role in the development of information processing speed. A long device lifetime elongates mean time to failure, which is critical for the sustainability of electronic systems. These demands have been achieved by “downsizing”, from vacuum tubes to semiconductors and from discrete to integrate devices.

However, as device dimensions have become nanoscale, a significantly high energy density has caused problems. Until recently, semiconductor devices had become smaller, their switching speed had increased, and their lifetime had been extended. In nanoscale, intensity of the electric field becomes large. This cannot be negligible. How do I deal with the problems?

Here I review from the vacuum tube era. Lifetime of vacuum tube was remarkably improved by the invention of (indirect heated) cathode [1]. Function of the filament was divided into a cathode and a filament, with the cathode responsible for efficient electron emission and the heater for raising the temperature, thereby reducing damage to the device and extending its lifetime. There are several types of cathodes. One type is that lowers the work function of the cathode as an electric double layer such as Th (Fig. 1) [2], and another raises the Fermi energy of the cathode as an n-type semiconductor like BaO (Fig. 2) [2]. I aim for a longer device lifetime by using such vacuum tube technology.

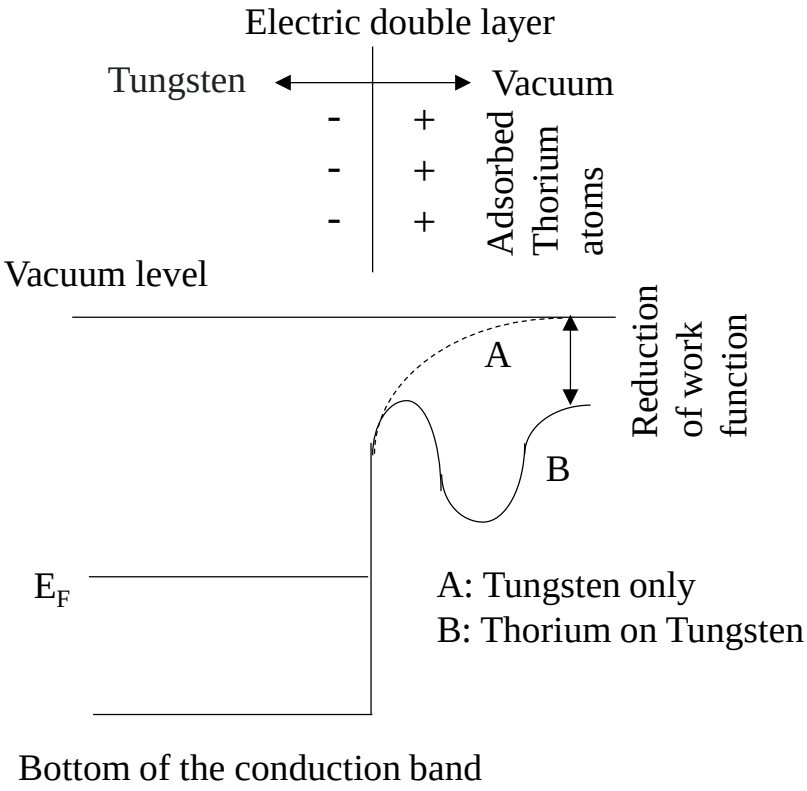


Figure 1. Changes in potential barriers in Thoriated Tungsten cathodes. Using tungsten as the base metal and forming a monolayer of thorium on the surface, the electric double layer formed at the interface draws electrons from the tungsten. In this case, the work function of tungsten decreases, making it easier to extract electrons.

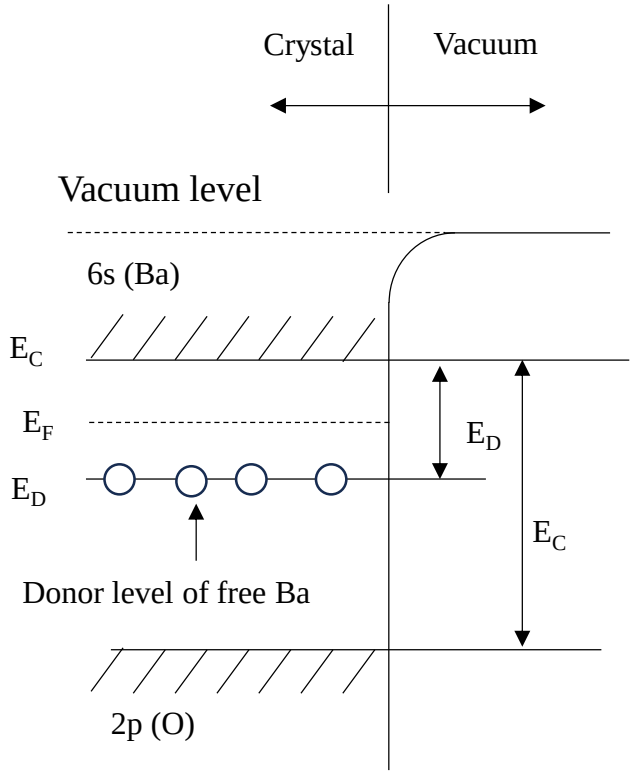


Figure 2. Energy levels of BaO Crystal. Barium (Ba) acts as the donor, causing the Fermi level to rise, and as an N-type semiconductor, it extracts electrons from Tungsten.

Let us think how to raise the fermi level of solid-state devices. In case of junction between different materials (heterojunction), the fermi level changes. The Bandgap Engineering Method [3] and trapped carriers also shift the fermi level [4]. Confinement of carriers affects the distribution of charges [5]. These effects also raise the work function. Now, Si metal-oxide-semiconductor (MOS) devices is most popular. To realize these effects in the MOS devices, I selected floating body cell (FBC) which Okhonin attempted to make capacitor-less memories [4]. The FBC uses SOI (Silicon On Insulator)-MOS (Metal Oxide Silicon) with an additional layer of buried oxide. The presence of this buried oxide leads to the accumulation of holes that have no place to go within the MOS channel during memory operation (see Fig. 21, will be explained later in this thesis), resulting in an increase in channel potential (floating body effects) [5]. In other words, as shown in Fig.3, the Body of the SOI on the equivalent circuit serves as the base of an NPN transistor [6], leading to the accumulation of excess holes in the Body. The increased channel potential raises the Fermi level and reduces the vacuum work function. This will be explained using an energy band diagram as shown in Fig.4 and Fig.5.

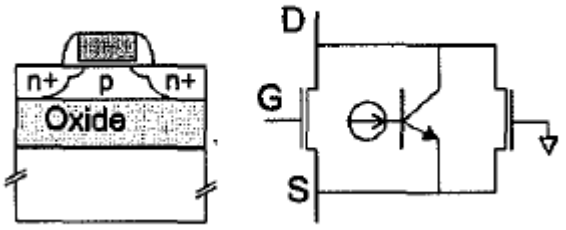


Figure 3. MOS on SOI cross-section and equivalent circuit schematic

In normal MOS case as shown in Fig.4(a), when the positive potential V_M is applied to the gate, the energy band structure of the A-A' section just below the gate is represented as shown in Fig.4 (b). Here, I define the depletion layer potential as *V*dep and the depletion layer width as xp. When the positive potential is applied to the metal layer, the interface portion on the semiconductor side becomes depleted and band bending occurs. When the positive bias becomes large and the Fermi level at intrinsic conditions is denoted as Ei, if Ei - Ef < *V*dep, the Fermi level at the surface is positioned above the center of the band. In this case, the surface becomes n-type, electrons Qinv accumulate, and an inversion layer is formed as shown in Fig. 4(b). Similarly, the band structure in the case of SOI-NMOS as shown in Fig. 5(a) is represented as shown in Fig. 5(b). As shown in Fig. 5(b), positive potential caused by the accumulation of holes in the body of the SOI NMOS reduces the potential difference between the gate and the body, thereby decreasing the depth of depletion layer. Thus, the curvature of the energy band becomes more abrupt, making it easier for electrons to accumulate.

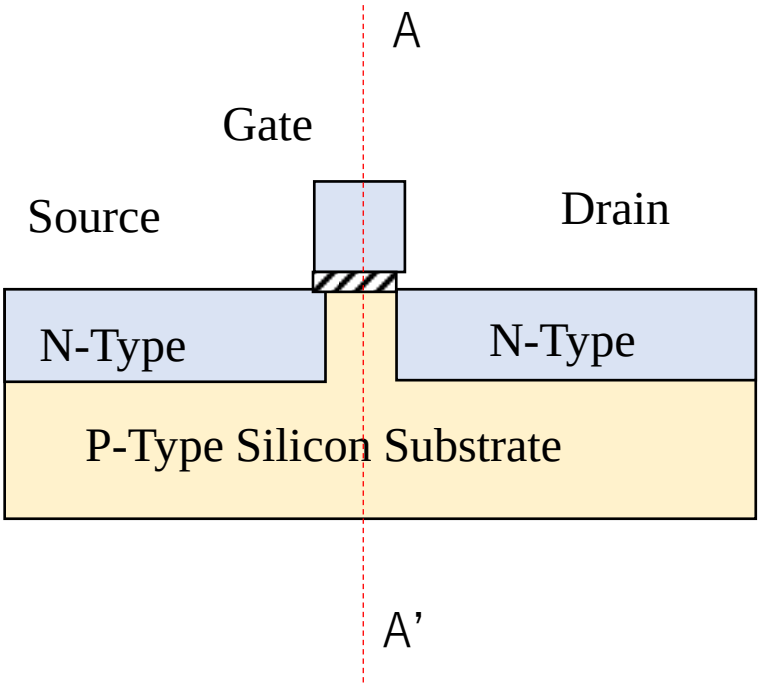


Figure 4(a). Cross-section of the general NMOS

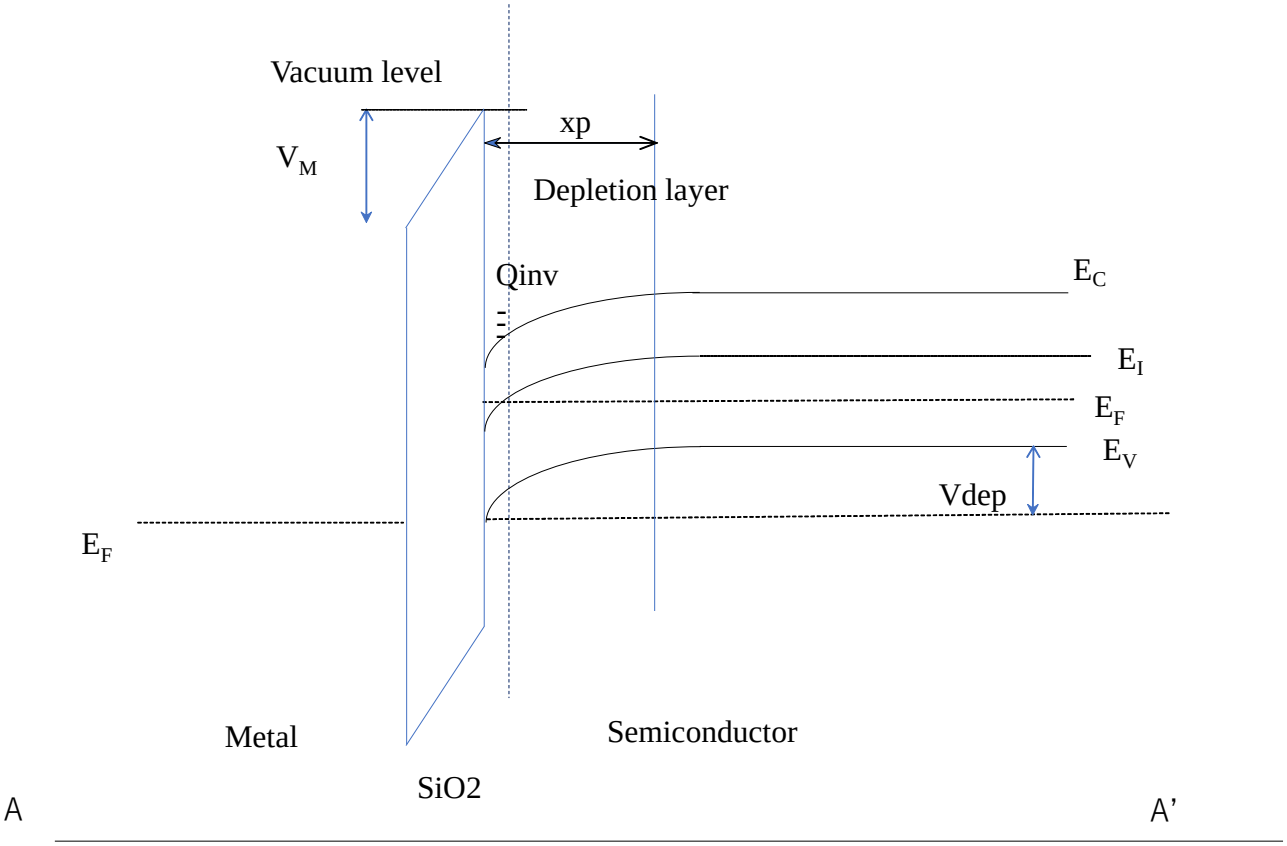


Figure 4(b). Energy band diagram of the A-A' section just below the gate in the general NMOS. When the positive bias becomes large and the Fermi level at intrinsic conditions is denoted as Ei, if Ei - Ef <

*V*dep, the Fermi level at the surface is positioned above the center of the band. In this case, the surface becomes n-type, electrons Qinv accumulate, and an inversion layer is formed

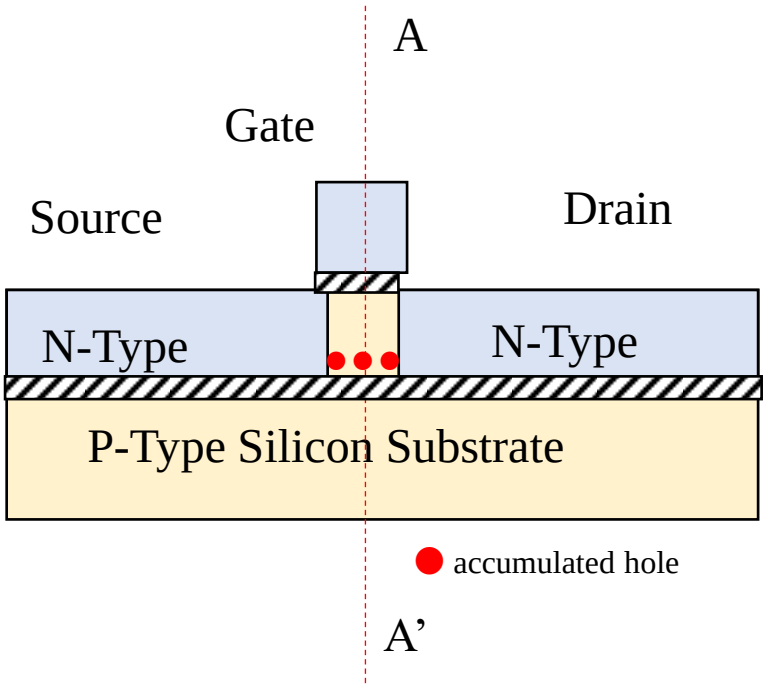


Figure 5(a). Cross-section of the SOI NMOS

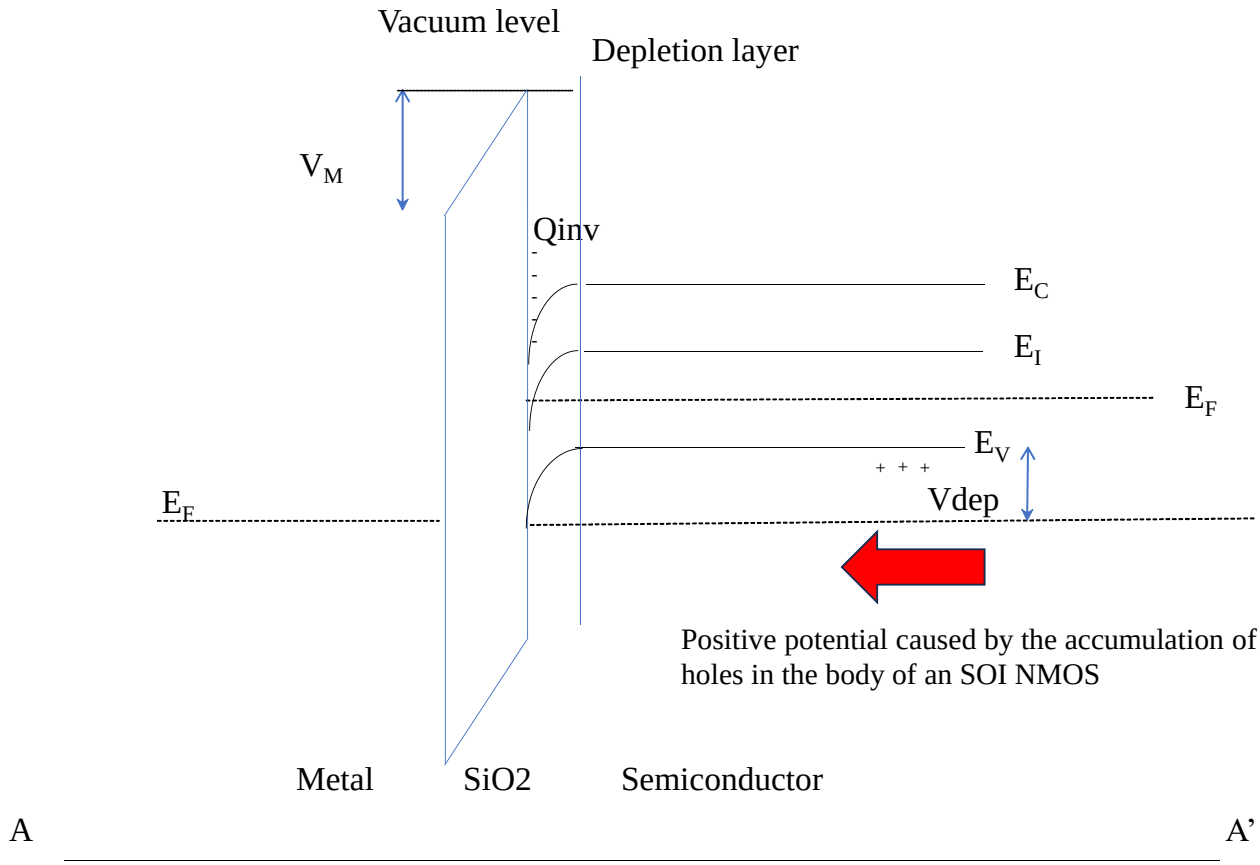


Figure 5(b). Energy band diagram of the A-A' section just below the gate in the SOI NMOS. In this case, positive potential caused by the accumulation of holes in the body of the SOI NMOS reduces the potential difference between the gate and the body, thereby decreasing the depth of depletion layer. Thus, the curvature of the energy band becomes more abrupt, making it easier for electrons to accumulate.

Details will be discussed later, it has been found that the body potential is 0.7 V in the Floating-Body state. The phenomenon that occurs at 2.3V in a conventional MOS occurs at 1.6 V in the SOI-MOS. The SOI-MOS transistor can operate at a lower gate voltage than the normal MOS.

Thus, FBC can be considered an advanced device in which two effects occur simultaneously: the reduction of the work function and the shift of the Fermi level due to cathode introduction. In this way, FBC is thought to achieve increased lifetime through a reduction in device stress, due to effects similar to those of cathode introduction in vacuum tubes. To extend the device lifetime through these effects, I conducted development on FBC. Our experimental results are shown to be consistent with the above proposal.

1.2 Research Focus: FBC

The main theme of this study is the ultra-long lifetime of FBC. FBC is a type of DRAM (Dynamic Random Access Memory). In DRAM, the presence or absence of charge in the capacitors directly connected to each MOS (Metal-Oxide-Silicon) transistor creates an electrical 1 or 0 state, which is the source of information storage. Since it is difficult to reduce the size of the capacitor directly connected to MOS transistor in DRAM, it is difficult to reduce the size of DRAM as a whole [7]. However, in FBC, the presence or absence of hot holes generated under high electric fields (impact ionization) in the channel region, which is electrically isolated from the substrate by the buried oxide layer unique to SOI MOS, enables the creation of electrical "1" or "0" states even without a capacitor. Since FBC does not use a capacitor, it is possible to reduce the entire DRAM size by reducing only the MOS transistor size. Because of its simple structure, future development is attracting attention. On the other hands, FBC operates based on impact ionization [8], it has the disadvantage of being affected by the hot carrier effect [9], which often occurs in high electric fields. In other words, there is a concern that electrons with high energy will create lattice defects, resulting in device failure and shortening the device lifetime.

In this study, I worked on the ultra-long life of FBC, a technology aimed at making capacitor-less DRAM in LSI. During FBC operation, it was confirmed that the body potential of the FBC increased by about 0.7 V due to the floating body effect. I discovered that the difference between the gate voltage V_g and the drain voltage V_d became smaller by the floating body effect peculiar to SOI. In this way, I presented FBC, which guarantees 50-year operation in the DRAM world, which is usually said to be 10 years [10] - [11]. This thesis is structured as follows.

1.3 Structure of this thesis

In Chapter 1, the background and motivation of this study are explained. First, the flow of development of devices using electrons, from vacuum tubes which began with communications, to LSI which consist of arithmetic elements (Logic) and memory elements (Memory) were explained.

In Chapter 2, the DRAM is explained and the operating principle of FBC which is a capacitorless DRAM using SOI-MOS transistors is explained.

In Chapter 3, the actual measurement results of the hot carrier effect of FBC are discussed.

In Chapter 4, the summary of this thesis is provided.

1.4 Evolution of Electronic Devices

1.4.1 Invention of the vacuum tube (application to wireless communications)

Electron-based arithmetic devices began with vacuum tubes. The starting point was the discovery of the T. Edison effect in 1884 [12]. When T. Edison covered a filament with a metal foil (plate) during his research on filament degradation, he observed that the electric current flowed through the vacuum between the filament and the plate. In 1904, J. Fleming invented the vacuum tube diode with rectifying action [13]. Figure 6 shows a schematic diagram of a vacuum tube diode. Plate current only flows when the plate is positive (rectifying action). Figure 7(a) and 7(b) briefly show the rectification action of this vacuum tube ·diode.

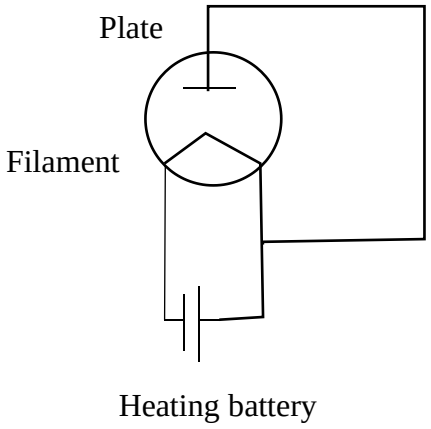


Figure 6. Schematic diagram of a vacuum tube diode

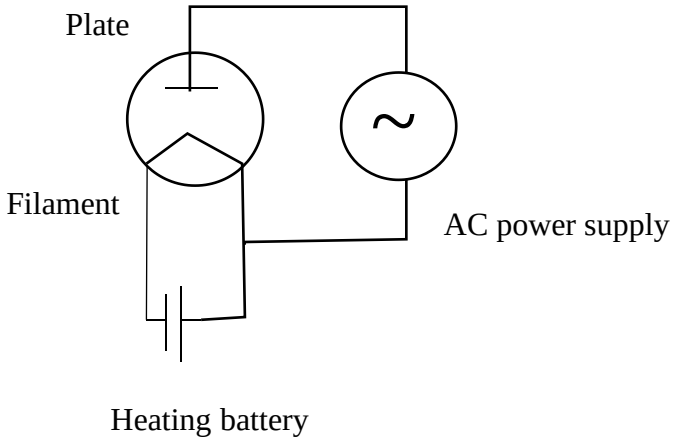


Figure 7(a). Rectification circuit diagram with a bipolar vacuum tube

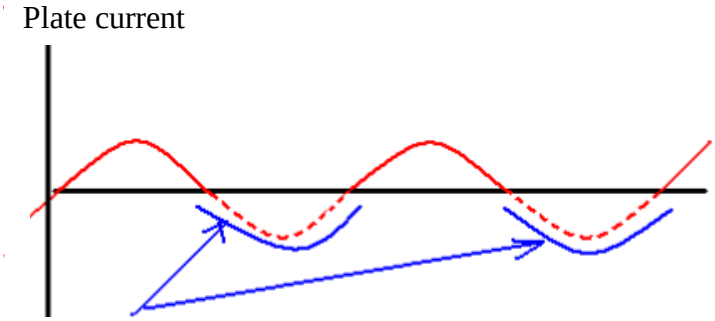


Figure 7(b). The electrical characteristics of rectification function in a bipolar vacuum tube

In 1906, de Forest invented the vacuum tube triode [14]. At this time the grid is introduced and a negative voltage is applied to the grid, which suppresses the flow of electrons. The more negative the grid voltage, the more electrons are repelled by the grid, reducing the electron flow to the plate. The age of the vacuum tube came to a head when de Forest discovered the amplifying effect of the vacuum tube triode [15]. A minute input signal applied to the grid causes a large change in plate current, which amplifies the signal. The cathode was introduced to the vacuum tube in 1914 by H.J. Round [1]. Function of the filament was divided into a cathode and a filament, with the cathode responsible for efficient electron emission and the heater for raising the temperature, thereby reducing damage to the device and extending its lifetime. As mentioned in the Background, there are several types of cathodes, and I will introduce typical ones. There is a type that lowers the work function of the cathode as an electric double layer such as Th (Fig. 1), and a type that raises the Fermi energy of the cathode as an n-type semiconductor like BaO (Fig. 2). Figure 8 shows a schematic diagram of the vacuum tube triode.

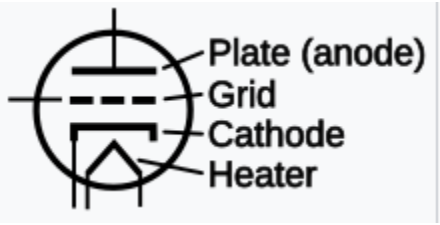


Figure 8. Schematic diagram of the vacuum tube triode

As a result, the lifetime of the vacuum tube was extended and the stability of operation was improved. The role of this cathode corresponds to buried oxide layer that induces the Floating-Body effect, which suppresses hot carrier effects. Suppressing the hot carrier effects is the key to ultra-long lifetime in the FBC in this study. Details will be explained in the main text. Figure 9 shows a photograph of standard vacuum tubes.

Figure 9. Photograph of a standard vacuum tube

The standard size of a vacuum tube is about 10 cm, and the distance between filament and plate is less than 1 cm. The invention of the vacuum tube was closely tied to the improvement of vacuum technology, coinciding with the success of He liquefaction in 1908 by Kamerlingh Onnes [16], and is closely related to the development of modern physics. The application of such rectification and amplification to wireless communications was its main motivation.

1.4.2 Invention of the transistor (utilization for arithmetic operations)

The age of triode with semiconductors for even longer lifetime began. The age of transistors has dawned. This led to the use of transistors in arithmetic operations. In 1947, physicists John Bardeen and Walter Brattain of Bell Laboratories in the United States successfully experimented with bipolar transistors to amplify signals [17]. In 1948, William Shockley invented a more stable type of transistor (field-effect transistor (later developed into MOS-FET)), and semiconductor research began in earnest [18]. The development from vacuum tubes to transistors has achieved solid-state devices and miniaturization of electronic devices, and has also greatly improved durability [18]. Figure 10 shows

a schematic diagram of a NPN bipolar transistor. Figure 11 shows a photograph of a standard bipolar transistor. Currently, the standard size of a transistor is about 5 mm.

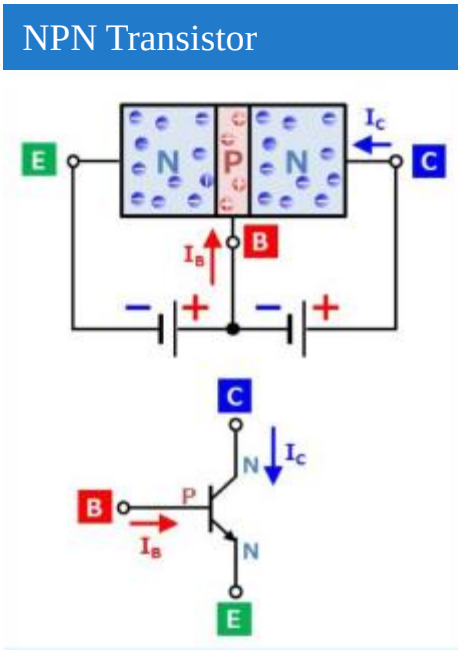


Figure 10. Schematic diagram of a NPN Bipolar Transistor

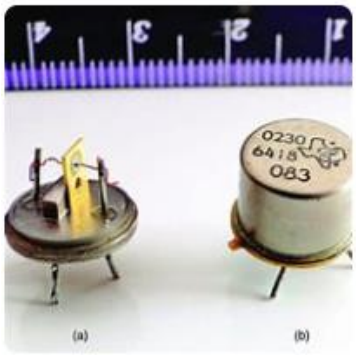


Figure 11. Photograph of a standard bipolar transistor

1.4.3 Improving lifetime of electronic devices

Electronic device technology is not only improving performance such as high-speed switching, but also improving device lifetime. It has evolved as a key traction force. The cathode of vacuum tube and the subsequent transition to semiconductor were also facilitated in terms of the lifetime. In addition, lighting technology has evolved from incandescent bulbs (about 1,000 hours) to fluorescent tubes (6,000 to 20,000 hours) and even LEDs (Light-Emitting Diodes) using semiconductor GaN (20,000 to

80,000 hours) in terms of lifetime [19]. In this way, it is easy to think that improving lifetime expectancy is a low-key study that seems to play an unsung role in technological innovation, but in fact it has become a driving force for technological innovation.

1.4.4 From the advent of integrated circuits (IC) to further improvement of integration (LSI)

IC (Integrated Circuit) appeared in the late 1950s, and mass production of semiconductors began. In the 1960s, LSI (Large Scale Integration) integrated circuits appeared. Demand increased dramatically due to the commercialization of LSI in calculators [20]. In the latter half of the 1970s, it further developed into VLSI (Very Large Scale Integration) [21]. In the 2020s, the standard size of transistors on LSIs has advanced to the nm age [22]. By the way, the ENIAC computer in 1946 was the fastest computer in the world at that time, but it was equipped with more than 17,000 vacuum tubes, weighed 60,000 pounds (about 27 tons), had a volume of 16,200 cubic feet (about 460 cubic meters), and consumed 174 kilowatts (about 233 horsepower) [23]. In the case of vacuum tubes, they cannot be made any smaller, the number of components as a system remains unchanged. Vacuum tubes do not lead to integrated circuits as a technology.

There are two devices that make up a calculator: logic and memory like this [24], but this time, the purpose of this study was to improve the performance (lifetime) of the memory device (DRAM). Figure 12 shows a photo of the Silicon Wafer of the current VLSI.

Figure 12. Photo of the Silicon Wafer of the current VLSI

1.4.5 MOS and Bipolar

Here, why the active devices that make up the LSI are now MOS instead of Bipolar will be briefly explained. Figure 13(a) shows a cross-sectional schematic diagram of NMOS and Fig. 13(b) shows a cross-sectional schematic diagram of NPN-Bipolar. As a principle of operation, MOS only uses surface levels and does not use PN junctions, and is a low-power consumption type [25]. Bipolar, on the other hand, operates by recombining the small number of carriers, so it always requires constant base current. As a result, Joule heat generation and large power consumption are weak points [26]. The high-speed operation, which was the biggest advantage of Bipolar, has also changed to MOS now that the gate length has become nm size due to the improvement of gate processing technology in recent years [27]. At present, the active devices on LSI are mainly MOS. Table I compares Vacuum Tube, Bipolar and MOS. Despite these advantages and disadvantages, MOS is now the mainstream, and there is still a demand for vacuum tubes and bipolar for analog products.

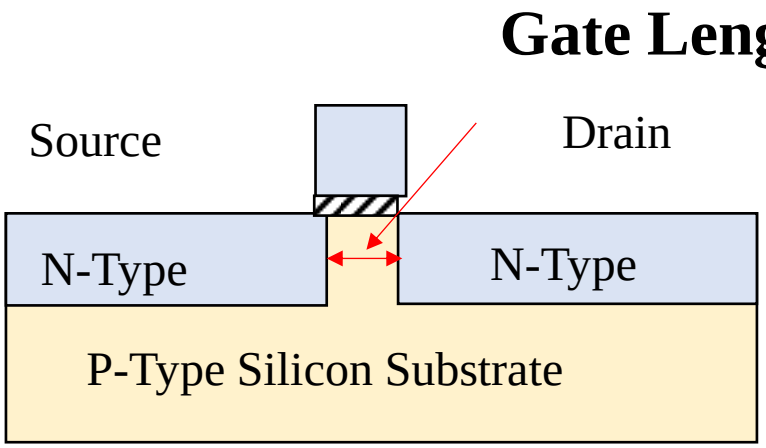


Figure 13(a). Cross-section of NMOS

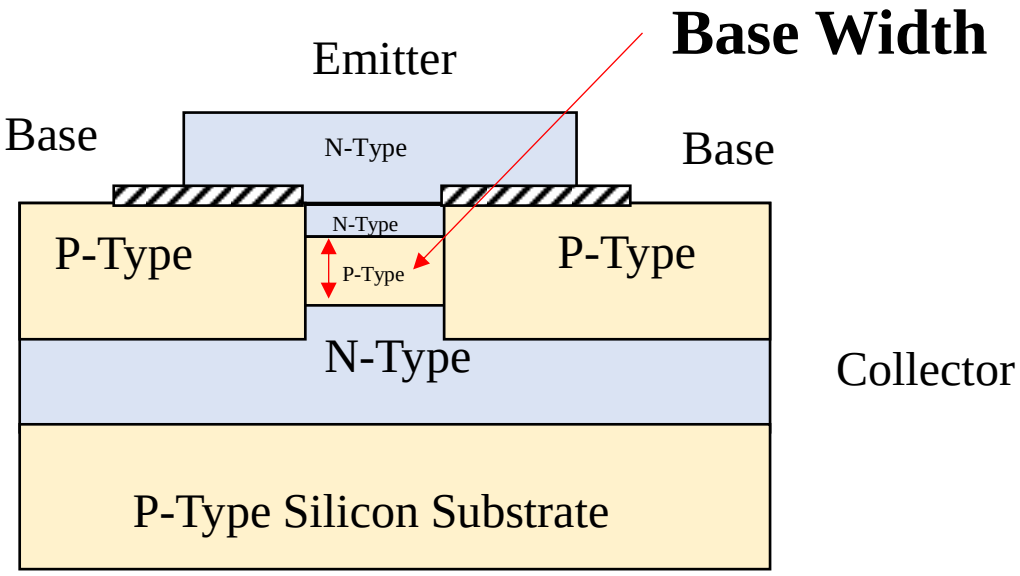


Figure 13(b). Cross-section of NPN-Bipolar

Table I. Electronic Devices Comparison Table

	vacuum tube	Bipolar	MOS
Size	cm	μm	nm
Endurance	~10000 Hours	~100 years	~100 years
Analog Operation	Excellent	Excellent	Good
Radiation Durability	Excellent	Good	Good
High Voltage/High Power Durability	Excellent	Excellent	Good
High-Frequency Characteristics	Excellent	Excellent	Good
Heat Generation	Bad	Somewhat Poor	Excellent

1.4.6 Hot Carrier Effect

MOS transistors also have a lifetime problem. One of them is the hot carrier effect [4], which will be discussed next. The hot carrier is a state in which the temperature of the carrier becomes higher than the temperature of the crystal when the electric field applied to the crystal increases. This is because in such a state, only a part of the energy obtained by electrons and holes from the electric field is transmitted to the crystal lattice. In the normal MOS with an actual gate length of 0.15 μm, if the drain voltage exceeds 2 V, it enters the area affected by this hot carrier effect [28]. As shown in Figure 14, the current from the MOS source to the drain creates hot carriers that jump into the gate electrode.

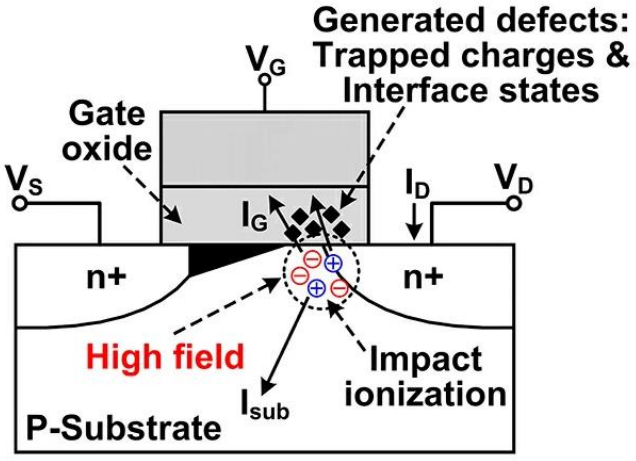


Figure 14. Hot Carrier Effects in MOS

At this time, the interface of the gate insulating film passing through is damaged, and lattice defects are generated. The occurrence of this lattice defect is an irreversible process. In fact, if the MOS transistor continues to operate, the electrons will be trapped in the lattice defects, and the drain current Id will gradually decrease. As a result, the lifetime of the MOS transistor is shortened. Overcoming this problem is one of the major themes of this study.

1.4.7 Schematic diagram of electron distribution under high electric field

Figure 15 schematically illustrates the distribution of hot carriers under high electric field. As shown in Fig. 15(a), under a high electric field, the distribution shifts by k_d in the direction of the electric field, and the area of the circle increases due to the increase in electron temperature, and the center shifts, indicating that the system as a whole has momentum.

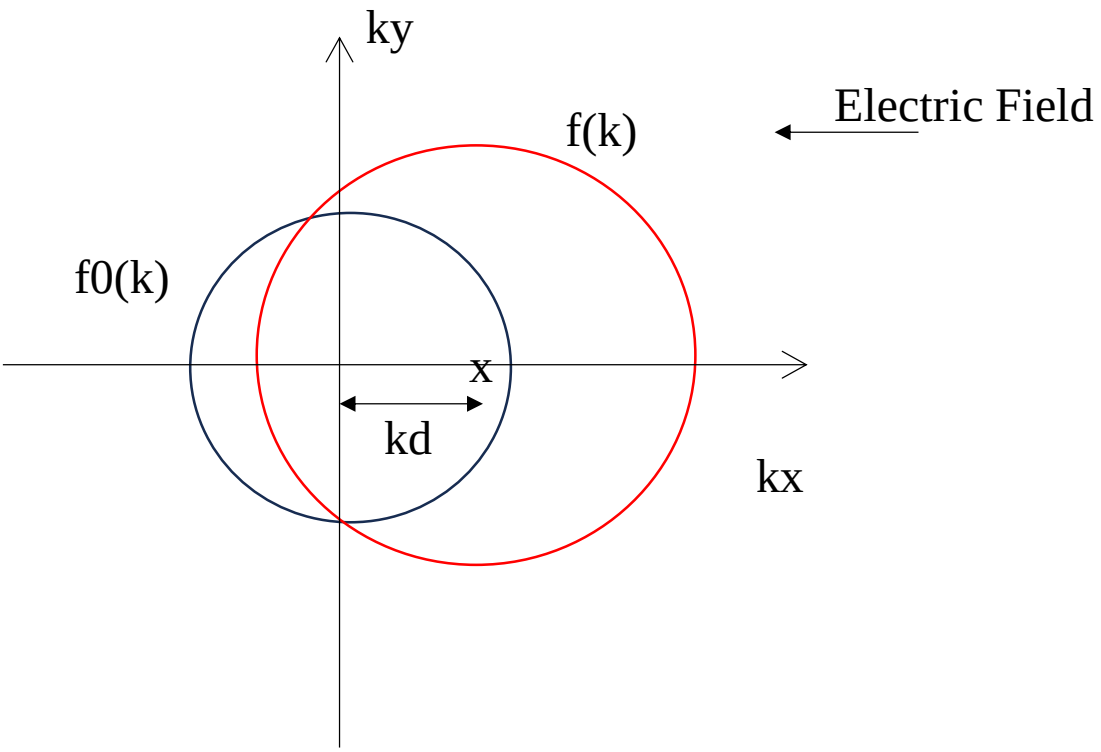


Figure 15(a). Schematic electron distribution under high electric field in *k*-space

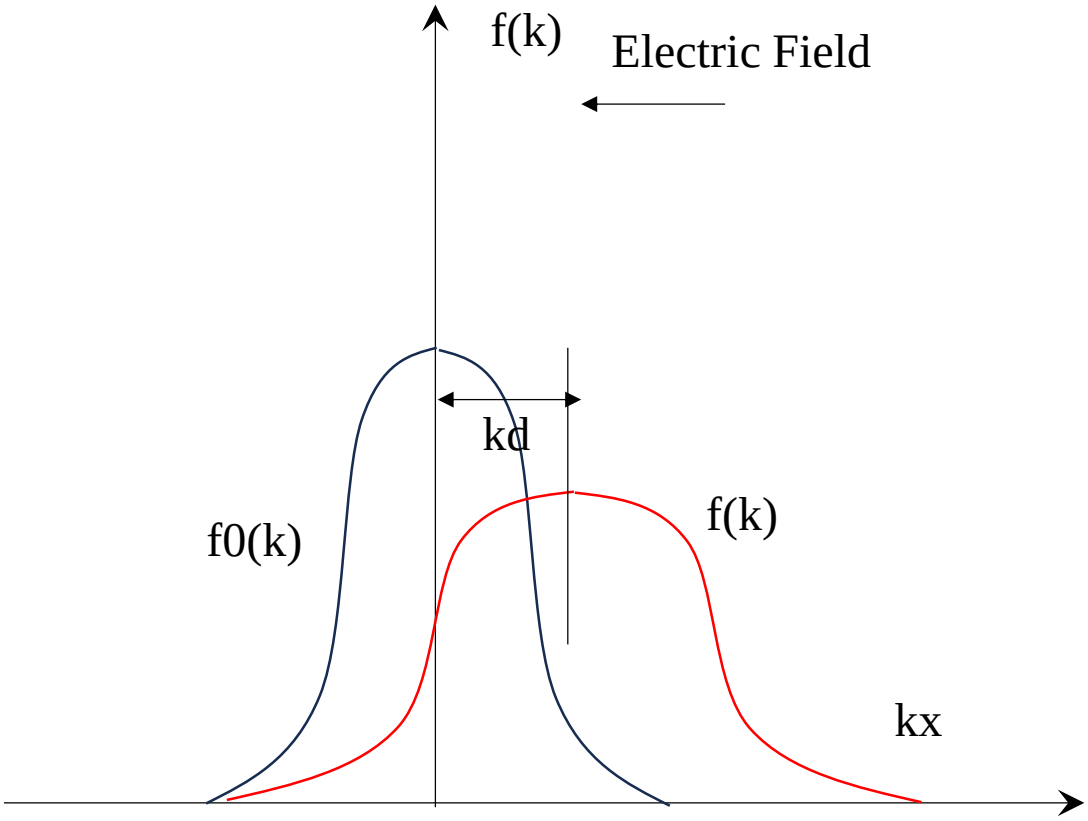


Figure 15(b). Schematic electron probability distribution under high electric field

Further, as shown in Fig. 15(b), the base spreads to the high energy side due to the increase in electron temperature. In other words, the proportion of high-energy carriers will increase. The carriers at the base of the distribution that extend to the side of this high electric field cause phenomena peculiar to the high electric field.

1.4.8 Problems with reducing the size of MOS

There is always a demand for LSI to reduce the device size from the viewpoint of improving the degree of integration. As shown in Fig.16, as the device size is reduced, the power supply voltage (drain voltage) is adjusted accordingly. It is necessary to reduce the device size and keep the electric field strength inside the device constant level. On the other hand, regarding the power supply voltage (drain voltage), further reduction below the current mainstream level of 1V is challenging due to issues such as the presence of leakage current and a decrease in the on-current (drain current), which leads to a reduction in the on-off ratio [29]. As such, the miniaturization of device sizes and the increase in

electric field within the device are in a trade-off relationship. As device sizes shrink, the occurrence of hot carrier effects tends to increase, leading to gate oxide degradation.

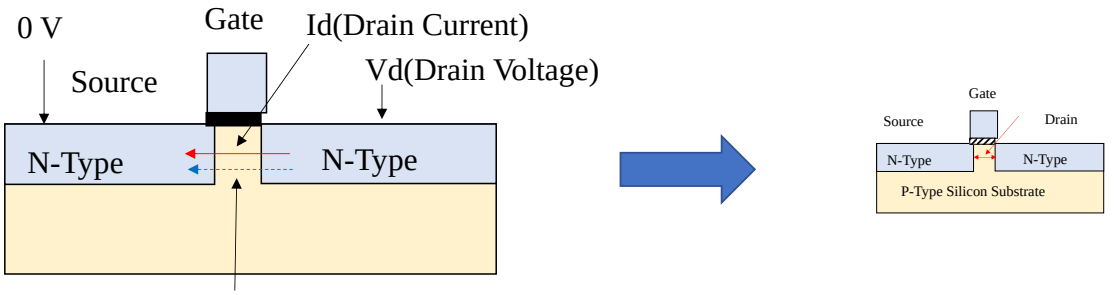


Figure 16. Size reducing image of MOS Transistor

1.4.9 Purpose of this study

In addition to overcoming these MOS weak points, I also conducted study on memory that can be used for 50 years using SOI - MOS. While it is said that the general lifetime of vinyl records is several decades [30], CDs are several decades [31], and personal computers are said to be from 5 to 10 years [32], the purpose is to extend the lifetime of memory (DRAM) to 50 years, and to extend the lifetime of personal computers to the same level as records and CDs. The role of this cathode corresponds to the floating body effect that suppresses the hot carrier effect, which is the key to ultra-long lifetime in the FBC in this study. Details will be explained in the main text.

Chapter 2 Basic Concepts of FBC

2.1 MOS Transistor

MOS transistor is a type of FET (Field Effect Transistor) and stands for Metal Oxide Semiconductor. Figure 17 shows the Cross-section of a Standard NMOS.

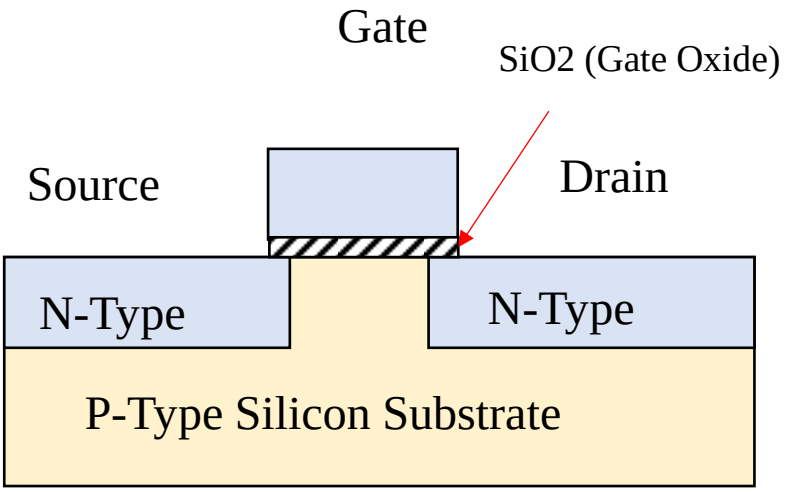


Figure 17. Cross-section of a Standard NMOS

In the case of a MOS-FET, it is common to use silicon dioxide (SiO_2) as the gate insulation layer between the Gate and the substrate and in the case of an N-type FET, applying a positive voltage to the Gate, a positive voltage to the Drain, and 0V to the Source results in the flow of Drain current between the Drain and Source, making it a switching device.

2.2 Impact ionization

As shown in Fig.18, impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers. For example, in semiconductors, an electron (or hole) with enough kinetic energy can knock a bound electron out of its bound state (in the valence band) and promote it to a state in the conduction band, creating an electron-hole pair. For carriers to have sufficient kinetic energy a sufficiently large electric field must be applied, essence requiring a sufficiently large voltage but not necessarily a large current [8].

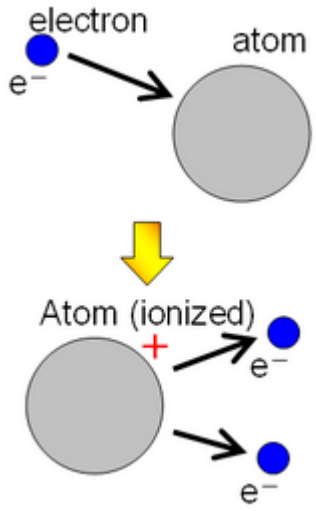


Figure 18. Schematic diagram of Impact ionization

2.3 SOI (Silicon On Insulator) MOS Transistor

In SOI-MOS, a silicon oxide layer is placed across the entire substrate between the Source/Drain and the substrate. Due to its structure, SOI devices are receiving greater attention as promising structures to realize low-power ULSI's [33] - [37]. From the viewpoint of device technology, the biggest concern is the floating-body effect, which is known as lowering of drain breakdown voltage [38], the kink effect [39], an abnormal subthreshold slope [40], current instability in switching operation [41] - [42], enhanced leakage current in DRAM cells [43] - [44], reducing the subthreshold voltage (Vth) [5]. Figure 19 shows the Cross-section of a Standard SOI-NMOS. As mentioned before, the reduction in Vth due to the floating body effect in SOI is especially important for FBC.

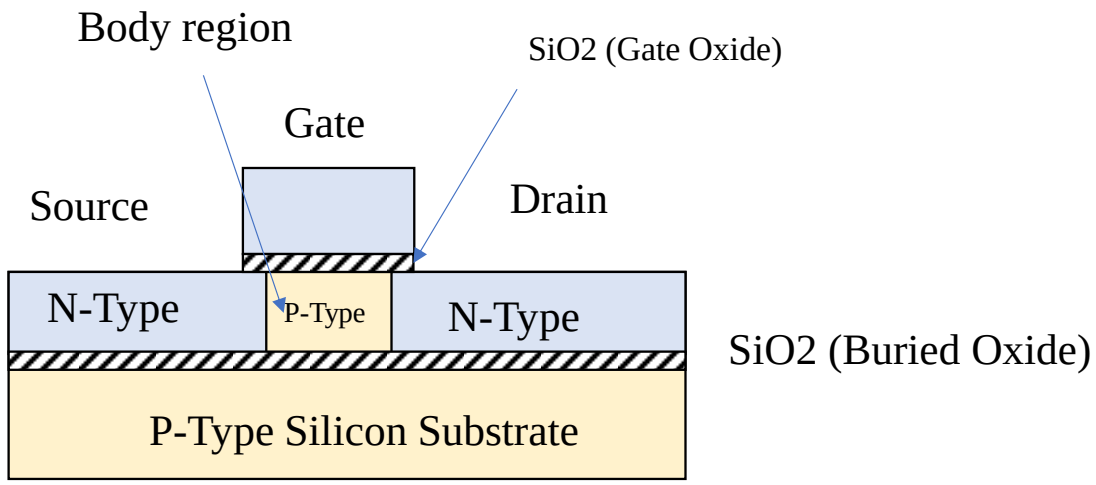


Figure 19. Cross-section of a Standard SOI-NMOS

2.4 General DRAM

In the case of general DRAM, 1 state and 0 state are distinguished by the presence or absence of charge in the capacitor directly connected to Drain as shown in Fig.20(a) and Fig.20(b). Therefore, the LSI cannot be shrunk just by shrinking the MOS. Shrinking the capacitor is difficult from the standpoint of securing capacitance. The capacitance required per bit of DRAM is typically around 20 to 40 femto Farads (fF), which remains the same even with reduced the size of MOS Transistors [2].

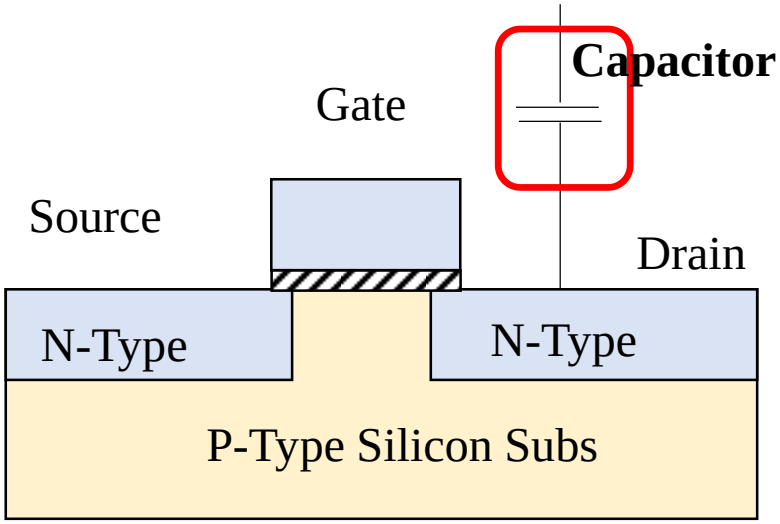


Figure 20(a). Cross-section of a Standard DRAM

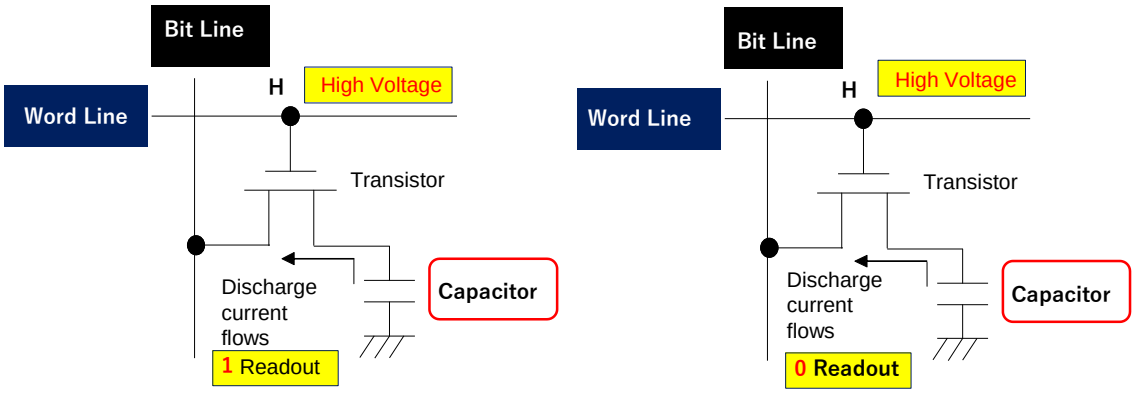


Figure 20(b). Schematic diagram of a Standard DRAM

2.5 Capacitor less DRAM FBC

Figure 21 shows the operation principle of fully depleted (FD) FBC [45]. Data "1" is written by creating holes by impact ionization and pushing up body potential to a high level. Employing negative plate bias, the created holes are accumulated on the back surface. On the other hand, data "0" is written by extracting holes from the body and pulling down the body potential to a low level. The stored signal can be differentiated using MOSFET current modulated by body potential.

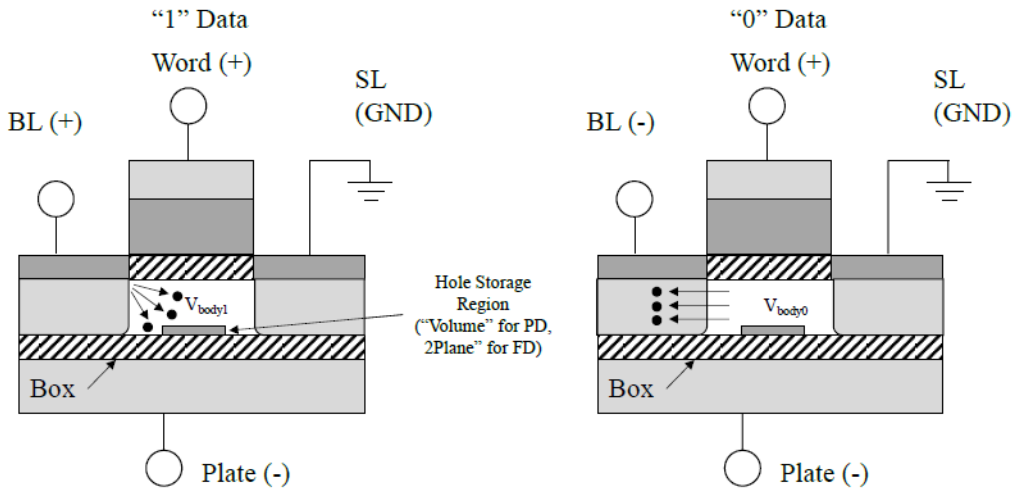


Figure 21. The operation principle of FD FBC

2.6 Principles and Characteristics of FBC

Several kinds of capacitor-less dynamic random-access memory (DRAM) cell have been proposed and developed [45] - [65]. Floating body cell (FBC) is a DRAM made entirely of CMOS without a capacitor, so FBC is an LSI that can only be shrunk using CMOS scaling. FBC is a potential candidate because of its simple structure and scalability [62]. Toward the FBC realization, there is an influence of a physical phenomenon different from normal MOS because of its structural and operational characteristics called silicon-on-insulator (SOI)-MOS. In particular, floating body effect and self-heating are phenomena unique to SOI, which may affect FBC operation and degradation. In this study, I conducted an experimental study of FBC from the HCI perspective. For this FBC, considering the sense margin of the FBC reading for practical use, there is a HCI regulation that the amount of drain current (Id) degradation is within 10% or Vth shift is within 10 mV in the read-in state in linear region in 50 years under the operation of drain voltage (V_d) at 2.3 V in the write-in state which is in saturation region. I examined if this FBC meets this requirement. In that process, I clarified the importance of the sidewall structure and the geometrical effect of the channel length L and channel width W of the FBC cell transistor and the floating body effect, in the HCI regime of the FBC. Table II compares FBC and other embedded memories.

Table II. COMPARISON TABLE OF EMBEDDED MEMORIES.

	Cell size (F^2)	Process	tRC (ns)	Advantage	Retention@median(s) @85°C	Issue to shrink	Scalability limits	Basis of memory
DRAM	6 - 8	CMOS + Capacitor	20	High Density	>10	Capacitor Transistor	Storage Capacitance	Charge Storage in Capacitor
eDRAM	12 - 20	CMOS + Capacitor	5	High Performance	>1	Capacitor Transistor	Storage Capacitance	Charge Storage in Capacitor
FBC (1Cell/Bit)	6	CMOS	20	Low Cost	>0.1	Transistor	Hole Density	Charge Storage in Floating Body
FBC (2Cell/Bit)	12		3					
SRAM	80	CMOS	1	High Performance	-	Transistor	Signal Stability	F-F

FBC has two operation modes. 1) single-cell operation (1 cell/bit) and 2) twin-cell operation (2 cell/bit) [60]. In the case of single-cell operation, the memory cell size is 6F2, in which F is the feature size. In the case of twin-cell operation, cell size is 12F2. The cell size of the single-cell operation is equal or even smaller than that of a conventional DRAM cell. In view of the single-cell operation, I think FBC can replace conventional DRAM. The cell size of the twin-cell operation is also smaller than that of SRAM cell, and the access time is almost the same or on the same order as that of SRAM. In view of the twin-cell operation, I think FBC can replace SRAM to a certain extent. The greatest advantage of FBC is its low cost, because it dispenses with both the trench capacitor and stack capacitor. The two operation modes use different reference cells in the read operation. In the single-cell operation, a dummy cell connected to BL is used as the reference cell. In the twin-cell operation, the neighboring cell sharing WL connected to BL is used as reference cell [45] - [65]. Figure 22 shows a schematic of the FBC structure.

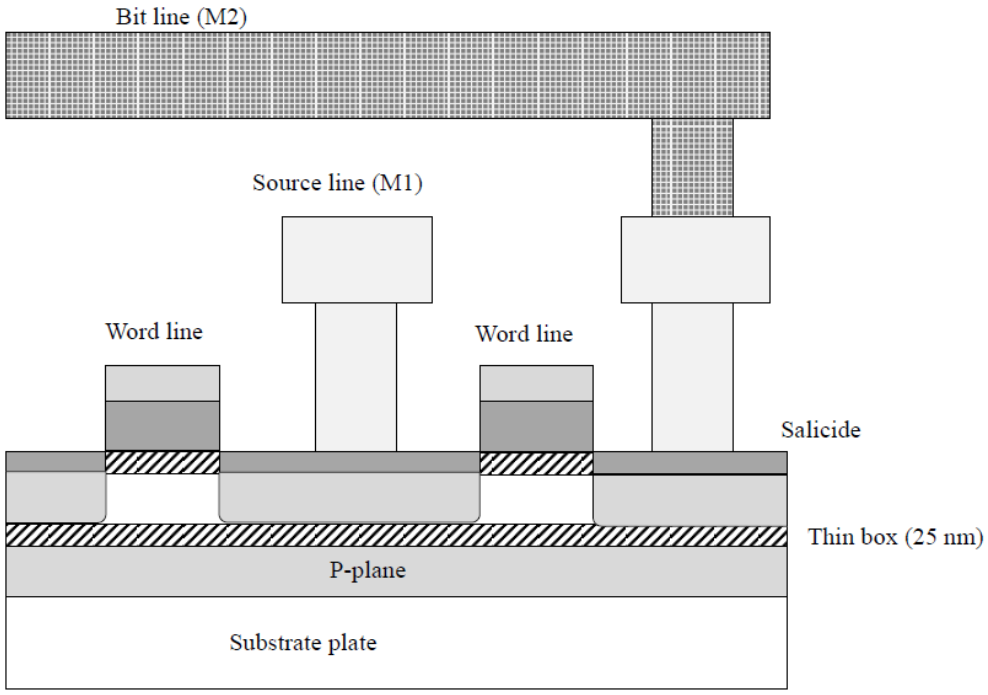


Figure 22. Schematic of the FBC structure

The memory cell consists of one transistor on SOI substrate with thin buried oxide. The unit cell size of the FBC is 6.24F2 because the source and drain regions are shared by the neighboring cells. Figure 23 shows a layout of the FBC array. The unit cell area is 6.24F2 (0.214 μm²) [45].

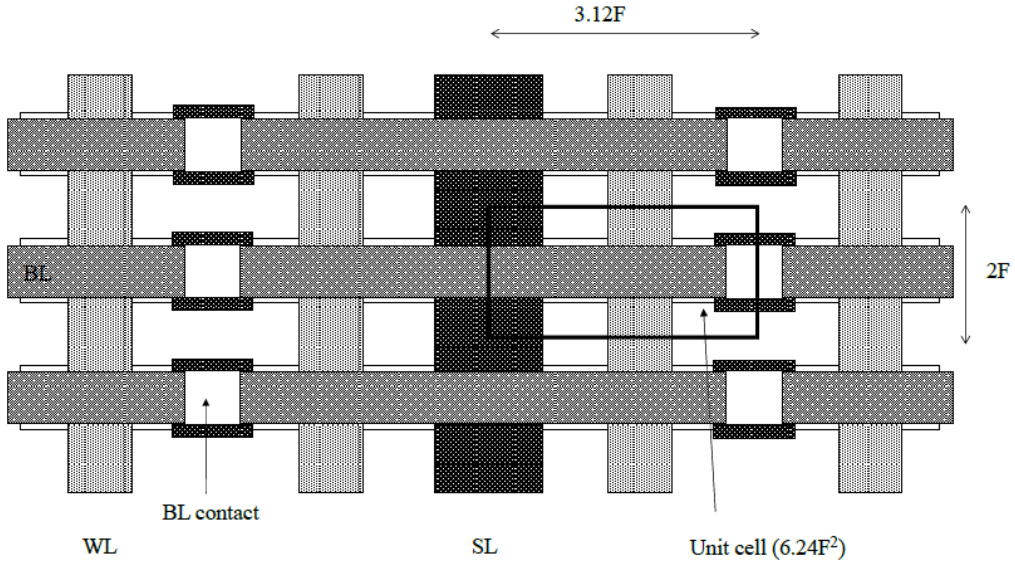


Figure 23. Layout image of the FBC array

2.7 The FBC cell transistor structure

We have succeeded in producing 128-Mb SOI DRAM employing FBC [56]. In this study, I demonstrate the measurement data of the HCI of the FBC in 128-Mb SOI DRAM. The FBC process is based on 90 nm node embedded DRAM (eDRAM). We have two types of FBC, one is eDRAM type and another is logic compatible one. The eDRAM type uses cell transistor of eDRAM for FBC cell. Figure 24(a) shows the cross-sectional structure of the eDRAM type. We have another type of FBC called logic compatible one. In this case, the cell transistor formation process for eDRAM is removed, and the logic transistor produces FBC cell transistor. Figure 24(b) shows the cross-sectional structure of the logic compatible type.

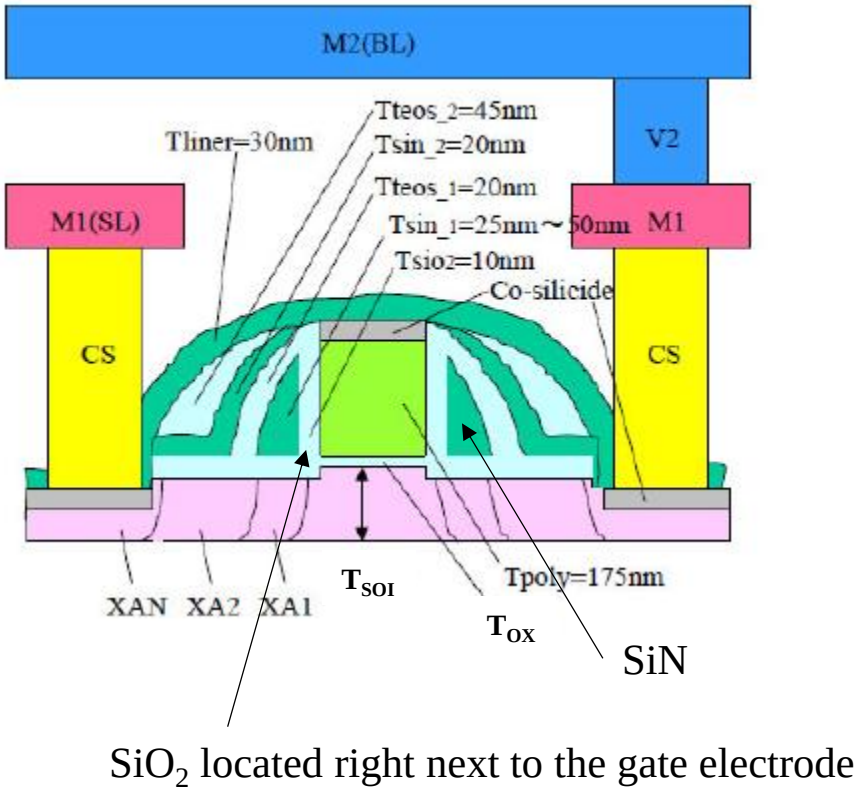


Figure 24(a). Cross-sectional structure of eDRAM type cell transistor

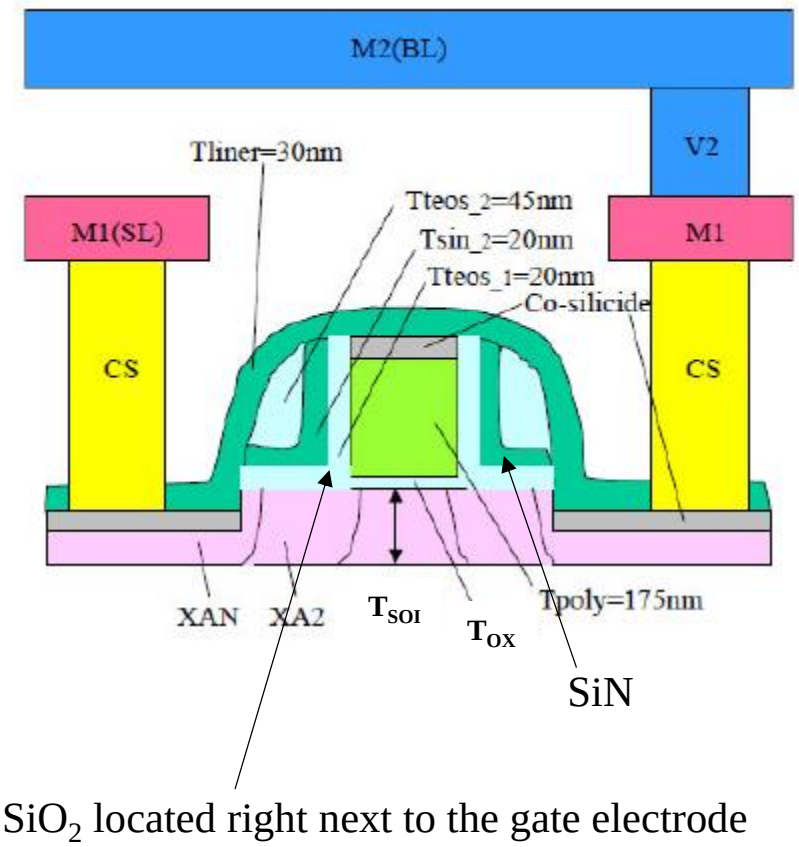


Figure 24(b). Cross-sectional structure of Logic CMOS type cell transistor

The gate length of the FBC cell transistor and the thickness of the gate silicon dioxide (SiO_2) was 150 and 6 nm, respectively. Table III indicates the outline of FBC.

Table III. Outline of the FBC Cell Transistor.

L_{gate}	150 nm
T_{OX}	6 nm
V_d	2.3 V
V_g	1.5 V
T_{SOI}	55 nm
T_{BOX}	25 nm

Figures 24(a) and 24(b) show that the sidewall structures are different between these two types. In the eDRAM type, the total thickness of sidewall spacers including SiO_2 and silicon nitride (SiN) films was thickened to reduce the electric field in order to improve retention characteristics.

Chapter 3 Results and discussions

3.1 Isub max model of hot carrier effect in MOS transistors

The current from the source to drain of the MOS transistors generate hot carriers, which jump to the gate electrode. As shown in Fig. 25, at this time, they damage the gate oxide they pass through, causing traps and shortening the lifetime of the MOS transistors. As the electric field applied to the crystal becomes stronger, only a portion of the energy that the electron and hole carriers gain from the electric field is transferred to the crystal lattice, creating a non-equilibrium state in which the temperature of the carriers is higher than that of the crystal. Such carriers are called hot carriers (hot electrons and hot holes). In fact, the drain current Id gradually decreases as the MOS transistors continues to operate.

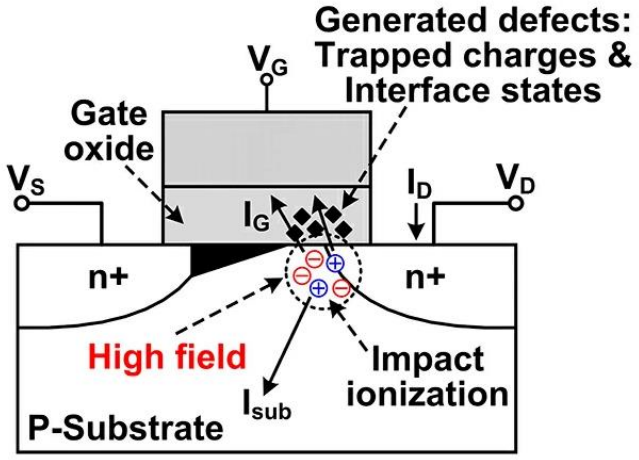


Figure 25. Schematic diagram of Hot Carrier Effects in MOSFETs

In the case of FBC, there is a regulation that V_d=2.3V operation and Id degradation must be within 10% in 50 years. I checked to see if the FBCs in this study met this requirement.

3.2 Measurement contents of the HCI of the FBC cell transistors

In this study, I defined HCI as degradation of I_d or V_{th} after saturation region stress condition at room temperature. After saturation region stress, both linear and saturation region I_d or V_{th} are degraded. However, since the read-in state of FBC is I_d or V_{th} in linear region as shown in later in Fig. 26, the degradation of I_d or V_{th} in linear region were focused in this study. Figure 26 shows the measurement contents of HCI of the FBC cell transistors [66] – [67].

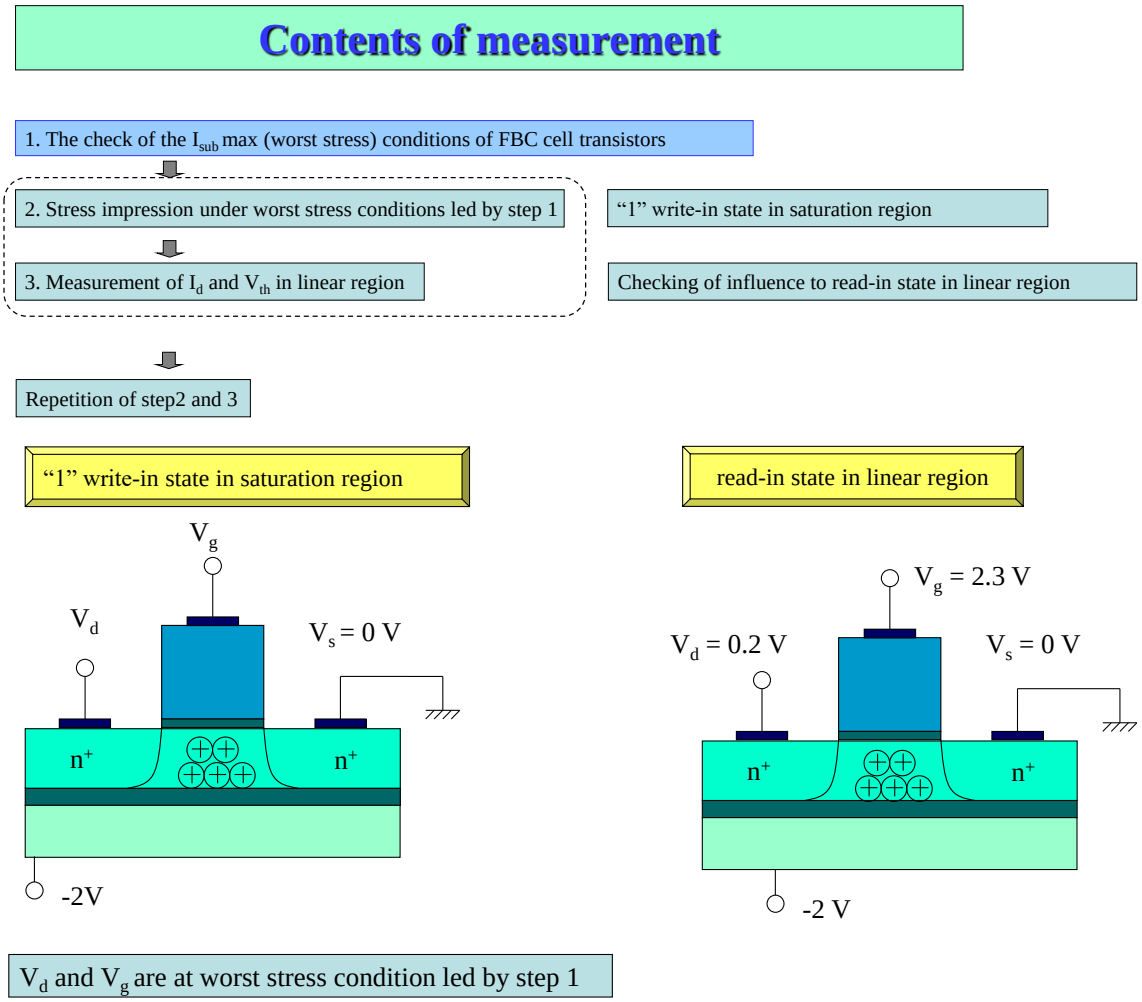


Figure 26. Measurement contents of HCI of FBC

For accurate measurements, at first the linear region I_d and V_{th} were measured with V_d at 0.2 V and gate voltage (V_g) at 2.3 V, which are denoted as I_{dlin0} and V_{thlin0}. Then the linear region I_d and V_{th} were measured again with V_d at 0.2 V and V_g at 2.3 V after the 50 years' equivalent saturation region stress condition of V_d at 2.3 V and V_g at worst stress condition. This I_d and V_{th} are denoted as $I_{dlin10y}$ and $V_{thlin10y}$, and V_g at worst stress condition will be discussed in more detail later in this thesis. I defined the degradation degree of Id as ΔI_{dlin} at (I_{dlin0} - $I_{dlin10y}$)/I_{dlin0} and the degradation degree of Vth as ΔV_{thlin} at (V_{thlin0} - $V_{thlin10y}$). If ΔI_{dlin} is less than 10% or ΔV_{thlin} is than 10 mV, the FBC satisfies the HCI specification regulation. Since the experimental time of 50 years is not realistic, accelerated test with V_d swing was performed. I investigated the time dependence of ΔI_{dlin} and ΔV_{thlin} on V_d in saturation region stress condition. For HCI, it was important how to

change V_g when changing V_d. For reliability-related measurements such as HCI, V_g in the stress condition of saturation region should be set to be the worst stress condition. There were numerous studies on the worst stress condition of SOI-MOS in saturation region [57 - 66], [68 - 75]. Nevertheless, it is unfixed today if there are any differences between bulk devices and SOI devices, partially depleted devices and fully depleted devices, and body contacted devices and floating body devices. Generally, it appears that the substrate current (I_{sub}) max condition ($V_g \sim 1/2V_d$) was the worst stress condition of HCI for SOI nMOS [66] - [68]. However, there is a report for SOI nMOS that degradation is larger when V_g at V_d (I_g max condition) [68], [71] - [73]. In this study, I verified the dependences of the HCI of the FBC on these two stress conditions. Figure 27 shows a layout image of a checked SOI NMOS transistor.

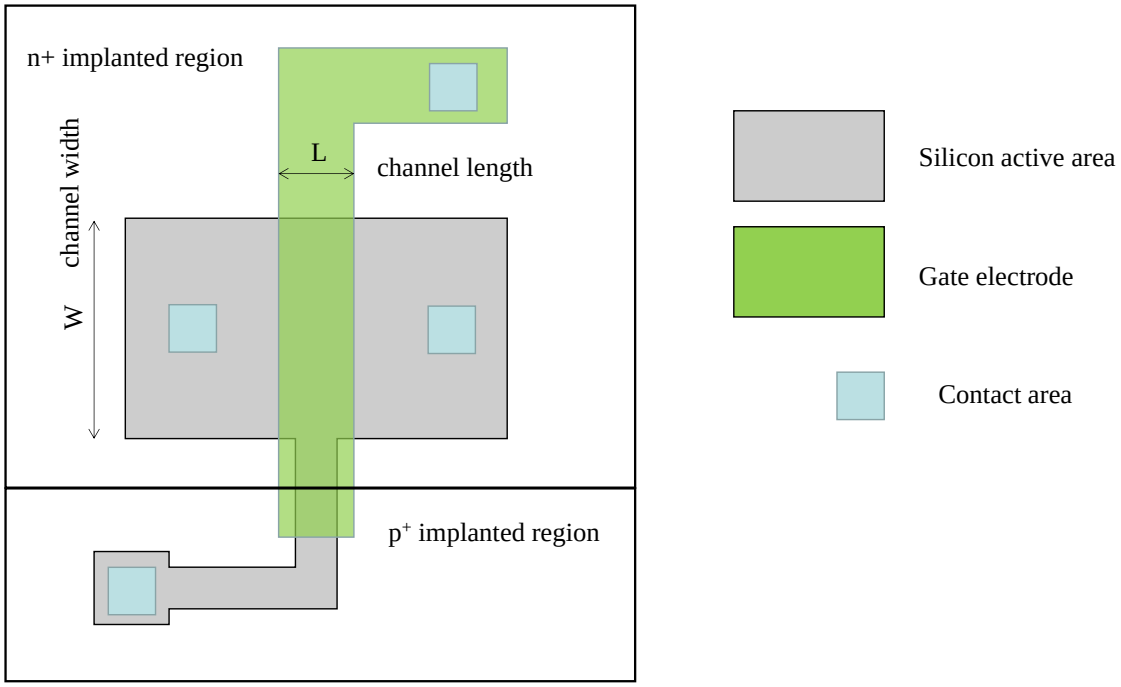
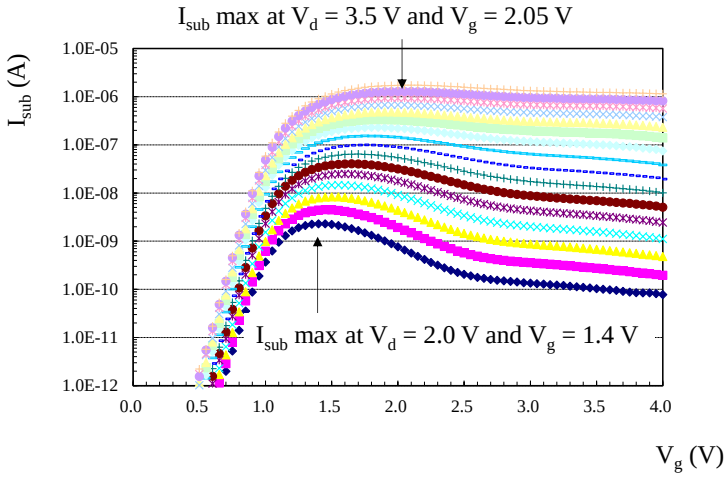


Figure 27. Layout image of body contacted SOI NMOS transistor

Figure 27 shows that body potential and current were checked through the p^+ implanted region of the silicon active area. A body contact condition and floating body condition (without body contact condition) were used for SOI-MOSFET (FBC Cell transistor). First, I verified the HCI on I_{sub} max condition with body voltage equal to 0 V. Figure 28(a)

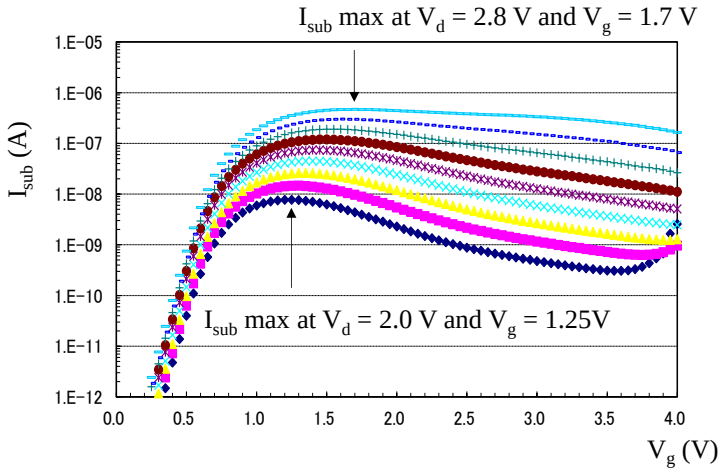
shows plots of I_{sub} vs. V_g in the V_d ranging from 2.0 to 3.5 V on the body contacted FBC cell transistor for Logic CMOS type with L/W = 0.15 µm/1.0 µm where L is defined as channel length, and W is defined as channel width as shown in Fig. 27. Each symbol of the same color means the same V_d. The V_g that maximizes I_{sub} at each V_d is listed in the table on the right. Maximized I_{sub} is denoted as I_{sub} max.



	V_d	V_g at I_{sub} max		$V_d/2$
+	3.5	2.05	>	1.75
●	3.4	2.05	>	1.70
x	3.3	2.00	>	1.65
x	3.2	2.00	>	1.60
▲	3.1	1.90	>	1.55
■	3.0	1.85	>	1.50
◆	2.9	1.85	>	1.45
-	2.8	1.75	>	1.40
-	2.7	1.75	>	1.35
+	2.6	1.70	>	1.30
●	2.5	1.65	>	1.25
x	2.4	1.60	>	1.20
x	2.3	1.55	>	1.15
▲	2.2	1.50	>	1.10
■	2.1	1.45	>	1.05
◆	2.0	1.40	>	1.00 (V)

Figure 28(a). Plots of I_{sub} vs. V_g in the V_d ranging from 2.0 to 3.5V on the body contacted FBC cell transistor for Logic CMOS type with L/W = 0.15 µm/1.0 µm. Each symbol of the same color means the same V_d.

The V_g that maximizes I_{sub} at each V_d is listed in the table on the right. Maximized I_{sub} is defined as I_{sub} max. Figure 28(b) shows same plots in the V_d ranging from 2.0 to 2.8 V for eDRAM type.



	V_d	V_g at I_{sub} max		$V_d/2$
-	2.8	1.70	>	1.40
-	2.7	1.60	>	1.35
+	2.6	1.00	>	1.30
●	2.5	1.50	>	1.25
x	2.4	1.45	>	1.20
x	2.3	1.40	>	1.15
▲	2.2	1.35	>	1.10
■	2.1	1.30	>	1.05
◆	2.0	1.25	>	1.00 (V)

Figure 28(b). Plots of I_{sub} vs. V_g in the V_d ranging from 2.0 to 2.8V on the body contacted FBC cell transistor for eDRAM type with L/W = 0.15μm/1.0 μm. Each symbol of the same color means the same V_d like Logic CMOS one. The V_g that maximizes I_{sub} at each V_d is listed in the table on the right.

As shown in Fig. 28, the Logic CMOS type and eDRAM type showed almost the same I_{sub} dependence on V_g. In SOI-MOS, bell-shape like bulk MOS does not appear clearly, and V_g which gives I_{sub} max falls in the region with more than 1/2 V_d as shown in Fig. 28. This comes from the fact that substrate current flows more than bulk-MOS by self-heating in SOI-MOS [74] - [76]. Same checks were also made for the FBC cell transistor with L/W = 0.15 μm/0.18 μm. Note that the measured transistor's channel width W was set to be 0.18 μm for the target transistor size, while a transistor with a channel width of 1.0 μm was added from the viewpoint of stability of measurement. Table IV summarizes typical V_g which gives I_{sub} max for both eDRAM type and Logic CMOS one. The description above corresponds to the first step of Fig. 26.

Table IV. Summary of typical V_g at I_{sub} max conditions for both eDRAM and Logic CMOS body contacted FBC cell transistors

	eDRAM type	
	W (μm)	
	0.18	1.00
V_d	V_g	V_g
2.0	1.25	1.25
2.2	1.35	1.35
2.4	1.45	1.45
2.6	1.55	1.55
2.8	1.60	1.70

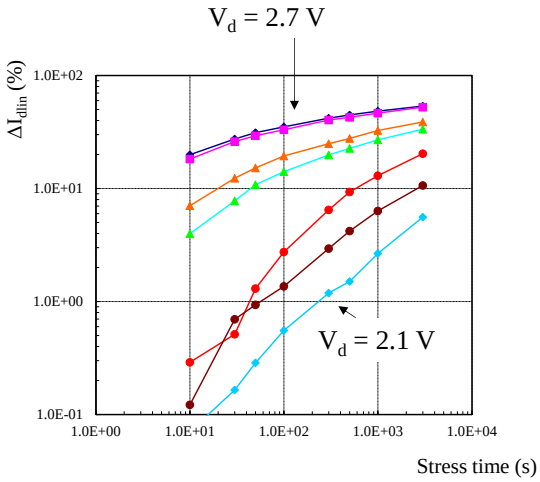
(V)

	Logic CMOS type	
	W (μm)	
	0.18	1.00
V_d	V_g	V_g
2.0	1.45	1.40
2.1	1.50	1.45
2.2	1.55	1.50
2.3	1.60	1.55
2.4	1.65	1.60
2.5	1.70	1.65
2.6	1.75	1.70
2.7	1.80	1.75
2.8	1.85	1.75
2.9	1.85	1.85
3.0	1.90	1.85
3.1	1.90	1.90
3.2	2.00	2.00
3.3	2.05	2.00
3.4	2.10	2.05
3.5	2.20	2.05
3.6	2.20	2.15
3.7		2.10
3.8	2.35	2.20
3.9		2.20
4.0	2.47	2.30
4.1		2.25
4.2	3.50	2.45
4.3		2.50
4.4	3.60	2.55
4.5		2.55
4.6	3.85	2.60
4.7		2.70

(V)

3.3 Measurement of the HCI by I_{sub} max condition

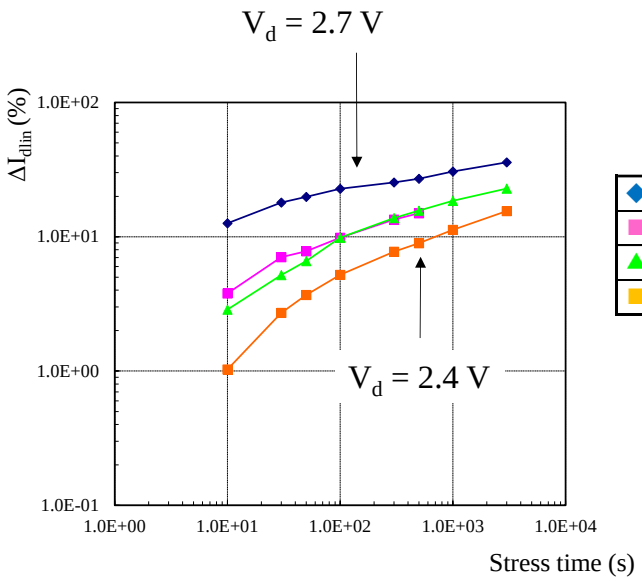
Next the 2nd and 3rd steps in the measurements of Fig. 26 were made for eDRAM type with L/W = 0.15 μm/1.0 μm case. The linear region I_d and V_{th} were measured again with V_d at 0.2 V and V_g at 2.3 V condition after 10 to 3000 seconds saturation region stress of V_d at 2.4 V and V_g at 1.45 V condition, which corresponds to I_{sub} max. Then the same measurements were made for saturation region stress of V_d at 2.5 V with V_g at 1.5 V, V_d at 2.6 V with V_g at 1.55 V, and V_d at 2.7 V with V_g at 1.58 V conditions, which also correspond to I_{sub} max. Figure 29(a) shows plots of ΔI_{dlin} vs. time in the V_d ranging from 2.1 to 2.7 V on the body contacted FBC cell transistor. Each symbol of the same color means the same V_d. Same measurements were also made for L/W = 0.15 μm/0.18 μm case. Figure 29(b) shows plots of ΔI_{dlin} vs. time in the V_d ranging from 2.4 to 2.7 V.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
◆	2.7	1.63	2.3
■	2.6	1.55	2.3
▲	2.5	1.50	2.3
▲	2.4	1.45	2.3
●	2.3	1.40	2.3
●	2.2	1.35	2.3
◆	2.1	1.30	2.3

(V)

Figure 29(a). Plots of ΔI_{dlin} vs. time in the V_d ranging from 2.1 to 2.7 V on the body contacted FBC cell transistor of eDRAM type with L/W = 0.15 μm/1.0 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
◆	2.7	1.58	2.3
■	2.6	1.55	2.3
▲	2.5	1.50	2.3
■	2.4	1.45	2.3

(V)

Figure 29(b). Plots of ΔI_{dlin} vs. time in the V_d ranging from 2.4 to 2.7 V on the body contacted FBC cell transistor of eDRAM type with $L/W = 0.15$ µm/0.18 µm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.

From Fig. 29, the times were extracted in the case of $\Delta I_{dlin} = 10\%$ on each V_d. This time was defined as lifetime in this study. Figure 30 shows plots of 1/Vd vs. lifetime. It is generally known that the hot carrier lifetime of a semiconductor is proportional to the inverse of the power supply voltage exponent, and based on experiments, the following equation has been derived [66].

Life Time ～ exp(A/Vd) A is a constant specific to the material.

From Fig. 30, I predicted the V_d with which lifetime becomes 50 years with $L/W = 0.15$ µm/1.0 µm case was 1.67 V, and that with $L/W = 0.15$ µm/0.18 µm case was 1.78 V [67]. Therefore, judging from ΔI_{dlin}, the lifetime is smaller with $W = 1.0$ µm case than that with $W = 0.18$ µm case.

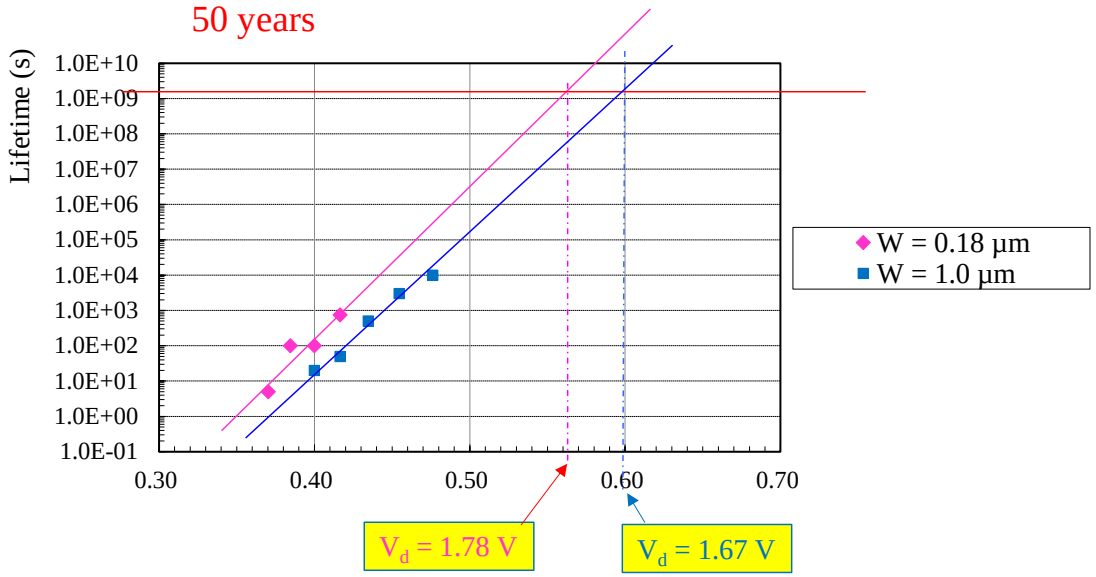
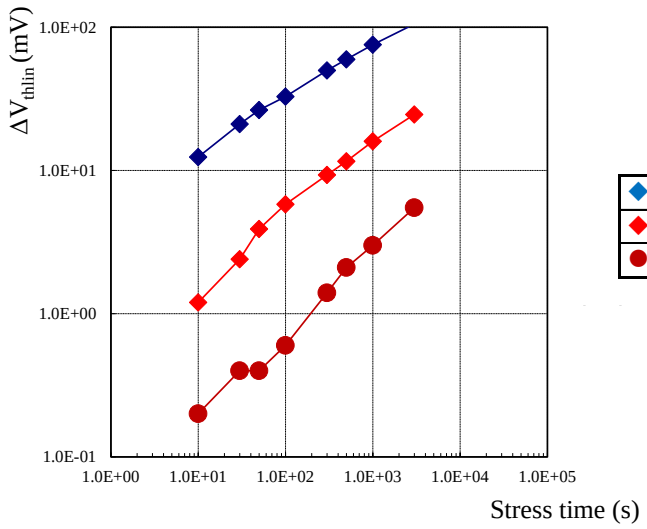


Figure 30. Plots of $1/V_d$ vs. lifetime of eDRAM type cell transistors on body contacted cases. Red symbols indicate W = 0.18 μm case and blue symbols indicate W = 1.0 μm case. Each stress V_g (Write-in V_g) was determined by Table IV.

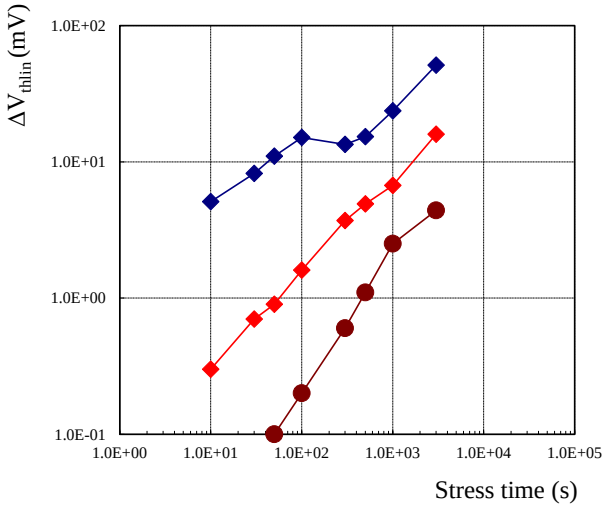
Next Fig. 31(a) shows plots of ΔV_{thlin} vs. time in the V_d ranging from 2.1 to 2.7 V on the body contacted FBC cell transistor. Each symbol of the same color means the same V_d. Same measurements were also made for L/W = 0.15 μm/0.18 μm case. Figure 31(b) shows plots of ΔV_{thlin} vs. time in the V_d ranging from 2.4 to 2.7 V. From Fig. 31, the times were extracted in the case of ΔV_{thlin} = 10 mV on each V_d. This time was also defined as lifetime in this study. Figure 32 shows plots of $1/V_d$ vs. lifetime.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
◆	2.7	1.63	2.3
◆	2.4	1.45	2.3
●	2.2	1.40	2.3

(V)

Figure 31(a). Plots of ΔV_{thlin} vs. time in the V_d ranging from 2.2 to 2.7 V on the body contacted FBC cell transistor of eDRAM type with $L/W = 0.15$ μm/1.0 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
◆	2.7	1.63	2.3
◆	2.4	1.45	2.3
●	2.2	1.40	2.3

(V)

Figure 31(b). Plots of ΔV_{thlin} vs. time in the V_d ranging from 2.2 to 2.7 V on the body contacted FBC cell transistor of eDRAM type with $L/W = 0.15$ μm/0.18 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.

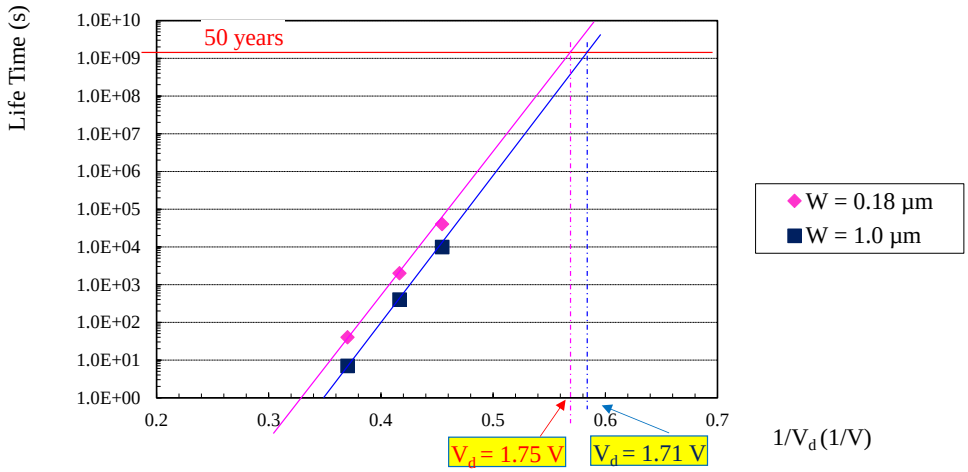
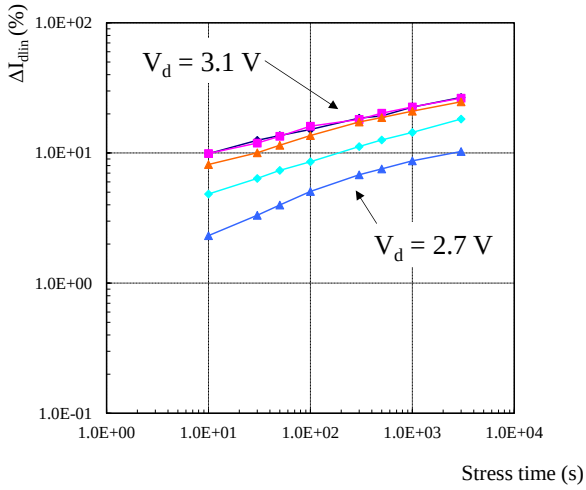


Figure 32. Plots of $1/V_d$ vs. lifetime determined by ΔV_{thlin} of eDRAM type cell transistors on body contacted cases. Red symbols indicate W = 0.18 µm case and blue symbols indicate W = 1.0 µm case. Each stress V_g (Write-in V_g) was determined by Table IV.

Each stress V_g (Write-in V_g) was determined by Table IV. From Fig. 32, I predicted the V_d with which lifetime becomes 50 years with L/W = 0.15 µm/1.0 µm case was 1.71 V, and that with L/W = 0.15 µm/0.18 µm case was 1.75 V. Therefore, judging from ΔV_{thlin}, the lifetime is also smaller with W = 1.0 µm case than that with W = 0.18 µm case.

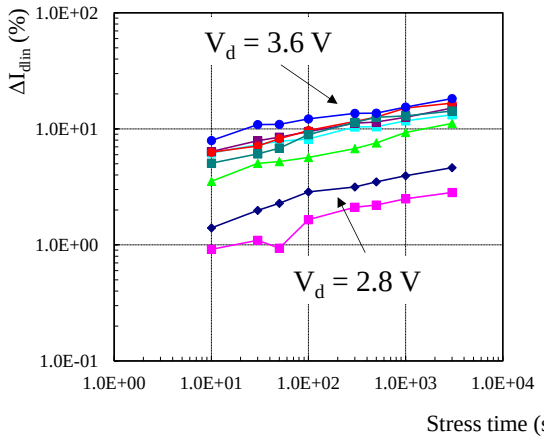
Next, the same measurements were made for Logic CMOS type. Measurement results are showed in Fig. 33(a) for the case of L/W = 0.15 µm/1.0 µm, and in Fig. 33(b) for the case of L/W = 0.15 µm/0.18 µm. From Fig. 33, the lifetime was extracted on each V_d. Figure 34 shows plots of $1/V_d$ vs. lifetime. From Fig. 34, I predicted the V_d with which lifetime becomes 50 years with L/W = 0.15 µm/1.0 µm case was 2.13 V, and that with L/W = 0.15 µm/0.18 µm case was 2.27 V.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
◆	3.1	1.90	2.3
■	3.0	1.85	2.3
▲	2.9	1.85	2.3
◆	2.8	1.75	2.3
▲	2.7	1.75	2.3

(V)

Figure 33(a). Plots of ΔI_{dlin} vs. time in the V_d ranging from 2.7 to 3.1 V on the body contacted FBC cell transistor of Logic CMOS type with L/W = 0.15 μm/1.0 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
●	3.6	2.40	2.3
■	3.4	2.10	2.3
●	3.3	2.05	2.3
■	3.2	2.00	2.3
■	3.1	1.90	2.3
▲	3.0	1.90	2.3
■	2.9	1.85	2.3
◆	2.8	1.85	2.3

(V)

Figure 33(b). Plots of ΔI_{dlin} vs. time in the V_d ranging from 2.8 to 3.6 V on the body contacted FBC cell transistor of Logic CMOS type with L/W = 0.15 μm/0.18 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.

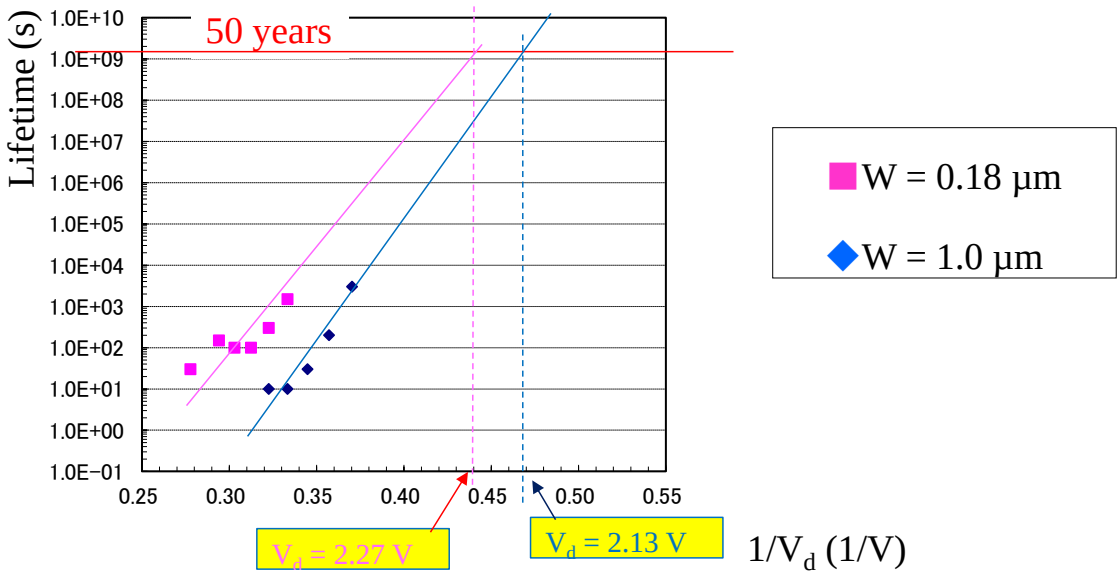
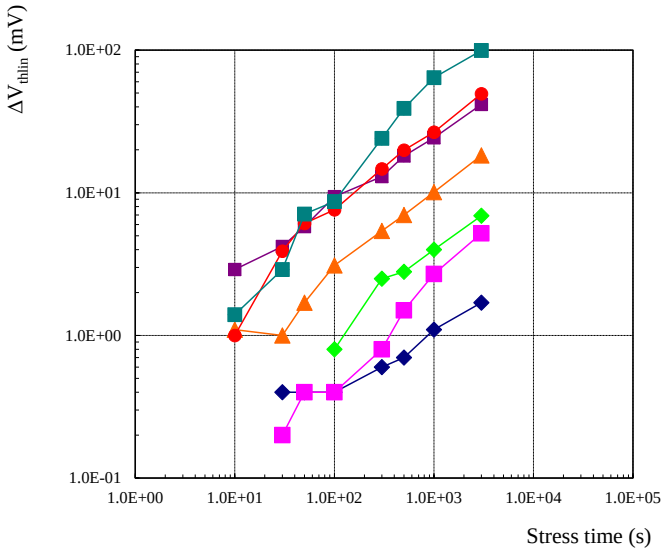


Figure 34. Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors on body contacted cases. Red symbols indicate $W = 1.0$ µm case and blue symbols indicate $W = 0.18$ µm case. Each stress V_g (Write-in V_g) was determined by Table IV.

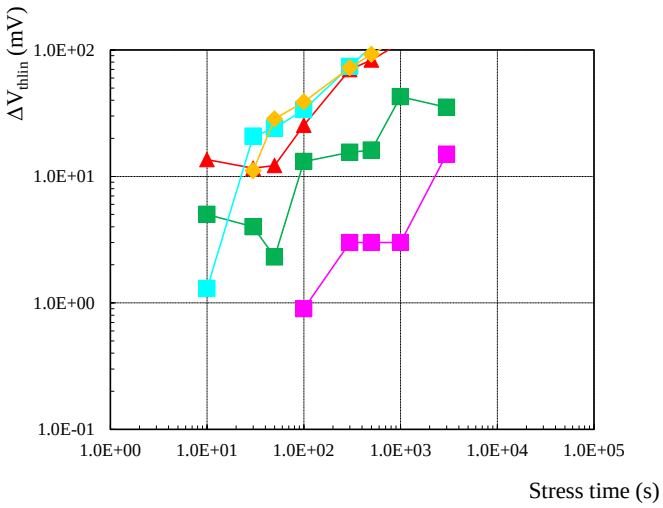
Next Fig. 35(a) shows plots of ΔV_{thlin} vs. time in the V_d ranging from 2.1 to 2.7 V on the body contacted FBC cell transistor. Each symbol of the same color means the same V_d. Same measurements were also made for $L/W = 0.15$ µm/0.18 µm case. Figure 35(b) shows plots of ΔV_{thlin} vs. time in the V_d ranging from 2.4 to 2.7 V. From Fig. 35, the lifetime was extracted on each V_d. Figure 36 shows plots of $1/V_d$ vs. lifetime. From Fig. 36, I predicted the V_d with which lifetime becomes 50 years with $L/W = 0.15$ µm/1.0 µm case and that with $L/W = 0.15$ µm/0.18 µm case were 2.22 V. Figure 36 shows that the lifetime of the Logic CMOS type transistors showed no significant dependence on channel width W. Table V shows a summary of the V_d of 50 years of lifetime under Isub max condition. The V_d of 50 years of lifetime of Logic CMOS type drastically improves by 0.5 ~ 0.6 V against eDRAM type. Considering that the parameter that directly affects cell readout is not ΔV_{th} but ΔI_d at constant gate voltage, I decided to adopt ΔI_{dlin} for the HCI specification of FBC from now on.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
■	4.3	2.50	2.3
●	4.0	2.30	2.3
■	3.7	2.10	2.3
◆	3.6	2.15	2.3
▲	3.5	2.05	2.3
■	3.4	2.05	2.3
◆	3.1	1.90	2.3

(V)

Figure 35(a). Plots of ΔV_{thlin} vs. time in the V_d ranging from 2.2 to 2.7 V on the body contacted FBC cell transistor of eDRAM type with $L/W = 0.15$ μm/1.0 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.



	V_d	Stress V_g (Write-in V_g)	Read-in V_g
◆	4.8	4.10	2.3
■	4.4	3.60	2.3
▲	4.0	2.47	2.3
■	3.8	2.35	2.3
■	3.4	2.10	2.3

(V)

Figure 35(b). Plots of ΔV_{thlin} vs. time in the V_d ranging from 2.2 to 2.7 V on the body contacted FBC cell transistor of eDRAM type with $L/W = 0.15$ μm/0.18 μm. Each symbol of the same color means the same V_d. Each stress V_g (Write-in V_g) was determined by Table IV.

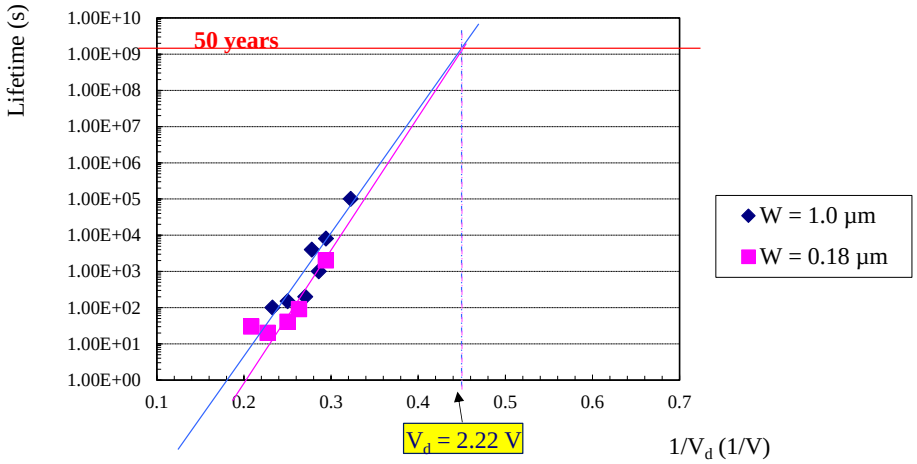


Figure 36. Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors on body contacted cases. Red symbols indicate W = 1.0 µm case and blue symbols indicate W = 0.18 µm case. Each stress V_g (Write-in V_g) was determined by Table IV.

Table V. Summary of V_d of 50 years of lifetime under the I_{sub} max condition on body contacted cases

		V_d (V) by Δ id		V_d (V) by Δ Vth		
		W (µm)	W (µm)	W (µm)	W (µm)	
	T_{SOI} (nm)	0.18	1.0	0.18	1.0	
eDRAM type	55	1.78	1.67	1.75	1.71	
Logic CMOS type	55	2.27	2.13	2.22	2.22	(V)

3.4 Analysis of difference in the HCI between eDRAM type and Logic CMOS one

As shown in Table V, the eDRAM type was inferior to the Logic CMOS one from the viewpoint of the V_d of 50 years of lifetime. Furthermore, the eDRAM type does not meet the V_d criteria of 2.3 V as 50 years of lifetime. There is a difference in cross-sectional structure between eDRAM type and Logic CMOS one. Figures 24(a) and 24(b) show that the SiO_2 thickness between SiN nitride film and silicon substrate are different. In eDRAM type, the SiO_2 located right next to the gate electrode is a thermal SiO_2 and the thickness is 10 nm and that of the Logic CMOS type is TEOS oxide and the thickness is 20 nm. It seems that the nitride sidewall existing outside of the SiO_2 becomes the source of the defects and trap center. Therefore, it seems that the influence from the nitride sidewall is more weakened in the Logic CMOS type compared with the eDRAM one by the difference of thickness of this SiO_2 [63]. Based on the analysis up to this point, I will now focus our discussion on Logic CMOS type.

3.5 $V_g = V_d$ model of hot carrier effect in SOI MOS transistors

Regarding the maximum condition of hot carrier effect in SOI MOS, there are two groups: one group argues for the Isub max condition as in Bulk-MOS [52] – [54, 55], and the other group argues for $V_g = V_d$ (Ig max condition) [56] – [59], which is different from Bulk-MOS, and even now there is no settled theory. Briefly explain the basis for claiming that the maximum condition for hot carrier effect in SOI MOS is $V_g = V_d$ (I_g max condition). Before that, I will review the basis for claiming that the Isub max condition is the maximum condition for hot carrier effect in SOI MOS. As shown in Fig. 37, in Bulk MOS devices, the hot carrier effect occurs due to carrier migration and collisions.

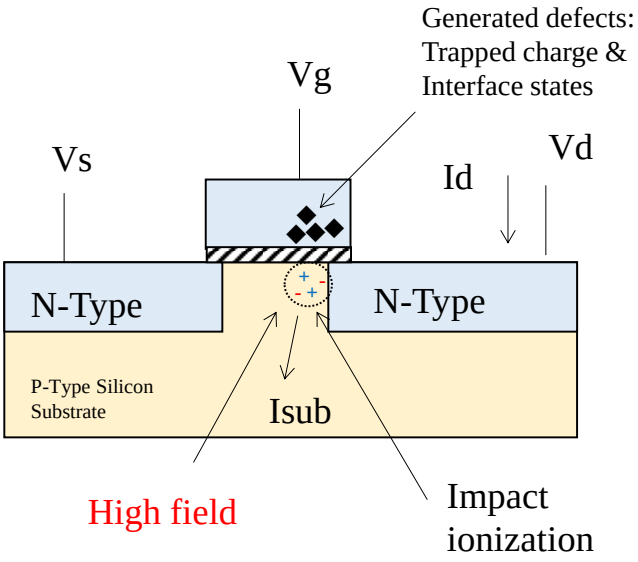


Figure 37. Schematic diagram of the hot carrier effect in Bulk MOS

Isub max is the maximum value of the substrate current and is the condition under which carrier migration and collisions occur most frequently. Hot carrier effect becomes more pronounced. On the other hand, the $V_g = V_d$ model is as follows. As shown in Fig. 38, in SOI devices, the channel is insulated from the substrate by the insulator, which limits carrier migration and tends to suppress Isub (is it there in the first place?). Therefore, in SOI devices, the hot carrier effect is reduced due to the limitation by the insulator, and maximization of hot carriers under Isub max conditions is not expected. Rather, the $V_g =$

V_d condition, where the electric field in the channel is maximized, is considered to be the condition for maximum hot carrier effect.

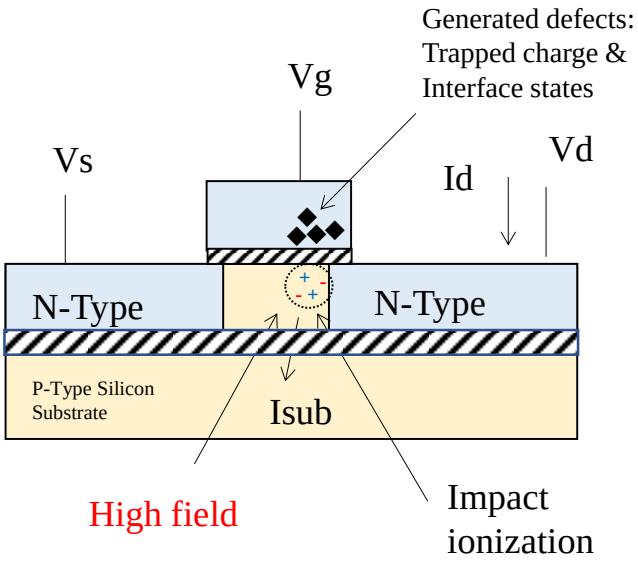


Figure 38. Schematic diagram of the hot carrier effect in SOI-MOS

3.6 Analysis of the HCI of Logic CMOS type cell transistor

As shown in Fig. 39 the actual maximum point of hot carrier effect in SOI-MOS depends on physical conditions such as device geometry, impurity concentration in the drain, thickness of the SOI-Si layer, thickness of the buried oxide layer, etc., and it is difficult to draw a general conclusion.

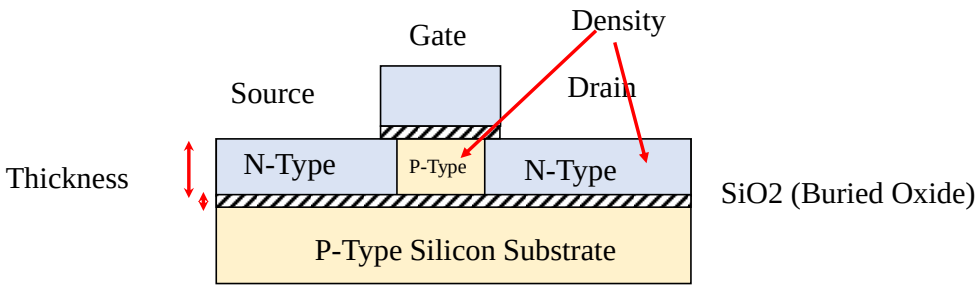


Figure 39. Factors affecting Hot Carrier Effect in SOI-MOS

So next I also checked the V_g at V_d (I_g max) condition. Thus, I measured the lifetime in both V_g at V_d case and I_{sub} max cases. In I_{sub} max case, body contact was needed in order to check I_{sub}. On the other hand, the body contact was not needed for $V_g = V_d$ case, but the body contact was applied to $V_g = V_d$ case as well in order to accurately compare $V_g = V_d$ and I_{sub} max case. To be precise, with and without body contact measurements were done for $V_g = V_d$ case. For comparison, without body contact measurements were also added to I_{sub} max case. Measurement results of the Logic CMOS type cell transistor in L/W = 0.15 µm/1.0 µm cases were shown in Fig. 40(a), Fig. 40 (b), Fig. 40(c) and Fig. 40(d). Table VI shows a summary of Fig. 40.

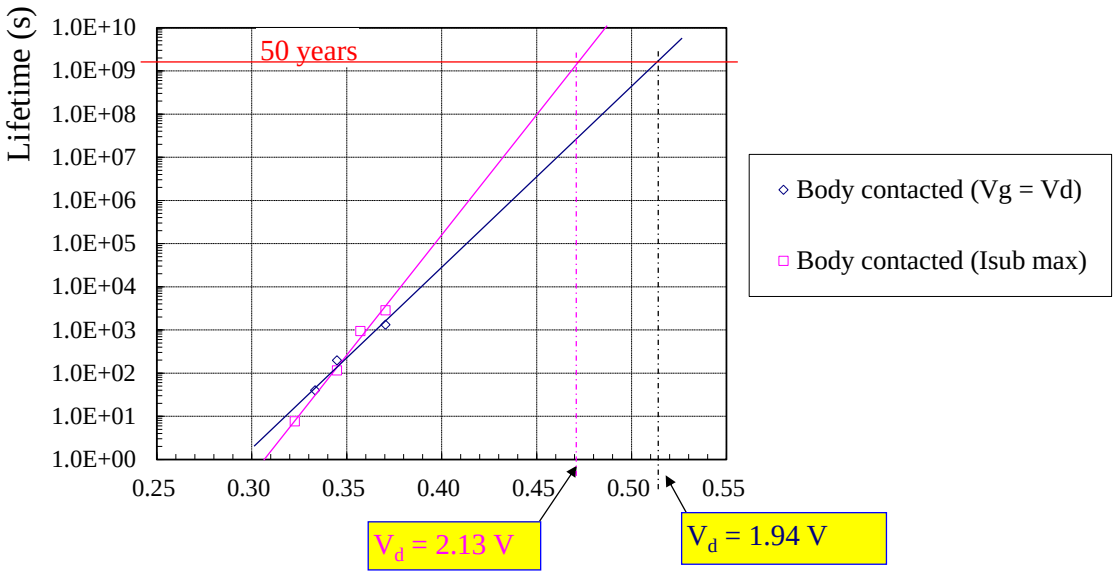


Figure 40(a). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in body contacted cases of L/W = 0.15 μm/1.0 μm. Stress conditions differ in two cases.

Open black symbols indicate $V_g = V_d$ case.

Open red symbols indicate I_{sub} max case. Each stress V_g (Write-in V_g) was determined by Table IV.

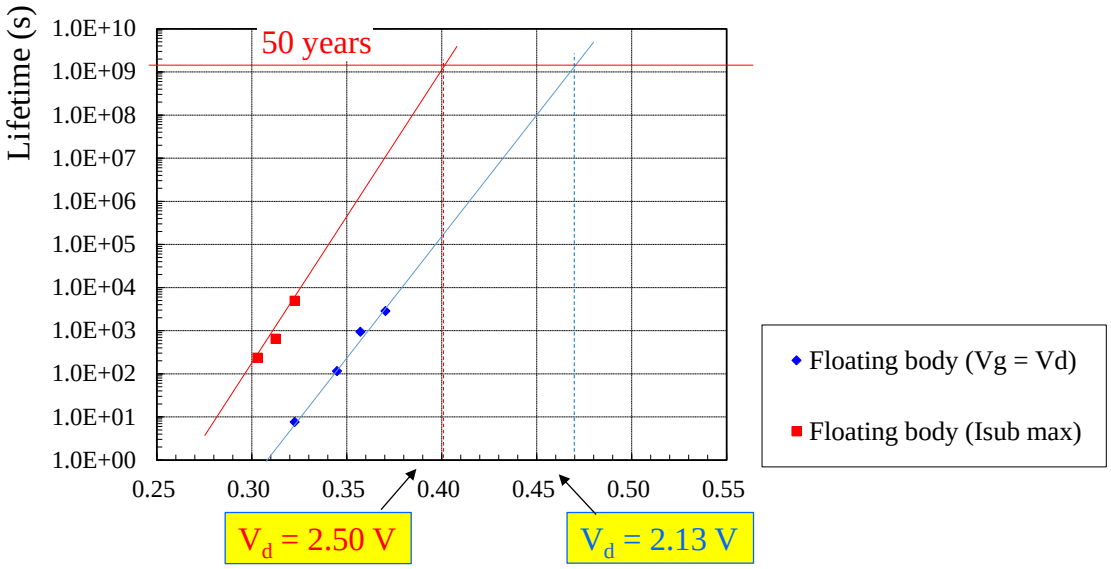


Figure 40(b). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in floating body cases of $L/W = 0.15$ μm/1.0 μm. Stress conditions differ in two cases.

Closed blue symbols indicate $V_g = V_d$ case.

Closed red symbols indicate I_{sub} max case. Each stress V_g (Write-in V_g) was determined by Table IV.

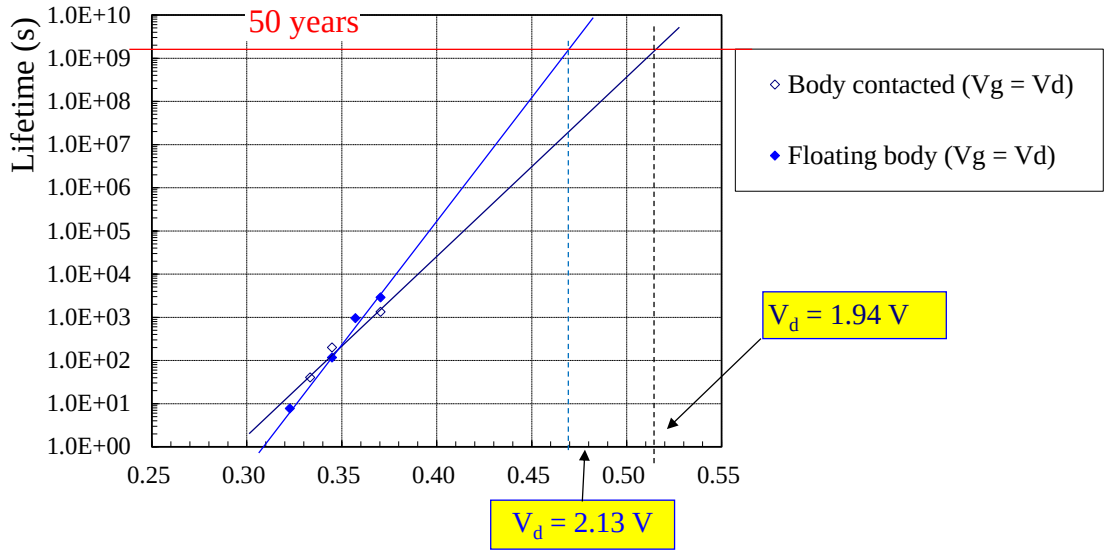


Figure 40(c). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in stress condition of $V_g = V_d$ cases of $L/W = 0.15$ μm/1.0 μm. Body potential differ in two cases.

Open black symbols indicate Body Contacted case (V_{sub} at 0 V).

Closed blue symbols indicate floating body case.

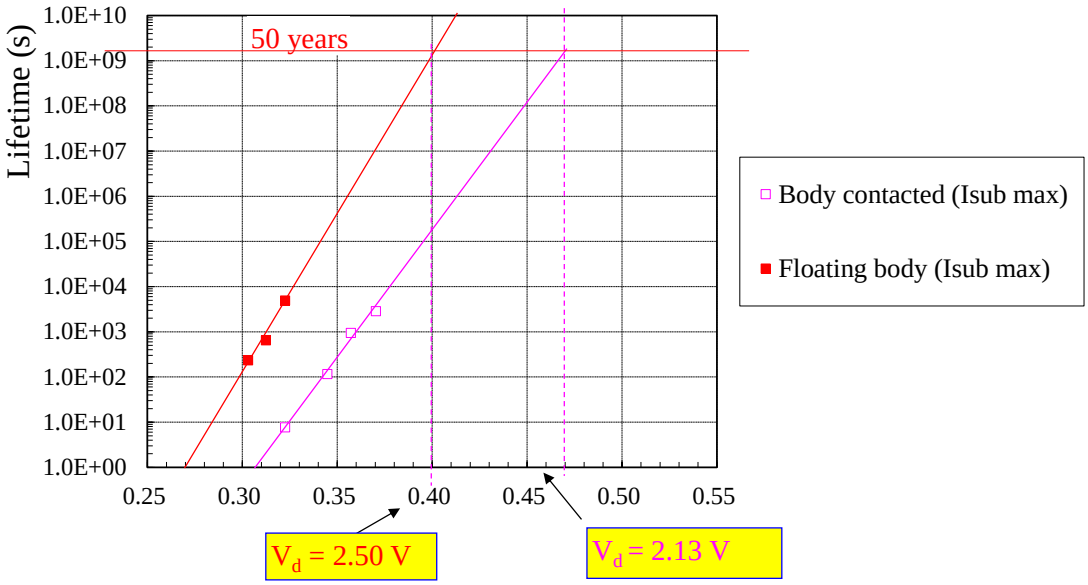


Figure 40(d). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in stress condition of I_{sub} max cases of $L/W = 0.15$ μm/1.0 μm. Body potential differ in two cases. Each stress V_g (Write-in V_g) was determined by Table IV.

Open red symbols indicate body contacted case (V_{sub} at 0 V).

Closed red symbols indicate floating body case.

Table VI. Dependence of V_d of 50 years of lifetime on stress and body potential conditions. Logic CMOS type cell transistors with $L/W = 0.15$ μm/1.0 μm.

Stress condition		V_d (V)
Body contacted (V_{sub} = 0 V)	$V_d = V_g$	1.94
	I_{sub} max	2.13
Floating Body	$V_d = V_g$	2.13
	I_{sub} max	2.50

Figures 40(a) and 40(b) compare the difference between I_{sub} max and $V_g = V_d$ cases. Figures 40(c) and 40(d) compare the difference between with and without body contact cases. Figures 40(a) and 40(b) show that the V_d of 50 years of lifetime in $V_g = V_d$ condition was lower than I_{sub} max case both with and without body contact cases. This means that the degradation of V_d is bigger in the $V_g = V_d$ condition than in I_{sub} max case. Figures 40(c) and 35(d) show that the V_d of 50 years of lifetime with body contact case was lower than without body contact case both in I_{sub} max and $V_g = V_d$ cases. I proposed the following model. It seems that the electric potential between gate and body was reduced by higher body potential by floating body effect without body contact case. Since HCI is proportional to electric field strength in body region of MOSFET [80], the HCI with body floating case seems to be more weakened than body contacted case. To confirm this model, the I_d-V_g measurement was performed by applying a potential from the body terminal in Fig. 27. Figure 41 shows plots of I_d vs. V_g in the V_{sub} (substrate voltage) ranging from 0.0 to 1.0 V for FBC cell transistor of Logic CMOS type with $L/W = 0.15$ μm/1.0 μm. Each symbol of the same color means the same V_{sub}.

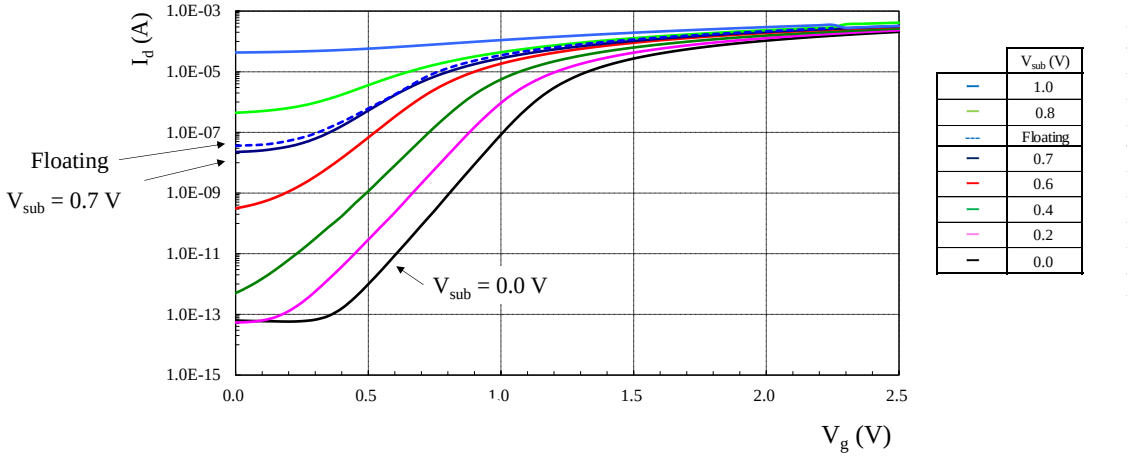


Figure 41. Plots of I_d vs. V_g in the V_{sub} ranging from 0.0 to 1.0 V of the FBC cell transistor of Logic CMOS type with $L/W = 0.15$ μm/1.0 μm. Each symbol of the same color means the same V_{sub}.

As shown in Fig. 41, V_{sub} at 0.7 V case shows almost the same plots as floating body case. In addition, measurements of ΔI_{dlin} vs. time were also made under V_{sub} at 0.7 V condition. Figure 42 shows plots of $1/V_d$ vs. lifetime. From Fig. 42, I predicted the lifetime with I_{sub} max was 2.55 V, and that with $V_g = V_d$ case was 2.34 V as shown in Table VII.

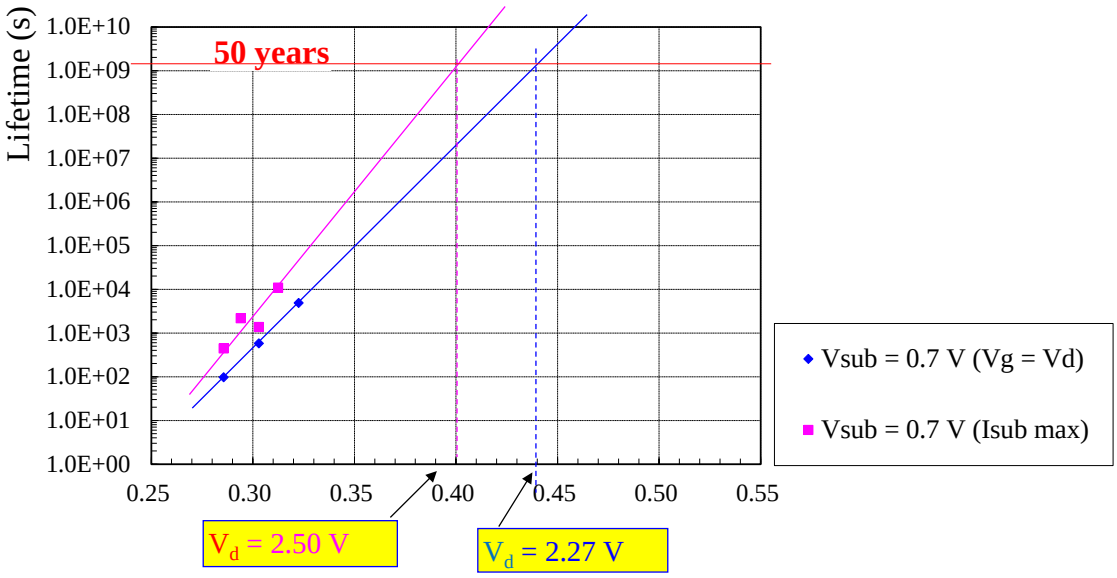


Figure 42. Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors with $L/W = 0.15$ µm/1.0 µm and V_{sub} at 0.7 V.

Stress conditions differ in two cases.

Closed blue symbols indicate I_{sub} max case. Each stress V_g (Write-in V_g) was determined by Table IV.

Open blue symbols indicate $V_g = V_d$ case.

Table VII. Summary of V_d of 50 years of lifetime under V_{sub} at 0.7 V condition. Logic CMOS type cell transistors with L/W = 0.15 μm/1.0 μm.

Stress condition		V_d (V)
Body contacted (V_{sub} = 0.7 V)	$V_d = V_g$	2.27
	I_{sub} max	2.50

From Table VI and VII, under I_{sub} max condition, V_d of 50 years of lifetime in body floating case and V_{sub} at 0.7 V case show almost the same value. These facts experimentally show that the body potential of floating body is 0.7 V in I_{sub} max condition. In other words, degradation of V_d is improved 0.7 V by the floating body effect under I_{sub} max condition in the FBC (SOI-MOS). The floating body effect in the FBC corresponds to the introduction of a cathode in the vacuum tube described in Chapter 1, which reduces damage to the device and significantly extends its lifetime. Under $V_g = V_d$ case, V_d of 50 years of lifetime in body contacted case and body floating case were 2.00 V and 2.19 V respectively. Although not actually measured experimentally, from Table VI and Table VII, it can be assumed that the body potential of $V_g = V_d$ case is thought to be raised, by floating effect not as good as I_{sub} max case, but with considerable amount over the body contacted case.

Body potential of real cell transistors of FBC is floating, so it needs to be cleared that V_d of 50 years of lifetime is higher than 2.3 V with W = 0.18 μm and stress condition of $V_g = V_d$ without body contact. As mentioned before, the measured transistor's channel width was set to 0.18 μm for the target transistor size but a transistor with a channel width of 1.0 μm was used in the experiments so far from the viewpoint of stability of measurement. As shown in Table VI, in W = 1.0 μm with body floating case, the V_d of 50 years of lifetime is 2.19 V at the worst condition of $V_d = V_g$, so in this case specification has not been reached. Thus, measurement results of the Logic CMOS type cell transistor

in L/W = 0.15 μm/0.18 μm cases were shown in Fig. 43(a), Fig. 43(b), Fig. 43(c) and Fig. 43(d). Table VIII shows a summary of Fig. 43.

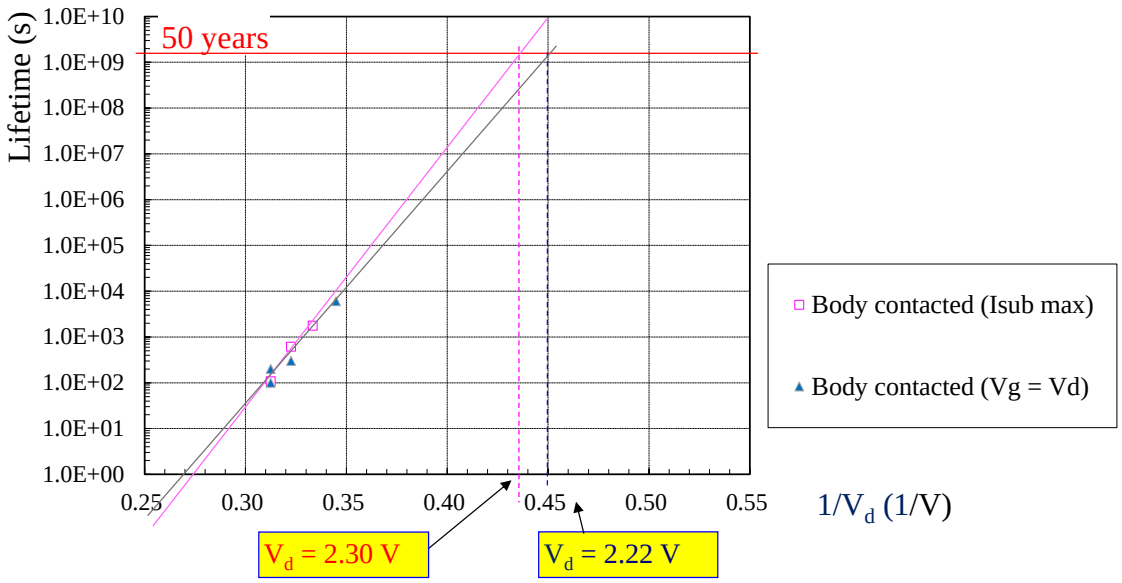


Figure 43(a). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in body contacted cases (V_{sub} at 0 V) of L/W = 0.15 μm/0.18 μm. Stress condition differs in two cases.

Open red symbols indicate I_{sub} max case. Each stress V_g (Write-in V_g) was determined by Table IV.

Closed blue symbols indicate $V_g = V_d$ case.

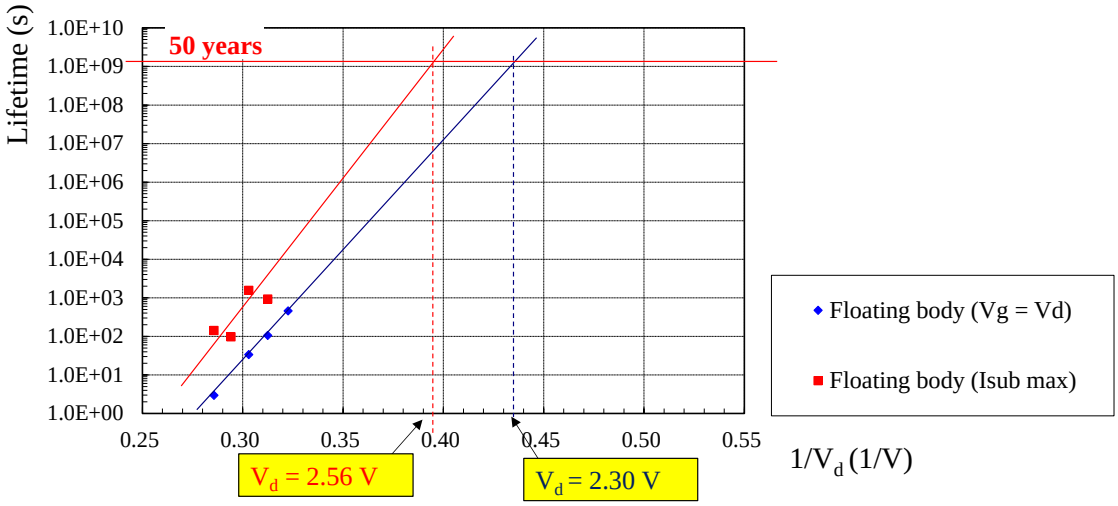


Figure 43(b). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in floating body cases of $L/W = 0.15$ μm/0.18 μm. Stress condition differs in two cases.
Closed blue symbols indicate $V_g = V_d$ case.
Closed red symbols indicate I_{sub} max case. Each stress V_g (Write-in V_g) was determined by Table IV.

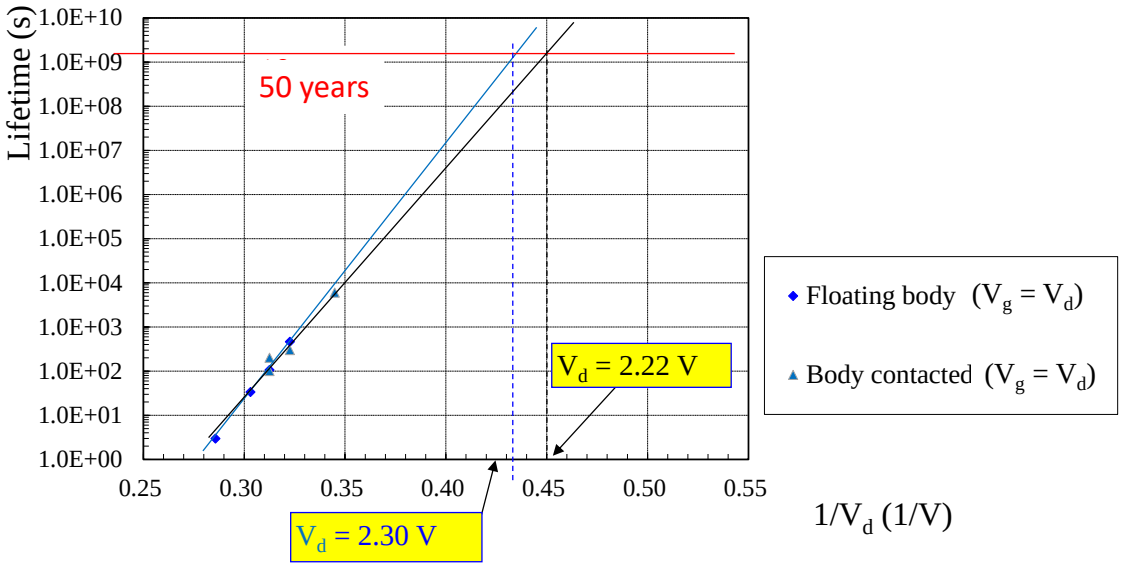


Figure 43(c). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in stress condition of $V_g = V_d$ cases of $L/W = 0.15$ μm/0.18 μm. Body potential differs in two cases.
Closed triangle gray symbols indicate body contacted case (V_{sub} at 0 V).
Closed rectangle blue symbols indicate body floating case.

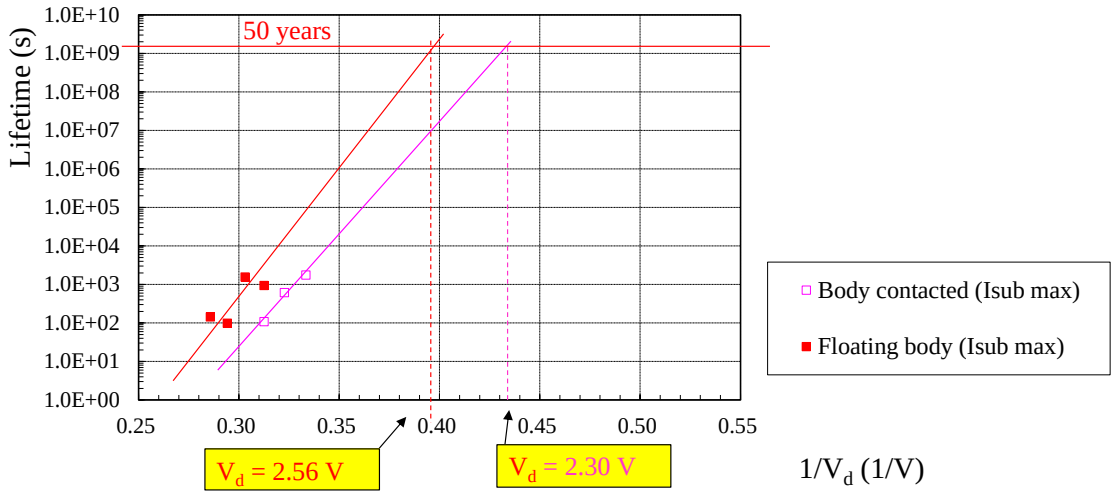


Figure 43(d). Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors in stress condition of I_{sub} max cases of $L/W = 0.15$ μm/0.18 μm. Body potential differs in two cases. Each stress V_g (Write-in V_g) was determined by Table IV.
Open red symbols indicate body contacted case (V_{sub} at 0 V).
Closed red symbols indicate floating body case.

Table VIII. Dependence of V_d of 50 years of lifetime on stress conditions of Logic CMOS type cell transistors with $L/W = 0.15$ μm/0.18 μm and 0.15 μm/1.0μm.

	V_d (V)			
	I_{sub} max		$V_g = V_d$	
	W (μm)	W (μm)	W (μm)	W (μm)
	0.18	1.00	0.18	1.00
Body contacted	2.30	2.13	2.22	1.94
Floating body	2.56	2.50	2.30	2.13

(V)

Figures 43(a) and 43(b) compare the difference between I_{sub} max and $V_g = V_d$ cases. Figures 43(c) and 43(d) compare the difference between with and without body contact cases like $W = 1.0$ μm case. Figures 43(a) and 43(b) show that the V_d of 50 years of lifetime in $V_g = V_d$ condition was lower than I_{sub} max case both with and without body

contacted cases as same as L/W = 0.15 μm/1.0 μm cases. Figures 43(c) and 43(d) show that the V_d of 50 years of lifetime without body contacted case were higher than with body contact case both in I_{sub} max and $V_g = V_d$ cases as same as L/W = 0.15 μm/1.0 μm cases. In L/W = 0.15 μm/0.18 μm cases, V_d of 50 years of lifetime shows almost the same dependence on stress conditions and body potential as same as L/W = 0.15μm /1.0 μm cases. As shown in Table VIII, in the case of the Logic CMOS type cell transistor with L/W = 0.15 μm/0.18 μm without body contact of stress condition with $V_g = V_d$ case, the V_d of 50 years of lifetime is 2.36 V. In this real size FBC, finally the HCI specification of 2.3 V has been satisfied.

3.7 Analysis of geometrical effect of channel length L on the HCI

As shown in Table VIII, $V_g = V_d$ is worst stress condition also in $W = 0.18$ μm real cell transistor case under floating body condition. As shown in Table VIII, small W and Floating body case show large V_d, and $V_g = V_d$ case shows small V_d. So lastly, the dependence of degradation of V_d on channel width W and channel length L were analyzed for Logic CMOS type cell transistors with floating body condition on $V_g = V_d$ case. Figure 39 shows the Plots of $1/V_d$ vs. lifetime in case of L ranging from 0.15 to 0.3 μm. From Fig. 44, I predicted the lifetime and Fig. 45 shows plots of L vs. V_d of 50 years of lifetime. V_d of 50 years of lifetime becomes smaller as L becomes smaller as shown in Fig. 45. If the voltage between Source and Drain is constant, the electric field strength in channel length direction simply becomes large as channel length becomes smaller.

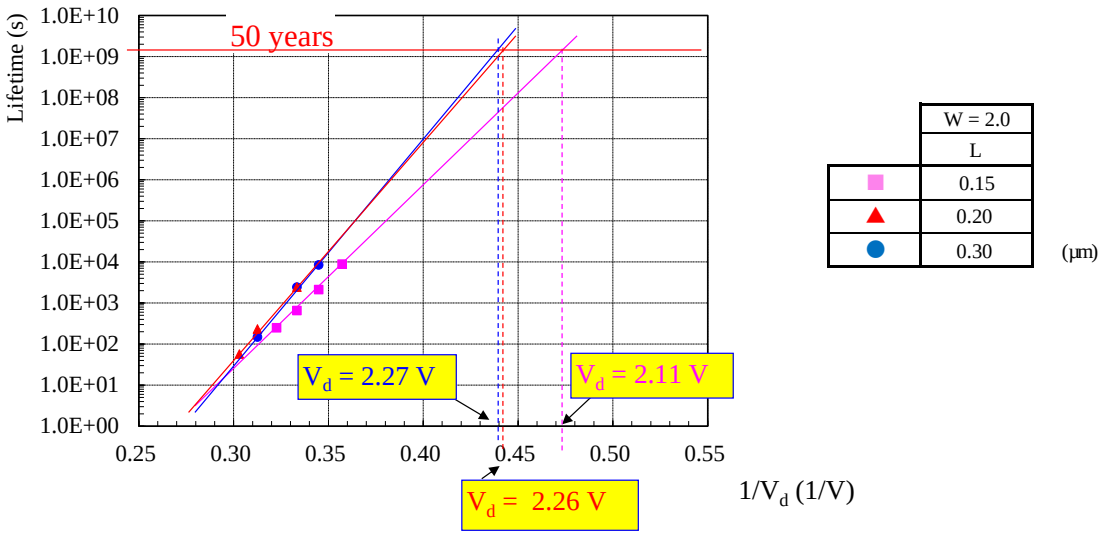


Figure 44. Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors with floating body condition on $V_g = V_d$ and $W = 2.0$ μm.

Channel length L differs in the three cases.

Closed pink rectangle symbols indicate $L = 0.15$ μm case.

Closed red triangle symbols indicate $L = 0.20$ μm case.

Closed blue circle symbols indicate $L = 0.30$ μm case.

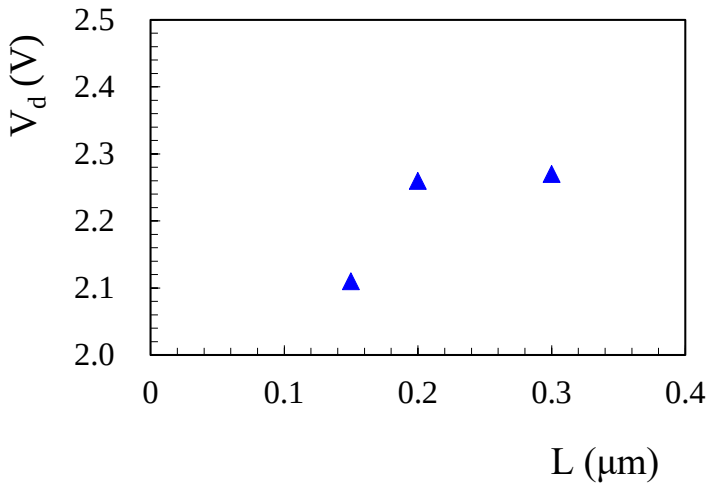


Figure 45. Plots of V_d of ten years of lifetime vs. channel length L from Fig. 44 of Logic CMOS type cell transistors.

3.8 Analysis of geometrical effect of channel width W on the HCI

Figure 46 shows the plots of $1/V_d$ vs. lifetime in case of W ranging from 0.18 to 2.0 μm of Logic CMOS type cell transistors with floating body condition on $V_g = V_d$ and L = 0.15μm case. From Fig. 46, I predicted the V_d of 50 years of lifetime, and Fig. 47 shows plots of W vs. V_d of 50 years of lifetime. V_d of 50 years of lifetime becomes larger as W becomes smaller as shown in Fig. 47. If the voltage between Source and Drain is constant, electric field strength in an edge part is thought to be more weakened with smaller W by fringe field effect. In other words, the electric field in the channel relaxes due to fringe field effect in the small W region [79] – [81]. It seems that also in channel width directions, V_d of 50 years of lifetime is lower in the direction of stronger electric field [80]. In this study, our measurement results show good agreement with this logic.

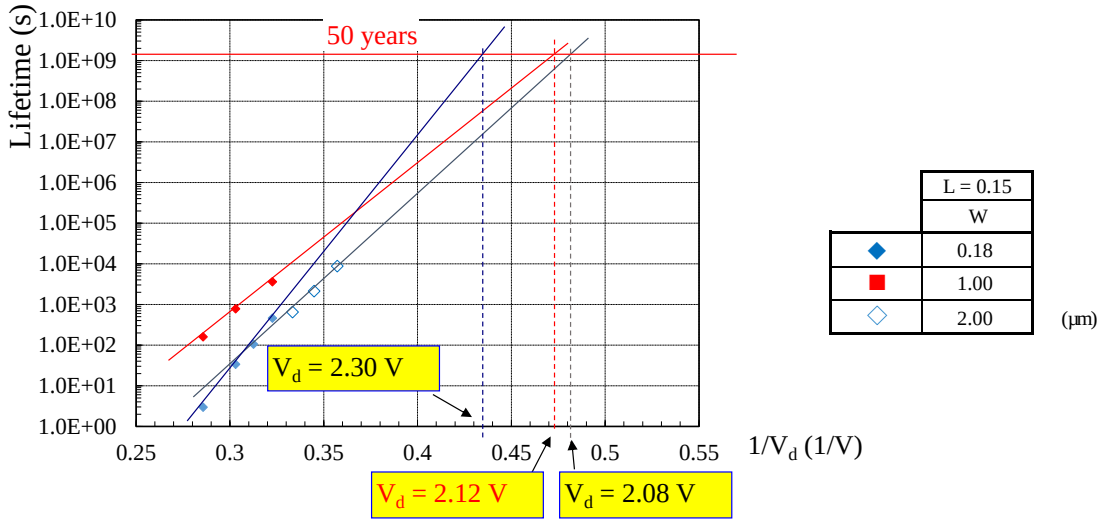


Figure 46. Plots of $1/V_d$ vs. lifetime of Logic CMOS type cell transistors with floating body condition on $V_g = V_d$ and L = 0.15 μm.

Channel width W differs in the four cases.

Closed blue rectangle symbols indicate W = 0.18 μm case.

Closed red rectangle symbols indicate W = 1.0 μm case.

Open blue triangle symbols indicate W = 2.0 μm case.

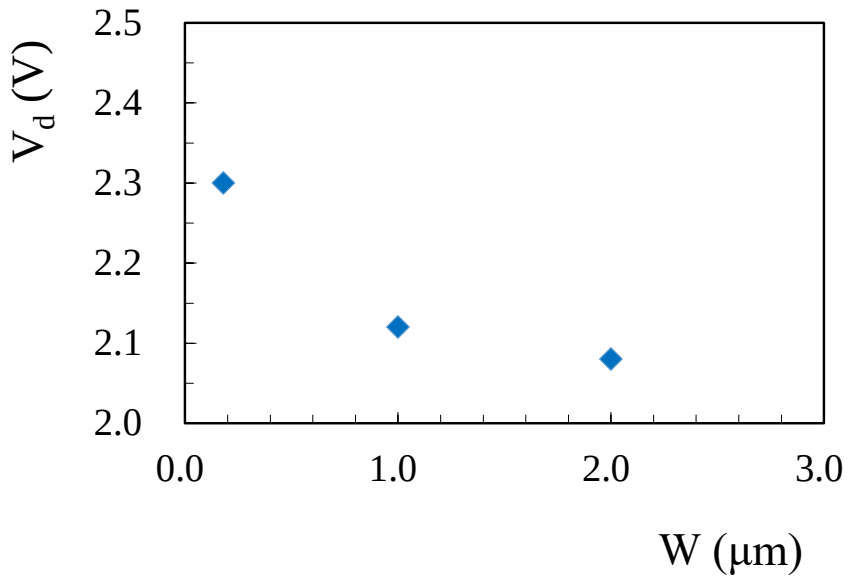


Figure 47. Plots of V_d of ten years of lifetime vs. channel width W from Fig. 46 of Logic CMOS type cell transistors.

Chapter 4 Conclusion

In the process of developing FBC [56, 59], HCI of SOI-MOS was experimentally analyzed. In FBC, under the condition of Vg = Vd, a 10% degradation in Id over 50 years was observed at Vd = 2.3 V. This means that FBC can operate for 50 years. Based on the structural difference between the Logic CMOS type and the eDRAM one, I experimentally clarified the importance of the sidewall structure of the cell transistor MOS of the FBC in the view point of HCI, especially the SiN and the SiO_2 film thickness. The worst stress condition in the Logic CMOS type HCI was clarified to be $V_g = V_d$ condition, not I_{sub} max one [68] - [71]. In both $V_g = V_d$ condition and I_{sub} max one, floating body effect improved the Logic CMOS type HCI. It was elucidated that the Logic CMOS type HCI was improved by the reduction of the channel width W [79] – [81]. I confirmed that the HCI specification of 2.3V of the FBC can be achieved at $V_g = V_d$ condition (worst stress condition) of the actual specification cell transistor by the above-mentioned comprehensive effects. In FBC (SOI-MOS), I experimentally confirmed that the presence of the buried oxide layer suppressed the hot carrier effect. The incorporation of a cathode in vacuum tubes, which extends their lifetime by reducing the work function and raising the Fermi level without changing the fundamental operating principle, thereby suppressing thermal electron acceleration and minimizing damage, is also considered to occur in FBC, and our prediction is considered to have been correct.

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