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Effects of SiO₂ cap annealing on MOS interfaces formed on Mg-doped p-type GaN surface

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In this paper, we report the effects of 800 °C SiO₂ cap annealing on the Al₂O₃/p-type GaN (p-GaN):Mg and SiO₂/p-GaN:Mg interfaces formed at relatively low temperatures, as determined by X-ray photoelectron spectroscopy (XPS) and sub-bandgap-light-assisted capacitance–voltage (C – V) measurement. For the sample with capless annealing at 800 °C and subsequent HF treatment before the Al₂O₃/p-GaN interface formation by atomic layer deposition at 300 °C, its C – V characteristics indicated the existence of high-density midgap states. By SiO₂ cap annealing and subsequent HF treatment to remove the cap layer, we found that the Al₂O₃/p-GaN interface showed a reduction in midgap state density. The same effect was confirmed at the SiO₂/p-GaN interface. Taking this finding and XPS results together, we consider the possibility that SiO₂ cap annealing at 800 °C and the subsequent HF treatment prior to the formation of the Al₂O₃/p-GaN and SiO₂/p-GaN interfaces led to the reduction of interface disorder.

1. Introduction

GaN is expected as a next-generation power device material because of its wide bandgap¹⁾, high breakdown field²⁾, high electron mobility¹⁾, high electron saturation velocity¹⁾, and good thermal conductivity¹⁾. A meta-oxide-semiconductor field-effect transistor (MOSFET) can benefit from these features of GaN to realize a highly efficient power device³⁾. Thus far, MOSFETs with excellent performance have been reported^{4–10)}. Further improvement in channel mobility can be expected because the bulk electron mobility of GaN is much higher than the reported channel mobility. To enhance the channel mobility, the control of the interface between the oxide layer and p-type GaN (p-GaN) is the most important. As reported in the literature, the interface state density (D_{it}) is usually quite low near the conduction band edge (E_C), thereby achieving the nearly ideal performance of n-type GaN (n-GaN) MOS interfaces^{11–14)}. Therefore, the inversion-type n-channel GaN MOSFET can be operated without any difficulties. However, D_{it} is relatively high near the valence band edge (E_V)^{15–18)}. In addition, the possibility that near-surface defects generate defect levels near E_V has also been reported^{19, 20)}. With the high density of these gap states, not only the channel mobility but also the reliability of GaN MOSFETs might be affected. Thus, the interface formation process should be investigated and optimized for p-GaN MOS structures. Nevertheless, the characterization of p-GaN MOS interfaces is difficult by electrical measurements because of the large band bending that typically results in deep depletion in the practical bias voltage range. For example, the capacitance–voltage (C – V) method, which is the most convenient method, cannot probe the midgap states at the GaN surfaces because the time constant of the midgap states becomes too large to respond to the bias voltage sweep, which poses difficulties in the optimization of the interface formation process for p-GaN MOS structures.

In our previous works^{21, 22)}, we demonstrated that sub-bandgap-light-assisted C – V measurements are useful for characterizing the midgap states at oxide/p-GaN interfaces. By these measurements, we investigated the effects of the formation process on oxide/p-GaN interfaces. We found that photoelectrochemical (PEC) etching is efficient in removing the near-surface defects of p-GaN. In our most recent work²²⁾, we found that the PEC-etched p-GaN surface is not free from the disorder that generate the interface states at the Al_2O_3 /p-GaN interfaces formed by atomic layer deposition (ALD) and that the disorder can be reduced by changing the interface formation process with SiO_2 cap annealing at 800 °C after PEC etching. However, the mechanism of reducing the interface disorder by

SiO₂ cap annealing is unclear.

In this work, we report the experimental results of investigating the effects of SiO₂ cap annealing at 800 °C before the formation of the Al₂O₃/p-GaN and SiO₂/p-GaN interfaces at relatively low temperatures by X-ray photoelectron spectroscopy (XPS) and sub-bandgap-light-assisted $C-V$ measurements. We also show that the midgap state density is affected by SiO₂ cap annealing.

2. Experimental methods

2.1 Sample preparation

MOS diode samples were fabricated on an epitaxial layer stack. Epitaxial layers of all samples in this study were grown on n⁺-GaN (0001) substrates by metalorganic chemical vapor phase epitaxy (MOVPE). From top to bottom, the epitaxial layer stack consisted of a 1-μm-thick p-GaN layer doped with Mg ($1 \times 10^{17} \text{ cm}^{-3}$), p⁺-GaN (1 μm, [Mg]~ $1 \times 10^{18} \text{ cm}^{-3}$), n⁺-GaN (2 μm, [Si]~ $2 \times 10^{18} \text{ cm}^{-3}$), and a 0.2-μm-thick n⁺-GaN buffer layer. The p⁺-GaN/n⁺-GaN tunneling junction enables us to eliminate the parasitic substrate capacitance and characterize the whole sample as a p-GaN MOS diode^{23, 24}.

The schematic diagram steps in the main process of fabricating MOS structures is shown in **Fig. 1**. The top of the epitaxial layer stack was treated with a diluted HF (HF:H₂O = 1:1) solution for thinning the surface native oxide layer before annealing at 800 °C for 20 min to achieve the dehydrogenation or activation of Mg acceptors. For the sample with cap annealing, a 30-nm-thick SiO₂ layer deposited by RF sputtering was used as a surface protection layer. For comparison, capless annealing was also carried out. After annealing, the HF treatment was performed again to remove the cap layer and/or thin the native oxide layer. Subsequently, an Al₂O₃ single oxide layer (30 nm) or a SiO₂ (bottom; 5 nm)/Al₂O₃ (top; 25 nm) layer stack was formed. The Al₂O₃ layer was formed by ALD at 300 °C using trimethylaluminum and H₂O, whereas the SiO₂ layer was deposited by RF sputtering at room temperature. By electron beam evaporation, we formed 300-μm-diameter electrodes and a back ohmic layer with a Ti (inner; 20 nm)/Au (outer; 50 nm) metal stack. Finally, for all samples, postmetallization annealing (PMA) was carried out at 300 or 400 °C.

XPS was carried out by using an Al α X-ray source (1486.6 eV). Charge-up calibration was performed by setting the C-C component of the C 1s spectrum to 285 eV. The sequence of sub-bandgap-light-assisted $C-V$ measurements are as follows. After illumination of the monochromatic light for 10 min at the positive bias end, the light was

turned off. Thereafter, the bias voltage was swept from the positive side to the negative side and returned to the positive bias side with the rate of 50 mV/s. All C – V measurements were carried out at a frequency of 1 kHz to inhibit the delay of the ionization of Mg acceptors with high ionization energy (~ 200 meV)²⁵⁾. The monochromatic light was prepared by using optical filters for the light from the Xe lamp. Oxide capacitance (C_{ox}) was measured under 360 nm UV light illumination.

2.2 Principle of sub-bandgap-light-assisted C – V measurements

As shown in **Fig. 2(a)**, for GaN, the charge neutrality level (E_{CNL}) lies at the position of 2.3 eV higher than the valence energy band edge (E_V)²⁶⁾. Interface states below E_{CNL} are donor-like, whereas those above E_{CNL} are acceptor-like. For p-GaN, in the absence of minority carriers, the deep donor states are positively charged and frozen independent of the surface Fermi level because of extremely large time constants, even though the interface states near E_V may be neutralized by emitting holes thermally. By illuminating the MOS diode under the deep depletion bias with the monochromatic light with the photon energy $h\nu$, we can neutralize the interface states below $E_V + h\nu$ owing to the emission of holes. Therefore, the C – V curve obtained after illumination shifts horizontally in the positive voltage direction as compared with that obtained before illumination because the interface fixed positive charge is reduced. If we vary $h\nu$, the $h\nu$ -dependent horizontal shift V_{hv} of the C – V curve should also vary because the amount of neutralization of the interface fixed charge changes. If the fixed charge originates from the interface states, we can derive D_{it} at $E_V + \frac{h\nu_2 - h\nu_1}{2}$ in the case of light irradiation with $h\nu_1$ and $h\nu_2$ as²⁷⁾

$$D_{it} = \frac{C_{ox}\Delta V_{hv}}{q\Delta h\nu}, \quad (1)$$

where C_{ox} is the oxide capacitance, q is the elemental charge, $\Delta V_{hv} = V_{hv2} - V_{hv1}$, and $\Delta h\nu = h\nu_2 - h\nu_1$. However, for a typical p-GaN MOS interface with high-density interface states, if $h\nu$ is higher than half of the bandgap E_g , the excitation of electrons from the optically neutralized states to the conduction band can occur as shown in **Fig. 2(b)**. Owing to band bending, the excited electrons can form the inversion layer at the oxide/GaN interface. Consequently, Eq. (1) no longer applies when $h\nu > E_g/2$ (1.7 eV). Still, V_{hv} of the C – V curve can occur. Since the amount of this shift increases as the interface state density, a

qualitative characterization of midgap states is possible.

3. Results and discussions

3.1 XPS results

Figures 3(a)–3(c) show the XPS Ga 3d spectra obtained after SiO₂ deposition, cap annealing, and subsequent cap-layer removal, respectively. For Figs. 3(a) and 3(b), the SiO₂ layer was thinned to 3 nm by buffered HF etching. We can see that the Ga–O component became more distinct after cap annealing, indicating that the GaN surface was oxidized to form a native oxide interlayer between SiO₂ and GaN. After the removal of the SiO₂ cap layer by HF treatment, the intensity of the Ga–O component decreased, indicating that the native oxide layer was thinned by HF treatment. The intensity of the Ga–O component relative to that of the Ga–N component was as small as the native oxide layer thickness of one monolayer. **Figure 4** shows the O 1s spectrum obtained at the same process step as in Fig. 3(c). The intensity of the O–H component in the O1s spectrum was similar to that of the HF-treated Au foil surface, indicating that this component likely originated from the absorbed water of monolayer coverage. Considering both the intensity relationships of the Ga–O and Ga–N components in the Ga 3d spectrum in Fig. 3(c), the thickness of the native oxide layer was at the monolayer level. Therefore, it is likely that the GaN surface was terminated by oxygen after HF treatment rather than covered by the native oxide layer. A schematic diagram of the change in interface structure during cap annealing process is shown in **Fig. 5**. Although almost the entire native oxide layer was removed by HF treatment prior to SiO₂ deposition, SiO₂ cap annealing enhanced the oxidation of the GaN surface, and the subsequent HF treatment removed the native oxide layer almost entirely. From another perspective, the shallow etching of the p-GaN surface was performed through SiO₂ cap annealing before interface formation.

3.2 Effects of SiO₂ cap annealing on Al₂O₃/GaN interface

The C – V characteristics obtained by sub-bandgap-light-assisted measurements of the Al₂O₃/GaN interface formed after capless annealing at 800 °C are shown in **Fig. 6(a)**, and those of the Al₂O₃/GaN interface formed after SiO₂ cap annealing at 800 °C are shown in **Fig. 6(b)**. Only the C – V curves obtained with the voltage sweep from the positive side to the negative side are shown. The hysteresis is omitted here for simplicity. The curves denoted by “dark” were measured without light illumination at the positive bias end. For capless annealing, the annealing temperature should have been as low as possible to

prevent the surface damage. The temperature of 800 °C was chosen because it was found to be sufficiently low for the efficient activation of Mg acceptors.^{28, 29)} As the first trial, the same temperature was set for samples with capless and cap annealing. For both samples, no accumulation capacitance was observed owing to the strong surface Fermi level (E_{FS}) pinning in the depletion region, which implied that the density of gap states, including interface and defect states, is high near E_V . The top plateau corresponds to $E_{FS} - E_V$ of 0.45 eV for the sample with capless annealing at 800 °C in Fig. 6(a) and that of 0.35 eV for the sample with cap annealing at 800 °C in Fig. 6(b). Therefore, the difference in the annealing method used, *i.e.*, whether the cap layer is used or not, does not markedly affect the gap state density near E_V . However, the midgap state density can be affected by the difference in the annealing method used. Namely, the amount of V_{hv} increased as $h\nu$ increased above 1.7 eV, indicating that the midgap state density was high in Fig. 6(a), whereas V_{hv} decreased in Fig. 6(b). Therefore, the midgap state density was possibly reduced by using the SiO₂ cap layer during annealing at 800 °C. In addition, by comparing Figs. 6(a) and 6(b), we found that the “dark” $C-V$ curve shifted horizontally to the positive voltage direction in the case of using the SiO₂ cap layer. There are possibilities that the density of positive interface fixed charge and the density of donor-type defects localized in the vicinity of the GaN surface decreased when using the SiO₂ cap layer. The positive interface fixed charges may originate from the frozen interface states deep inside the band gap. Therefore, the aforementioned reduction in midgap density is in good agreement with the “dark” $C-V$ curve shift. Nevertheless, we cannot deny the possibility of the reduction in the density of near-surface donor-type defects such as nitrogen vacancies (V_N) when using the SiO₂ cap layer. The generation of V_N -related defects might have been suppressed by using the SiO₂ cap layer during 800 °C annealing.

3.3 Effects of SiO₂ cap annealing on SiO₂/GaN interface

To investigate the effect of the final oxide material used in the completed MOS structure, we attempted to use the SiO₂ layer in the MOS structure with SiO₂ cap annealing at 800 °C. However, the SiO₂ layer deposited by RF sputtering lacked resistivity. Therefore, we adopted the oxide stack structure obtained by combining a thin (5 nm) inner SiO₂ layer with a thick (25 nm) outer Al₂O₃ layer. The $C-V$ characteristics obtained by sub-bandgap-light-assisted $C-V$ measurements are shown in **Fig. 7**. Compared with those in Fig. 6(a), V_{hv} 's seem to be reduced. Therefore, this result seems to coincide with the preceding result that the midgap state density at the Al₂O₃/GaN interface might have been

reduced by using the SiO₂ cap layer during annealing at 800 °C. In addition, the top plateau corresponds to $E_{\text{FS}} - E_{\text{V}}$ of 0.30 eV, which is slightly closer to E_{V} than that in Fig. 6(b) for the Al₂O₃/GaN interface.

3.4 Density distribution and origin of gap states

The gap state density (D_{T}) distributions derived from “dark” C – V characteristics by the Terman method are compared among three MOS diode samples as shown in **Fig. 8**. Note that the midgap state density was reduced by using the SiO₂ cap layer during 800 °C annealing. Considering the time constant of gap states, the gap states located deeper than 1 eV cannot respond to the bias voltage sweep. Therefore, the D_{T} distribution beyond $E - E_{\text{V}}$ of 1 eV is considered the reference data. Still, this difference is in good agreement with the difference in V_{hv} of C – V curves depending on the annealing method used. Namely, it can be considered that the use of the SiO₂ cap layer resulted in a reduction in D_{T} at the midgap.

The relatively high D_{T} in the range of 0.3 – 0.5 eV above E_{V} was observed in the samples with a single Al₂O₃ layer. In addition, the SiO₂/Al₂O₃ stack sample showed strong pinning at around $E_{\text{V}} + 0.3$ eV. According to previous reports, the observed Fermi level pinning was possibly caused by the defect level assigned to the V_{N} -related defects^{19, 20, 30–33}). In Figs. 6 and 7, the “dark” C – V curve shows a deep depletion in a wide range of negative bias voltages, indicating the possible existence of bulk donor defects such as V_{N} in the vicinity of the GaN surface. To overcome this problem, photoelectrochemical etching can be used, as reported previously. In our previous research, the D_{T} distribution of the MOS sample with capless annealing at 800 °C showed a discrete peak at $E_{\text{V}} + 0.7$ – 0.8 eV^{21, 22}). This defect level was assigned to the Mg_{Ga} V_{N} complex. In this work, no defect level at $E_{\text{V}} + 0.7$ – 0.8 eV was observed in all samples in Fig. 8. This difference might result from the difference in annealing time. Here, 800 °C annealing was carried out for 20 min, whereas that in the previous work was carried out for 5 min.

The obtained results imply that the reduction in D_{T} resulted from SiO₂ cap annealing. There is a possibility that the native oxide/GaN interface was improved by the reduction of interface disorder after SiO₂ cap annealing at 800 °C. According to previous reports^{34, 35}), the native oxide layer can be epitaxial and crystalline even though the quality of the layer depends on the formation process used. Therefore, the native oxide/GaN interface can be well ordered. Still, the layer itself might contain defects. Thus, the thinning of the native oxide layer seems to be necessary for achieving excellent MOS interface properties. The monolayer oxygen termination shown in Fig. 5 after the HF treatment following SiO₂ cap

annealing might be the best situation before the formation of oxide/GaN interfaces. However, D_T near E_V is still high, as can be seen in Fig. 8. Further optimization of the temperature and duration of the cap annealing process is necessary for achieving further reduction in D_T near E_V .

We also investigated the current density–voltage (J – V) characteristics of all fabricated MOS diode samples. The results are summarized in Fig. 9. We can see that the insulating properties of the oxide layers are excellent without any significant leakage currents, even though slight differences can be seen. Since all Al_2O_3 layers were deposited at 300 °C and were not subjected to 800 °C annealing, their amorphous nature was maintained resulting in high resistivity³⁶). Therefore, the measured C – V characteristics were not affected by leakage currents resulting in the appropriate characterizations of the $\text{Al}_2\text{O}_3/\text{GaN}$ and SiO_2/GaN interfaces.

4. Conclusions

We carried out XPS and sub-bandgap-light-assisted C – V measurements to examine the effects of SiO_2 cap annealing at 800 °C before the $\text{Al}_2\text{O}_3/\text{p-GaN}$ interface formation by ALD at 300 °C and the $\text{SiO}_2/\text{p-GaN}$ interface formation by RF sputtering at room temperature. XPS results indicated that the native oxide layer thickness increased after SiO_2 cap annealing and that a monolayer oxygen termination might have been achieved after the subsequent HF treatment. For the sample with capless annealing at 800 °C and subsequent HF treatment before the formation of the $\text{Al}_2\text{O}_3/\text{p-GaN}$ interface by ALD at 300 °C, its C – V characteristics indicated the existence of high-density midgap states. By SiO_2 cap annealing and subsequent HF treatment, we found that the $\text{Al}_2\text{O}_3/\text{p-GaN}$ interface showed a reduction in midgap state density. The same effect was confirmed at the $\text{SiO}_2/\text{p-GaN}$ interface. Taking all results together, SiO_2 cap annealing at 800 °C and the subsequent HF treatment before the formation of the $\text{Al}_2\text{O}_3/\text{p-GaN}$ and $\text{SiO}_2/\text{p-GaN}$ interfaces possibly led to the reduction of interface disorder.

Acknowledgments

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Figure Captions

Fig. 1. Schematic diagram of sample preparation sequence.

Fig. 2. Schematic diagrams of (a) concept of sub-bandgap light irradiation to change interface charge and (b) generation of inversion layer at oxide/p-GaN interface by irradiation of monochromatic sub-bandgap light with $h\nu > E_g/2$.

Fig. 3. XPS Ga 3d spectra with neighboring N 2s and O 2s spectra. (a) After SiO₂ deposition. (b) After SiO₂ cap annealing at 800 °C. (c) After HF treatment to remove SiO₂ cap layer. The experimental data of (b) are taken from Fig. 11 in our previous paper (Ref. 22) with permission.

Fig. 4. XPS O 1s spectra obtained after HF treatment following SiO₂ cap annealing.

Fig. 5. Schematic diagram of change in sample surface structure during SiO₂ cap annealing.

Fig. 6. C – V characteristics obtained by sub-bandgap-light-assisted measurements of Al₂O₃/p-GaN MOS samples with (a) capless annealing and (b) SiO₂ cap annealing.

Fig. 7. C – V characteristics obtained by sub-bandgap-light-assisted measurements of Al₂O₃/SiO₂/p-GaN MOS samples with SiO₂ cap annealing.

Fig. 8. D_T distributions derived from C – V characteristics measured without monochromatic light illumination for three MOS diode samples.

Fig. 9. J – V characteristics for all MOS diode samples.

Figures

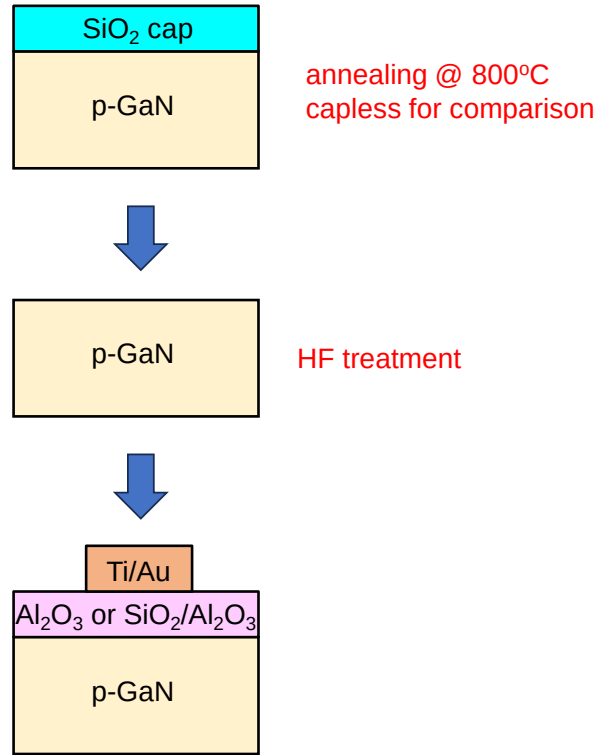


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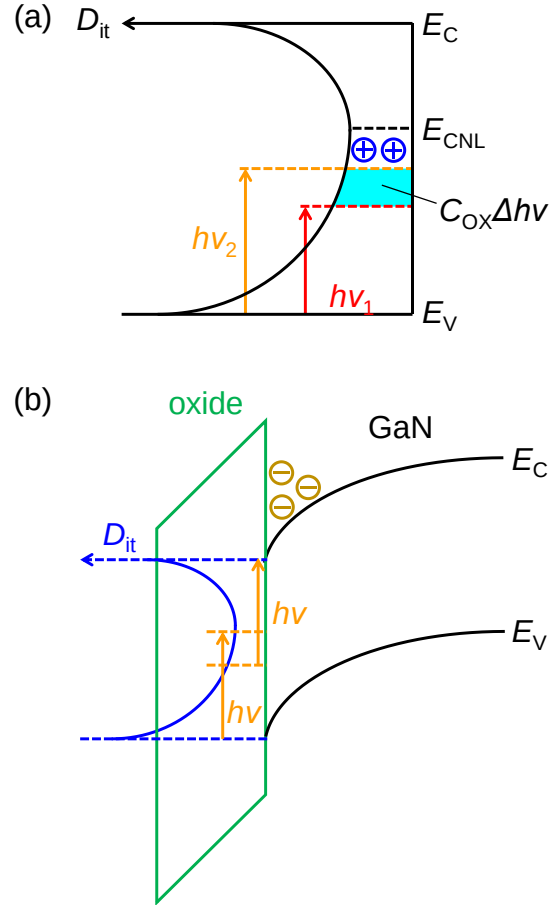


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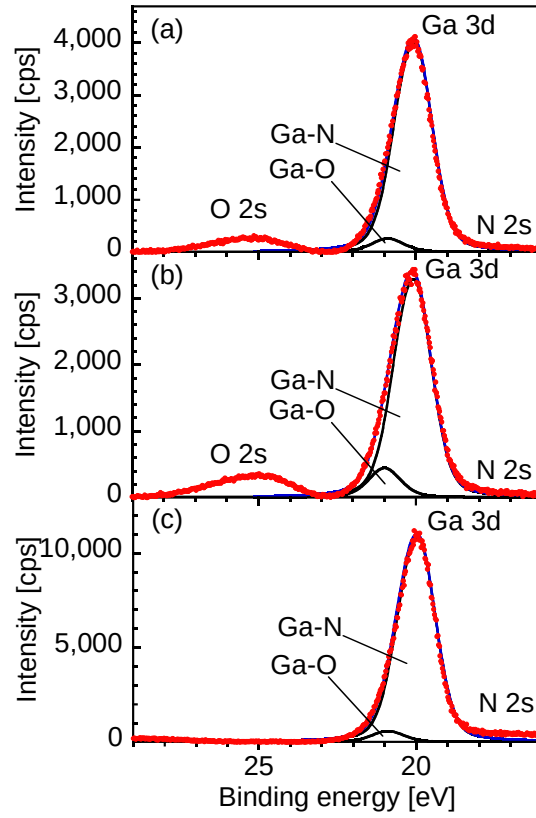


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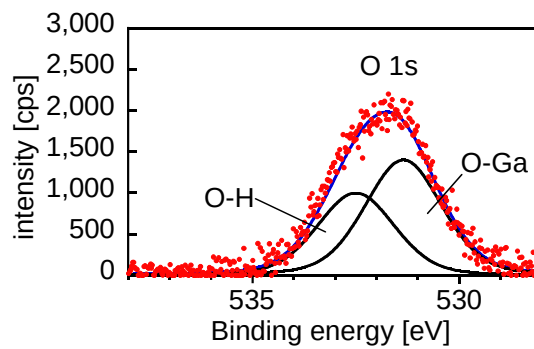


Fig. 4. XPS O 1s spectra obtained after HF treatment following SiO₂ cap annealing.

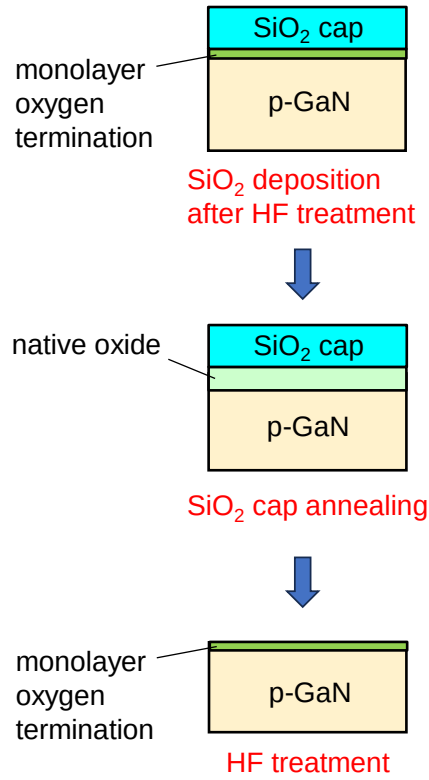


Fig. 5. Schematic diagram of change in sample surface structure during SiO₂ cap annealing.

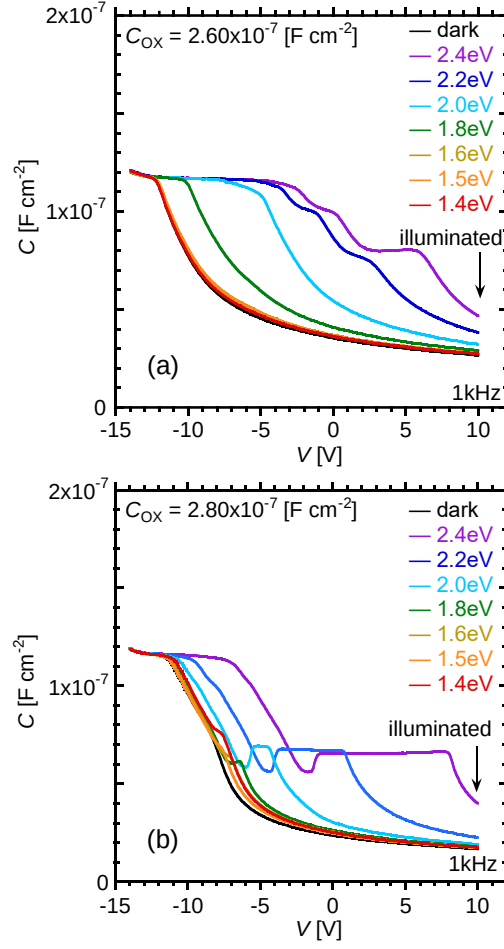


Fig. 6. C – V characteristics obtained by sub-bandgap-light-assisted measurements of $\text{Al}_2\text{O}_3/\text{p-GaN}$ MOS samples with (a) capless annealing and (b) SiO_2 cap annealing.

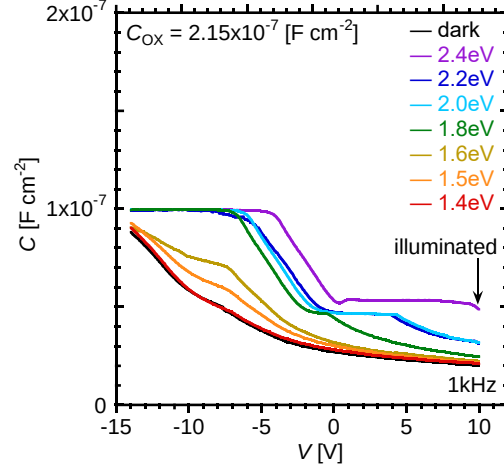


Fig. 7. C - V characteristics obtained by sub-bandgap-light-assisted measurements of $\text{Al}_2\text{O}_3/\text{SiO}_2/\text{p-GaN}$ MOS samples with SiO_2 cap annealing.

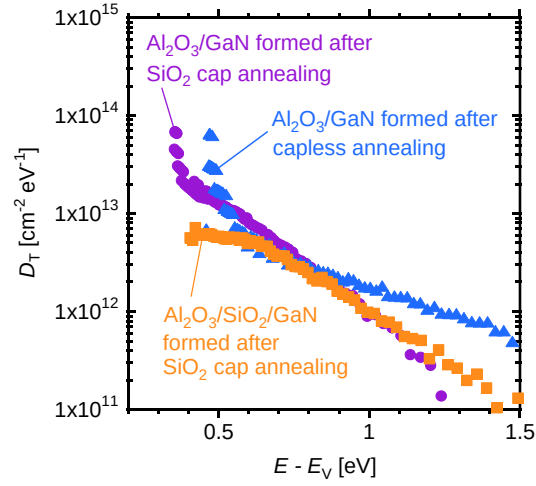


Fig. 8. D_T distributions derived from C - V characteristics measured without monochromatic light illumination for three MOS diode samples.

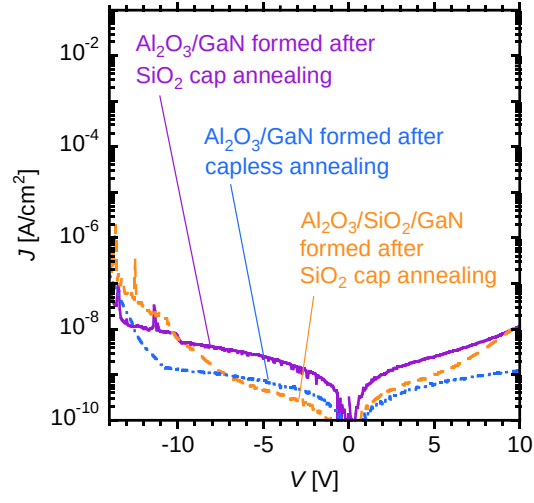


Fig. 9. J – V characteristics for all MOS diode samples.